MP150

Offline Primary-Side Regulator For Low Power Applications

The Future of Analog IC Technology

DESCRIPTION

MP150 is a primary-side regulator that provides accurate constant voltage (CV) regulation without the opto-coupler, and supports Buck, Buck-boost, Boost and Flyback topologies. It has an integrated 500V MOSFET that simplifies the structure and reduces costs. These features help to make it a competitive candidate for off-line low power applications, such as home appliances and standby power.

MP150 is a green-mode operation regulator. Both the peak current and switching frequency decrease as the load decreases to provide excellent efficiency performance at light load, thus improving the overall average efficiency.

The MP150 features various protections, including thermal shutdown (TSD), VCC under-voltage lockout (UVLO), over-load protection (OLP), short-circuit protection (SCP), and open loop protection.

MP150 is available in the TSOT23-5 and SOIC8 packages.

FEATURES

- Primary-side constant voltage (CV) control, supporting Buck, Buck-boost, Boost and Flyback topologies
- Integrated 500V/30Ω MOSFET
- < 150mW No-load power consumption
- Up to 2W output power
- Maximum DCM output current less than 120mA
- Maximum CCM output current less than 200mA
- Frequency foldback
- Maximum frequency limitation
- Peak current compression
- Internal high-voltage current source

APPLICATIONS

- Home Appliance, White Goods and Consumer Electronics
- Industrial Controls
- Standby Power

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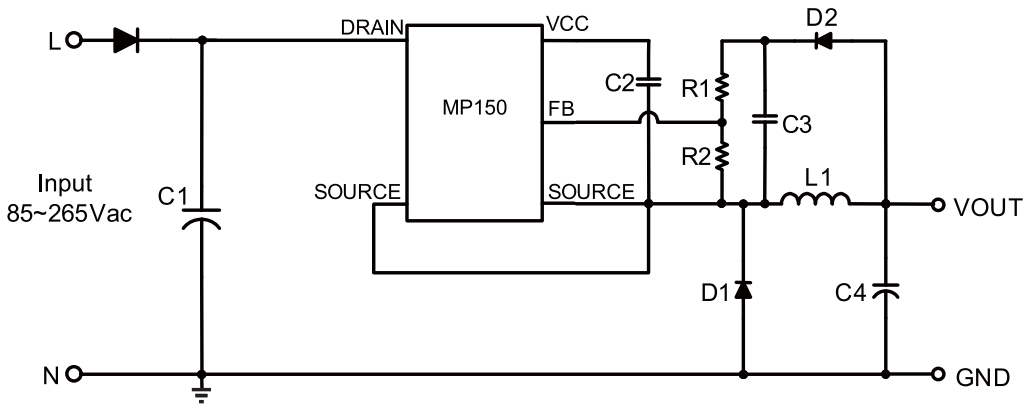
TYPICAL APPLICATION



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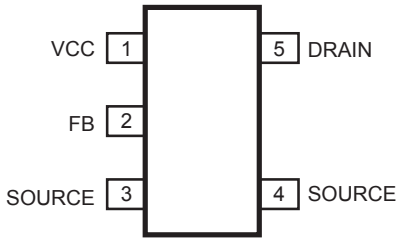
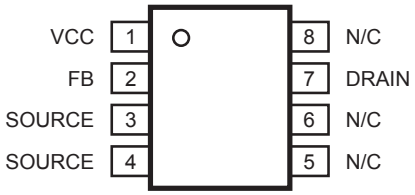
ORDERING INFORMATION

Part Number*	Package	Top Marking
MP150GJ	TSOT23-5	ADG
MP150GS	SOIC8	MP150

* For Tape & Reel, add suffix –Z (e.g. MP150GJ–Z);
* For Tape & Reel, add suffix –Z (e.g. MP150GS–Z);

PACKAGE REFERENCE

TOP VIEW	TOP VIEW
	
TSOT23-5	SOIC8

ABSOLUTE MAXIMUM RATINGS (1)

Drain to SOURCE ..... -0.7V to 500V
All Other Pins ..... -0.7V to 6.5V
Continuous Power Dissipation (T_A = +25°C) (2)
TSOT23-5 ..... 1W
SOIC8..... 1W
Junction Temperature..... 150°C
Lead Temperature ..... 260°C
Storage Temperature.....-60°C to +150°C
ESD Capability Human Body Mode 4.0kV
ESD Capability Machine Mode..... 200V

Recommended Operating Conditions (3)

Operating Junction Temp. (T_J) .-40°C to +125°C
Operating VCC range ..... 5.3V to 5.6V

Thermal Resistance (4) θ_{JA} θ_{JC}

TSOT23-5 ..... 100 ..... 55 ... °C/W
SOIC8..... 96 ..... 45 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature TA. The maximum allowance continuous power dissipation at any ambient temperature is calculated by PD(MAX)=(TJ(MAX)-TA)/θ_{JA}. Exceeding the maximum allowance power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuit protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{CC} = 5.8V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Start-up Current Source (Drain Pin)						
Internal regulator supply current	$I_{regulator}$	VCC=4V;V_{Drain}=100V	2.5	3.5	4.5	mA
Drain pin leakage current	I_{Leak}	VCC=5.8V;V_{Darin}=400V		10	12	μA
Breakdown voltage	$V_{(BR)DSS}$		500			V
Supply Voltage Management (VCC Pin)						
VCC level (increasing) where the internal regulator stops	VCC_{OFF}		5.4	5.6	5.8	V
VCC level (decreasing) where the internal regulator turns on	VCC_{ON}		5.1	5.3	5.6	V
VCC regulator on and off hysteresis				250		mV
VCC level (decreasing) where the IC stops working	VCC_{stop}			3.4		V
VCC level (decreasing) where the protection phase ends	VCC_{pro}			2.4		V
Internal IC consumption	I_{CC}	VCC=5.8V, f_s=37kHz, D= 40%			430	μA
Internal IC consumption (no switching)	I_{CC}				300	μA
Internal IC Consumption, Latch off Phase	$I_{CCLATCH}$	VCC=5.3V		16		μA
Internal MOSFET (Drain Pin)						
Breakdown voltage	V_{BRDSS}		500			V
ON resistance	R_{on}			30		Ω
Internal Current Sense						
Peak current limit	I_{Limit}		260	290	345	mA
Leading-edge blanking	τ_{LEB1}			350		ns
SCP point	I_{SCP}			450		mA
Leading-edge blanking for SCP	τ_{LEB2}			180		ns
Feedback input (FB Pin)						
Minimum off time	τ_{minoff}		15	18	21	μs
Primary MOSFET feedback turn-on threshold	V_{FB}		2.45	2.55	2.65	V
OLP feedback trigger threshold	V_{FB_OLP}			1.7		V
OLP delay time	τ_{OLP}	f_s=37kHz		170		ms
Open-loop detection	V_{OLD}			60		mV
Thermal Shutdown						
Thermal shutdown threshold				150		ºC

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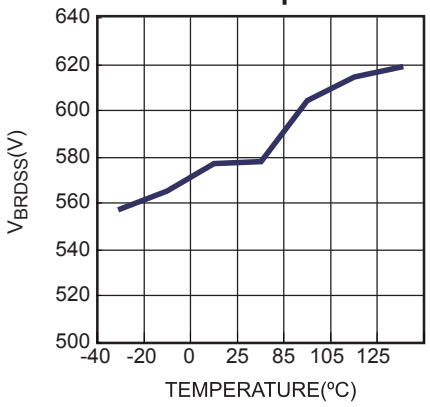
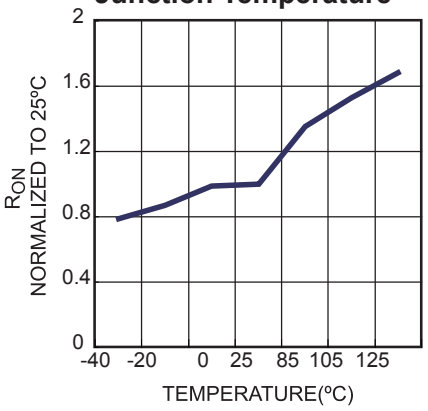
TYPICAL CHARACTERISTICS

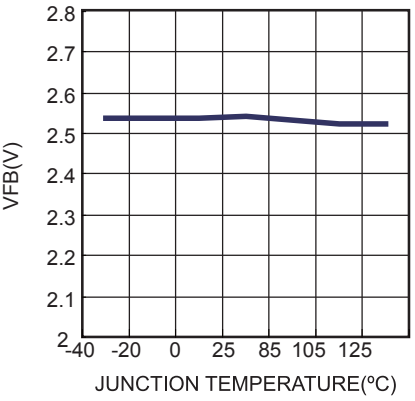
Breakdown Voltage vs. Junction Temperature



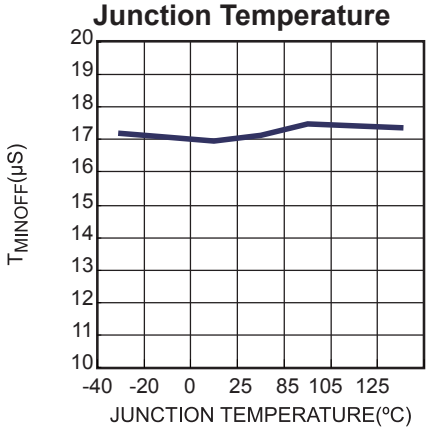
On-State Resistance vs. Junction Temperature



Feedback Voltage vs. Junction Temperature



Minimum Off Time vs. Junction Temperature



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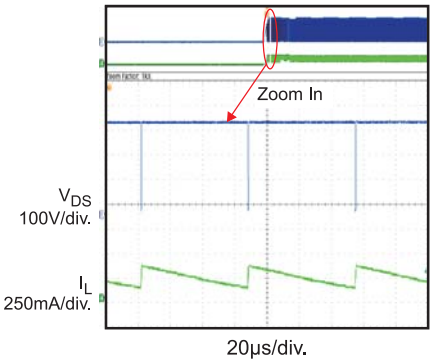
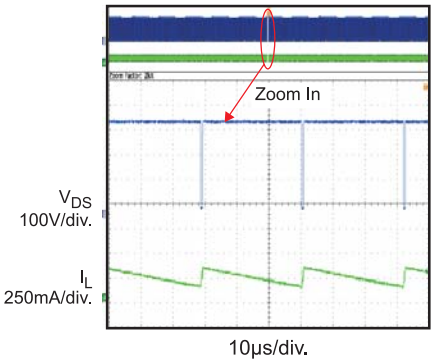
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 265VAC, V_{OUT} = 5V, I_{OUT} = 200mA, L = 1mH, C_{OUT} = 100µF, T_A = +25°C, unless otherwise noted.

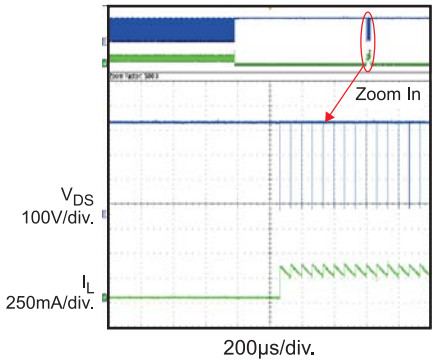
Start Up



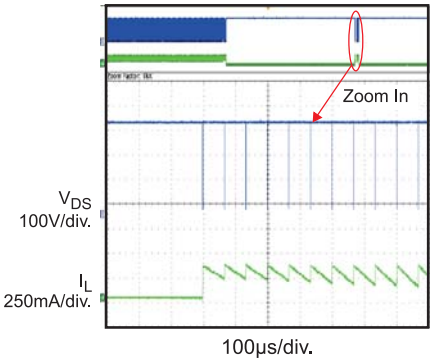
Normal Operation



SCP



Open Loop Protection



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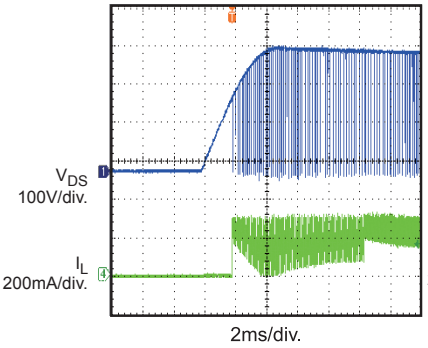
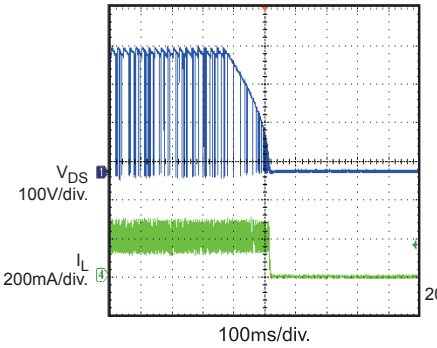
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 230VAC, V_{OUT} = 5V, I_{OUT} = 200mA, L = 1mH, C_{OUT} = 100µF, T_A = +25°C, unless otherwise noted.

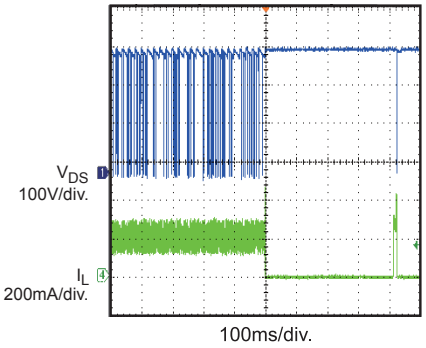
Input Power Start Up



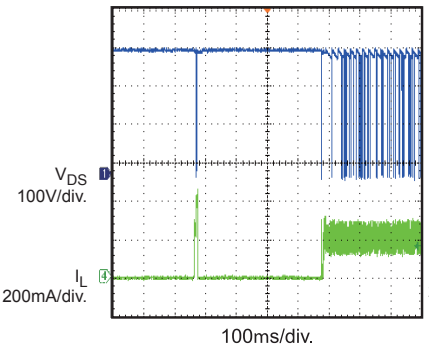
Input Power Shut Down



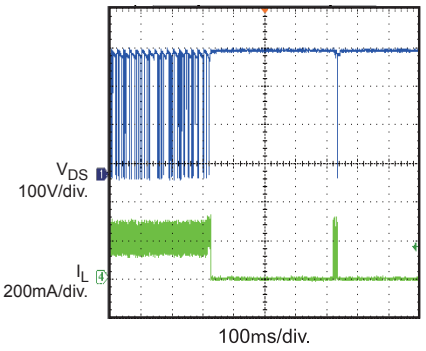
SCP Entry



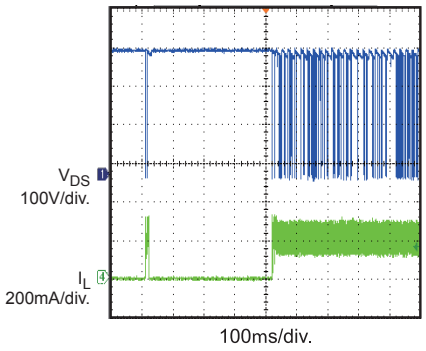
SCP recovery



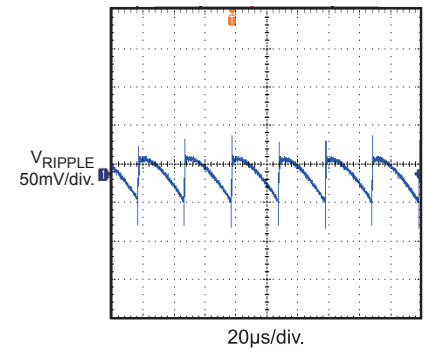
Open Loop Entry



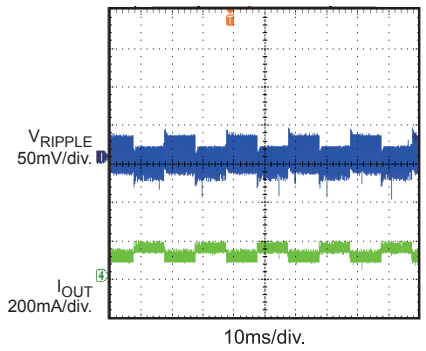
Open Loop Recovery



Output Voltage Ripple



Load Transient



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PIN FUNCTIONS

Pin # TSOT23-5	Pin # SOIC8	Name	Description
1	1	VCC	Control Circuit Power Supply.
2	2	FB	Regulator Feedback.
3,4	3,4	SOURCE	Internal Power MOSFET Source. Ground reference for VCC and FB pins.
5	7	DRAIN	Internal Power MOSFET Drain. High voltage current source input.
	5,6,8	N/C	Not connected.

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FUNCTIONAL BLOCK DIAGRAM

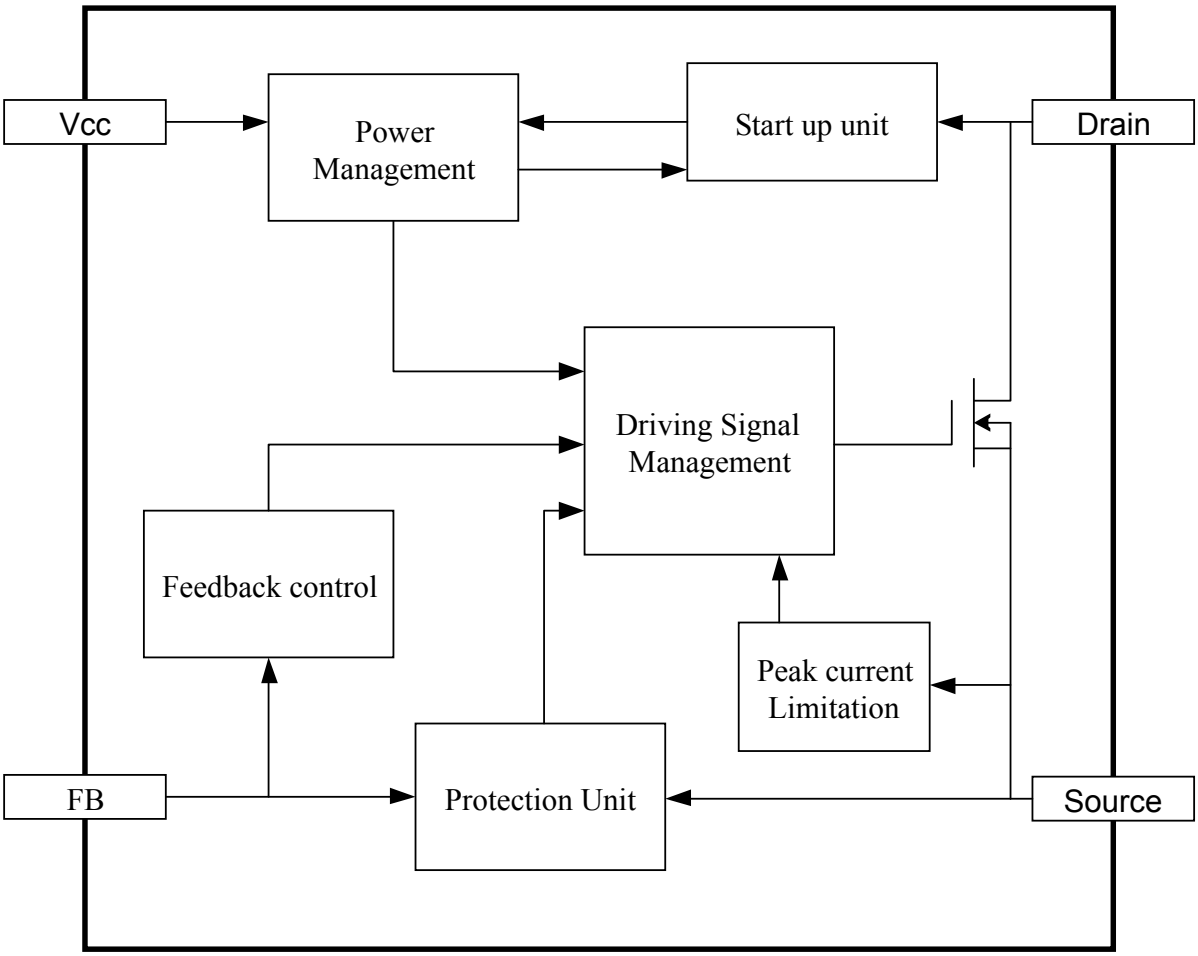

Figure 1: Functional Block Diagram

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OPERATION

The MP150 is a green-mode-operation regulator. The peak current and the switching frequency both decrease as the load decreases to provide excellent efficiency at light load, and thus improve the overall average efficiency. The typical application diagram shows that the regulator operates using a minimal number of external components. It incorporates the following features:

Start-up and Under Voltage Lock-out

The internal high-voltage regulator supplies the IC from the Drain pin. The IC starts switching and the internal high voltage regulator turns off when the voltage on VCC reaches 5.6V. When the VCC voltage drops below 5.3V, the internal high voltage regulator turns on again to charge the external VCC capacitor. Use a capacitor in the several μF range stabilize the VCC voltage and this can lower the cost by decreasing the value of the capacitor.

When the voltage on VCC drops blow 3.4V, the IC stops, then the internal high-voltage regulator charges the VCC capacitor.

When faults occur, such as overload, short circuit, and over-heating, the IC stops working and an internal current source (16μA) discharges the VCC capacitor. Before the VCC voltage drops below 2.4V, the internal high-voltage regulator remains off and the VCC capacitor remains discharged. Estimate the restart time after a fault as:

$$t_{restart} = C_{VCC} \times \frac{V_{CC} - 2.4V}{16uA} + C_{VCC} \times \frac{5.6V - 2.4V}{3.5mA}$$

Figure 2 shows the typical waveform with VCC under-voltage lockout.

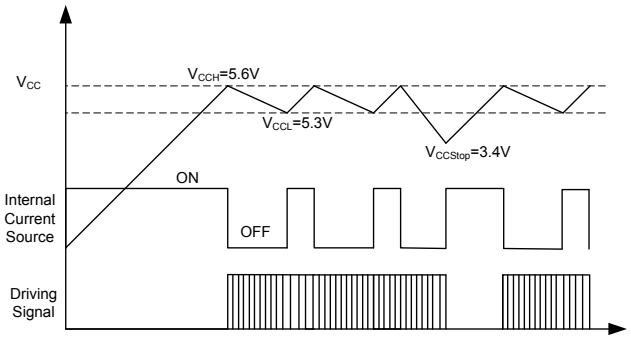

Figure 2: VCC Under-Voltage Lockout

Constant Voltage Operation

The MP150 is a fully-integrated regulator when used in a Buck solution as shown in the typical application on page 1.

The integrated MOSFET turns ON at the beginning of each cycle when the feedback voltage is below the reference voltage (2.5V), which indicates insufficient output voltage. The peak current limit determines the ON period. After the ON period elapses, the integrated MOSFET turns OFF. The freewheeling diode (D1) remains OFF until the inductor current charges the sampling capacitor (C3) voltage to the output voltage level. Then the sampling capacitor voltage changes with the output voltage. The sampling capacitor can sample and hold the output voltage to regulate the output voltage. The sampling capacitor voltage decreases after the inductor current drops below the output current. When the feedback voltage falls below the reference voltage (2.5V), a new switching cycle begins.

Figure 3 shows the detailed operation timing diagram under CCM.

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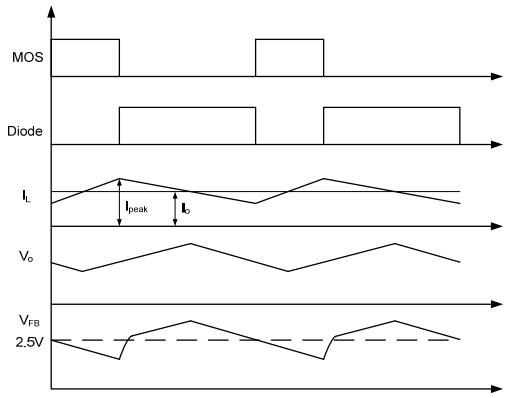

Figure 3: V_{FB} vs V_{OUT}

Monitoring the sampling capacitor regulates the output voltage, as per the following equation:

$$Vo = 2.5V \times \frac{R1+R2}{R2}$$

Frequency Foldback

Under light load or no load conditions, the output drops very slowly, which increases the time for the MOSFET to turn ON again; i.e., frequency decreases as the load decreases. So the MP150 can maintain a high efficiency under light load condition by reducing the switching frequency automatically.

The switching frequency can be obtained as:

$$f_s = \frac{(V_{in} - V_o)}{2L(I_{peak} - I_o)} \cdot \frac{V_o}{V_{in}}, \text{ for CCM}$$

$$f_s = \frac{2(V_{in} - V_O)}{LI^2_{peak}} \cdot \frac{I_o V_o}{V_{in}}, \text{ for DCM}$$

At the same time, the peak current limit decreases from 290mA as the OFF time increases. In standby mode, the frequency and the peak current are both minimized, allowing for a small dummy load. As a result, the peak-current-compression function helps to reduce no-load consumption. Determine the peak current limitation from the following equation where τ_{off} is the power module OFF time:

$$I_{Peak} = 290mA - (1mA/\mu s) \times (\tau_{off} - 18\mu s)$$

Minimum OFF Time Limit

The MP150 implements a minimum OFF time limit. During the normal operation, the minimum OFF time limit is 18µs; during start up, the minimum OFF time limit gradually drops from 72µs, to 36µs, then to 18 µs (see Figure 4). Each minimum OFF time has 128 switching cycles. This soft-start function allows for safe start-up.

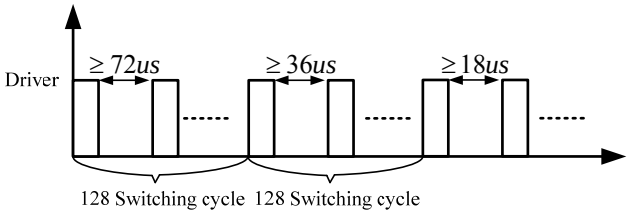

Figure 4: t_{minoff} at Start-Up

EA Compensation

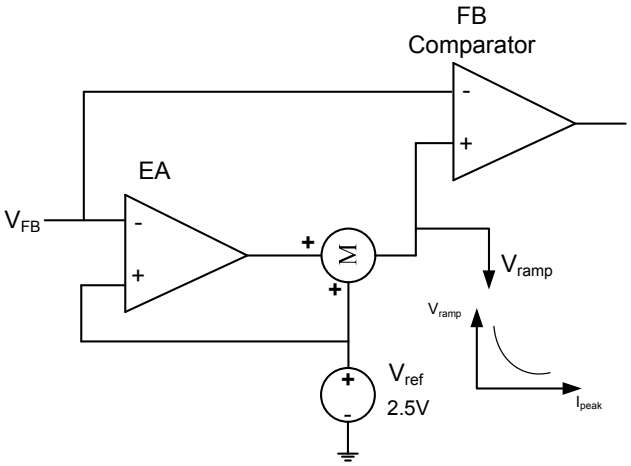

Figure 5: EA and Ramp Compensation

To improve load regulation, the MP150 implements an error amplifier (EA) compensation function (Figure 5). The MP150 samples the feedback voltage 6µs after the MOSFET turns off. EA compensation regulates the 2.5V reference voltage with the load, thus improving the power module regulation.

RAMP Compensation

An internal ramp compensation circuit precisely maintains the output voltage. An additional exponential voltage sinking source pulls down the feedback comparator's reference voltage as shown in Figure 5. The ramp compensation is relative to the load conditions: Under full-load conditions, the compensation is ~1mV/µs; With a

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decreasing load, the compensation increases exponentially.

Over Load Protection (OLP)

As the load increases, the peak current and the switching frequency increase with the load. When the switching frequency and peak current reaches their maximums, the output voltage will decrease if the load continues to increase. Then the FB voltage will drop below OLP threshold.

By continuously monitoring the FB voltage, the timer starts when the FB voltage drops below the 1.7V error flag threshold. Removing the error flag resets the timer. If the timer continues to completion at 170ms (f_a =37kHz), OLP occurs. This timer duration avoids triggering OLP when the power supply starts up or enters a load transition phase, and therefore requires that the power supply start up in less than 170ms. A different switching frequency (f_s) changes the over-load protection delay time, as shown below:

$$\tau_{Delay} \approx 170ms \times \frac{37kHz}{fs}$$

Short-Circuit Protection (SCP)

The MP150 shuts down when the peak current rises above 450mA as its short-circuit protection threshold. The power supply resumes operation after removing the fault.

Thermal shutdown (TSD)

To prevent from any lethal thermal damage, the MP150 shuts down switching when the inner temperature exceeds 150°C. During thermal shutdown (TSD), the VCC drops to 2.4V, and then the internal high voltage regulator recharges VCC.

Open Loop Detection

If the V_{FB} drops below 60mV, the IC will stop working and begins a re-start cycle. The open-loop detection is blanked for 128 switching cycles during start-up.

Leading-Edge Blanking

An internal leading-edge blanking (LEB) unit between the current sense resistor inside the IC and the current comparator input avoids prematurely switching pulse termination due to the parasitic capacitance. During the blanking period, the current comparator is disabled and cannot turn off the external MOSFET. Figure 6 shows leading edge blanking.

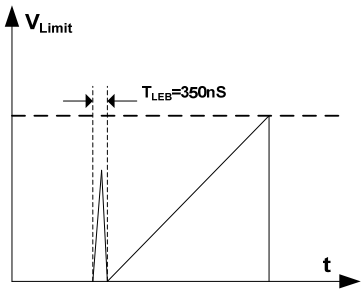

Figure 6: Leading-Edge Blanking

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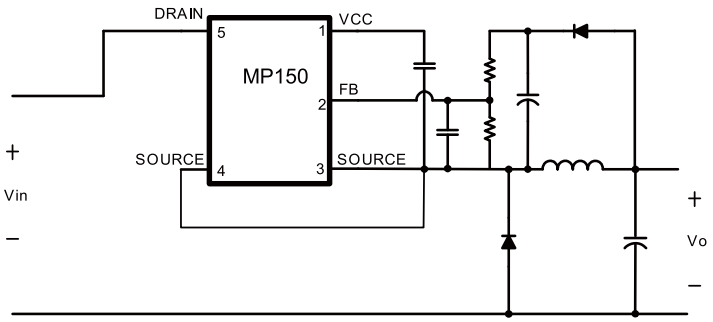
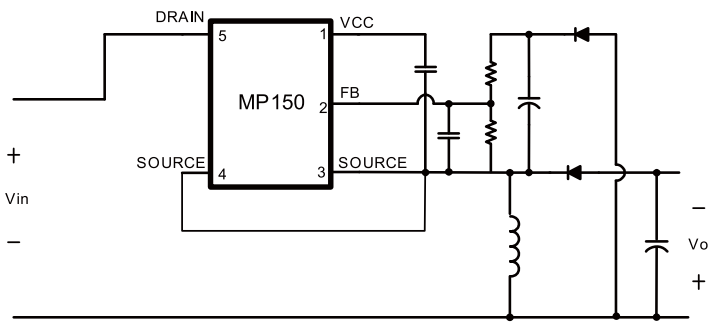
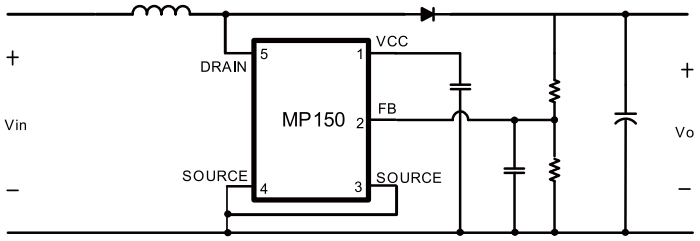
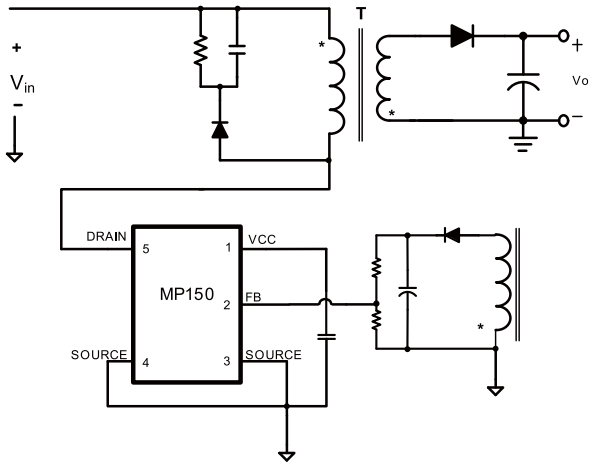
APPLICATION INFORMATION

Table 1. Common Topologies Using MP150

Topology	Circuit Schematic	Features
High-Side Buck		1. No-isolation, 2. Positive output 3. Low cost 4. Direct feedback
High-Side Buck-Boost		1. No-isolation, 2. Negative output 3. Low cost 4. Direct feedback
Boost		1. No-isolation, 2. Positive output 3. Low cost 4. Direct feedback
Flyback		1. Isolation, 2. Positive output 3. Low cost 4. Indirect feedback

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Topology Options

MP150 can be used in common topologies, such as Buck, Buck-Boost, Boost and Flyback. Please find the Table.1 for more information.

Component Selection

Input Capacitor

The input capacitor supplies the converter's DC input voltage. Figure 7 shows the typical half-wave rectifier's DC bus voltage waveform.

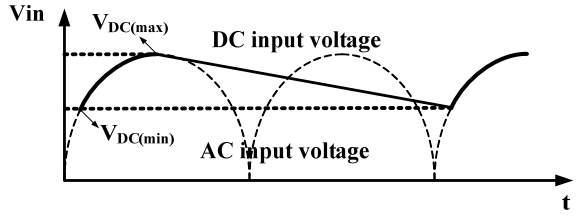

Figure 7: Input Voltage Waveform

When using the half-wave rectifier, set the input capacitor 3μF/W for the universal input condition. When using the full-wave rectifier, choose a smaller capacitor, but avoid a minimum DC voltage below 70V to avoid thermal shutdown.

Inductor

MP150 has a minimum OFF time limit that determines the maximum power output. The maximum power increases with the inductor value. Using a smaller inductor may cause the output to fail at full load, but a larger inductor results in a higher OLP load. The optimal inductor value is the smallest that can supply the rated power. The maximum power is:

$$P_{omax} = V_o(I_{peak} - \frac{V_o \tau_{minoff}}{2L}), \text{ for CCM}$$

$$P_{omax} = \frac{1}{2} L I_{peak}^2 \cdot \frac{1}{\tau_{minoff}}, \text{ for DCM}$$

To account for converter parameters—such as peak current limit and minimum OFF time—estimate the minimum inductor power (P_{min}) for the maximum power, and selecting an inductor with a P_{min} value that exceeds the rated power.

Using output voltages 5V and 12V as examples, Figure 8 shows the curve for P_{min} at 5V, and Figure 9 shows the curve for P_{min} at 12V. (I_{peak}=0.29A, τ_{minoff}=18μs).

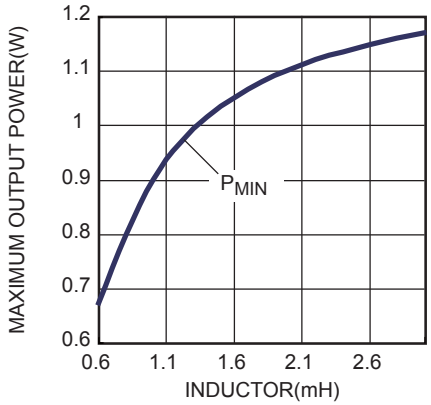

Figure 8: P_{min} vs. L at 5V

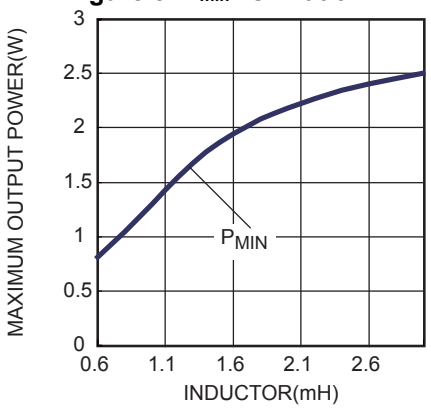

Figure 9: P_{min} vs. L at 12V

When designing a 0.5W converter (5V, 0.1A), estimate the minimum inductor value at 0.6mH based on Figure 8. Similarly, for a 1.2W converter (12V, 0.1A), estimate the minimum inductor at 0.9mH based on Figure 9.

Use a standard off-the-shelf inductor to reduce costs. Use a standard inductance that exceeds calculated inductance.

Freewheeling Diode

Choose a diode with a maximum reverse voltage rating that exceeds the maximum input voltage, and a current rating that exceeds the output current.

The reverse recovery of the freewheeling diode can affect the efficiency and circuit operation. Select an ultra-fast diode, such as the EGC10JH for DCM and the UGC10JH for CCM.

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Output Capacitor

The output capacitor maintains the DC output voltage. Estimate the output voltage ripple as:

$$V_{CCM_ripple} = \frac{\Delta i}{8 f_s C_o} + \Delta i \cdot R_{ESR} \text{ for CCM}$$

$$V_{DCM_ripple} = \frac{I_o}{f_s C_o} \cdot \left(\frac{I_{pk} - I_o}{I_{pk}} \right)^2 + I_{pk} \cdot R_{ESR} \text{ for DCM}$$

Use ceramic, tantalum, or low-ESR electrolytic capacitors to lower the output voltage ripple.

Feedback Resistors

The resistor divider determines the output voltage. Choose appropriate R1 and R2 values to maintain the FB voltage at 2.5V. Avoid very large values for R2 (typical values between 5kΩ to10kΩ.

Feedback Capacitor

The feedback capacitor provides a sample-and-hold function. Small capacitors result in poor regulation at light load condition, and large capacitors can impact circuit operation. Estimate the capacitor range as per the following equation:

$$\frac{1}{2} \frac{V_o}{R_1 + R_2} \cdot \frac{C_o}{I_o} \le C_{FB} \le \frac{V_o}{R_1 + R_2} \cdot \frac{C_o}{I_o}$$

Choose an appropriate value given practical considerations.

Dummy Load

A dummy load maintains the load regulation. This ensures sufficient inductor energy to charge the sample-and-hold capacitor to detect the output voltage. Start with a 3mA dummy load and adjust as necessary.

Surge Performance

To obtain a good surge performance, select an appropriate input capacitor that meets different surge tests. Figure 10 shows the half-wave rectifier. Table 2 shows the required capacitance under normal conditions for different surge voltages.

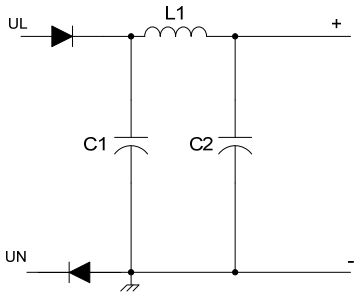

Figure 10: Half-Wave Rectifier

Table 2: Recommended Capacitor Values

Surge voltage	500V	1000V	2000V
C1	1μF	10μF	22μF
C2	1μF	4.7μF	10μF

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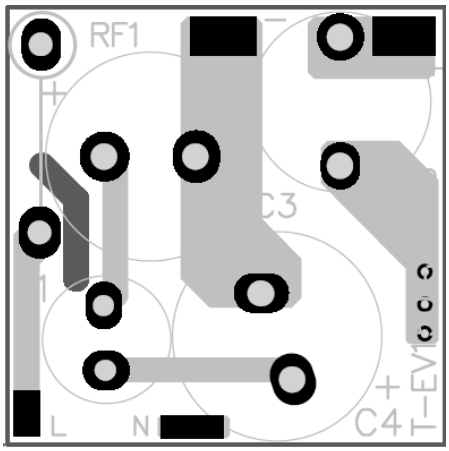
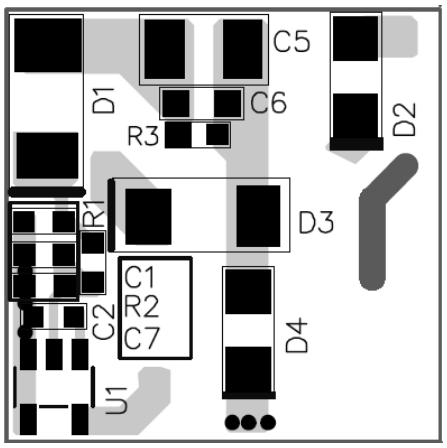
Layout Guide

PCB layout is very important to achieve reliable operation, good EMI, and good thermal performance. Follow these guidelines to optimize performance.

1) Minimize the loop area formed by the input capacitor, IC part, freewheeling diode, inductor and output capacitor.
2) Place the power inductor far away from the input filter.
3) Add a capacitor in the several-hundred pF range between the FB and source pins, as close as to the IC as possible.
4) Connect the exposed pad with the Drain pin to a large copper area to improve thermal performance.



Top



Bottom Layer

Design Example

Below is a design example following the application guidelines given the following specifications:

Table 3: Design Example

V_{IN}	85 to 265Vac
V_{OUT}	5V
I_{OUT}	200mA

Figure 12 shows the detailed application schematic. The Typical Performance Characteristics section lists typical performance and circuit waveforms. For more device applications, refer to the related Evaluation Board Datasheets.

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TYPICAL APPLICATION CIRCUITS

Figure 11 shows a typical application example of a 5V, 200mA non-isolated power supply using MP150.

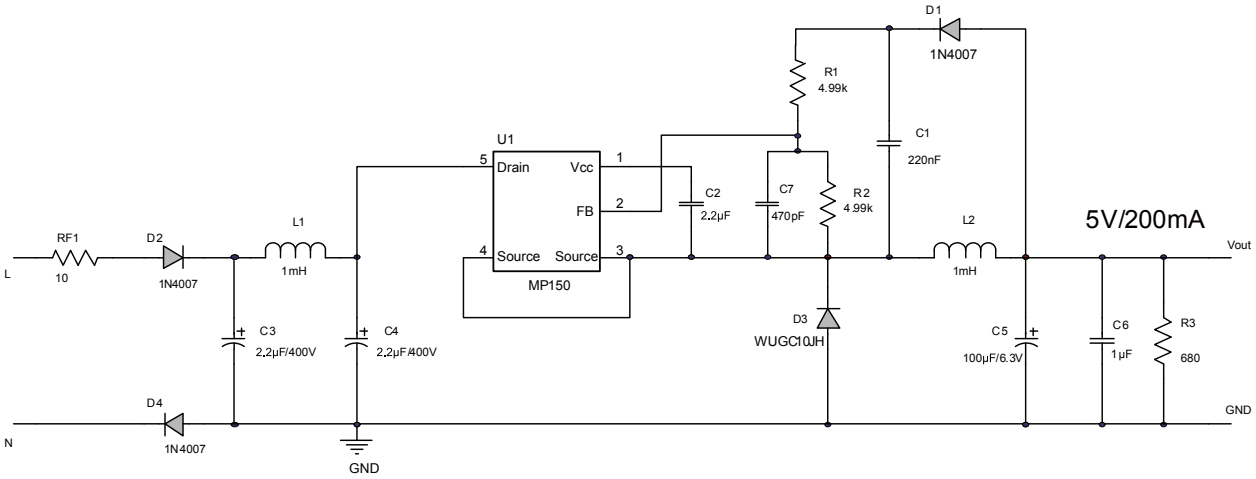

Figure 11: Typical Application Example; 5V, 200mA

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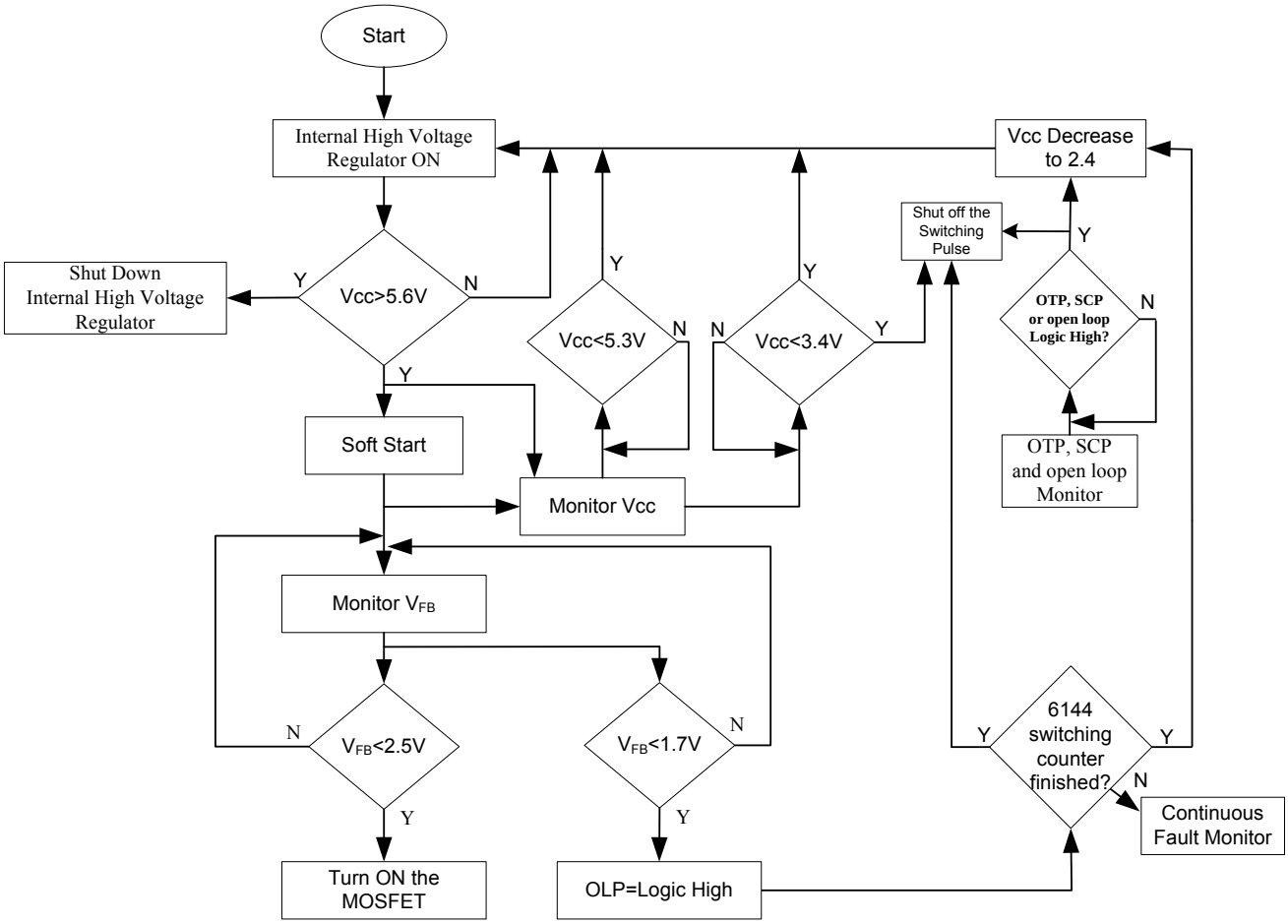
FLOW CHART



UVLO, OTP, SCP, OLP and Open Loop Protection are auto restar

Figure 12: Control Flow Chart

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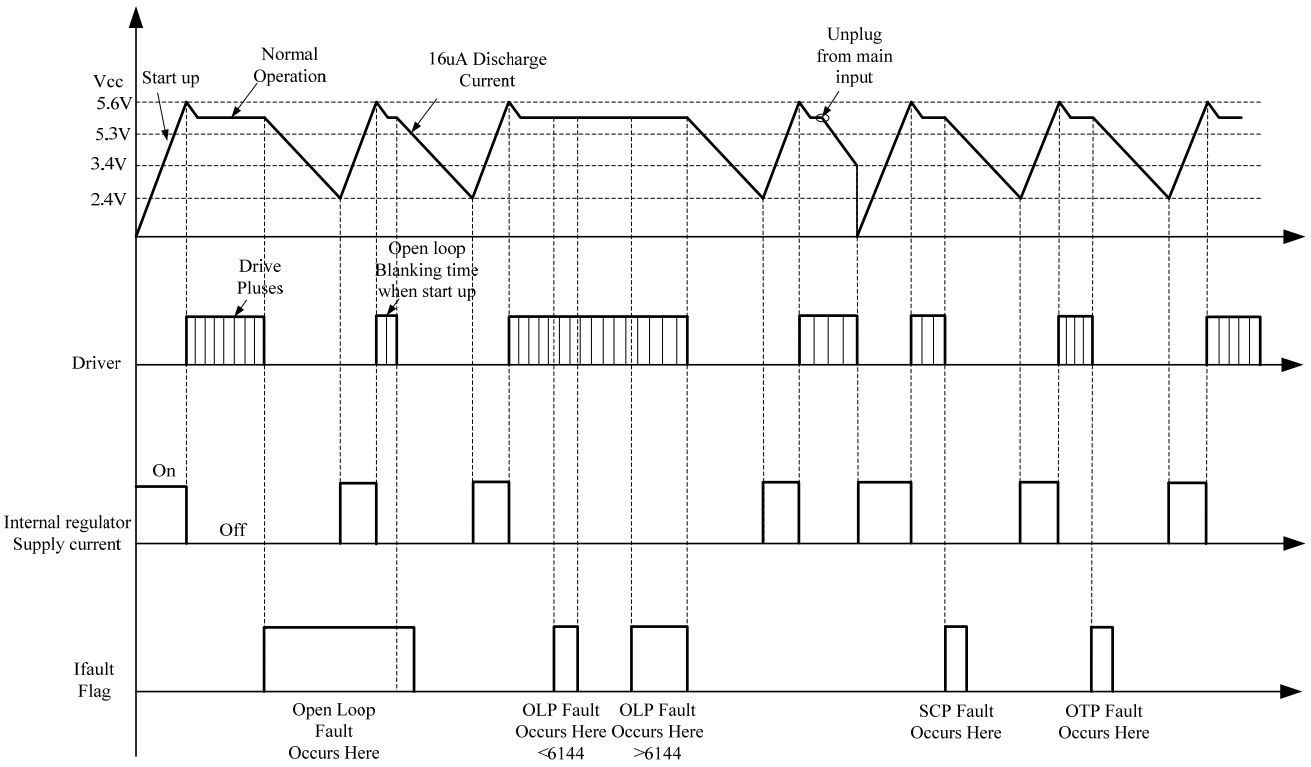

Figure 13: Signal Evolution Resulting from Faults

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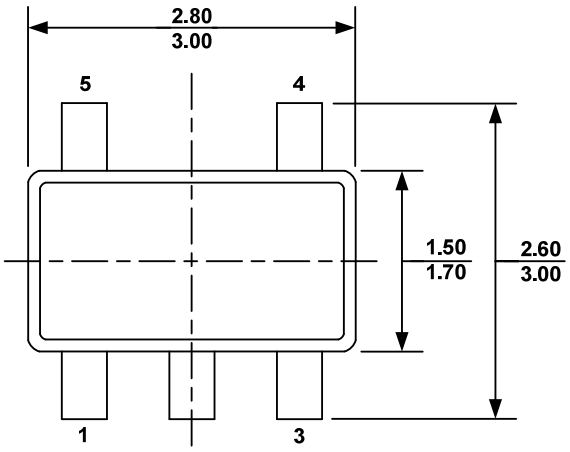
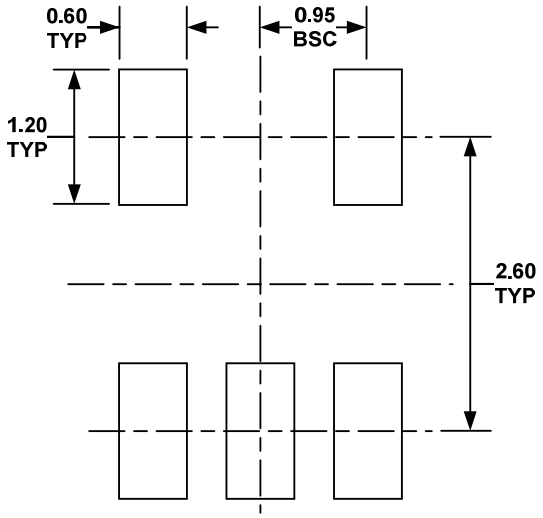


TOP VIEW



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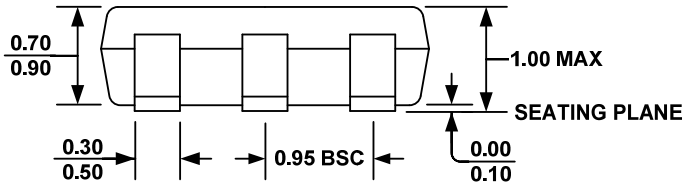
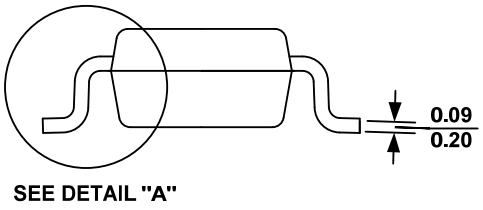
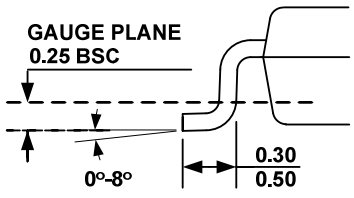


FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AA.
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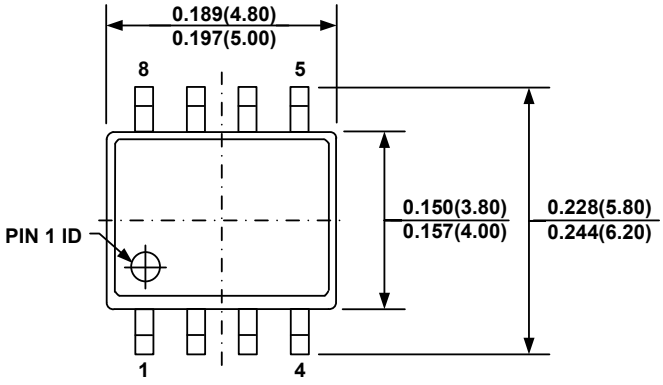
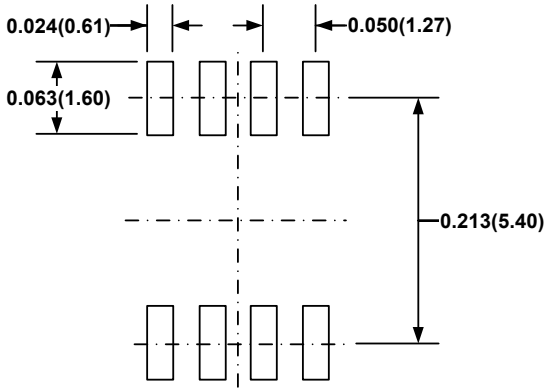


TOP VIEW



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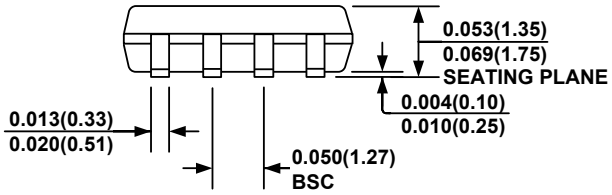
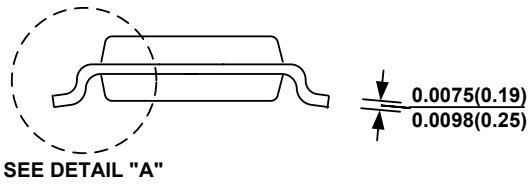
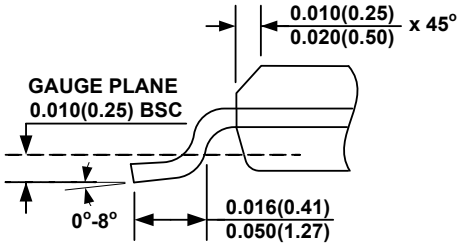


FRONT VIEW



SIDE VIEW



DETAIL "A"

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