MP1498

High-Efficiency, 2A, 16V, 1.4MHz Synchronous, Step-Down Converter

The Future of Analog IC Technology

DESCRIPTION

The MP1498 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in internal power MOSFETs. It offers a very compact solution to achieve 2A continuous output current with excellent load and line regulation over a wide input supply range. The MP1498 has synchronous mode operation for higher efficiency over the output current load range.

Current-mode operation provides a fast transient response and eases loop stabilization.

Protective features include over-current protection, thermal shutdown, and external SS control.

The MP1498 requires a minimal number of readily-available external components and is available in a space-saving 8-pin TSOT23 package.

FEATURES

- Wide 4.5V-to-16V Operating Input Range
- 100mΩ/40mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- Proprietary Switching-Loss–Reduction Technique
- High-Efficiency Synchronous Mode Operation
- Fixed 1.4MHz Switching Frequency
- Can Synchronize to a 300kHz-to-3MHz External Clock
- Externally-Programmable Soft-Start
- OCP and Hiccup
- Thermal Shutdown
- Output Adjustable from 0.8V
- Available in an 8-pin TSOT-23 Package

APPLICATIONS

- Notebook Systems and I/O Power
- Digital Set-Top Boxes
- Flat-Panel Televisions and Monitors
- Distributed Power Systems

All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit MPS website under Products, Quality Assurance page.

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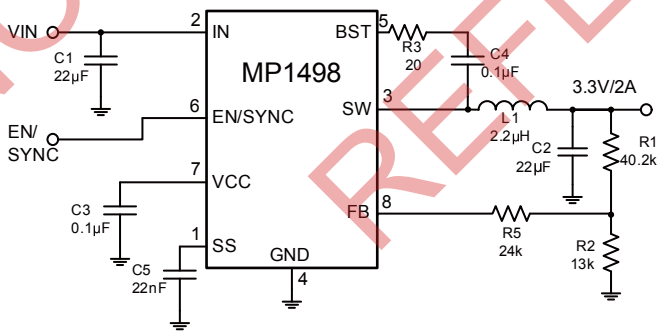
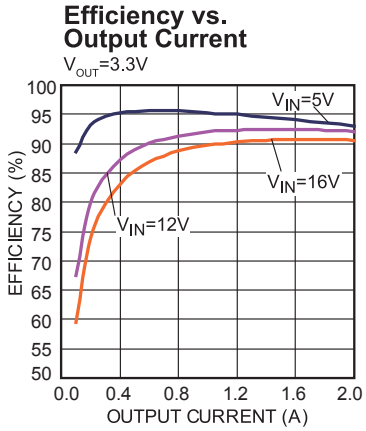
TYPICAL APPLICATION





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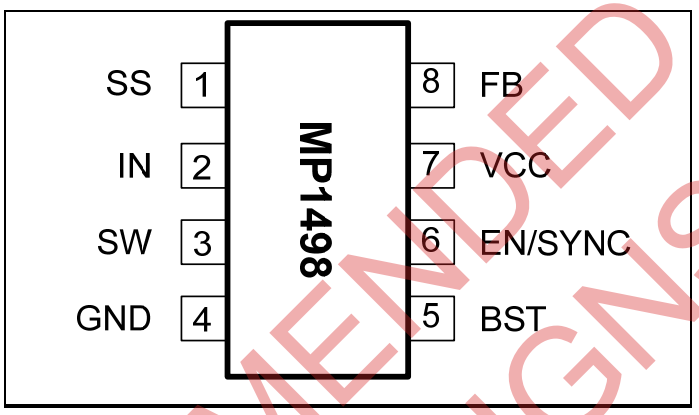
ORDERING INFORMATION

Part Number*	Package	Top Marking
MP1498DJ	TSOT-23-8	ADU

For Tape & Reel, add suffix –Z (e.g. MP1498DJ–Z);
For RoHS, compliant packaging, add suffix –LF (e.g. MP1498DJ–LF–Z).

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} .....-0.3V to 17V
V_{SW} ...-0.3V (-5V for <10ns) to 17V (19V for 5ns)
V_{BST} ..... V_{SW}+6V
All Other Pins ..... -0.3V to 6V (2)
Continuous Power Dissipation (T_A = +25°C) (3)
..... 1.25W
Junction Temperature .....150°C
Lead Temperature .....260°C
Storage Temperature..... -65°C to 150°C

Recommended Operating Conditions (4)

Supply Voltage V_{IN} .....4.5V to 16V
Output Voltage V_{OUT}..... 0.8V to V_{IN}–3V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (5) θ_{JA} θ_{JC}

TSOT-23-8..... 100 ..... 55... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) About the details of the EN pin's ABS MAX rating, please refer to Page 9, Enable section.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current (Shutdown)	I_{IN}	V_{EN} = 0V			1	μA
Supply Current (Quiescent)	I_q	V_{EN} = 2V, V_{FB} = 1V		0.8	1	mA
HS-Switch ON Resistance	HS_{RDS-ON}	V_{BST-SW}=5V		100		mΩ
LS-Switch ON Resistance	LS_{RDS-ON}	V_{CC}=5V		40		mΩ
Switch Leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} =12V			1	μA
Current Limit (6)	I_{LIMIT}	Under 40% Duty Cycle	3.4			A
Oscillator Frequency	f_{SW}		1100	1400	1700	kHz
Fold-back Frequency	f_{FB}	V_{FB}= 0V		0.15		f_{SW}
Maximum Duty Cycle (6)	D_{MAX}	V_{FB}=700mV		89		%
Minimum ON Time (6)	τ_{ON_MIN}			40		ns
Sync Frequency Range	f_{SYNC}		0.3		3	MHz
Feedback Voltage	V_{FB}	T_A=25°C	784	800	816	mV
		-40°C<T_A<85°C(7)	780	800	820	
Feedback Current	I_{FB}	V_{FB}=820mV		10	50	nA
EN Rising Threshold	$V_{EN\ RISING}$		1.2	1.4	1.6	V
EN Falling Threshold	$V_{EN\ FALLING}$		1.1	1.25	1.4	V
EN Input Current	I_{EN}	V_{EN}=2V		2		μA
		V_{EN}=0		0		μA
EN Turn Off Delay	EN_{Td-off}			5		μs
V_{IN} Under-Voltage Lockout Threshold-Rising	$INUV_{Vth}$		3.7	3.9	4.1	V
V_{IN} Under-Voltage Lockout Threshold-Hysteresis	$INUV_{HYS}$			650		mV
VCC Regulator	V_{CC}			5		V
VCC Load Regulation		I_{CC}=5mA		3		%
Soft-Start Current	I_{SS}		10	14	18	μA
Thermal Shutdown(6)				150		°C
Thermal Hysteresis(6)				20		°C

Notes:

6) Guaranteed by design.

7) Not tested in production and guaranteed by over-temperature correlation.

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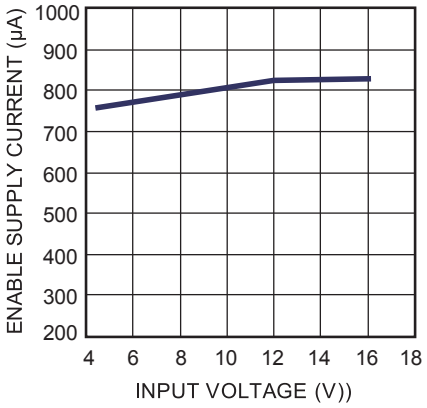
TYPICAL CHARACTERISTICS

V_{IN}=12V, V_{OUT}=3.3V,L=2.2µH,T_A = 25°C, unless otherwise noted.

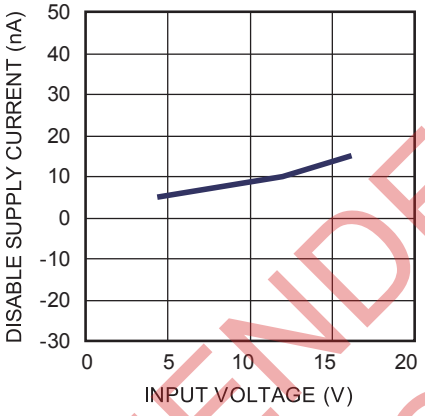
Enabled Supply Current vs. Input Voltage

VFB=1V

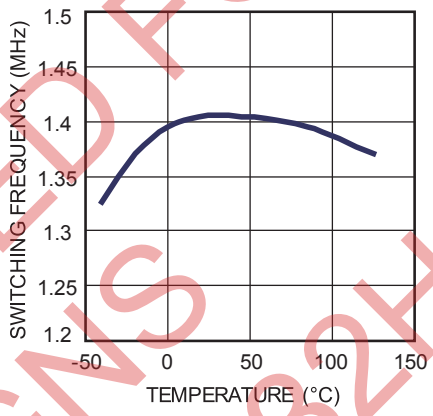


Disabled Supply Current vs. Input Voltage

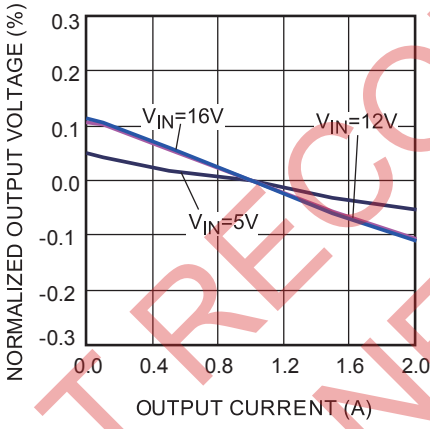
VEN=0V



Switching Frequency vs. Ambient Temperature

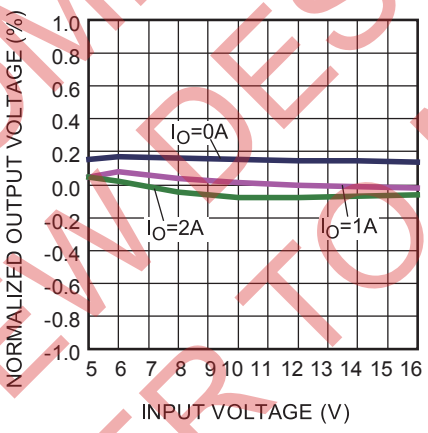


Load Regulation

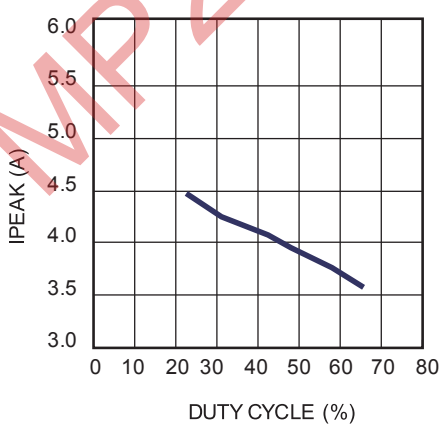


Line Regulation

V_{IN}=5V-16V



Current Limit vs. Duty Cycle



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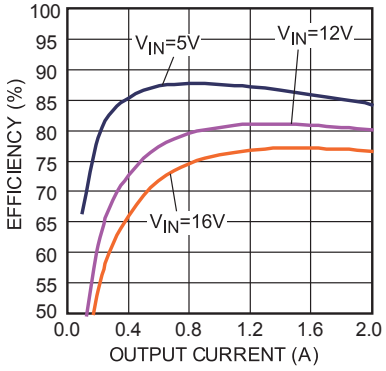
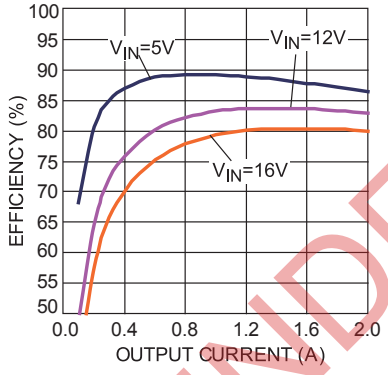
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board in the Design Example section. V_{IN}=12V, V_{OUT}=3.3V,L=2.2µH,T_A = 25°C, unless otherwise noted.

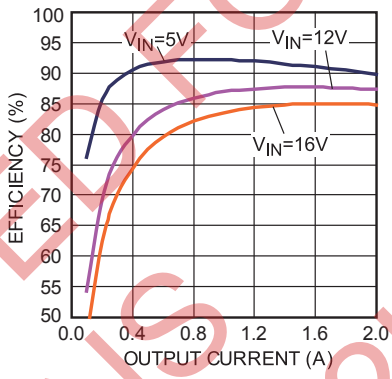
Efficiency vs. Output Current
V_O=1V, L=1µH, I_O=0.1A-2A



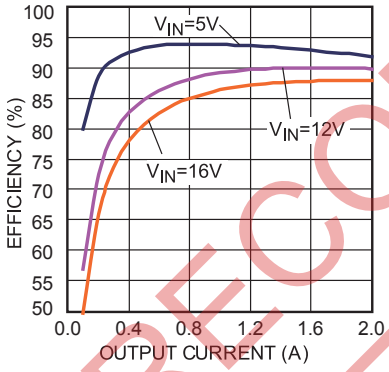
Efficiency vs. Output Current
V_O=1.2V, L=1µH, I_O=0.1A-2A



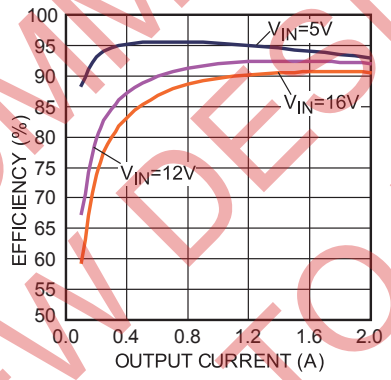
Efficiency vs. Output Current
V_O=1.8V, L=1.5µH, I_O=0.1A-2A



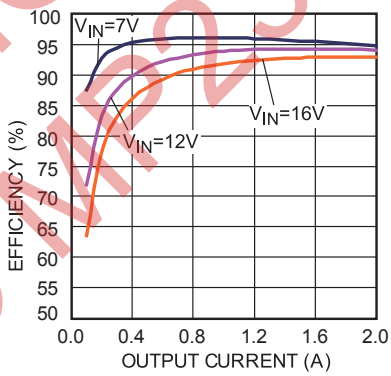
Efficiency vs. Output Current
V_O=2.5V, L=1.5µH, I_O=0.1A-2A



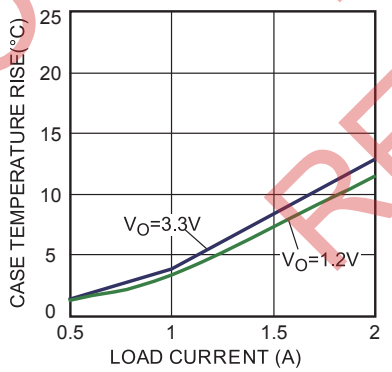
Efficiency vs. Output Current
V_O=3.3V, L=2.2µH, I_O=0.1A-2A



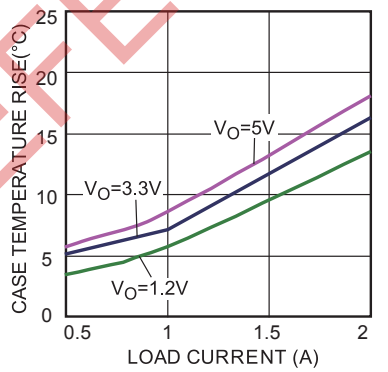
Efficiency vs. Output Current
V_O=5V, L=2.2µH, I_O=0.1A-2A



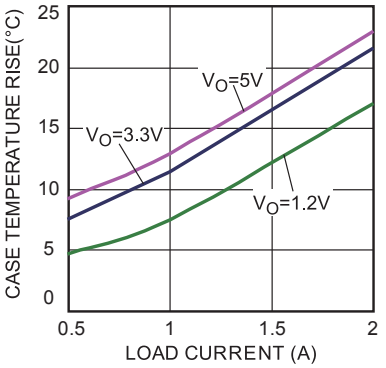
Case Temperature Rise vs. Output Current
V_{IN}=5V,I_{OUT}=0.5A-2A,2 layers PCB, size: 6.35cm×4.83cm



Case Temperature Rise vs. Output Current
V_{IN}=12V,I_{OUT}=0.5A-2A,2 layers PCB, size: 6.35cm×4.83cm



Case Temperature Rise vs. Output Current
V_{IN}=16V,I_{OUT}=0.5A-2A,2 layers PCB, size: 6.35cm×4.83cm



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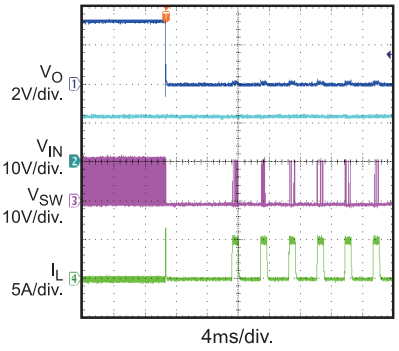
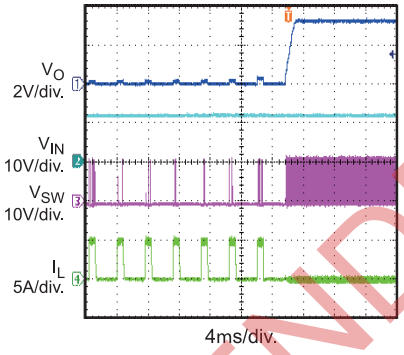
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section. V_{IN}=12V, V_{OUT}=3.3V,L=2.2µH,T_A = 25°C, unless otherwise noted.

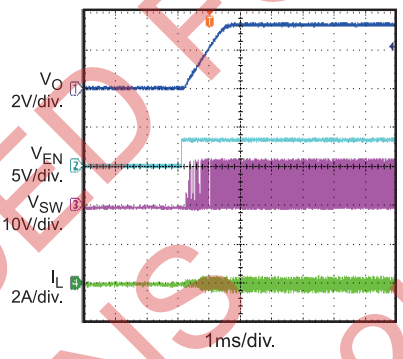
Short Entry
I_{OUT} = 0A



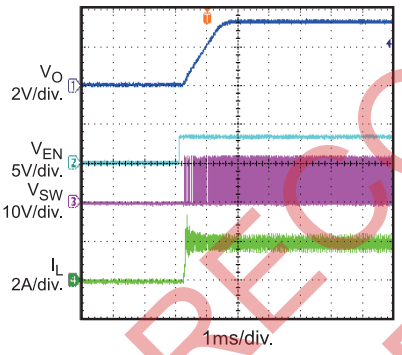
Short Recovery
I_{OUT} = 0A



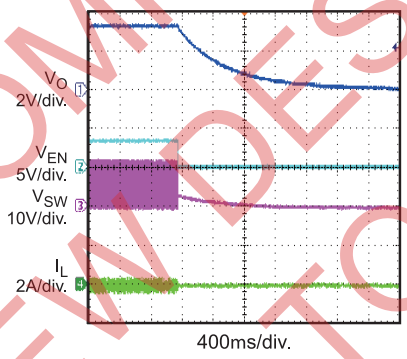
Startup through Enable
I_{OUT} = 0A



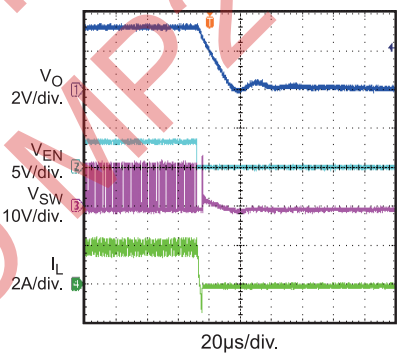
Startup through Enable
I_{OUT} = 2A



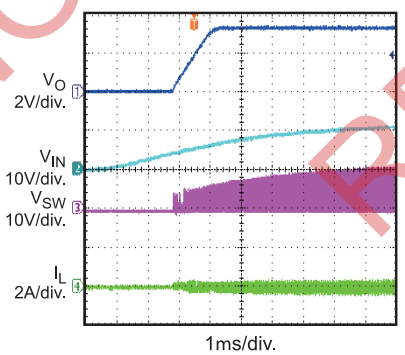
Shutdown through Enable
I_{OUT} = 0A



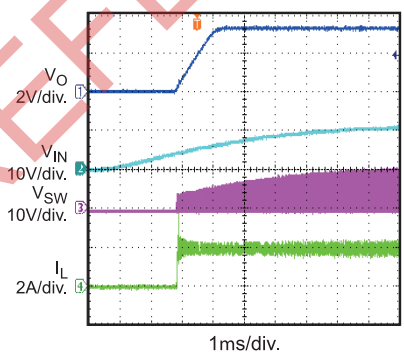
Shutdown through Enable
I_{OUT} = 2A



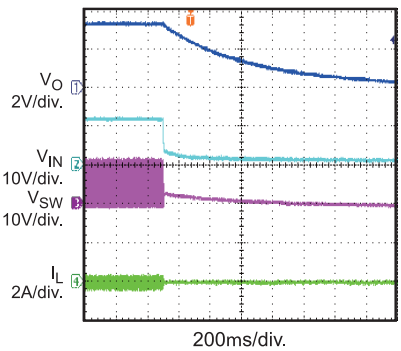
Startup through Input Voltage
I_{OUT} = 0A



Startup through Input Voltage
I_{OUT} = 2A



Shutdown through Input Voltage
I_{OUT} = 0A



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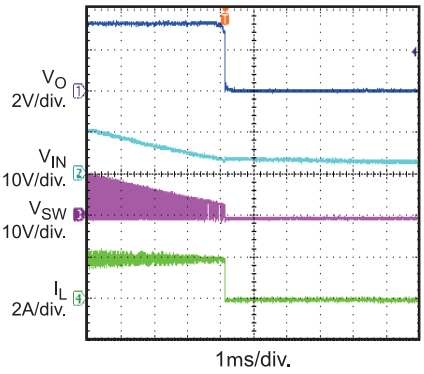
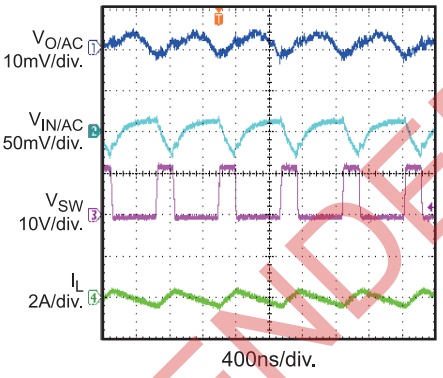
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section.
V_{IN}=12V, V_{OUT}=3.3V,L=2.2µH,T_A = 25°C, unless otherwise noted.

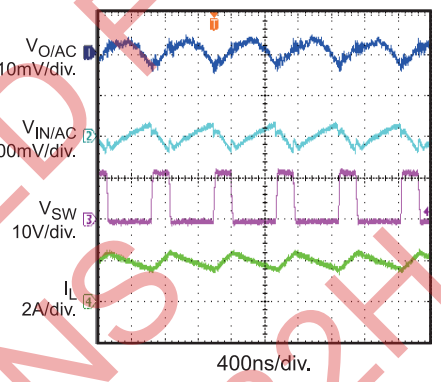
Shutdown through Input Voltage
I_{OUT} = 2A



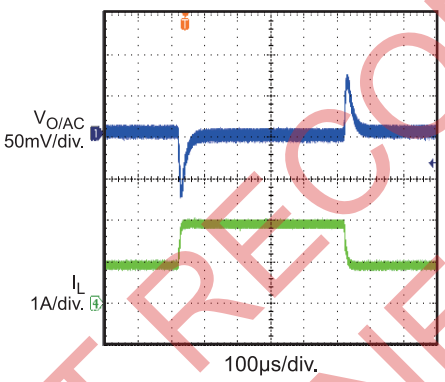
Input Ripple
I_{OUT} = 0A



Output Ripple
I_{OUT} = 2A



Load Transient Reponse
I_{OUT} = 1A-2A



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PIN FUNCTIONS

Package Pin #	Name	Description
1	SS	Soft-Start. Connect an external capacitor to program the soft start time for the switch-mode regulator.
2	IN	Supply Voltage. The IN pin supplies power for internal MOSFET and regulator. The MP1498 operates from a +4.5V to +16V input rail. Requires a low-ESR, and low-inductance capacitor (C1) to decouple the input rail. Place the input capacitor very close to this pin and connect it with wide PCB traces and multiple vias.
3	SW	Switch Output. Connect this pin to the inductor and bootstrap capacitor. This pin is driven up to the VIN voltage by the high-side switch during the PWM duty cycle ON time. The inductor current drives the SW pin negative during the OFF time. The low-side switch's ON-resistance and the internal body diode fix the negative voltage. Use wide PCB traces and multiple vias.
4	GND	System Ground. The regulated output voltage reference ground. Connect to GND with copper and vias.
5	BST	Bootstrap. Connect a capacitor between SW and BST pins to form a floating supply across the high-side switch driver.
6	EN/SYNC	Enable. EN=high to enable the MP1498. Apply an external clock to change the switching frequency. For automatic start-up, connect EN pin to V_{IN} with 100KΩ resistor.
7	VCC	Internal 5V LDO Output. Powers the driver and control circuits. Decouple with a 0.1μF-0.22μF capacitor. Avoid capacitor values that exceed 0.22μF.
8	FB	Feedback. An external resistor divider from the output to GND, tapped to the FB pin, sets the output voltage. The comparator lowers the oscillator frequency linearly with the FB voltage. It is recommended to place the resistor divider as close to FB pin as possible. Avoid placing vias on the FB traces.

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BLOCK DIAGRAM

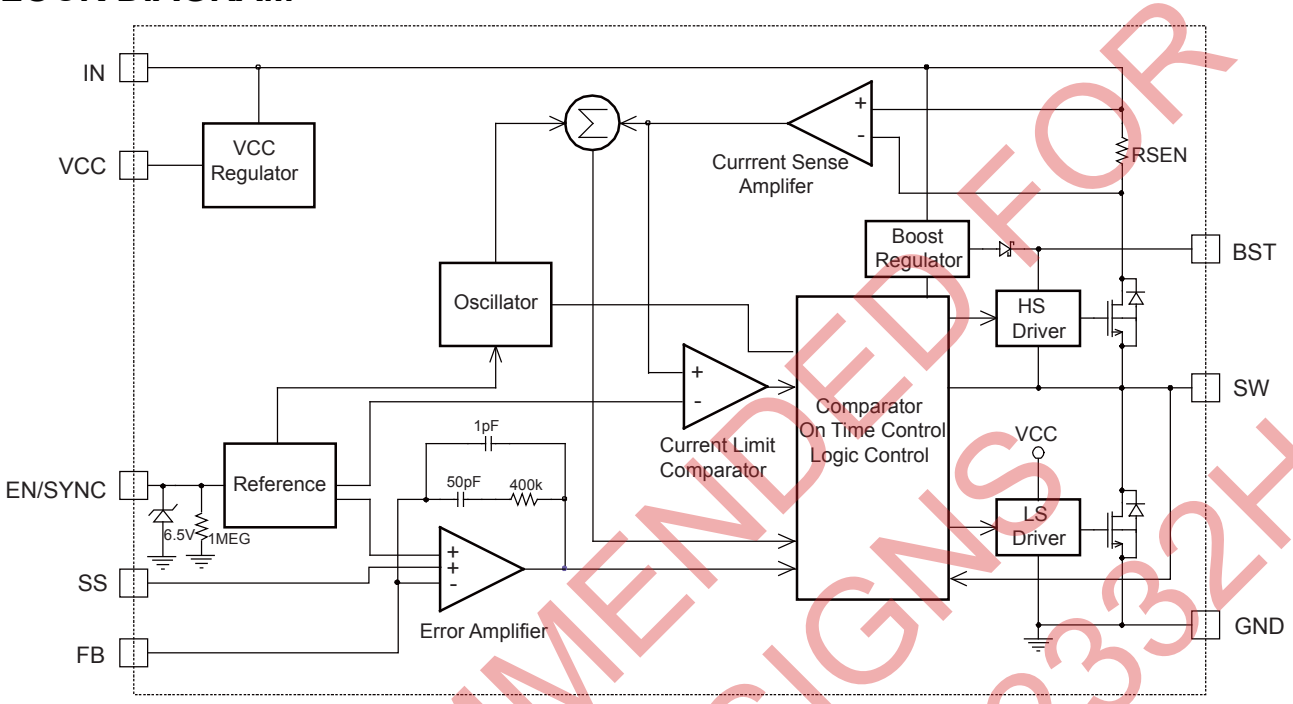

Figure 1: Functional Block Diagram

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OPERATION

The MP1498 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs. It offers a very compact solution to achieve a continuous 2A output current with excellent load and line regulation over a wide input supply range.

The MP1498 operates in a fixed-frequency, peak-current–control mode to regulate the output voltage. The internal clock initiates a PWM cycle. The integrated high-side power MOSFET turns on and remains on until its current reaches the value set by the COMP voltage. When the power switch is off, it remains off until the next clock cycle starts. If the current in the power MOSFET does not reach the COMP set current value within 89% of one PWM period, the power MOSFET will be forced to turn off. The high-side power MOSFET has an 80ns minimum off time to refresh the BST voltage.

Internal Regulator

The 5V internal regulator powers most of the internal circuitries. This regulator takes the V_{IN} input and operates in the full V_{IN} range. When V_{IN} exceeds 5.0V, the output of the regulator is in full regulation. When V_{IN} is below 5.0V, the output decreases and requires a 0.1μF ceramic decoupling capacitor.

Error Amplifier

The error amplifier compares the FB pin voltage to the internal 0.8V reference (REF) and outputs a current proportional to the difference between the two. This output current then charges or discharges the internal compensation network to form the COMP voltage, which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

Enable/SYNC Control

EN is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator, drive it low to turn it off after a 5μs delay. An internal 1MΩ resistor from EN to GND allows EN to float to shut down the chip.

The EN pin is clamped internally using a 6.5V series-Zener-diode as shown in Figure 2. Connecting the EN pin through a pullup resistor to any voltage connected to V_{IN} limits the EN input current to less than 100μA.

For example, when connecting V_{IN} to a 12V source, $R_{PULLUP} \geq [(12V–6.5V) \div 100\mu A = 55k\Omega]$.

Connecting the EN pin directly to a voltage source without any pullup resistor requires limiting the amplitude of the voltage source to below 6.5V to prevent damaging the Zener diode.

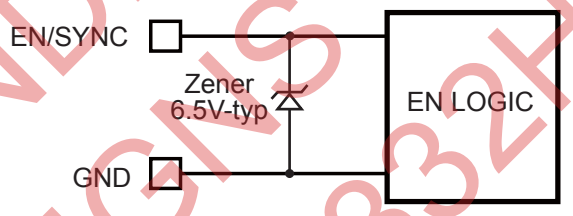

Figure 2: Zener Diode Circuit

For external clock synchronization, connect a clock with a frequency range of 300kHz to 3MHz after setting the output voltage: The internal clock rising edge will synchronize with the external clock's rising edge. Select an external clock signal with a pulse-width less than 700ns.

Under-Voltage Lockout

The MP1498 has under-voltage lockout (UVLO) protection. When VCC exceeds the UVLO rising threshold voltage, the MP1498 powers up. It shuts off when the VCC voltage falls below the UVLO falling threshold voltage. This is non-latch protection.

The MP1498 is disabled when the input voltage falls below 3.25V. If an application requires a higher UVLO, use the EN pin as shown in Figure 3 to adjust the input voltage UVLO by using two external resistors. For best results, use the enable resistors to set the UVLO falling threshold (VSTOP) above 4.5V. Set the rising threshold (VSTART) to provide enough hysteresis to allow for any input supply variations.

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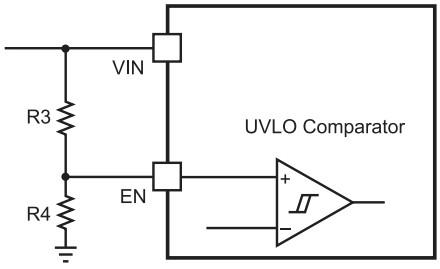

Figure 3: Adjustable UVLO

External Soft-Start

The MP1498 employs a soft-start (SS) mechanism to smooth the output during power-up. When the EN pin goes high, an internal current source (14μA) charges the SS capacitor. The SS capacitor voltage overtakes the REF voltage to the PWM comparator. The output voltage smoothly ramps up with the SS voltage. Once the SS voltage reaches the same level as the REF voltage, it keeps ramping up while V_{REF} takes over the PWM comparator. At this point, the soft-start finishes and the device enters steady state operation.

If the output is pre-biased to a certain voltage during startup, the IC will disable the high-side and low-side switches until the voltage on the internal soft-start capacitor exceeds the sensed output voltage at the FB pin.

The SS capacitor value can be determined as follows:

$$C_{SS}(nF) = \frac{\tau_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} \quad (1)$$

If the output capacitors have large capacitances, avoid setting a short SS time to avoid hitting the current limit during SS. Use a minimum value of 4.7nF if the output capacitance value is larger than 330μF.

Over-Current Protection and Hiccup

The MP1498 has a cycle-by-cycle over-current limit that protects against the inductor current peak value exceeding the set current limit threshold. Under-voltage protection (UVP) triggers if the FB voltage drops below the under-voltage (UV) threshold—typically 50% below the reference. Once UVP triggers, the MP1498 enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-shorted to ground. The average short-circuit current falls to alleviate thermal issues and to protect the regulator. The MP1498 exits hiccup mode once the over-current condition is removed.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C, it shuts down the whole chip. When the temperature drops below its lower threshold (typically 130°C) the chip is enabled again.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection with a rising threshold of 2.2V and a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by V_{IN} through D1, M1, R3, C4, L1 and C2 (Figure 4). If (V_{IN}-V_{SW}) exceed 5V, U1 will regulate M1 to maintain a 5V BST voltage across C4. A 20Ω resistor placed between SW and BST cap is strongly recommended to reduce SW spike voltage.

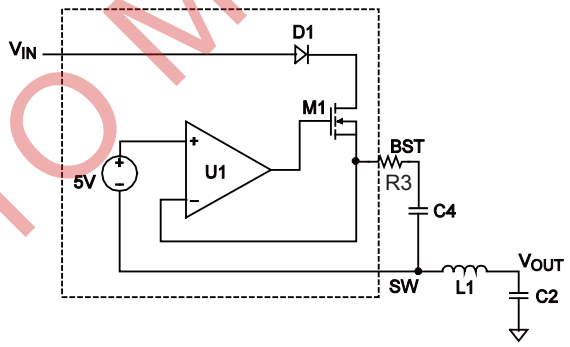

Figure 4: Internal Bootstrap Charging Circuit

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Startup and Shutdown

If both V_{IN} and EN exceed their respective thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries. The frequency needs to fold-back linearly with FB so V_{OUT} starts up smoothly.

Three events can shut down the chip: EN low, V_{IN} low, and thermal shutdown. For the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage (see Typical Application on page 1). The feedback resistor (R1) sets the feedback loop bandwidth in conjunction with the internal compensation capacitor. R2 is then:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.8V} - 1}$$

The T-type network shown in Figure 5 is highly recommended.

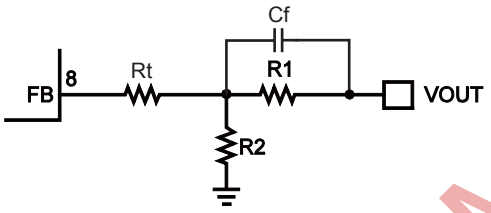

Figure 5: T-Type Network

Table 1 lists the recommended T-type resistors value for common output voltages.

Table 1: Resistor Values for Common Output Voltages

V_{OUT}(V)	R1(kΩ)	R2(kΩ)	Rt(kΩ)	Cf(pF)	L(μH)
1	20.5	84.5	140	0	1
1.2	30.1	61.9	140	0	1
1.8	40.2	32.4	59	15	1.5
2.5	40.2	19.1	43	15	1.5
3.3	40.2	13	24	15	2.2
5	40.2	7.68	24	15	2.2

Selecting the Inductor

Use a 1μH-to-10μH inductor with a DC current rating of at least 25% percent higher than the maximum load current for most applications. For highest efficiency, select an inductor with a DC resistance less than 15mΩ. For most designs, calculate the inductance value as:

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is the inductor ripple current.

Choose an inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Use a larger inductance for improved light-load efficiency.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore requires a capacitor supply the AC current to the step-down converter while maintaining the DC input voltage. Use low-ESR capacitors for the best performance, such as ceramic capacitors with X5R or X7R dielectrics that have low ESR and small temperature coefficients. For most applications, use a 22μF capacitor.

The input capacitor (C1) requires an adequate ripple current rating because it absorbs the input switching current. Estimate the RMS current in the input capacitor as:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at $V_{IN}=2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose the input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, place a small, high-quality, ceramic capacitor—e.g. 0.1μF—as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to prevent excessive input voltage ripple. Estimate the input voltage ripple caused by the capacitance as:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

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Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where L_1 is the inductor value and R_{ESR} is the equivalent series resistance of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency. The capacitance also causes the majority of the output voltage ripple. For simplification, estimate the output voltage ripple as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP1498 can be optimized for a wide range of capacitance and ESR values.

External Bootstrap Diode

An external bootstrap diode can enhance the efficiency of the regulator, given the following conditions:

- V_{OUT} is 5V or 3.3V; and
- Duty cycle is high: $D = \frac{V_{OUT}}{V_{IN}} > 65\%$

In these cases, connect an external BST diode from the VCC pin to BST pin, as shown in Figure 6

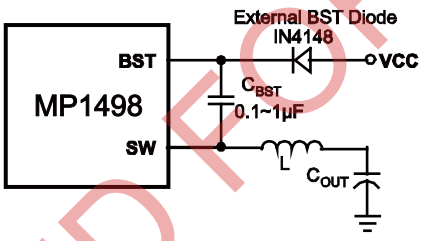

Figure 6: Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the BST capacitor is 0.1μF to 1μF.

PC Board Layout [8]

PCB layout is very important to achieve stable operation especially for VCC capacitor and input capacitor placement. For best results, follow these guidelines:

1) Connect the GND pin directly to a large ground plane. Add vias near the GND pin if the bottom layer is a ground plane.
2) Place the VCC capacitor as close to the VCC and GND pins as possible. Make the trace length of the VCC pin→VCC capacitor anode→VCC capacitor cathode→ IC GND pin as short as possible.
3) Place the ceramic input capacitor close to IN and GND pins. Keep the connection of input capacitor and IN pin as short and wide as possible.
4) Route SW, BST net away from sensitive analog areas such as FB. Avoid routing the SW, BST trace under the IC.
5) Place the T-type feedback resistor (R5) close to chip to ensure that the trace to the FB pin is as short as possible.

Notes:

8) The recommended layout is based on the Figure 7 Typical Application circuit on the next page.

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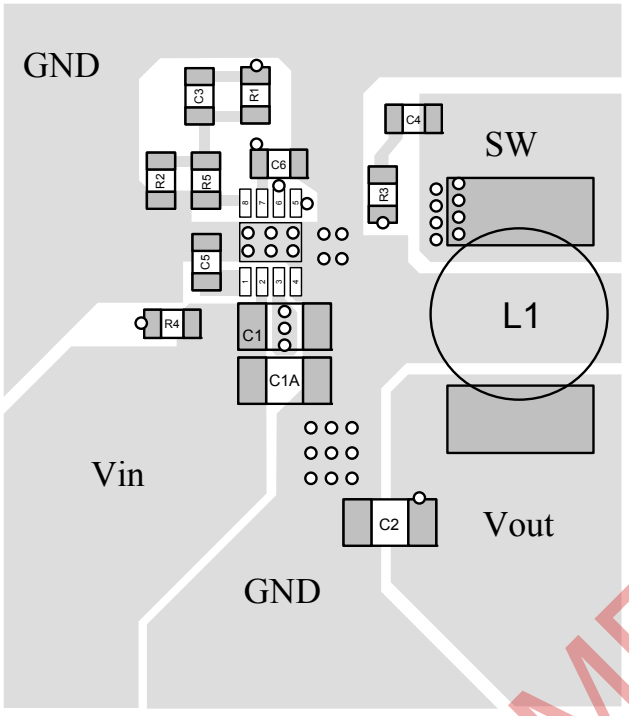

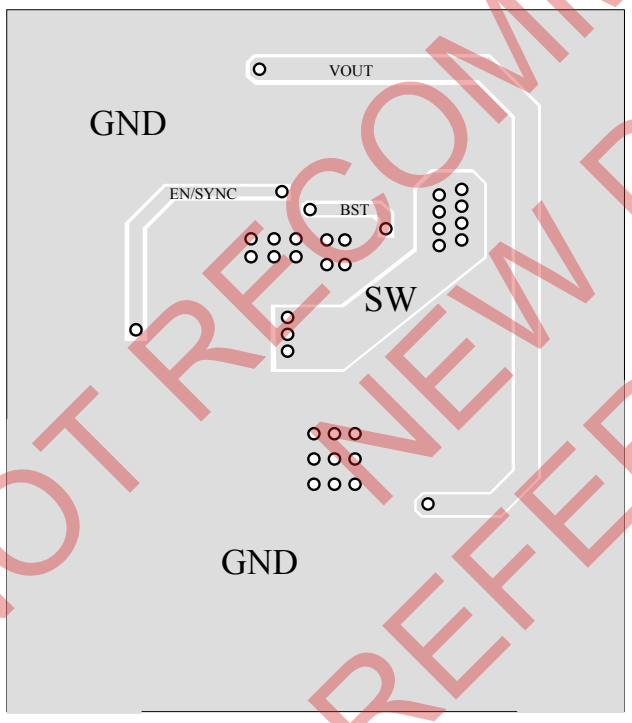

Design Example

Below is a design example following the application guidelines for the specifications:

Table 2: Design Example

V_{IN}	12V
V_{OUT}	3.3V
Io	2A

Figure 8 shows the detailed application schematic. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more device applications, please refer to the related Evaluation Board Datasheets.

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TYPICAL APPLICATION CIRCUITS

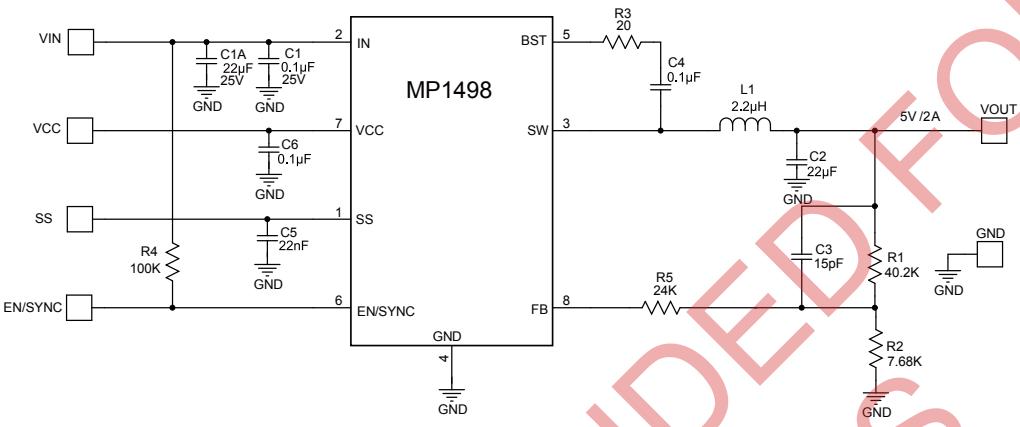

Figure 7: V_{IN}=12V, 5V/2A Output

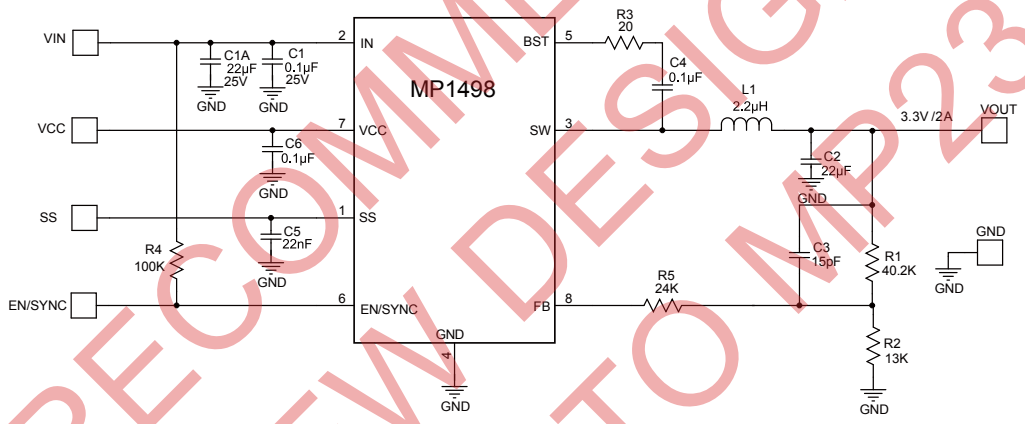

Figure 8: V_{IN}=12V, 3.3V/2A Output

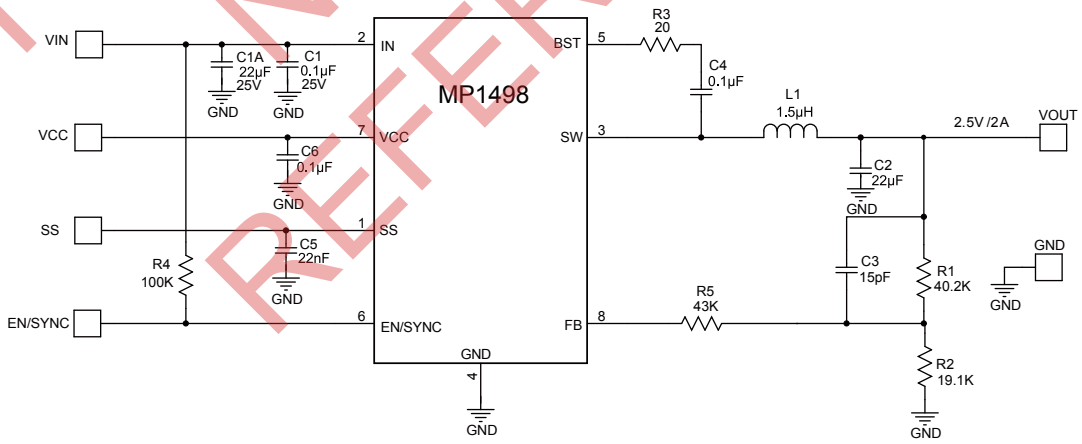

Figure 9: V_{IN}=12V, 2.5V/2A Output

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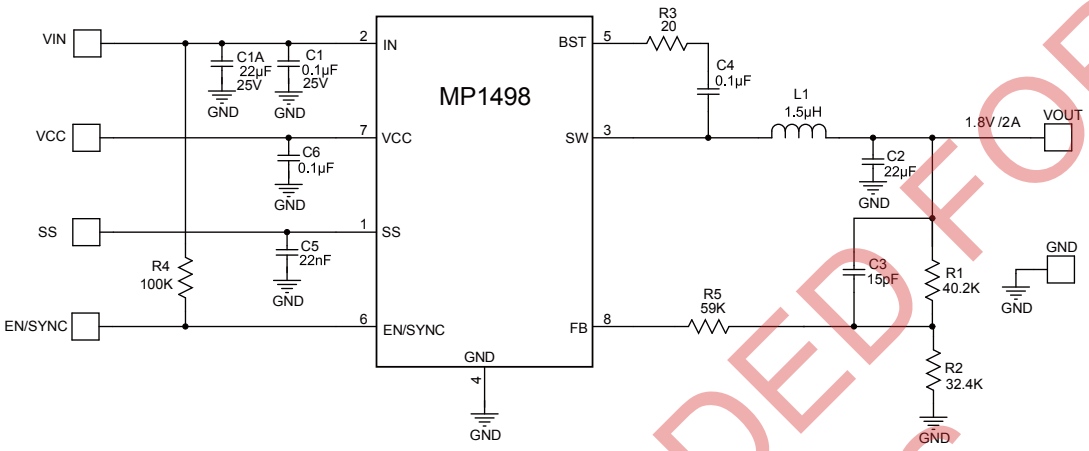

Figure 10: V_{IN}=12V, 1.8V/2A Output

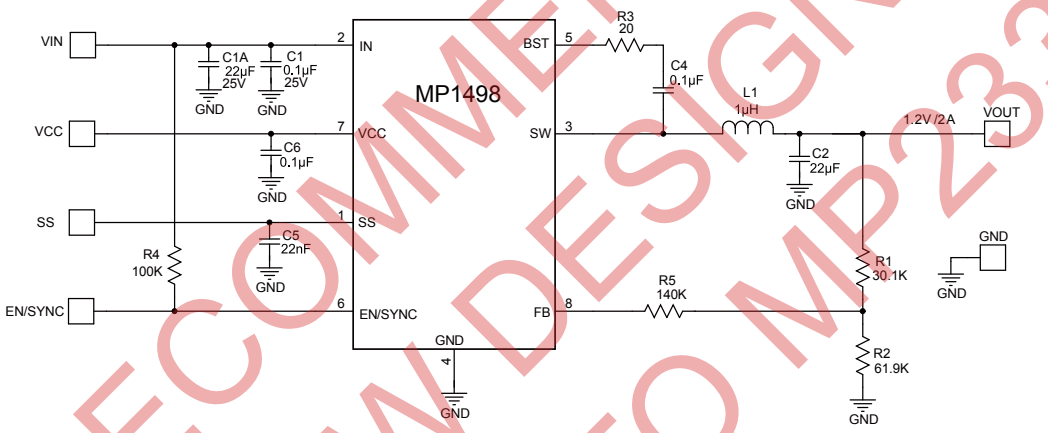

Figure 11: V_{IN}=12V, 1.2V/2A Output

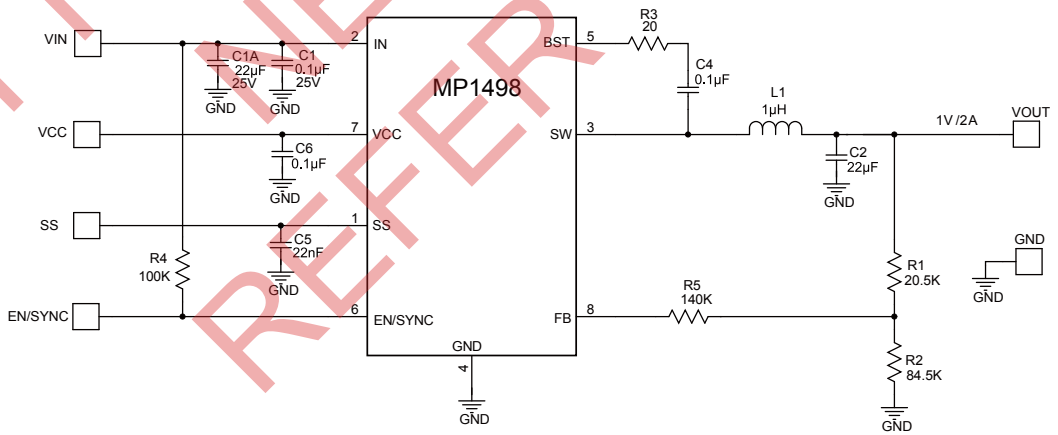

Figure 12: V_{IN}=12V, 1V/2A Output

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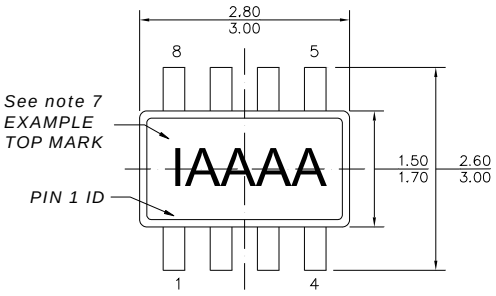
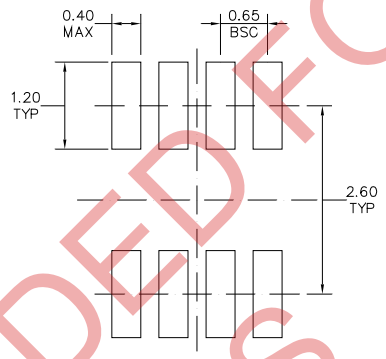
PACKAGE INFORMATION

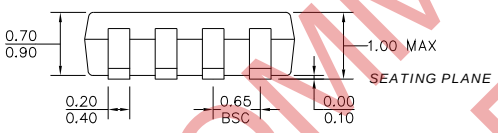
TSOT23-8



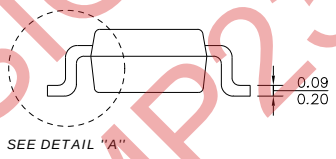
TOP VIEW



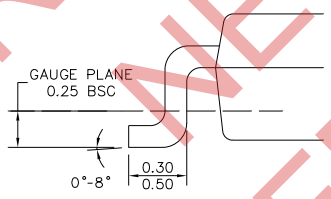
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-193, VARIATION BA.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

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