MP1474S

High-Efficiency, 2A, 16V, 500kHz Synchronous, Step-Down Converter

The Future of Analog IC Technology

DESCRIPTION

The MP1474S is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs. It offers a compact solution to achieve a 2A continuous output current with excellent load and line regulation over a wide input-supply range. The MP1474S has synchronous-mode operation for higher efficiency over the output current-load range.

Current-mode operation provides fast, transient response and eases loop stabilization.

Full protection features include over-current protection (OCP) and thermal shutdown (TSD).

The MP1474S requires a minimal number of readily available, standard, external components and is available in a space-saving 8-pin TSOT23 package.

FEATURES

- Wide 4.5V to 16V Operating-Input Range
- 150mΩ/70mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- High-Efficiency Synchronous-Mode Operation
- Fixed 500kHz Switching Frequency
- Synchronizes from a 300kHz to 2MHz External Clock
- Power-Save Mode at Light Load
- Internal Soft-Start
- Power Good Indicator
- Over-Current Protection and Hiccup
- Thermal Shutdown
- Output Adjustable from 0.8V
- Available in a 8-pin TSOT-23 Package

APPLICATIONS

- Notebook Systems and I/O Power
- Digital Set-Top Boxes
- Flat-Panel Television and Monitors
- Distributed Power Systems

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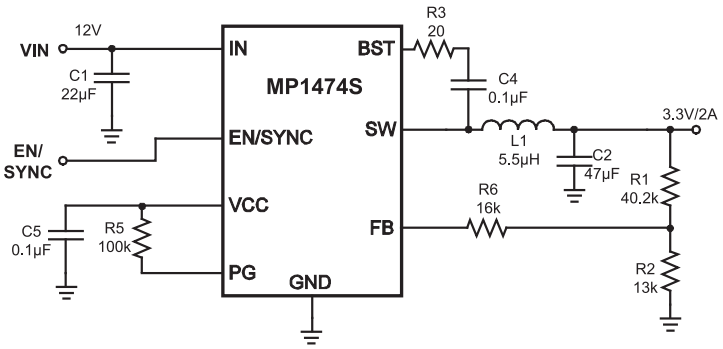
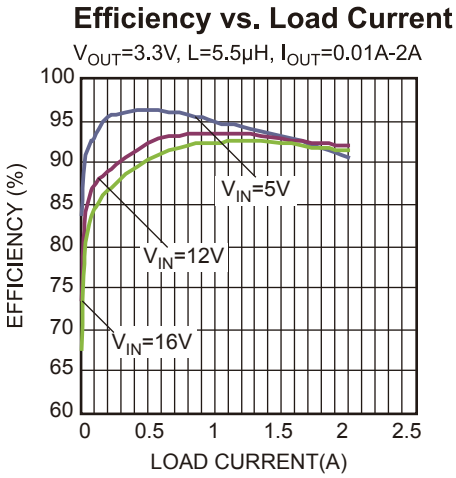
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP1474SGJ	TSOT23-8	*See Below*

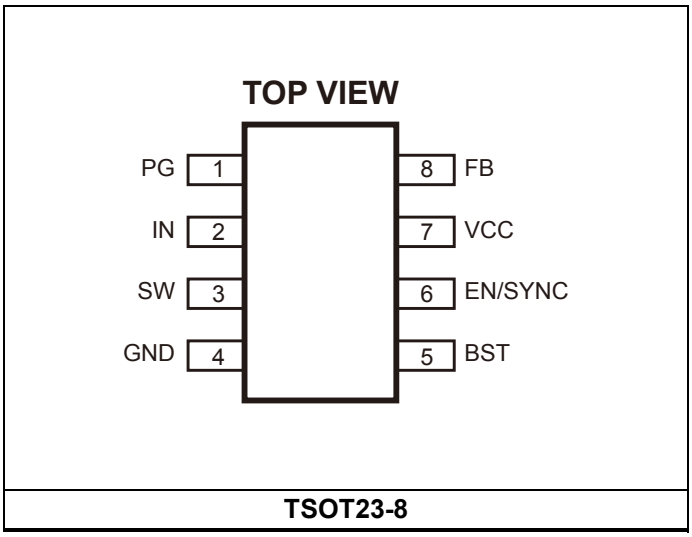
* For Tape & Reel, add suffix –Z (e.g. MP1474SGJ–Z).

TOP MARKING

|ALDY

ALD: product code of MP1474SGJ;
Y: year code;

PACKAGE REFERENCE



TSOT23-8

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ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to 17V
V_{SW} .....
-0.3V (-5V for <10ns) to 17V (19V for <10ns)
V_{BST} ..... V_{SW}+6V
All Other Pins.....-0.3V to 6V (2)
Continuous Power Dissipation (T_A = +25°C) (3)
.....1.25W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature.....-65°C to 150°C

Recommended Operating Conditions (4)

Supply Voltage V_{IN} ..... 4.5V to 16V
Output Voltage V_{OUT}..... 0.8V to V_{IN}*D_{MAX}
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (5) θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}	
TSOT23-8	100	55	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) About the details of EN/SYNC pin's ABS MAX rating, please refer to Page 12, Enable/SYNC control section.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted. Typical value is tested at T_J=+25°C

Parameter	Symbol	Condition		Min	Typ	Max	Units
Supply Current (Shutdown)	I_{IN}	V_{EN} = 0V			2		μA
Supply Current (Quiescent)	I_q	V_{EN} = 2V, V_{FB} = 1V			0.5	1	mA
HS Switch-On Resistance	HS_{RDS-ON}	V_{BST-SW}=5V			150		mΩ
LS Switch-On Resistance	LS_{RDS-ON}	V_{CC} =5V			70		mΩ
Switch Leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} =12V or 0V				1	μA
Current Limit (6)	I_{LIMIT}	Under 40% Duty Cycle		3			A
Oscillator Frequency	f_{SW}	V_{FB}=0.75V	T_J=+25°C	410	500	630	kHz
			T_J=-40°C to +125°C	350		650	kHz
Foldback Frequency	f_{FB}	V_{FB}<400mV			0.5		f_{SW}
Maximum Duty Cycle	D_{MAX}	V_{FB}=700mV		90	95		%
Minimum On Time(6)	T_{ON-MIN}				40		ns
Sync Frequency Range	f_{SYNC}			0.3		2	MHz
Feedback Voltage	V_{FB}	T_J =25°C		791	807	823	mV
		-40°C<T_J<+125°C (7)		787	807	827	
Feedback Current	I_{FB}	V_{FB}=830mV			10	50	nA
EN Rising Threshold	$V_{EN-RISING}$			1	1.4	1.75	V
EN Falling Threshold	$V_{EN-FALLING}$			0.9	1.25	1.6	V
EN Input Current	I_{EN}	V_{EN}=2V			2		μA
		V_{EN}=0			0		μA
EN Turn-Off Delay	EN_{td-off}				8		μs
Power-Good Rising Threshold	PG_{vth-Hi}				0.9		V_{FB}
Power-Good Falling Threshold	PG_{vth-Lo}				0.85		V_{FB}
Power-Good Delay	PG_{Td}				0.6		ms
Power-Good Sink-Current Capability	V_{PG}	Sink 2mA				0.4	V
Power-Good Leakage Current	$I_{PG-LEAK}$					1	μA
VIN Under-Voltage Lockout Threshold—Rising	$INUV_{Vth}$			3.6	3.9	4.3	V
VIN Under-Voltage Lockout Threshold—Hysteresis	$INUV_{HYS}$				700		mV
VCC Regulator	V_{CC}				5		V
VCC Load Regulation		I_{CC}=5mA			2		%
Soft-Start Period	T_{SS}	Vo from 10% to 90%			1.2		ms
Thermal Shutdown (6)	T_{SD}				150		°C
Thermal Hysteresis (6)	$T_{SD\ HYS}$				20		°C

Notes:

6) Guaranteed by design.

7) Not tested in production; guaranteed by over-temperature correlation.

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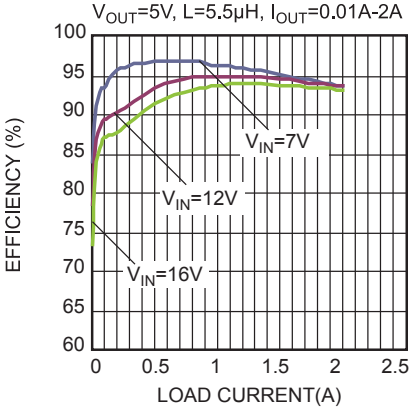
TYPICAL CHARACTERISTICS

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 3.3V, L=5.5µH, T_A = 25°C, unless otherwise noted.

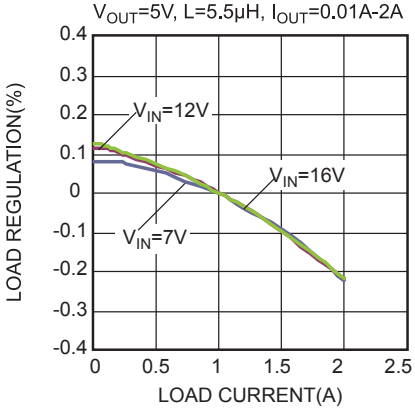
Efficiency vs. Load Current

V_{OUT}=5V, L=5.5µH, I_{OUT}=0.01A-2A



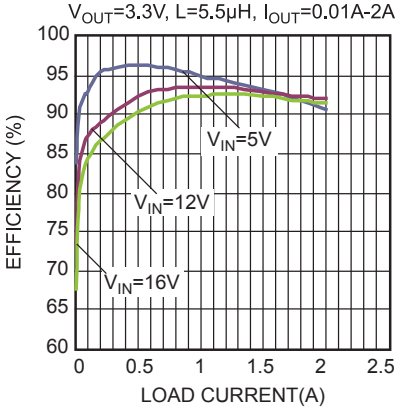
Load Regulation

V_{OUT}=5V, L=5.5µH, I_{OUT}=0.01A-2A



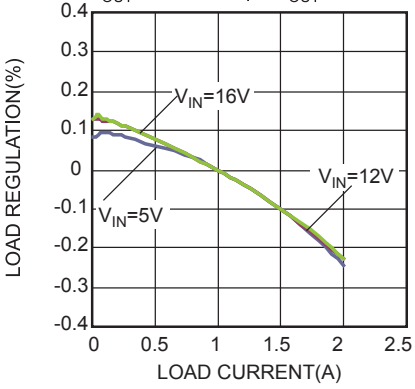
Efficiency vs. Load Current

V_{OUT}=3.3V, L=5.5µH, I_{OUT}=0.01A-2A



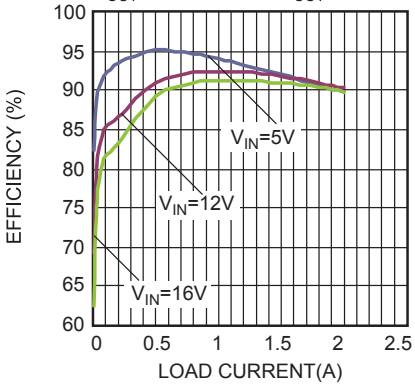
Load Regulation

V_{OUT}=3.3V, L=5.5µH, I_{OUT}=0.01A-2A



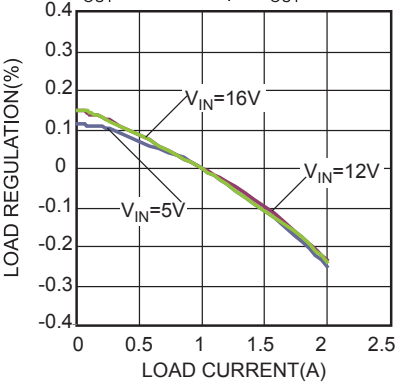
Efficiency vs. Load Current

V_{OUT}=2.5V, L=4.7µH, I_{OUT}=0.01A-2A



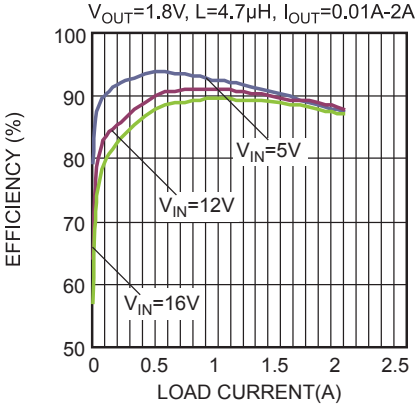
Load Regulation

V_{OUT}=2.5V, L=4.7µH, I_{OUT}=0.01A-2A



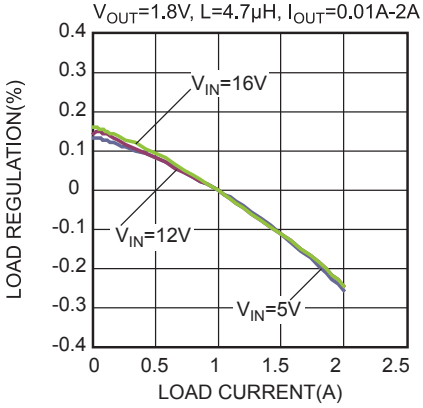
Efficiency vs. Load Current

V_{OUT}=1.8V, L=4.7µH, I_{OUT}=0.01A-2A



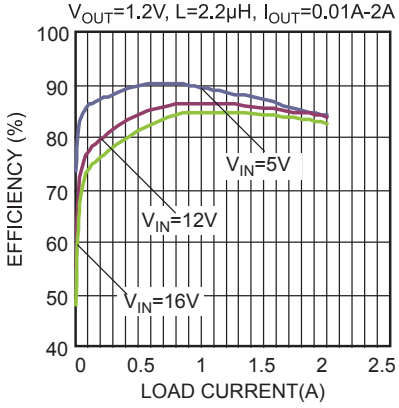
Load Regulation

V_{OUT}=1.8V, L=4.7µH, I_{OUT}=0.01A-2A



Efficiency vs. Load Current

V_{OUT}=1.2V, L=2.2µH, I_{OUT}=0.01A-2A



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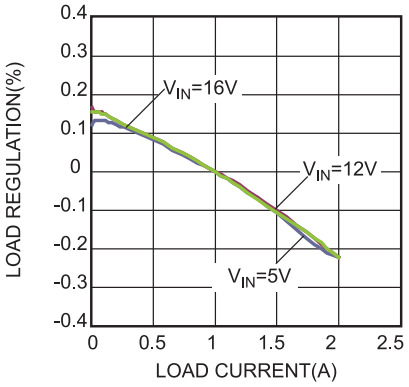
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 3.3V, L=5.5µH, T_A = 25°C, unless otherwise noted.

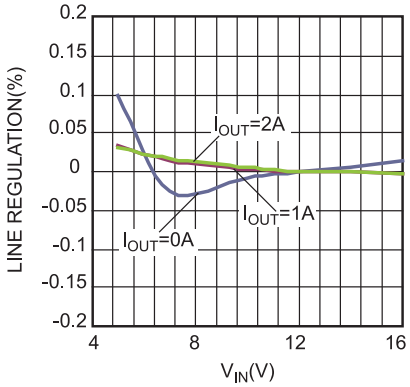
Load Regulation

V_{OUT}=1.2V, L=2.2µH, I_{OUT}=0.01A-2A



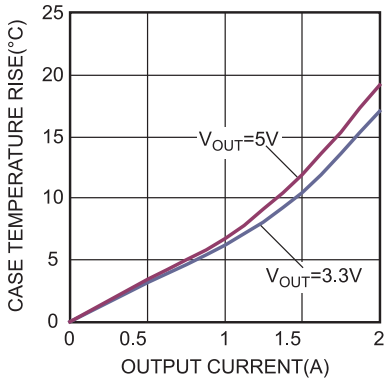
Line Regulation

V_{OUT}=3.3V, V_{IN}=5-16V

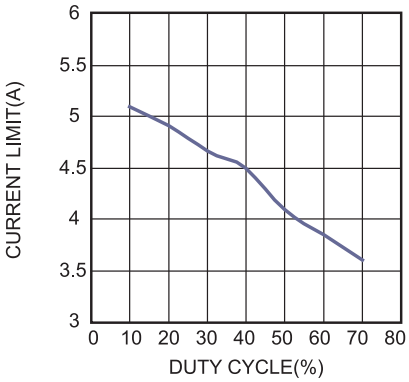


Case Temperature Rise vs. Output Current

I_{OUT}=0A-2A

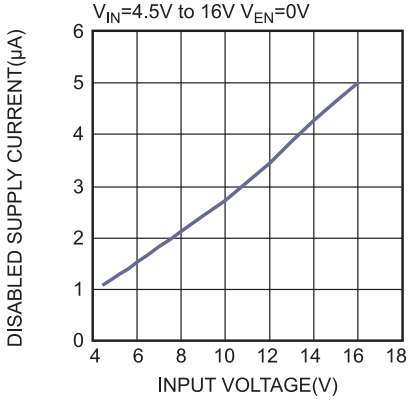


Current Limit vs. Duty Cycle



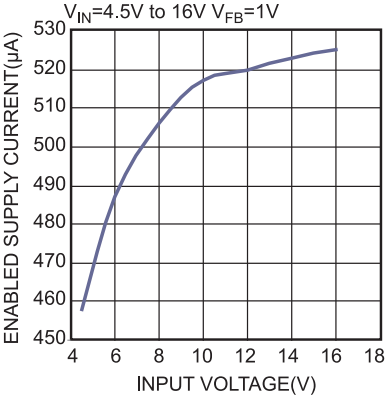
Disabled Supply Current vs. Input Voltage

V_{IN}=4.5V to 16V V_{EN}=0V



Enabled Supply Current vs. Input Voltage

V_{IN}=4.5V to 16V V_{FB}=1V



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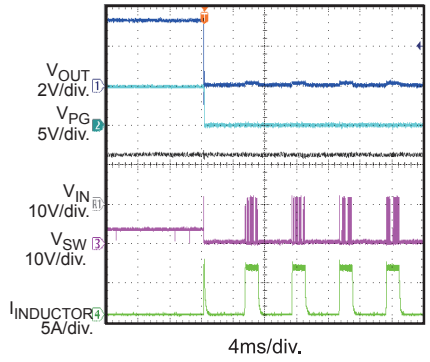
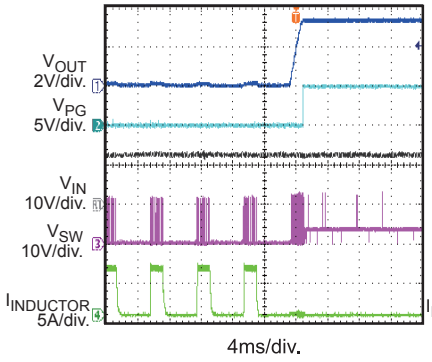
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 3.3V, L=5.5µH, T_A = 25°C, unless otherwise noted.

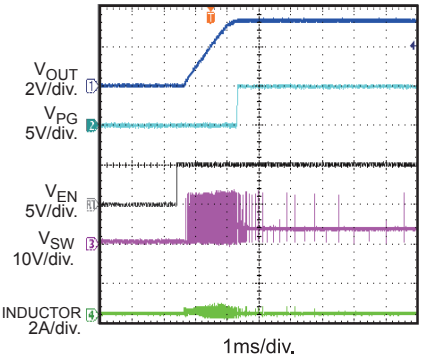
Short Entry
I_{OUT}=0A



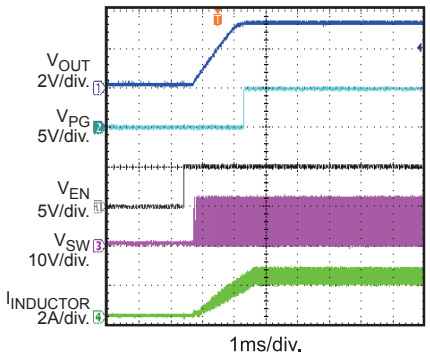
Short Recovery
I_{OUT}=0A



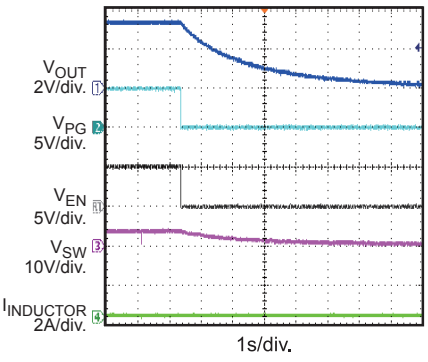
Start-Up through Enable
I_{OUT}=0A



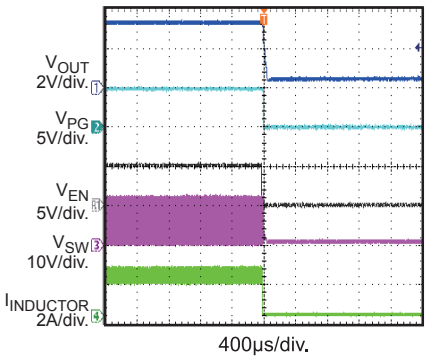
Start-Up through Enable
I_{OUT}=2A



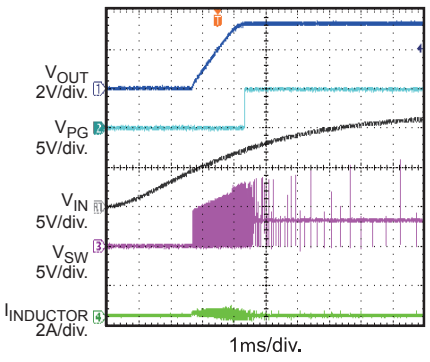
Shutdown through Enable
I_{OUT}=0A



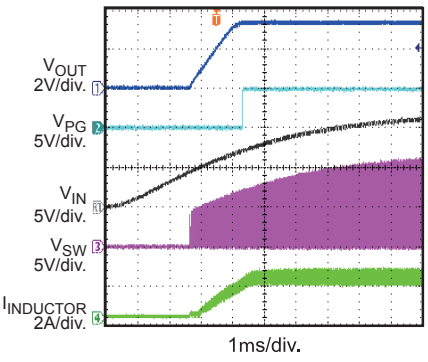
Shutdown through Enable
I_{OUT}=2A



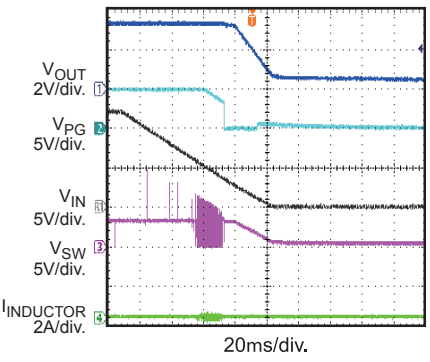
Start-Up through Input Voltage
I_{OUT}=0A



Start-Up through Input Voltage
I_{OUT}=2A



Shutdown through Input Voltage
I_{OUT}=0A



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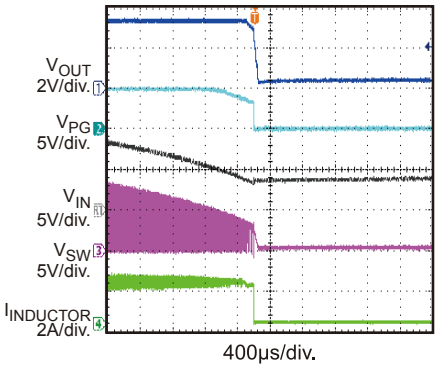
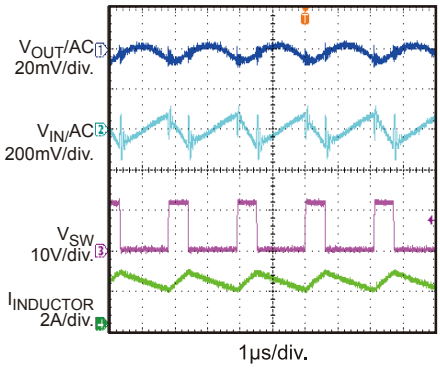
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 3.3V, L=5.5µH, T_A = 25°C, unless otherwise noted.

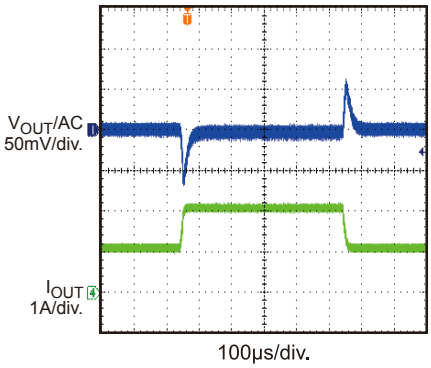
Shutdown Through Input Voltage
I_{OUT}=2A



Input / Output Ripple
I_{OUT}=2A



Load Transient Response
I_{OUT}=1A-2A



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PIN FUNCTIONS

Package Pin #	Name	Description
1	PG	Power Good Indicator. PG is the open drain of the internal MOSFET. Connect PG to VCC (or another voltage source) through a resistor (e.g. 100k). When the FB voltage reaches 90% of the REF voltage, PG is pulled high (after a 0.6ms delay). After the FB voltage drops to 85% of the REF voltage, PG is pulled low.
2	IN	Supply Voltage. IN supplies power to the internal MOSFET and regulator. The MP1474S operates from a +4.5V to +16V input rail; it requires a low ESR and low-inductance capacitor (C1) to decouple the input rail. Place the input capacitor very close to PG and connect it with wide PCB traces and multiple vias.
3	SW	Switch Output. Connect SW to the inductor and bootstrap capacitor. SW is driven up to V_{IN} by the high-side switch during the PWM duty cycle on-time. The inductor current drives SW negative during the off-time. The on resistance of the low-side switch and the internal body diode fixes the negative voltage. Connect using wide PCB traces and multiple vias.
4	GND	System Ground. Reference ground of the regulated output voltage. PCB layout requires extra care (see recommended “PCB Layout Guidelines” on page 16). For best results, connect to GND with copper and vias.
5	BST	Bootstrap. BST requires a capacitor connected between SW and BST to form a floating supply across the high-side switch driver.
6	EN/SYNC	Enable/Synchronize. EN/SYNC=high to enable the MP1474S. Apply an external clock to change the switching frequency. For automatic start-up, connect EN/SYNC to V_{IN} with a 100kΩ resistor.
7	VCC	Internal 5V LDO Output. VCC powers the driver and control circuits. Decouple with a 0.1μF to 0.22μF capacitor. Do NOT use a capacitor ≥0.22μF.
8	FB	Feedback. Connect FB to the tap of an external resistor divider from the output to GND to set the output voltage. To prevent current-limit runaway during a short-circuit fault, the frequency foldback comparator lowers the oscillator frequency when the FB voltage is below 400mV. Place the resistor divider as close to FB as possible. Avoid placing vias on the FB traces.

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FUNCTIONAL BLOCK DIAGRAM

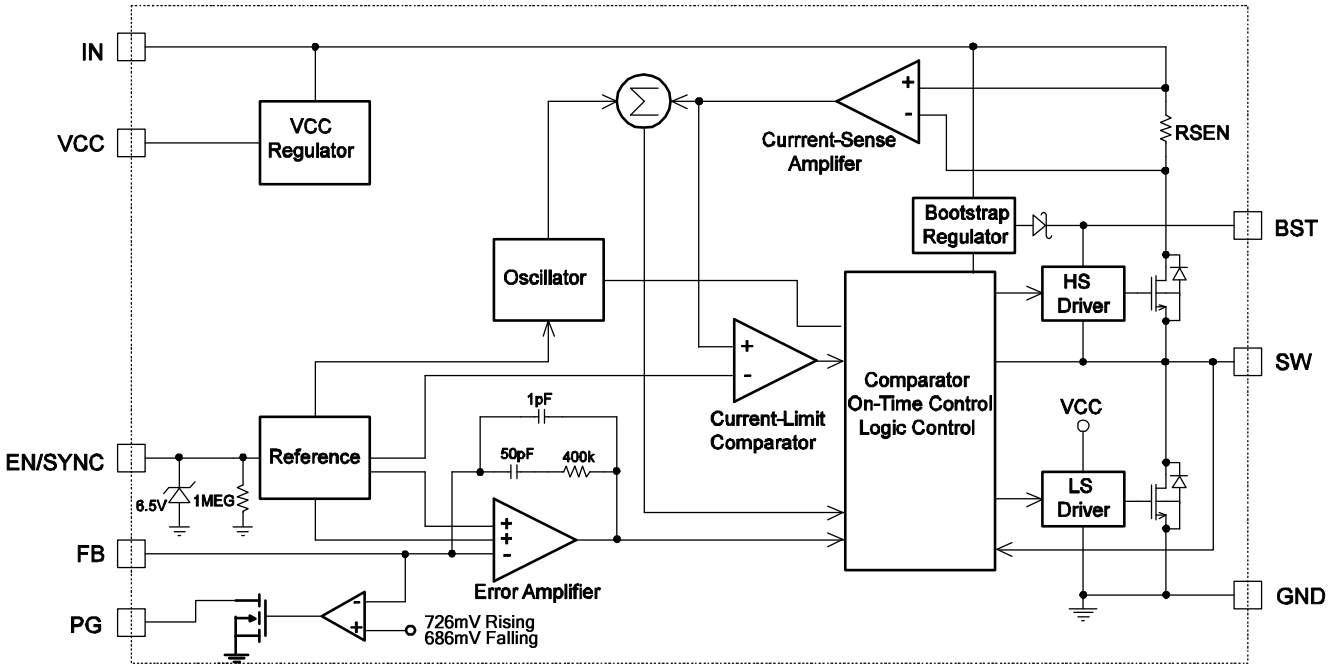

Figure 1. Functional Block Diagram

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OPERATION

The MP1474S is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs. It offers a compact solution that achieves a 2A continuous output current with excellent load and line regulation over a 4.5V to 16V input-supply range.

The MP1474S has three working modes: advanced asynchronous modulation (AAM) mode, discontinuous conduction mode (DCM), and continuous conduction mode (CCM). The load current increases as the device operates from AAM mode to DCM to CCM.

AAM Control Operation

In a light-load condition, MP1474S works in advanced asynchronous modulation (AAM) mode (see Figure 2). The V_{AAM} is an internally fixed voltage when input and output voltages are fixed. V_{COMP} is the error amplifier output (which represents the peak inductor-current information). When V_{COMP} is lower than V_{AAM}, the internal clock is blocked. This causes the MP1474S to skip pulses, achieving the light-load power save. Refer to AN032 for additional details.

The internal clock re-sets every time V_{COMP} is higher than V_{AAM}. At the same time, the high-side MOSFET (HS-FET) turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP}.

The light-load feature in this device is optimized for 12V input applications.

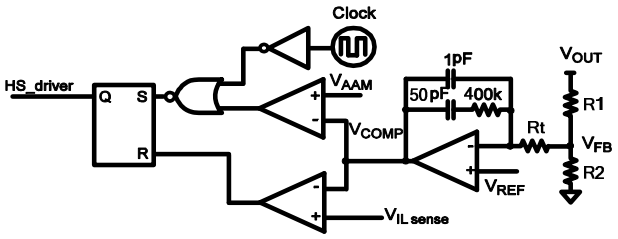

Figure 2. Simplified AAM Control Logic

DCM Control Operation

The V_{COMP} voltage ramps up as the output current increases. When its minimum value exceeds V_{AAM}, the device enters discontinuous conduction mode (DCM). In DCM, the internal clock initiates the PWM cycle, the

HS-FET turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP} (after a period of dead time), and the low-side MOSFET (LS-FET) turns on and remains on until the inductor-current value decreases to zero. The device repeats the same operation in every clock cycle to regulate the output voltage (see Figure 3).

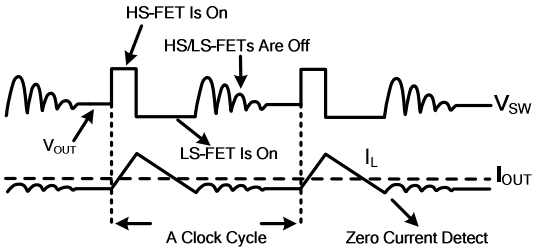

Figure 3. DCM Control Operation

CCM Control Operation

The device enters continuous conduction mode (CCM) from DCM once the inductor current no longer drops to zero in a clock cycle. In CCM, the internal clock initiates the PWM cycle, the HS-FET turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP} (after a period of dead time), and the LS-FET turns on and remains on until the next clock cycle begins. The device repeats the same operation in every clock cycle to regulate the output voltage.

If $V_{ILsense}$ does not reach the value set by V_{COMP} within 95% of one PWM period, the HS-FET is forced off.

Internal Regulator

A 5V internal regulator powers most of the internal circuitries. This regulator is supplied by V_{IN} and operates in the full V_{IN} range. When V_{IN} exceeds 5V, the output of the regulator is in full regulation. When V_{IN} is less than 5V, the output decreases, and the device requires a 0.1µF ceramic decoupling capacitor.

Error Amplifier (EA)

The error amplifier compares the FB voltage to the internal 0.807V reference (V_{REF}) and outputs a current proportional to the difference between the two. This output current then charges or discharges the internal compensation network to form the COMP voltage, which controls the

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power MOSFET current. The optimized, internal compensation network minimizes the external component count and simplifies the control loop design.

Enable/SYNC Control

EN/SYNC is a digital control pin that turns the regulator on and off. Drive EN/SYNC high to turn on the regulator; drive EN/SYNC low to turn off the regulator. An internal 1MΩ resistor from EN/SYNC to GND allows EN/SYNC to be floated to shut down the chip.

EN/SYNC is clamped internally using a 6.5V series-Zener-diode (see Figure 4). Connecting EN/SYNC through a pull-up resistor to the voltage on IN limits the EN/SYNC input current to less than 100μA.

For example, with 12V connected to IN, $R_{PULLUP} \geq (12V – 6.5V) \div 100\mu A = 55k\Omega$.

Connecting EN/SYNC directly to a voltage source without a pull-up resistor requires limiting the amplitude of the voltage source to ≤6V to prevent damage to the Zener diode.

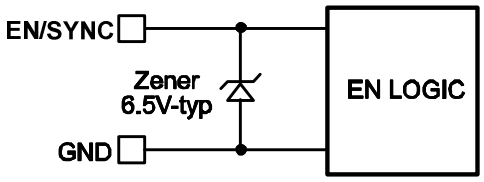

Figure 4. 6.5V Zener Diode Connection

For external clock synchronization, connect a clock with a frequency range between 300kHz and 2MHz. The internal clock rising edge synchronizes with the external clock rising edge. Select an external clock signal with a pulse width less than 1.7μs.

Under-Voltage Lockout (UVLO)

The MP1474S has under-voltage lockout protection (UVLO). When the VCC voltage exceeds the UVLO rising threshold voltage, the device begins to power up. It shuts off when the VCC voltage drops below the UVLO falling threshold voltage. This is non-latch protection.

The MP1474S is disabled when the input voltage falls below 3.2V. If an application requires a higher under-voltage lockout (UVLO) threshold, use EN/SYNC to adjust the input voltage UVLO by using two external resistors (see Figure 5). For best results, set the UVLO falling threshold (VSTOP) above 4.5V using the enable resistors. Set the rising threshold (VSTART) to provide enough hysteresis to allow for input-supply variations.

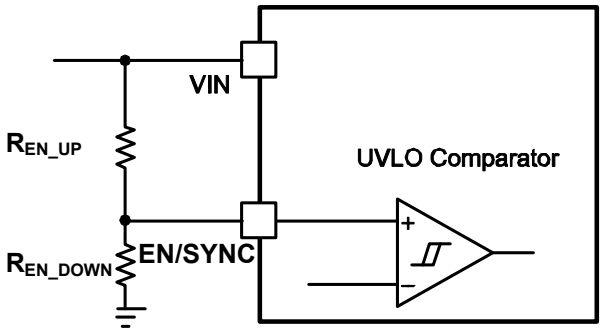

Figure 5. Adjustable UVLO

Internal Soft-Start

The soft-start prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage (V_{SS}) that ramps up from 0V to 1.2V. When V_{SS} is less than V_{REF}, the error amplifier uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, the error amplifier uses V_{REF} as the reference. The SS time is set internally to 1.2ms.

Pre-Bias Start-Up

The MP1474S is designed for a monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the BST voltage is refreshed and charged. Also, the voltage on the soft-start capacitor is charged. If BST voltage exceeds its rising threshold voltage, and the soft-start capacitor voltage exceeds the sensed-output voltage at FB, the device starts to operate normally.

Power Good Indicator (PG)

MP1474S has an open-drain pin as the power good indicator (PG). Pull PG up to VCC (or another external source) through a 100kΩ resistor. When V_{FB} exceeds 90% of V_{REF}, PG goes high (after a 0.6ms delay time). If V_{FB} goes below 85% of V_{REF}, an internal MOSFET pulls PG down to ground.

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Over-Current Protection (OCP) and Hiccup

The MP1474S has a cycle-by-cycle over-current limit when the inductor current peak value exceeds the set current-limit threshold. Meanwhile, the output voltage drops until V_{FB} is below the under-voltage (UV) threshold (50% below the reference, typically). Once UV is triggered, the MP1474S enters hiccup mode to re-start the part periodically. This protection mode is useful when the output is dead-shorted to ground and greatly reduces the average short-circuit current to alleviate thermal issues and protect the regulator. The MP1474S exits hiccup mode once the over-current condition is removed.

Thermal Shutdown (TSD)

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the die temperature exceeds 150°C, it shuts down the whole chip. When the temperature drops below its lower threshold, (130°C, typically), the chip is enabled again.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. The UVLO rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by V_{IN} through D1, M1, R3, C4, L1, and C2 (see Figure 6). If (V_{IN}-V_{SW}) exceeds 5V, U1 regulates M1 to maintain a 5V BST voltage across C4. It is recommended strongly to place a 20Ω resistor between the SW and BST cap to reduce SW spike voltage.

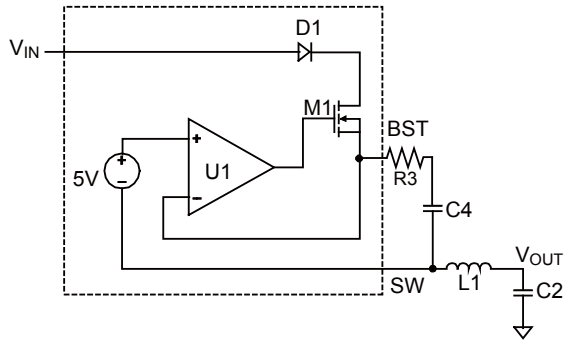

Figure 6. Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If both V_{IN} and $V_{EN/SYNC}$ exceed their respective thresholds, the chip starts up. The reference block starts first, generating stable reference voltage and currents, then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: $V_{EN/SYNC}$ low, V_{IN} low, and thermal shutdown. During the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage (see "Typical Application" on page 1). Choose R1 around 40.2kΩ; R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.807V} - 1}$$

The T-type network is highly recommended when V_{OUT} is low (see Figure 7).

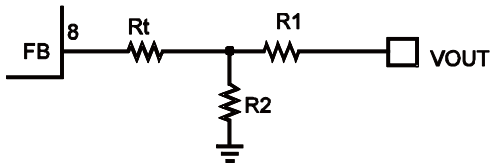

Figure 7. T-Type Network

Table 1 lists the recommended T-type resistor values for common output voltages.

Table 1. Resistor Selection for Common Output Voltages(8)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	Rt (kΩ)
1.0	20.5	84.5	82
1.2	30.1	61.9	82
1.8	40.2	32.4	33
2.5	40.2	19.1	33
3.3	40.2	13	16
5	40.2	7.68	16

Notes:

8) The recommended parameters are based on a 500kHz switching frequency; a different input voltage, output-inductor value, and output-capacitor value may affect the selection of R1, R2, and Rt. For additional component parameters, please refer to "Typical Application Circuits" on pages 17 and 18.

Selecting the Inductor

For most applications, use a 1μH to 22μH inductor with a DC current rating at least 25% higher than the maximum load current. For highest efficiency, use an inductor with a DC resistance less than 15mΩ. For most designs, the inductance value is derived from the following equation:

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is the inductor-ripple current.

Choose the inductor-ripple current at approximately 30% of the maximum load current. The maximum inductor peak current is calculated by the following equation:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Use a larger inductor for improved efficiency under light-load conditions (below 100mA).

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore it requires a capacitor to supply the AC current while maintaining the DC input voltage. Use low ESR capacitors for optimum performance. Use ceramic capacitors with X5R or X7R dielectrics for best results because of their low ESR and small temperature coefficients. For most applications, use a 22μF capacitor.

Since C1 absorbs the input-switching current, it requires an adequate ripple-current rating. The RMS current in the input capacitor is estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose an input capacitor that has a RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, a small, high-quality ceramic capacitor (e.g. 0.1μF) should be placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide sufficient charge in order to prevent excessive voltage ripple at input. The input-voltage ripple caused by capacitance can be estimated as:

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$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output-voltage ripple low. The output-voltage ripple is estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where L_1 is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and the capacitance causes the majority of the output-voltage ripple. For simplification, the output-voltage ripple is estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output-ripple is approximated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor affect the stability of the regulation system. The MP1474S can be optimized for a wide range of capacitance and ESR values.

External Bootstrap Diode

In particular conditions, BST voltage may become insufficient (see equations below). During these conditions, an external bootstrap diode can enhance the efficiency of the regulator and avoid insufficient BST voltage at light-load PFM operation. Insufficient BST voltage is more likely to happen during either of following conditions:

- V_{IN} is below 5V
- V_{OUT} is 5V or 3.3V; and D_{uty} cycle is high: $D = \frac{V_{OUT}}{V_{IN}} > 65\%$

If the BST voltage is insufficient, the output-ripple voltage may become extremely large during a light-load condition. If this occurs, add an external BST diode from VCC to BST (see Figure 8).

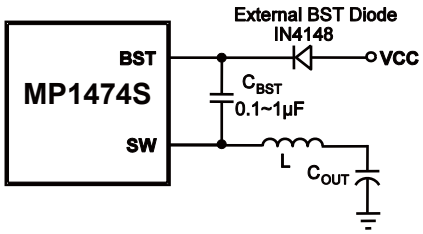

Figure 8. Optional External Bootstrap Diode

The recommended external BST diode is IN4148, and the BST capacitor value is 0.1μF to 1μF.

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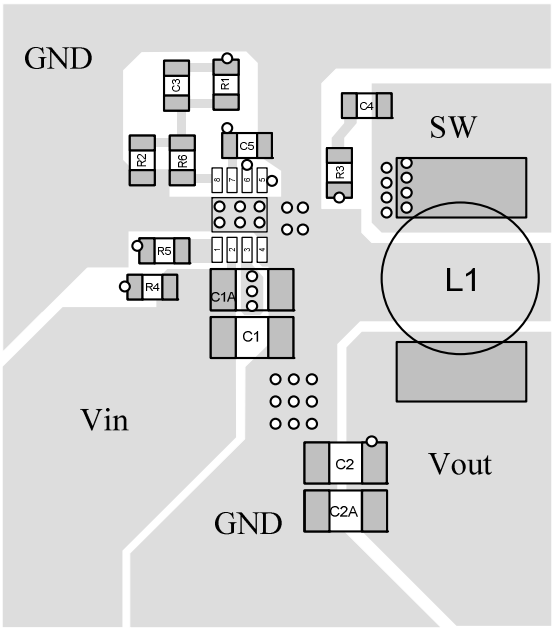
PCB Layout Guidelines [9]

Efficient PCB layout is critical to achieve stable operation, especially for the placement of the VCC capacitor and input capacitor. For best results, refer to Figure 9 and the guidelines below:

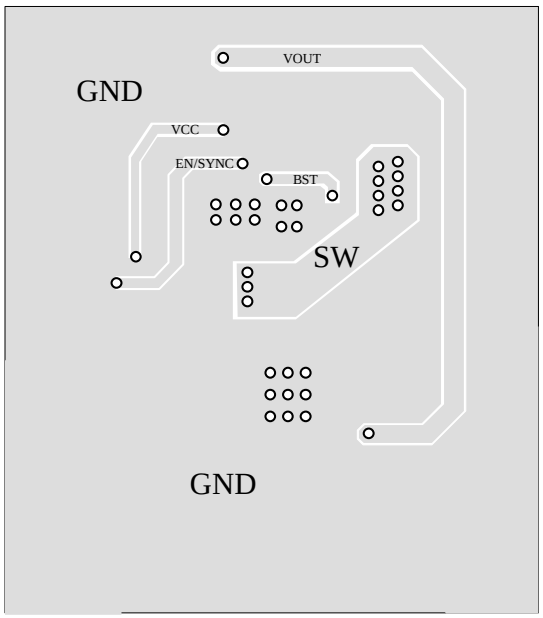
1. Use large ground plane to connect directly to GND. If the bottom layer is ground plane, add vias near GND.
2. Place the VCC capacitor as close as possible to VCC and GND. The trace length of VCC to the VCC capacitor anode to the VCC capacitor cathode to GND should be as short as possible.
3. Place the ceramic input capacitor close to IN and GND. Keep the connection between the input capacitor and IN as short and wide as possible.
4. Route SW and BST away from sensitive analog areas (such as FB).
5. Place the T-type feedback resistor R6 close to the chip to ensure the trace connected to FB is as short as possible

Notes:

9) The recommended layout is based on Figure 10 in the "Typical Application circuit" section on page 17.



Top Layer



Bottom Layer

Figure 9. Recommended PCB Layout

Design Example

Table 2 shows a design example following the application guidelines for the specifications:

Table 2. Design Example

V_{IN}	12V
V_{OUT}	3.3V
I_{OUT}	2A

The detailed application schematic is shown in Figure 11. The typical performance and circuit waveforms have been shown in the "Typical Performance Characteristics" section. For additional device applications, please refer to the related evaluation board datasheets.

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TYPICAL APPLICATION CIRCUITS

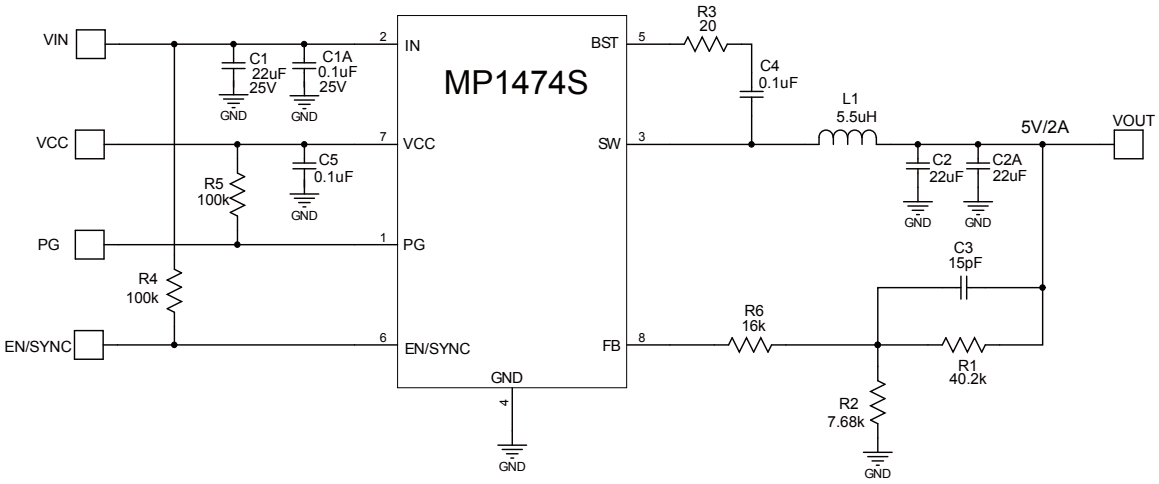

Figure 10. $12V_{IN}$, 5V/2A Output

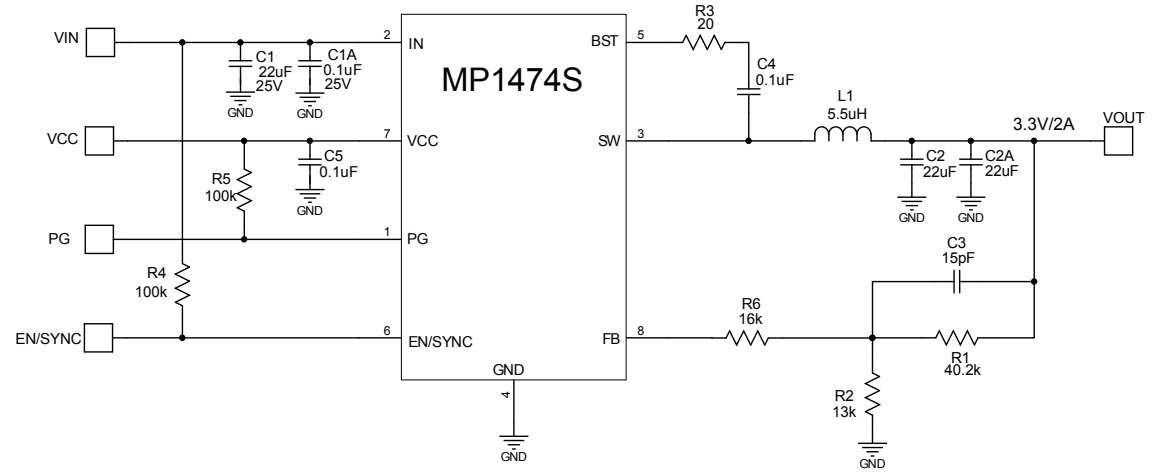

Figure 11. $12V_{IN}$, 3.3V/2A Output

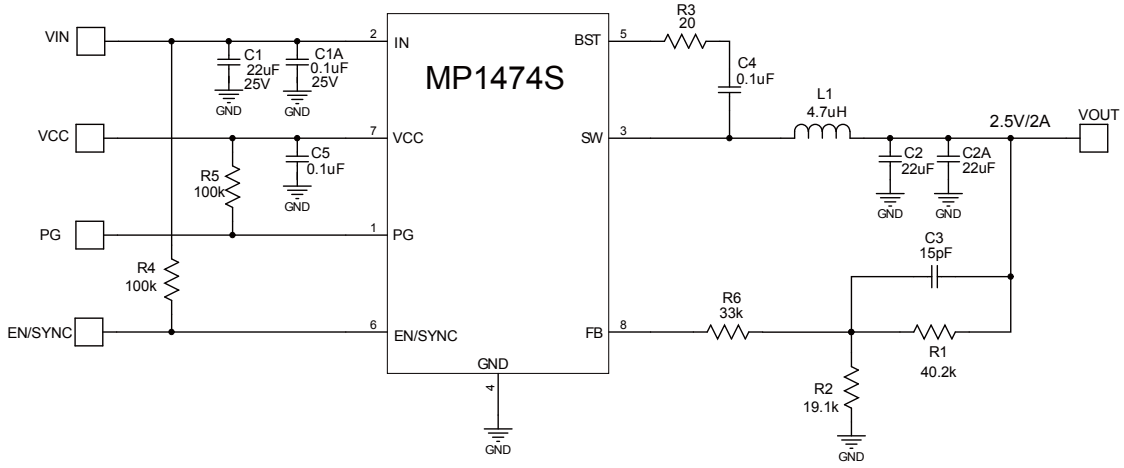

Figure 12. $12V_{IN}$, 2.5V/2A Output

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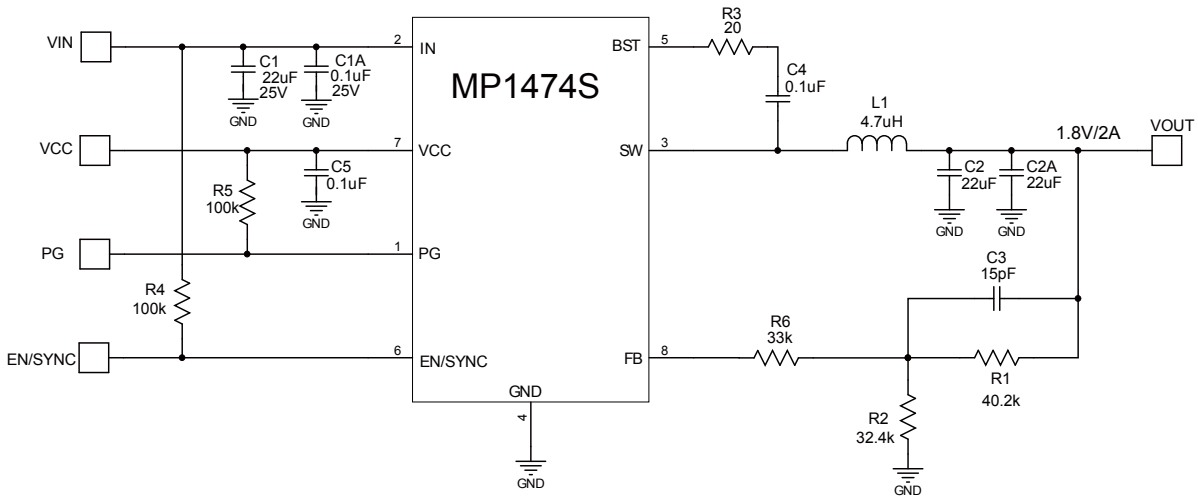

Figure 13. $12V_{IN}$, 1.8V/2A Output

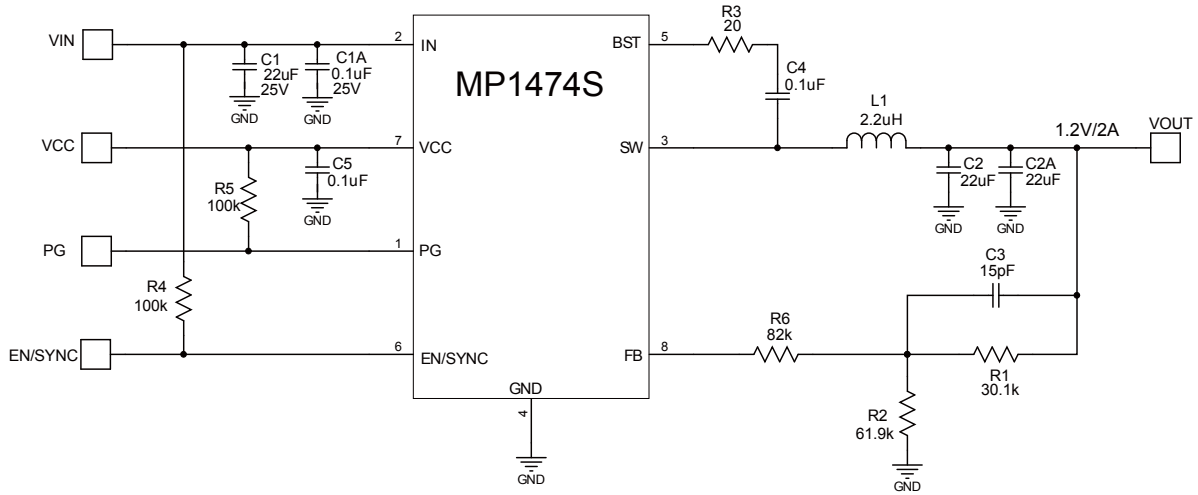

Figure 14. $12V_{IN}$, 1.2V/2A Output

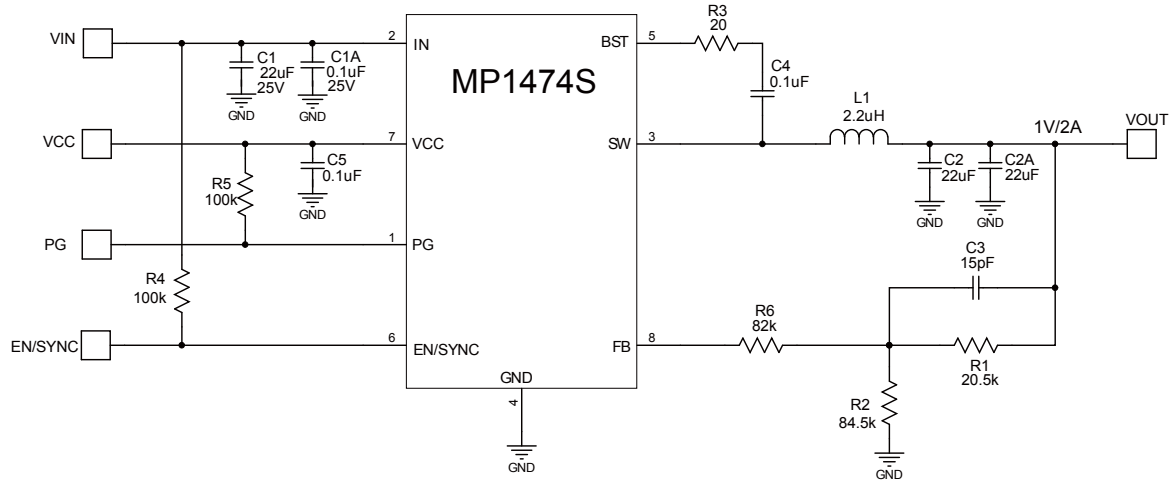

Figure 15. $12V_{IN}$, 1V/2A Output

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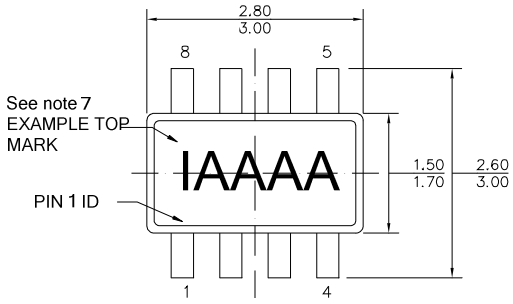
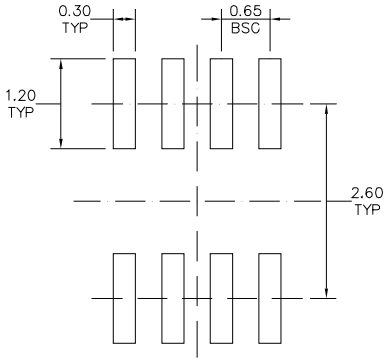
PACKAGE INFORMATION

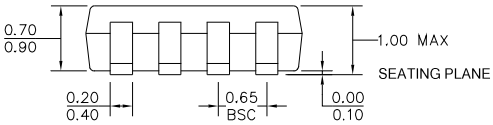
TSOT23-8



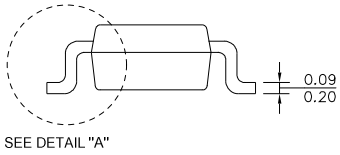
TOP VIEW



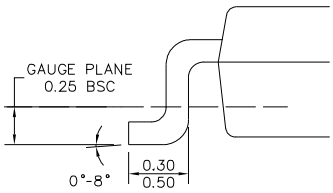
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-193, VARIATION BA.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT (SEE EXAMPLE TOP MARK).

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