MP1471A

High-Efficiency, 3A 16V, 500kHz Synchronous, Step-Down Converter In a 6-Pin TSOT 23

The Future of Analog IC Technology

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP1477

DESCRIPTION

The MP1471A is a high-frequency, synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs. It offers a very compact solution to achieve a 3A output current over a wide input supply range, with excellent load and line regulation. The MP1471A has synchronous-mode operation for higher efficiency over the output current-load range.

Current-mode operation provides fast transient response and eases loop stabilization.

Protection features include over-current protection and thermal shutdown.

The MP1471A requires a minimal number of readily-available, standard, external components and is available in a space-saving 6-pin TSOT23 package.

FEATURES

- Wide 4.5V-to-16V Operating Input Range
- 110mΩ/57mΩ Low-$R_{DS(ON)}$ Internal Power MOSFETs
- Proprietary Switching-Loss–Reduction Technology
- High-Efficiency Synchronous-Mode Operation
- Fixed 500kHz Switching Frequency
- Internal AAM Power-Save Mode for High Efficiency at Light Load
- Internal Soft-Start
- Over-Current Protection and Hiccup
- Thermal Shutdown
- Output Adjustable from 0.8V
- Available in a 6-pin TSOT-23 package

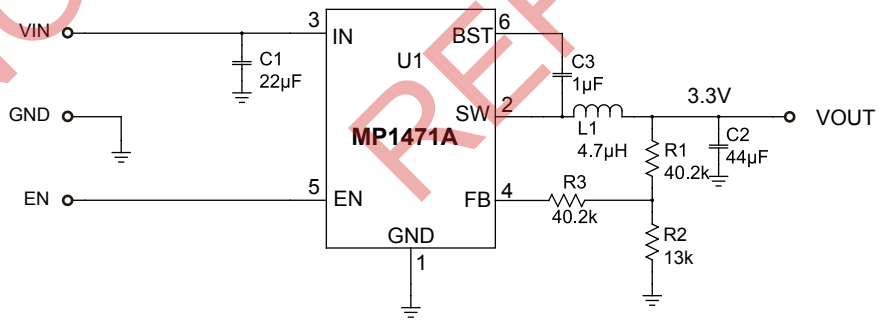
APPLICATIONS

- Game Consoles
- Digital Set-Top Boxes
- Flat-Panel Television and Monitors
- General Purposes

All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit MPS website under Products, Quality Assurance page.

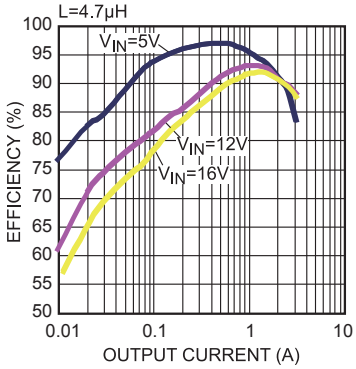
"MPS" and "The Future of Analog IC Technology" are registered trademarks of Monolithic Power Systems, Inc.

TYPICAL APPLICATION



Efficiency vs. Output Current

V_{OUT}=3.3V, I_{OUT}=0.01A to 3A, L=4.7µH



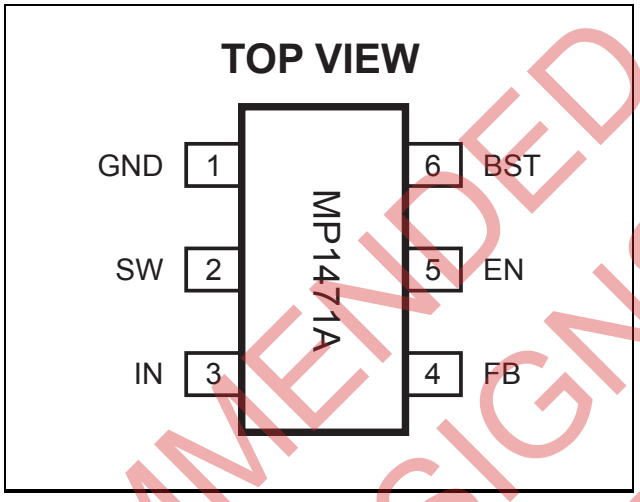
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2013 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking
MP1471AGJ	TSOT23-6	AGM

* For Tape & Reel, add suffix –Z (e.g. MP1471AGJ–Z);

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} .....-0.3V to 17V
V_{SW} .....
-0.3V (-5V for <10ns) to 17V (19V for <10ns)
V_{BST} ..... V_{SW}+6V
All Other Pins.....–0.3V to 6V
Continuous Power Dissipation (T_A = +25°C) (2)
..... 1.25W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... -65°C to 150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} .....4.5V to 16V
Output Voltage V_{OUT}.....0.8V to V_{IN}*Dmax
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}
TSOT-23-6	100	55 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP1477

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2013 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS (5)

V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current (Shutdown)	I_{IN}	V_{EN} = 0V			1	μA
Supply Current (Quiescent)	I_q	V_{EN} = 2V, V_{FB} = 1V		0.84	1.1	mA
HS Switch-On Resistance	HS_{RDS-ON}	V_{BST-SW}=5V		110		mΩ
LS Switch-On Resistance	LS_{RDS-ON}	Vcc=5V		57		mΩ
Switch Leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} =12V			1	μA
Current Limit	I_{LIMIT}	Duty=40%	3.9	4.6		A
Oscillator Frequency	f_{SW}	V_{FB}=0.75V	410	500	590	kHz
Maximum Duty Cycle	D_{MAX}	V_{FB}=700mV	88	92		%
Minimum On Time(5)	T_{ON_MIN}			60		ns
Feedback Voltage	V_{FB}		788	804	820	mV
EN Rising Threshold	V_{EN_RISING}		1.4	1.5	1.6	V
EN Falling Threshold	$V_{EN_FALLING}$		1.23	1.32	1.41	V
EN Input Current	I_{EN}	V_{EN}=2V		1.8		μA
		V_{EN}=0		0		μA
V_{IN} Under-Voltage Lockout Threshold, Rising	$INUV_{Vth}$		3.9	4.15	4.4	V
V_{IN} Under-Voltage Lockout Threshold Hysteresis	$INUV_{HYS}$			340		mV
Soft-Start Period	T_{SS}	Vout from 0% to 100%		1.5		ms
Thermal Shutdown(5)				150		°C
Thermal Hysteresis(5)				20		°C

Notes:

5) Derived from bench characterization. Not tested in production.

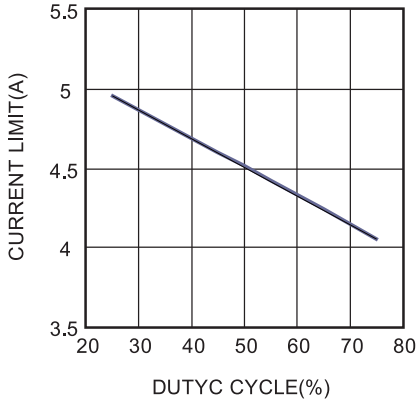
NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP1477

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2013 MPS. All Rights Reserved.

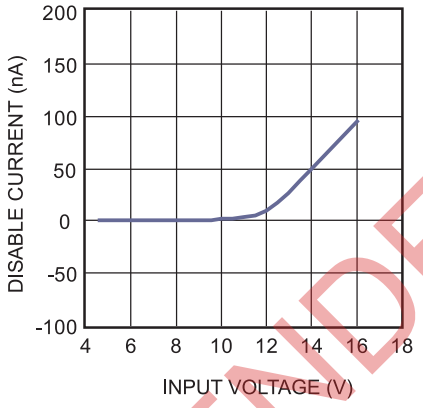
TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, T_A = +25°C, unless otherwise noted.

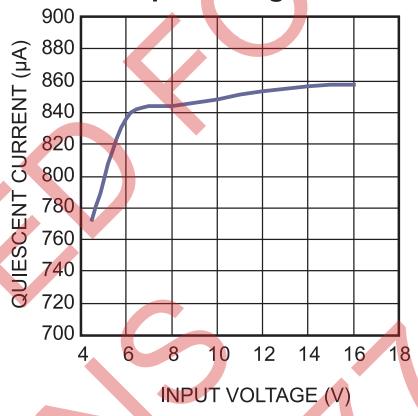
Current Limit vs. Duty Cycle



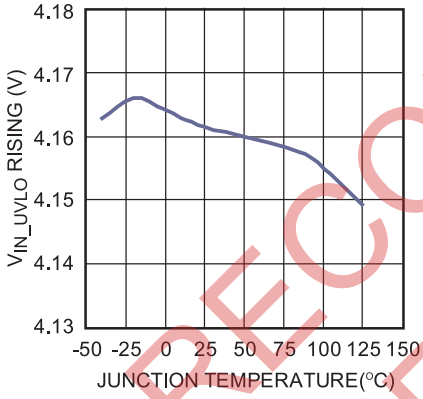
Disable Current vs. Input Voltage



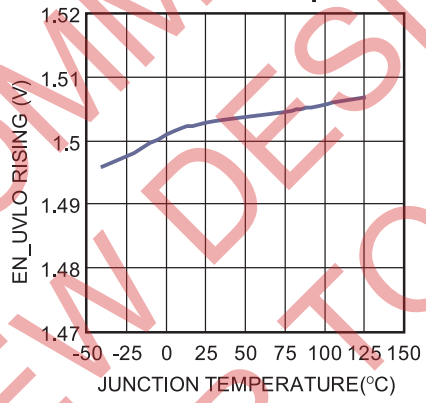
Quiescent Current vs. Input Voltage



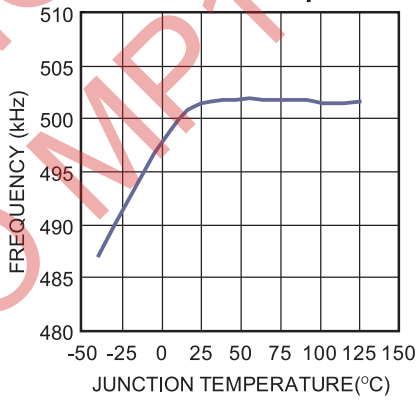
V_{IN_ULVO} Rising vs. Junction Temperature



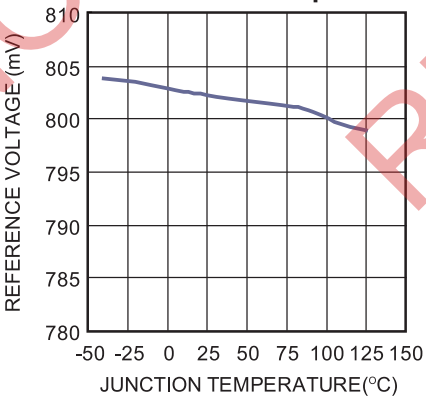
EN_ULVO Rising vs. Junction Temperature



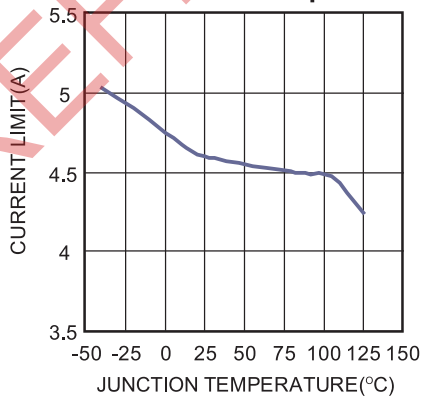
Frequency vs. Junction Temperature



V_{REF} vs. Junction Temperature



Current Limit vs. Junction Temperature



NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP1477

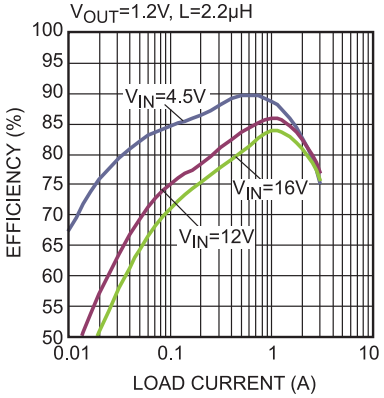
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2013 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, T_A = +25°C, unless otherwise noted.

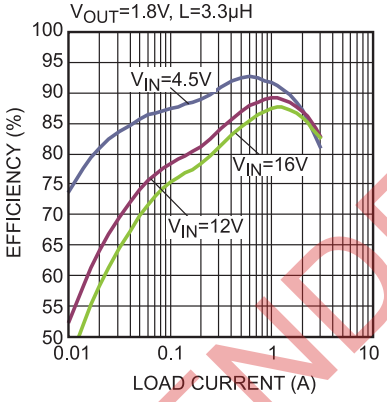
Efficiency vs. Load Current

V_{OUT}=1.2V, L=2.2µH



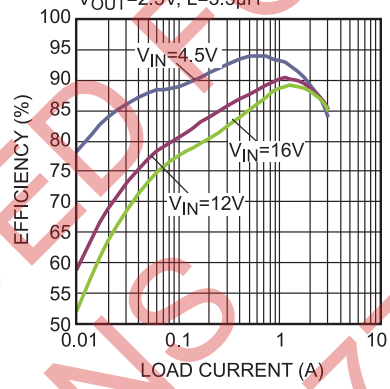
Efficiency vs. Load Current

V_{OUT}=1.8V, L=3.3µH



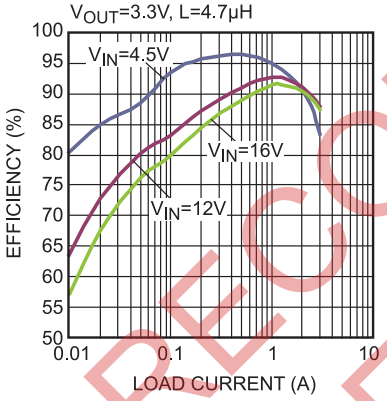
Efficiency vs. Load Current

V_{OUT}=2.5V, L=3.3µH



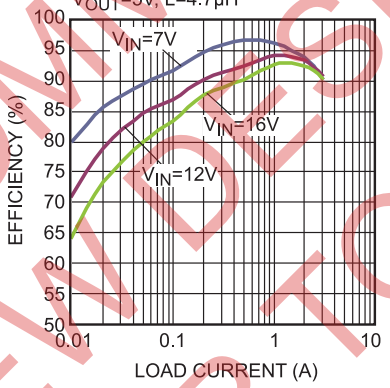
Efficiency vs. Load Current

V_{OUT}=3.3V, L=4.7µH

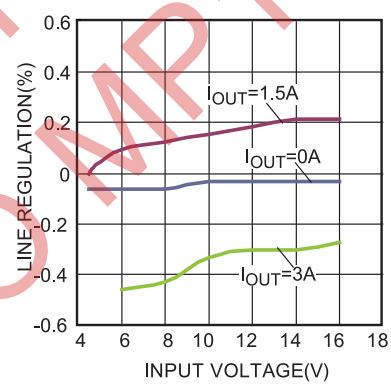


Efficiency vs. Load Current

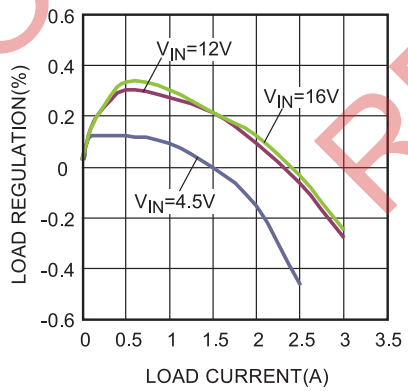
V_{OUT}=5V, L=4.7µH



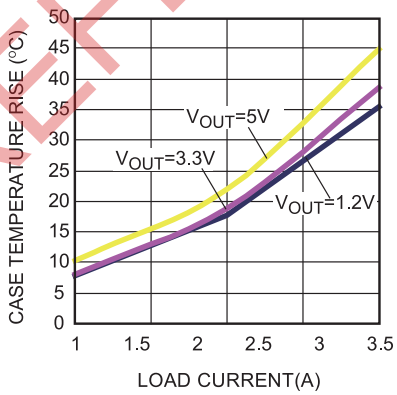
Line Regulation



Load Regulation

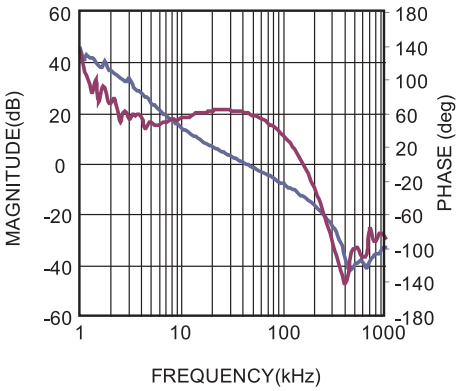


Case Temperature Rise vs. I_{OUT}



Magnitude and Phase vs. Frequency

I_{OUT}=3A



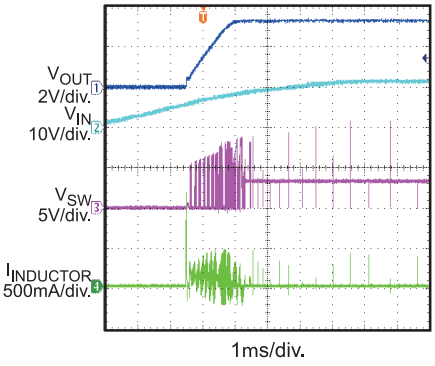
NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP1477

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2013 MPS. All Rights Reserved.

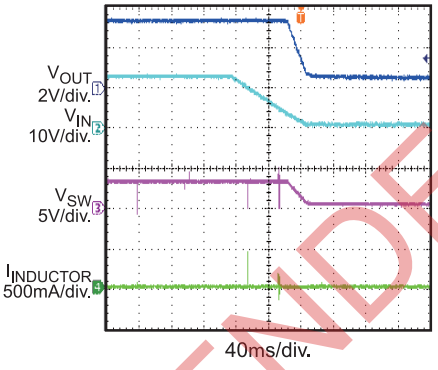
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, T_A = +25°C, unless otherwise noted.

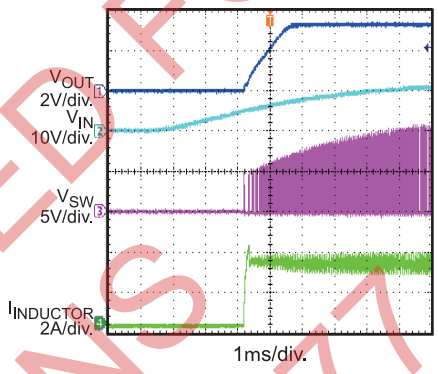
Start Up through Input Voltage
I_{OUT} = 0A



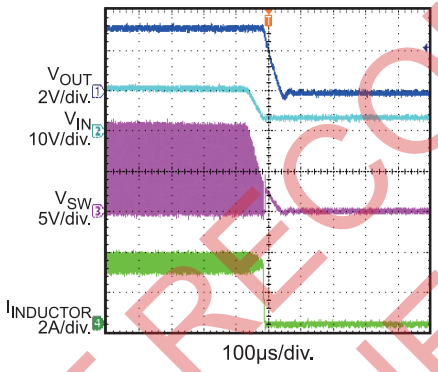
Shutdown through Input Voltage
I_{OUT} = 0A



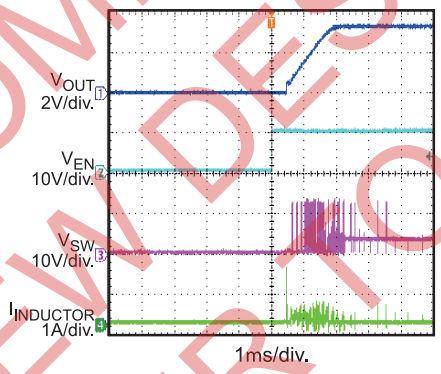
Start Up through Input Voltage
I_{OUT} = 3A



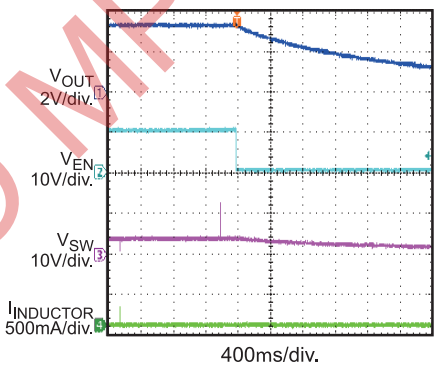
Shutdown through Input Voltage
I_{OUT} = 3A



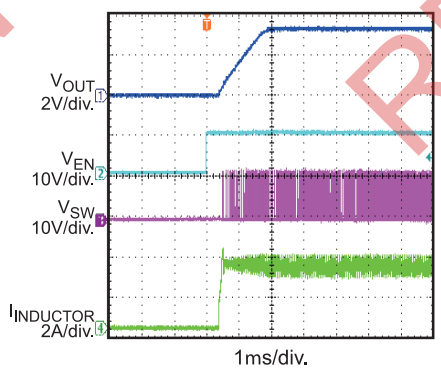
Start Up through Enable
I_{OUT} = 0A



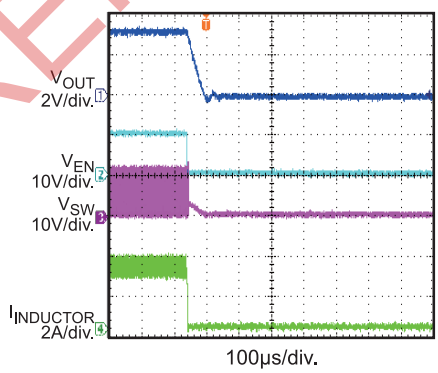
Shutdown through Enable
I_{OUT} = 0A



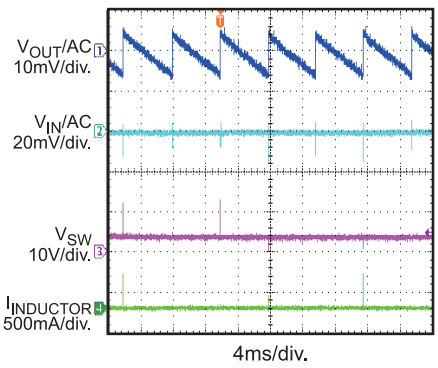
Start Up through Enable
I_{OUT} = 3A



Shutdown through Enable
I_{OUT} = 3A



Input/Output Ripple
I_{OUT} = 0A



NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP1477

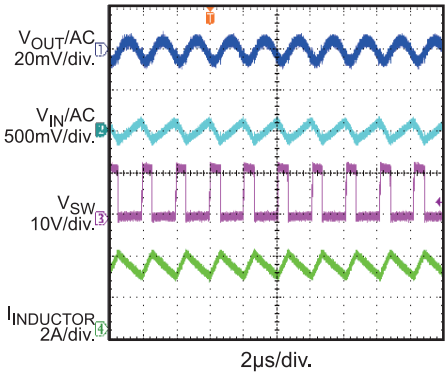
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2013 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, T_A = +25°C, unless otherwise noted.

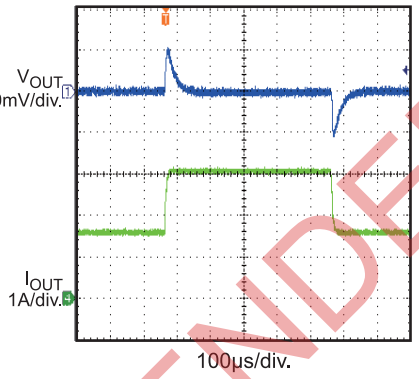
Input/Output Ripple

I_{OUT} = 3A



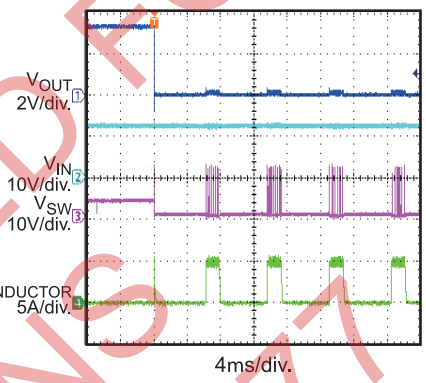
Transient Response

I_{OUT} = 1.5A to 3A, 2.5A/µs



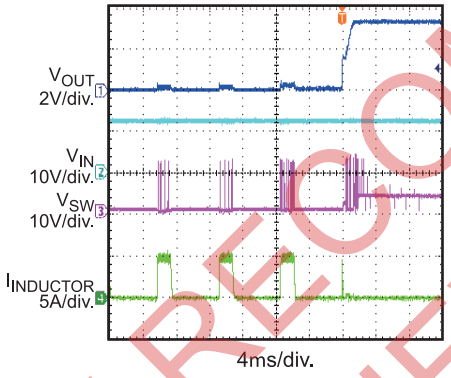
Short Circuit Entry

I_{OUT} = 0A



Short Circuit Recovery

I_{OUT} = 0A



NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP1477

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2013 MPS. All Rights Reserved.

PIN FUNCTIONS

Package Pin #	Name	Description
1	GND	System Ground. Reference ground of the regulated output voltage: requires extra care during PCB layout. Connect to GND with copper traces and vias.
2	SW	Switch Output. Connect using wide a PCB trace.
3	IN	Supply Voltage. The MP1471A operates from a 4.5V-to-16V input rail. Requires C1 to decouple the input rail. Connect using a wide PCB trace.
4	FB	Feedback. Connect to the tap of an external resistor divider from the output to GND to set the output voltage. The frequency fold-back comparator lowers the oscillator frequency when the FB voltage drops below 140mV to prevent current-limit runaway during a short circuit fault.
5	EN	EN=HIGH to enable the MP1471A. For automatic start-up, connect EN to V_{IN} using a 100kΩ resistor.
6	BST	Bootstrap. Connect a capacitor and a resistor between SW and BST pins to form a floating supply across the high-side switch driver. Use a 1μF BST capacitor.

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP1477

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2013 MPS. All Rights Reserved.

BLOCK DIAGRAM

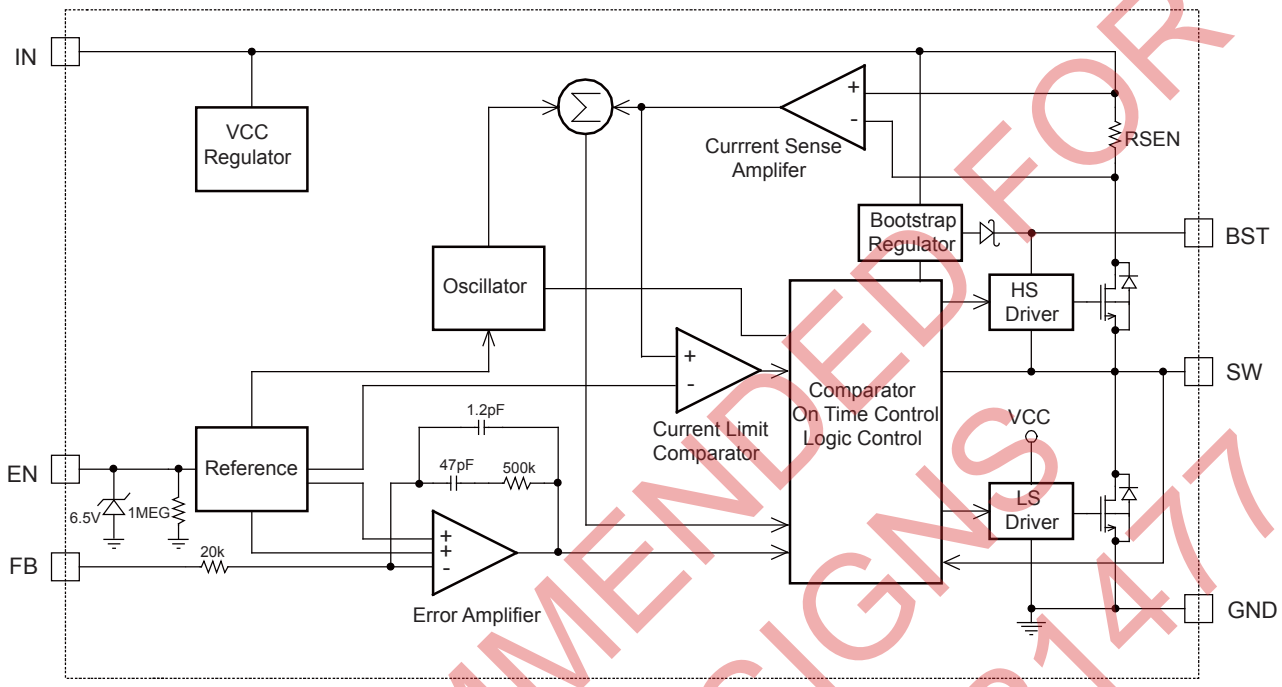


Figure 1: Functional Block Diagram

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP1477

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2013 MPS. All Rights Reserved.

OPERATION

The MP1471A is a high-frequency, synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs. It offers a very compact solution to achieve a 3A output current over a wide input supply range, with excellent load and line regulation.

The MP1471A operates in a fixed-frequency, peak-current–control mode to regulate the output voltage. An internal clock initiates the PWM cycle to turn on the integrated high-side power MOSFET. This MOSFET remains on until its current reaches the value set by the COMP voltage. When the power switch is off, it remains off until the next clock cycle starts. If the current in the power MOSFET does not reach the COMP set current value within 90% of one PWM period, the power MOSFET is forced to turn off.

Internal Regulator

The 5V internal regulator powers most of the internal circuits. This regulator takes V_{IN} and operates in the full V_{IN} range. When V_{IN} exceeds 5.0V, the regulator output is in full regulation. When V_{IN} falls below 5.0V, the output decreases.

Error Amplifier

The error amplifier compares the FB voltage against the internal 0.8V reference (REF) and outputs a current proportional to the difference between the two. This output current charges or discharges the internal compensation network to form the COMP voltage, which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external component counts and simplifies the control-loop design.

AAM Operation

The MP1471A has AAM (Advanced Asynchronous Modulation) power-save mode for light load. The AAM voltage is set at 0.5V internally. Under the heavy load condition, the V_{COMP} is higher than V_{AAM}. When the clock goes high, the high-side power MOSFET turns on and remains on until $V_{ILsense}$ reaches the value set by the COMP voltage. The internal clock resets every time when V_{COMP} exceed V_{AAM}.

In light-load condition, the value of V_{COMP} is low. When V_{COMP} is less than V_{AAM} and V_{FB} is less than V_{REF}, V_{COMP} ramps up until it exceeds V_{AAM}. During this time, the internal clock is blocked, thus the MP1471A skips some pulses for PFM (Pulse Frequency Modulation) mode and achieves the light load power save.

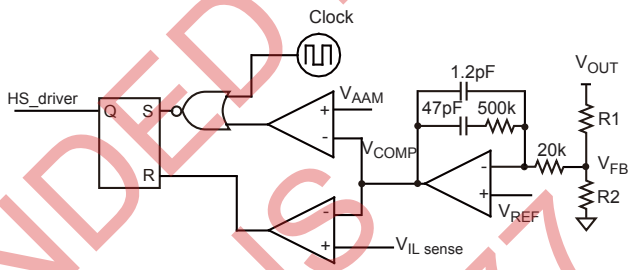


Figure 2: Simplified AAM Control Circuit

When the load current is light, the inductor peak current is set internally to about 650mA for V_{IN}=12V, V_{OUT}=3.3V, and L=4.7µH. Figure 3 shows the inductor peak current vs. inductor value curve.

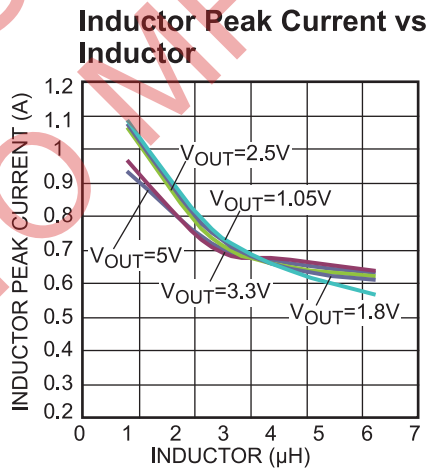


Figure 3: Inductor Peak Current vs. Inductor Value

Enable

EN is a digital control pin that turns the regulator on and off: Drive EN HIGH to turn on the regulator, drive it LOW to turn it off. An internal 1MΩ resistor from EN to GND allows EN to float to shut down the chip.

The EN pin is clamped internally using a 6.5V series-Zener-diode as shown in Figure 4. Connecting the EN input pin through a pullup

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP1477

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2013 MPS. All Rights Reserved.

resistor to the V_{IN} voltage limits the EN input current to less than 100μA.

For example, with 12V connected to Vin, $R_{PULLUP} \geq (12V-6.5V) \div 100\mu A = 55k\Omega$

Connecting the EN pin directly to a voltage source without any pullup resistor requires limiting the amplitude of the voltage source to ≤ 6V to prevent damage to the Zener diode.

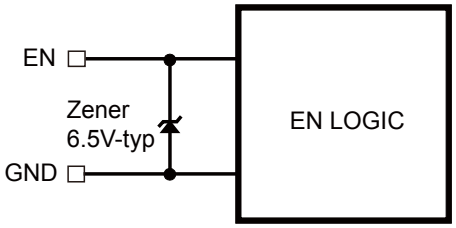


Figure 4: 6.5V Zener Diode

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP1471A UVLO comparator monitors the output voltage of the internal regulator, VCC. The UVLO rising threshold is about 4.15V while its falling threshold is consistently 3.8V.

Internal Soft-Start

Soft-start prevents the converter output voltage from overshooting during startup. When the chip starts, the internal circuit generates a soft-start voltage (SS) that ramps up from 0V to 1.2V: When SS falls below the internal reference (REF), SS overrides REF so that the error amplifier uses SS as the reference; when SS exceeds REF, the error amplifier resumes using REF as its reference. The SS time is internally set to 1.5ms.

Over-Current-Protection and Hiccup

The MP1471A has a cycle-by-cycle over-current limit for when the inductor current peak value exceeds the set current-limit threshold. First, when the output voltage drops until FB falls below the Under-Voltage (UV) threshold (typically 140mV) to trigger a UV event, the MP1471A enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-shorted to ground. This greatly reduces the average short-circuit current to alleviate thermal issues and to protect the regulator. The MP1471A exits hiccup mode once the over-current condition is removed.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C, it shuts down the whole chip. When the temperature falls below its lower threshold (typically 130°C) the chip is enabled again.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection, with a rising threshold of 2.2V and a hysteresis of 150mV. V_{IN} regulates the bootstrap capacitor voltage internally through D1, M1, R4, C4, L1 and C2 (Figure 5). If (V_{IN}-V_{SW}) exceeds 5V, U2 will regulate M1 to maintain a 5V BST voltage across C4.

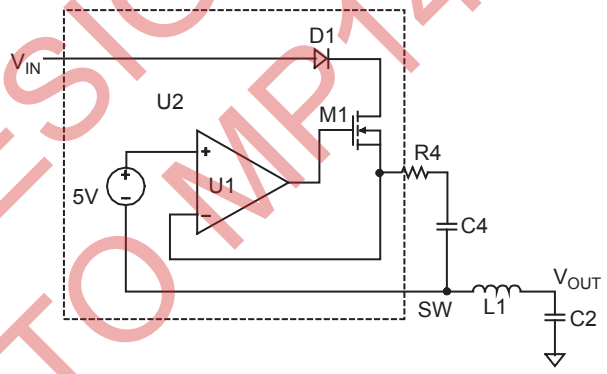


Figure 5 : Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If both V_{IN} and EN exceed their respective thresholds, the chip starts. The reference block starts first, generating a stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuits.

Three events can shut down the chip: EN low, V_{IN} low, and thermal shutdown. The shutdown procedure starts by initially blocking the signaling path to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP1477

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2013 MPS. All Rights Reserved.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage. The feedback resistor R1 also sets the feedback-loop bandwidth through the internal compensation capacitor (see the Typical Application circuit). Choose R1 around 10kΩ, and R2 by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.8V} - 1}$$

Use a T-type network for when V_{OUT} is low.

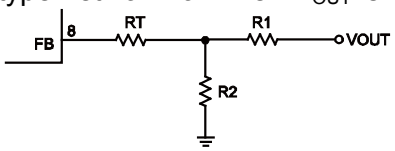


Figure 6: T-Type Network

Table 1 lists the recommended T-type resistors value for common output voltages.

Table 1—Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	Rt (kΩ)	L_{OUT} (µH)	C_{OUT} (µF)
1.05	10	32.4	150	2.2	44
1.2	20.5	41.2	120	2.2	44
1.8	40.2	32.4	75	3.3	44
2.5	40.2	19.1	59	3.3	44
3.3	40.2	13	40.2	4.7	44
5	40.2	7.68	24.9	4.7	44

Selecting the Inductor

Use a 1µH-to-22µH inductor with a DC current rating of at least 25% percent higher than the maximum load current for most applications. For highest efficiency, select an inductor with a DC resistance less than 15mΩ. For most designs, derive the inductance value from the following equation.

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is the inductor ripple current. Choose an inductor current approximately 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light-load conditions (below 100mA), use a larger inductance for improved efficiency.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, and therefore requires a capacitor to both supply the AC current to the step-down converter and maintain the DC input voltage. Use low ESR capacitors for the best performance, such as ceramic capacitors with X5R or X7R dielectrics of their low ESR and small temperature coefficients. A 22µF capacitor is sufficient for most applications.

The input capacitor (C1) requires an adequate ripple current rating because it absorbs the input switching. Estimate the RMS current in the input capacitor with:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. Place a small, high-quality, ceramic capacitor (0.1µF) as close to the IC as possible when using electrolytic or tantalum capacitors. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive input voltage ripple. Estimate the input voltage ripple caused by the capacitance with:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. Use low ESR capacitors to limit the output voltage ripple. Estimate the output voltage ripple with:

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP1477

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2013 MPS. All Rights Reserved.

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where L_1 is the inductor value and R_{ESR} is the equivalent series resistance (ESR) of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple. For simplification, estimate the output voltage ripple with:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP1471A can be optimized for a wide range of capacitance and ESR values.

External Bootstrap Diode

An external bootstrap (BST) diode can enhance the efficiency of the regulator given the following applicable conditions:

- V_{OUT} is 5V or 3.3V; and
- Duty cycle is high: $D = \frac{V_{OUT}}{V_{IN}} > 65\%$

Connect the external BST diode from the output of voltage regulator to the BST pin, as shown in Figure 7.

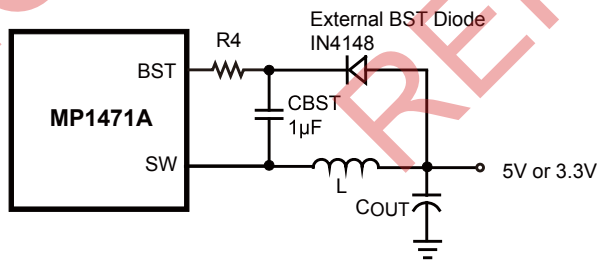


Figure 7 : Optional External Bootstrap Diode

For most applications, use an IN4148 for the external BST diode is IN4148, and a 1µF capacitor for the BST capacitor.

PC Board Layout

PCB layout is very important to achieve stable operation. For best results, use the following guidelines and Figure 8 as reference.

1) Keep the connection between the input ground and GND pin as short and wide as possible.

2) Keep the connection between the input capacitor and IN pin as short and wide as possible.

3) Use short and direct feedback connections. Place the feedback resistors and compensation components as close to the chip as possible.

4) Route SW away from sensitive analog areas such as FB.

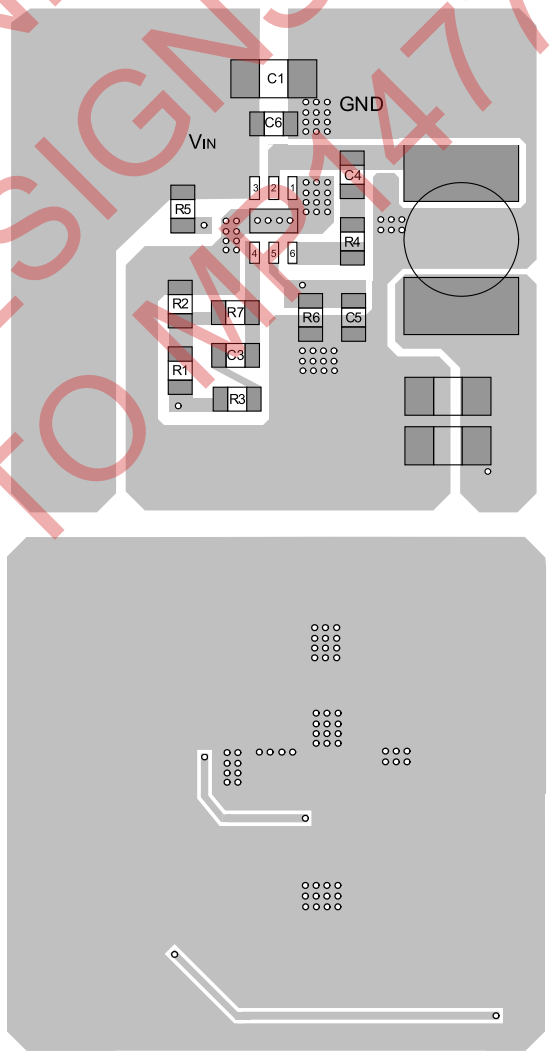


Figure 8: Sample Layout

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP1477

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2013 MPS. All Rights Reserved.

Design Example

Below is a design example following the application guidelines for the specifications:

Table 2—Design Example

V_{IN}	12V
V_{OUT}	3.3V
Io	3A

The detailed application schematic is shown in Figure 10. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more device applications, please refer to the related Evaluation Board Datasheets.

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP1477

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2013 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS

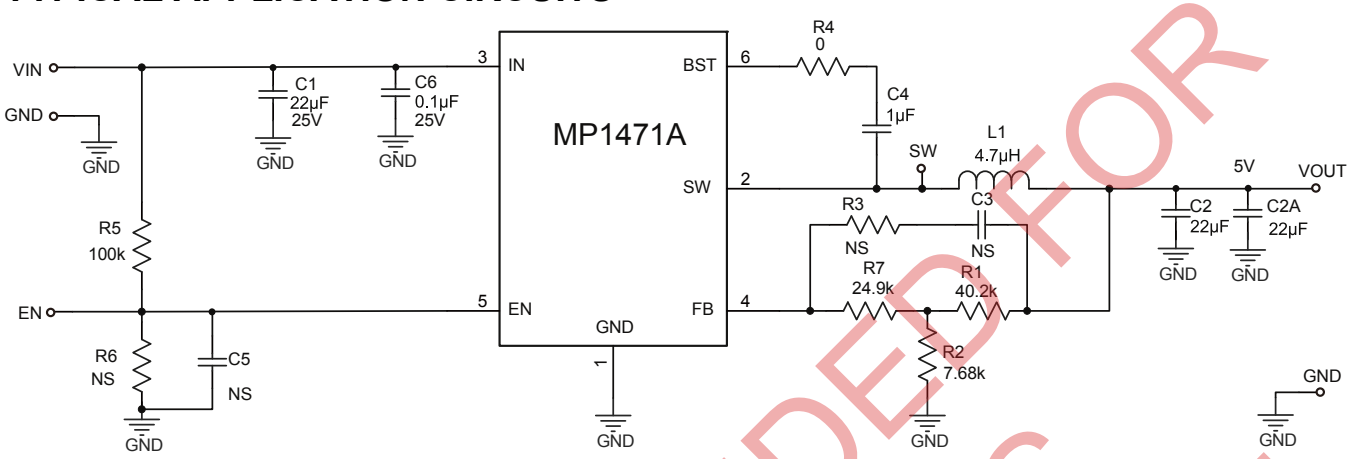


Figure 9: $12V_{IN}$, 5V/3A

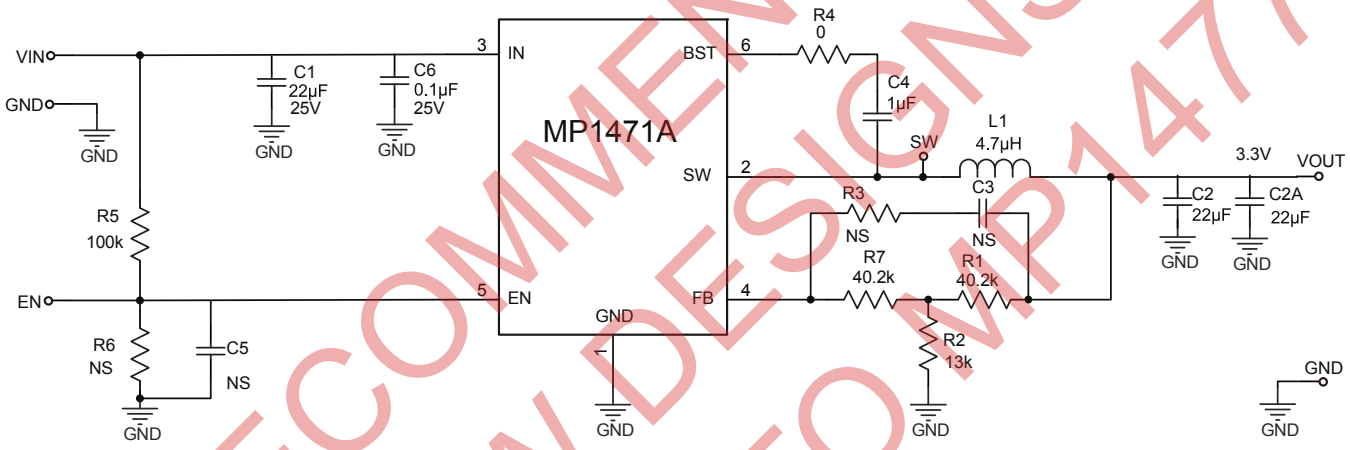


Figure 10: $12V_{IN}$, 3.3V/3A

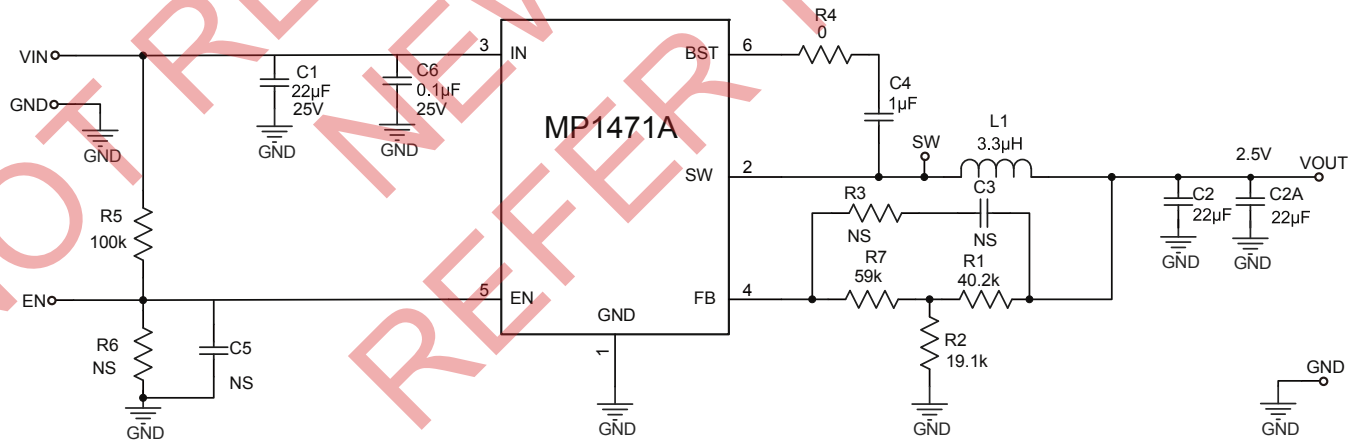


Figure 11: $12V_{IN}$, 2.5V/3A

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP1477

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2013 MPS. All Rights Reserved.

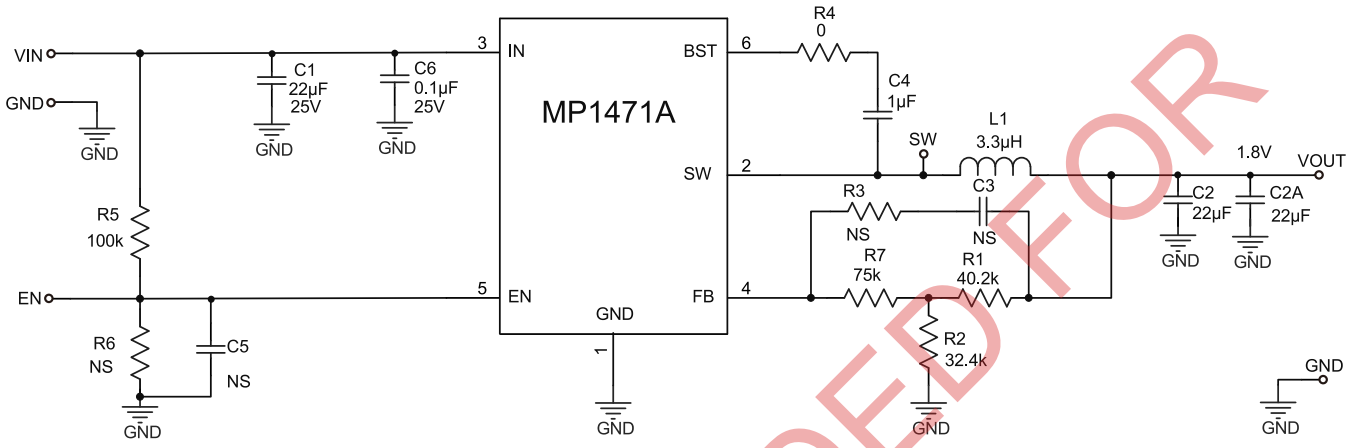


Figure 12: $12V_{IN}$, 1.8V/3A

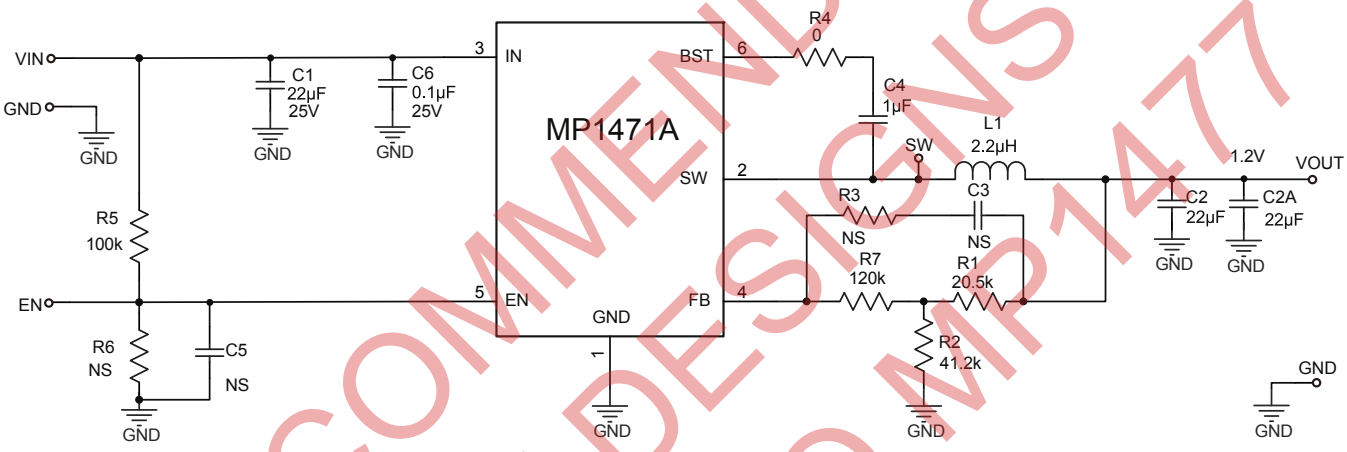


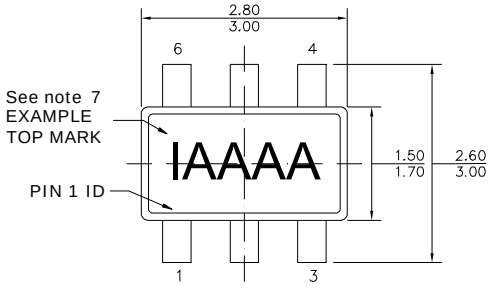
Figure 13: $12V_{IN}$, 1.2V/3A

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP1477

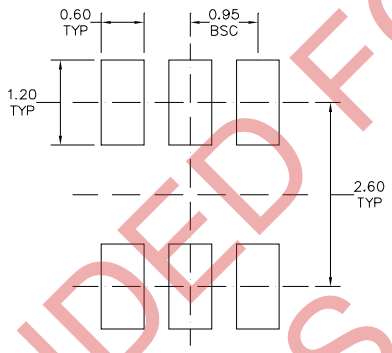
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2013 MPS. All Rights Reserved.

PACKAGE INFORMATION

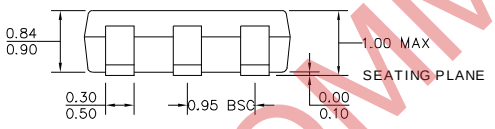
TSOT23-6



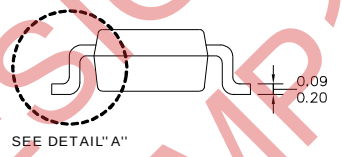
TOP VIEW



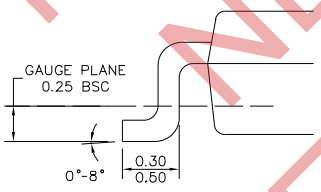
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO193, VARIATION AB.
6) DRAWING IS NOT TO SCALE
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP1477

NOTICE: The information in this document is subject to change without notice. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2013 MPS. All Rights Reserved.