DESCRIPTION

The MP020A-5 is an offline, primary-side regulator that provides accurate constant voltage and constant current regulation without an optocoupler or a secondary feedback circuit. The MP020A-5 has an integrated 700V MOSFET.

The MP020A-5's variable off-time control allows a flyback converter to operate in discontinuous conduction mode (DCM). The MP020A-5 also features protection functions such as VCC under-voltage lockout (UVLO), over-current protection (OCP), over-temperature protection (OTP), open-circuit protection (OCkP), and over-voltage protection (OVP). Its internal high-voltage start-up current source and power-saving technologies limit the no-load power consumption to less than 30mW.

The MP020A-5's variable switching frequency technology provides natural spectrum shaping to smooth the EMI signature, making it suitable for offline, low-power battery chargers and adapters.

The MP020A-5 is available in a SOIC8-7A package.

FEATURES

- Primary-Side Control without Optocoupler or Secondary Feedback Circuit
- Precise Constant Current and Constant Voltage Control (CC/CV)
- Integrated 700V MOSFET with Minimal External Components
- Variable Off Time, Peak-Current Control
- 550μA High-Voltage Current Source
- 30mW No-Load Power Consumption
- Programmable Cable Compensation
- OVP, OCP, OCkP, OTP, and VCC UVLO
- Natural Spectrum Shaping for Improved EMI Signature
- Low Cost and Simple External Circuit
- Available in a SOIC8-7A Package

APPLICATIONS

- Cell Phone Chargers
- Adapters for Handheld Electronics
- Standby and Auxiliary Power Supplies
- Small Appliances

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ORDERING INFORMATION

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<th>Part Number*</th>
<th>Package</th>
<th>Top Marking</th>
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<tr>
<td>MP020A-5GS</td>
<td>SOIC8-7A</td>
<td>See Below</td>
</tr>
</tbody>
</table>

* For Tape & Reel, add suffix –Z (e.g. MP020A-5GS–Z)

TOP MARKING

MP020A-5
LLLLLLLLL
MPSYWW

MP020A-5: Product code of MP020A-5GS
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

PACKAGE REFERENCE

TOP VIEW

<p>| | | |</p>
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<td></td>
<td>5</td>
</tr>
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<td>4</td>
<td></td>
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</tr>
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VCC  GND  FB  CP  DRAIN  GND  GND

SOIC8-7A
**ABSOLUTE MAXIMUM RATINGS** (1)

- DRAIN to GND: -0.7V to 700V
- VCC to GND: -0.3V to 30V
- CP to GND: -0.3V to 7V
- FB input: -0.7V to 10V

Continuous power dissipation (T_A = +25°C) (2)
- SOIC8-7A: 1.3W

Thermal Resistance (4)
- θ_JA: 76°C/W
- θ_JC: 45°C/W

**Recommended Operating Conditions** (3)

- Operating junction temp. (T_J): -40°C to +125°C
- Operating VCC range: 6.6V to 28V

**NOTES:**

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_JA, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A)/θ_JA. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.
## ELECTRICAL CHARACTERISTICS

**VCC = 15V, T_A = 25°C, unless otherwise noted.**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
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<tr>
<td><strong>Supply Voltage Management (VCC)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>VCC on threshold</td>
<td>V_CCH</td>
<td></td>
<td>16.8</td>
<td>17.3</td>
<td>17.8</td>
<td>V</td>
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<tr>
<td>VCC off threshold</td>
<td>V_CCL</td>
<td></td>
<td>6</td>
<td>6.3</td>
<td>6.6</td>
<td>V</td>
</tr>
<tr>
<td>VCC operating voltage</td>
<td></td>
<td></td>
<td>6.6</td>
<td></td>
<td>28</td>
<td>V</td>
</tr>
<tr>
<td>Quiescent current</td>
<td>I_Q</td>
<td>At no load condition, VCC = 20V</td>
<td>360</td>
<td>410</td>
<td></td>
<td>µA</td>
</tr>
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<td>Operating current</td>
<td>I_OP</td>
<td>60kHz, VCC = 20V</td>
<td>500</td>
<td></td>
<td></td>
<td>µA</td>
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<tr>
<td>Leakage current from VCC</td>
<td>I_Leak_VCC</td>
<td>VCC = 0 → 16V, DRAIN floating</td>
<td>0.1</td>
<td>1</td>
<td></td>
<td>µA</td>
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<tr>
<td><strong>Internal MOSFET (DRAIN)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Break-down voltage</td>
<td>V_BRDSS</td>
<td>VCC = 20V, V_FB = 7V</td>
<td>700</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Supply current from DRAIN</td>
<td>I_Charge</td>
<td>VCC = 4V, V_DRAIN = 100V</td>
<td>450</td>
<td>550</td>
<td>750</td>
<td>µA</td>
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<tr>
<td>Leakage current from DRAIN</td>
<td>I_Leak_Drain</td>
<td>V_DS = 500VDC</td>
<td>1</td>
<td>10</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>On-state resistance</td>
<td>R_ON</td>
<td>I_D = 10mA, T_J = 20°C</td>
<td>10</td>
<td>13</td>
<td></td>
<td>Ω</td>
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<tr>
<td>Minimum switching frequency</td>
<td>f_MIN</td>
<td>At no load condition</td>
<td>120</td>
<td></td>
<td></td>
<td>Hz</td>
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<tr>
<td><strong>Internal Current Sense</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Current limit</td>
<td>I_Limit</td>
<td>V_FB = -0.5V</td>
<td>365</td>
<td>380</td>
<td>395</td>
<td>mA</td>
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<td>Leading-edge blanking</td>
<td>t_LEB</td>
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<td>230</td>
<td>300</td>
<td>370</td>
<td>ns</td>
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<tr>
<td><strong>Feedback Input (FB)</strong></td>
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<td></td>
<td></td>
<td></td>
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<tr>
<td>FB input current</td>
<td>I_FB</td>
<td>V_FB = 4V, V_CP = 3V</td>
<td>10</td>
<td>14</td>
<td>18</td>
<td>µA</td>
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<tr>
<td>FB threshold</td>
<td>V_FB</td>
<td></td>
<td>3.93</td>
<td>4</td>
<td>4.07</td>
<td>V</td>
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<td>DCM detect threshold</td>
<td>V_DCM</td>
<td></td>
<td>80</td>
<td>120</td>
<td>160</td>
<td>mV</td>
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<td>FB open-circuit threshold</td>
<td>V_FBOPEN</td>
<td></td>
<td>-0.22</td>
<td>-0.15</td>
<td>-0.08</td>
<td>V</td>
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<td>FB OVP threshold</td>
<td>V_FB_OVP</td>
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<td>6.2</td>
<td>6.35</td>
<td>6.5</td>
<td>V</td>
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<td>OVP sample delay</td>
<td>t_OVP</td>
<td></td>
<td>3.5</td>
<td></td>
<td></td>
<td>µs</td>
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<tr>
<td><strong>Output Cable Compensation (CP)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cable compensation voltage</td>
<td>V_CP</td>
<td>Full load</td>
<td>2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td><strong>Thermal Shutdown</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal shutdown threshold</td>
<td></td>
<td></td>
<td>150</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Thermal shutdown recovery threshold</td>
<td></td>
<td></td>
<td>120</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>
TYPICAL CHARACTERISTICS

Charge Current vs. Junction Temperature

Leakage Current vs. Junction Temperature

Breakdown Voltage vs. Junction Temperature

VCC ON Threshold vs. Junction Temperature

VCC OFF Threshold vs. Junction Temperature

Feedback Threshold vs. Junction Temperature

DCM Detect Threshold vs. Temperature Chart

FB Open Circuit Threshold vs. Junction Temperature

FB OVP Threshold vs. Junction Temperature
TYPICAL CHARACTERISTICS (continued)

<table>
<thead>
<tr>
<th>OVP Sample Delay vs. Junction Temperature</th>
</tr>
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<tbody>
<tr>
<td><img src="image1" alt="OVP Sample Delay vs. Junction Temperature Graph" /></td>
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<table>
<thead>
<tr>
<th>On State Resistance vs. Junction Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image2" alt="On State Resistance vs. Junction Temperature Graph" /></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Current Limit vs. Junction Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image3" alt="Current Limit vs. Junction Temperature Graph" /></td>
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</tbody>
</table>
TYPICAL PERFORMANCE CHARACTERISTICS
Performance waveforms are tested on the evaluation board in the Design Example section.

\( V_{IN} = 230\,\text{VAC}, V_{OUT} = 5\,\text{V}, I_{OUT} = 1\,\text{A}, L = 1.6\,\text{mH}, T_A = 25^\circ\text{C}, \) unless otherwise noted.

**Input Power Start-Up**

\[ V_{DS}, 100\,\text{V/div.}, V_{OUT}, 2\,\text{V/div.} \]

200ms/div.

**Input Power Shutdown**

\[ V_{DS}, 100\,\text{V/div.}, V_{OUT}, 2\,\text{V/div.} \]

40ms/div.

**OCP Entry**

\[ V_{DS}, 100\,\text{V/div.}, V_{OUT}, 2\,\text{V/div.} \]

400ms/div.

**OCP Recovery**

\[ V_{DS}, 100\,\text{V/div.}, V_{CC}, 5\,\text{V/div.} \]

400ms/div.

**OVP Entry**

\[ V_{DS}, 100\,\text{V/div.}, V_{CC}, 10\,\text{V/div.} \]

1s/div.

**OVP Recovery**

\[ V_{DS}, 100\,\text{V/div.}, V_{CC}, 10\,\text{V/div.} \]

1s/div.

**Output Voltage Ripple**

\[ V_{OUT}, \text{AC Coupled}, 50\,\text{mV/div.} \]

10μs/div.

**Load Transient**

\[ V_{OUT}, 1\,\text{V/div.}, I_{OUT}, 200\,\text{mA/div.} \]

20ms/div.

**Normal Operation**

\[ V_{DS}, 100\,\text{V/div.}, V_{OUT}, 2\,\text{V/div.} \]

2μs/div.
TYPICAL PERFORMANCE CHARACTERISTICS (continued)
Performance waveforms are tested on the evaluation board in the Design Example section. 
$V_{IN} = 230V_{AC}$, $V_{OUT} = 5V$, $I_{OUT} = 1A$, $L = 1.6mH$, $T_A = 25^\circ C$, unless otherwise noted.

MP020A-5 CV/CC Characteristics
### PIN FUNCTIONS

<table>
<thead>
<tr>
<th>SOIC8-7A Pin #</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VCC</td>
<td><strong>Supply.</strong> The IC begins functioning when VCC charges to the on threshold ((V_{\text{CH}})) through an internal high-voltage current source. When VCC falls below the off threshold ((V_{\text{CL}})), the internal high-voltage current source turns on to charge VCC. Connect a 0.1(\mu)F decoupling ceramic capacitor for most applications.</td>
</tr>
<tr>
<td>2, 5, 6</td>
<td>GND</td>
<td><strong>Ground.</strong></td>
</tr>
<tr>
<td>3</td>
<td>FB</td>
<td><strong>Feedback.</strong> FB provides the output reference voltage and detects the falling voltage edges to determine the operation mode (CV mode or CC mode).</td>
</tr>
<tr>
<td>4</td>
<td>CP</td>
<td><strong>Output cable compensation.</strong> Connect a 1(\mu)F ceramic capacitor as a low pass filter. The upper resistor of the resistor divider connected to FB adjusts the compensation voltage.</td>
</tr>
<tr>
<td>8</td>
<td>DRAIN</td>
<td><strong>Internal MOSFET drain.</strong> DRAIN is the input for the high-voltage start-up current source.</td>
</tr>
</tbody>
</table>
Figure 1: Functional Block Diagram
OPERATION

Start-Up
Initially, the IC is self-supplying through an internal high-voltage current source, which is drawn from DRAIN. The internal high-voltage current source turns off for better efficiency when VCC reaches its on threshold (VCH). Then the transformer’s auxiliary winding takes over as the power source. When VCC falls below its off threshold (VCL), the IC stops switching, and the internal high-voltage current source turns on again (see Figure 1).

![Primary Current Waveform](image)

Figure 1: Primary Current Waveform

When IP(t) rises up to IPK, the internal MOSFET turns off (see Figure 4). Then the energy stored in the inductor transfers to the secondary side through the transformer.

The inductor (LM) stores energy with each cycle as a function shown in Equation (2):

\[
E = \frac{1}{2} L_M \times I_{PK}^2
\]

(2)

The power transferred from the input to the output can be determined with Equation (3):

\[
P = \frac{1}{2} L_M \times I_{PK}^2 \times f_S
\]

(3)

Where fS is the switching frequency. When IPK is constant, the output power depends on fS.

Constant Voltage (CV) Operation
The MP020A-5 detects the auxiliary winding voltage from FB and operates in constant voltage (CV) mode to regulate the output voltage. Assume the secondary winding is the master and the auxiliary winding is the slave. When the secondary-side diode turns on, the FB voltage can be calculated with Equation (4):

\[
V_{FB} = \frac{N_{P_{AU}}}{N_S} \times (V_O + V_D) \times \frac{R_{DOWN}}{R_{UP} + R_{DOWN}}
\]

(4)

Where VD is the secondary-side diode forward-drop voltage, VO is the output voltage, NP_AU is the number of auxiliary winding turns, NS is the number of secondary side winding turns, and RUP and RDOWN are the resistor divider for sampling.
Leading-Edge Blanking

The parasitic capacitances induce a spike on the sense resistor when the power switch turns on. The MP020A-5 includes a 300ns leading-edge blanking period to avoid falsely terminating the switching pulse. During this blanking period, the current sense comparator is disabled, and the gate driver cannot switch off (see Figure 4).

DCM Detection

The MP020A-5 operates in DCM in both CV and CC modes. To avoid operating in continuous conduction mode (CCM), the MP020A-5 detects the falling edge of the FB input voltage with each cycle. If the chip does not detect a 120mV falling edge, it stops switching.

OVP and OCKP

The MP020A-5 includes over-voltage protection (OVP) and open-circuit protection (OCKP). If the voltage at FB exceeds 6.35V for 3.5µs, or the FB input’s 0.15V falling edge cannot be monitored, the MP020A-5 immediately shuts off the driving signals and enters hiccup mode. The MP020A-5 resumes normal operation when the fault has been removed.

Thermal Shutdown

When the temperature of the IC exceeds 150°C, over-temperature protection (OTP) is triggered, and the IC enters auto-recovery mode. When the temperature falls below 120°C, the IC recovers.
Output Cable Compensation

To compensate for the secondary-side cable voltage drop for a more precise output voltage, the MP020A-5 has an internal output cable compensation circuit (see Figure 5). The internal ZCD sample can detect the duty of the secondary-side diode. A low-pass filter converts the duty signal to a DC voltage ($V_{CP}$) that changes as the load current varies.

$V_{CP}$ can be converted to a current signal drawn from FB. The voltage drop on $R_{UP}$ helps the output cable compensation. When the system operates in the maximum load, the CP voltage reaches a maximum of 2V.

Determine the compensation voltage with Equation (7):

$$V_{FCP} = \frac{5.6 \times D_S \times 2 \times R_{UP} \times N_S}{N_{P,AU}}$$

Where $V_{FCP}$ is the secondary-side compensation voltage drop, $D_S$ is the secondary-diode duty cycle in CC mode (0.4 for the MP020A-5), $R_{UP}$ is the upper resistor of the resistor divider, $N_S$ is the number of turns for the secondary-side transformer windings, and $N_{P,AU}$ is the number of transformer auxiliary winding turns.

![Figure 5: Output Cable Compensator](image-url)
APPLICATION INFORMATION

Input Filter
The input filter helps convert the AC input to a DC source through the rectifier. Figure 6 shows the input filter, and Figure 7 shows the typical DC bus voltage waveform.

![Input Filter Diagram](image)

**Figure 6: Input Filter**

![DC Input Voltage Waveform](image)

**Figure 7: DC Input Voltage Waveform**

Bulk capacitors (C1 and C2) filter the rectified AC input. The inductor (L) forms a π filter with C1 and C2 to restrain the differential mode EMI noise. The resistor (R) parallel with L restrains the mid-frequency band EMI noise. Normally, R is 1 - 10kΩ.

C1 and C2 are usually set as 2µF/W to 3µF/W for the universal input condition. For 230VAC single-range applications, halve the capacitor values. Avoid using very low minimum DC voltages to ensure that the converter can supply the maximum power load, which can be calculated with Equation (8):

\[
V_{DC(min)} \geq \frac{N_p}{N_s} \cdot (V_o + V_o) \cdot \frac{D_s}{1 - D_s} \quad (8)
\]

If \( V_{DC(min)} \) cannot satisfy this expression, increase the value of the input capacitors to increase \( V_{DC(min)} \).

Output Capacitor
Use low ESR or very low ESR output capacitors to meet the output voltage ripple requirement without using an LC post filter. Using low ESR capacitors improves output voltage regulation and feedback voltage sampling at high temperatures or low temperatures. Use an output capacitor with an ESR below 100mΩ for better efficiency over high ESR output capacitors.

Output Diode
Use a Schottky diode because of its fast switching speed and low forward-voltage drop for better high- or low-temperature CV regulation and efficiency.

If the lower average efficiency (3% to 4%) is sufficient, replace the output diode with a fast or ultra-fast diode to reduce costs. Be sure to readjust the resistor divider values to the correct output voltage because the forward voltage drop is higher than the Schottky diode’s.

Leakage Inductance
The transformer’s leakage inductance decreases the system efficiency and affects the output current or voltage constant precision. Optimize the transformer structure to minimize the leakage inductance. Aim for a leakage inductance less than 5% of the primary inductance.

RCD Snubber
The transformer’s leakage inductance causes the MOSFET drain voltage to spike and excessive ringing on the drain voltage waveform, which affects the output voltage sampling 3.5µs after the MOSFET turns off.

The RCD snubber circuit can limit the DRAIN voltage spike. Figure 8 shows the RCD snubber circuit.
The damping resistor in series with the RCD has a relatively large value to prevent any excessive voltage ringing that can affect the CV sampling and increase the output ripple. Use a 200 - 500Ω damping resistor to restrain the drain-voltage ringing.

**Divided Resistor**

For better application performance, select the resistor divider’s total value to be between 40 - 100kΩ. Smaller resistors draw larger currents from the auxiliary winding, which increases the no-load consumption. Larger resistors may also pick up noise from adjacent components.

If necessary, use a resistor between 1kΩ and 2kΩ connected between the FB and resistor divider. \( R_{FB} \) can also limit substrate injection current effects (see Figure 9).

**Dummy Load**

When the system operates without a load and no dummy load, the output voltage rises above the normal operation because of the minimum switching frequency limitation. Use a dummy load for good load regulation. However, a large dummy load deteriorates efficiency and no-load consumption, so selecting the dummy load is a tradeoff between efficiency and load regulation. For most applications, use a dummy load around 10mW, which satisfies the 30mW requirement.
Maximum Switching Frequency
Use a secondary-side diode conduction time that exceeds 5.4µs, as shown in Equation (12):

\[ T_{S,\text{ON}} = I_{\text{PK}} \cdot \frac{N_S \cdot L_M}{N_P \cdot (V_O + V_D)} > 5.4\mu s \] (12)

For high- or low-temperature applications, select a maximum switching frequency below 75kHz.

PCB Layout Guide
Efficient PCB layout is critical for reliable operation, good EMI, and good thermal performance. For best results, refer to Figure 10 and follow the guidelines below.

1. Minimize the loop area formed by the input capacitor, the MP020A-5 drain-source, and the primary winding to reduce EMI noise.
2. Provide at least 1in² of top-side copper for adequate heat-sinking.
3. The copper area connected to GND is the heat conduction path for the MP020A-5.
4. Minimize the clamp circuit loop to reduce EMI.
5. Minimize the secondary loop area of the output diode and output filter to reduce EMI noise.
6. Provide sufficient copper area at the anode and cathode terminal of the output diode to act as a heat sink.
7. Place the AC input away from the switching nodes to minimize the noise coupling that may bypass the input filter.
8. Place the bypass capacitor as close as possible to the IC and source.
9. Place the feedback resistors next to FB.
10. Minimize the feedback sampling loop to minimize noise coupling.
11. Use a single-point connection at the negative terminal of the input filter capacitor for the MP020A-5 source pin and bias winding return.

Design Example
Table 1 shows a design example following the application guidelines based on the specifications below.

| \( V_{IN} \) | 85 ~ 265V\text{AC} |
| \( V_{OUT} \) | 5V |
| \( I_{OUT} \) | 1A |
| \( f_S \) | 60kHz |

Figure 14 through Figure 16 show the detailed application schematic. This circuit was used for the typical performance and circuit waveforms. For more device applications, please refer to the related evaluation board datasheets.

The transformer structure used in Figure 14 can benefit from passing the 3-wire conducted EMI test (output GND connect to earth) without the Y-cap. The Y-cap results in leakage current, which is prohibited in some cell phone charger applications. Figure 15 illustrates how the common noise of the secondary-side diode is restrained. The secondary-side winding splits to two separate windings (\( N_{SEC1} \) and \( N_{SEC2} \)), which
have the same turns and approximate parasitic capacitors ($C_{SP1}$ and $C_{SP2}$), but their hot spot is opposite (Point 9 and Point 10 in Figure 15). Therefore, the common mode noise current produced at the secondary-side windings can counteract each other.

The transformer structure is simple if the application does not need to pass the 3-wire conducted EMI or uses a Y-cap. Figure 16 shows a schematic with a simple transformer structure.
TYPICAL APPLICATION CIRCUITS

Figure 11: 5V/1A with Complicated Transformer Structure

Figure 15: Secondary Side Windings Structure to Restrain the Common Mode Noise
Figure 16: 5V/1A with Simple Transformer Structure
FLOW CHART

Figure 17: Flow Chart
NOTICE: The information in this document is subject to change without notice. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

NOTE:
1) CONTROL DIMENSION IS IN INCHES  DIMENSION IN BRACKET IS IN MILLIMETERS
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) JEDEC REFERENCE IS MS-012.
6) DRAWING IS NOT TO SCALE