



## ORDERING INFORMATION

| Part Number* | Package   | Top Marking | MSL Rating |
|--------------|-----------|-------------|------------|
| MDC97476GJ   | TSOT-23-6 | CDKY        | 1          |
| MDC97477GJ   |           | CDLY        |            |
| MDC97478GJ   |           | CDMY        |            |

\* For Tape & Reel, add suffix -Z (e.g. MDC97476GJ-Z).

## TOP MARKING

| CDKY

CDK: Product code of MDC97476  
Y: Year code

## TOP MARKING

| CDLY

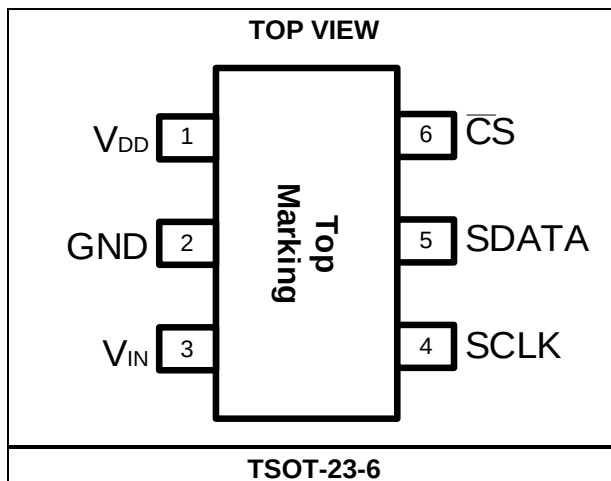
CDL: Product code of MDC97477  
Y: Year code

## TOP MARKING

| CDMY

CDM: Product code of MDC97478  
Y: Year code

## PACKAGE REFERENCE



## PIN FUNCTIONS

| Pin # | Name            | I/O    | Description                                                                                     |
|-------|-----------------|--------|-------------------------------------------------------------------------------------------------|
| 1     | VDD             | Power  | <b>Positive power supply pin.</b> The VDD pin's voltage ( $V_{DD}$ ) ranges between 3V and 3.6V |
| 2     | GND             | Ground | <b>Ground pin.</b>                                                                              |
| 3     | VIN             | Input  | <b>Analog input pin.</b> The VIN pin's voltage ranges between 0V and $V_{DD}$ .                 |
| 4     | SCLK            | Input  | <b>Digital clock input.</b>                                                                     |
| 5     | SDATA           | Output | <b>Digital data output.</b> The SDATA pin is clocked out at the falling edge of SCLK.           |
| 6     | $\overline{CS}$ | Input  | <b>Chip select.</b> The falling edge of the $\overline{CS}$ pin starts the conversion.          |

### ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

$V_{DD}$  to GND .....-0.3V to +4V  
 $V_{IN}$  to GND.....-0.3V to  $V_{DD} + 0.3V$   
SCLK to GND .....-0.3V to 5.5V  
 $\overline{CS}$  to GND .....-0.3V to 5.5V  
SDATA to GND .....-0.3V to  $V_{DD} + 0.3V$   
Junction temperature ( $T_J$ ).....150°C  
Lead temperature .....260°C  
Storage temperature.....-65°C to +150°C

### ESD Ratings

Human body model (HBM) .....3.5kV  
Charged-device model (CDM) .....250V

### Recommended Operating Conditions <sup>(2)</sup>

$V_{DD}$  ..... 3V to +3.6V  
Digital input pins .....0V to 5V  
Operating temp ( $T_A$ )..... -40°C to +85°C

### Thermal Resistance <sup>(3)</sup>

$\theta_{JA}$   $\theta_{JC}$   
TSOT-23-6..... 143..... 76... °C/W

#### Notes:

- 1) Exceeding these ratings may damage the device.
- 2) The device is not guaranteed to function outside of its operating conditions.
- 3) Measured on a JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS (MDC97476)

$V_{DD} = 3.3V$ ,  $V_{CS}$ ,  $V_{SCLK} = 0V$  to  $3.3V$  <sup>(4)</sup>,  $f_{SCLK} = 20MHz$ ,  $f_{SAMPLE} = 1MSPS$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$  <sup>(5)</sup>, unless otherwise noted.

| Parameter                                  | Symbol              | Conditions               | Min   | Typ                  | Max             | Units |
|--------------------------------------------|---------------------|--------------------------|-------|----------------------|-----------------|-------|
| Dynamic Characteristics                    |                     |                          |       |                      |                 |       |
| Signal-to-noise ratio                      | SNR                 | f <sub>IN</sub> = 120kHz | 68.5  | 72                   |                 | dBFS  |
| Signal-to-(noise and distortion) ratio     | SINAD               | f <sub>IN</sub> = 120kHz | 68    | 71                   |                 | dBFS  |
| Total harmonic distortion                  | THD                 | f <sub>IN</sub> = 120kHz |       | -83                  |                 | dB    |
| Spurious free dynamic range                | SFDR                | f <sub>IN</sub> = 120kHz |       | 83                   |                 | dB    |
| Static Characteristics                     |                     |                          |       |                      |                 |       |
| No missing codes                           |                     |                          | 12    |                      |                 | Bits  |
| Integral nonlinearity                      | INL                 |                          | -1.3  |                      | +1.2            | LSB   |
| Differential nonlinearity                  | DNL                 |                          | -0.95 |                      | +1.25           | LSB   |
| Gain error <sup>(6)</sup>                  | GE                  |                          | -4    |                      | +4              | LSB   |
| Offset error <sup>(6)</sup>                | V <sub>OFF</sub>    |                          | -11   |                      | +11             | LSB   |
| Analog Input                               |                     |                          |       |                      |                 |       |
| Input voltage range                        | V <sub>IN</sub>     |                          | 0     | 0 to V <sub>DD</sub> | V <sub>DD</sub> | V     |
| DC leakage current                         | I <sub>L</sub>      |                          |       |                      | 1               | μA    |
| Input capacitance <sup>(7)</sup>           | C <sub>IN_A</sub>   |                          |       | 14                   |                 | pF    |
| Digital Input                              |                     |                          |       |                      |                 |       |
| Input high voltage                         | V <sub>INH</sub>    |                          | 2.4   |                      |                 | V     |
| Input low voltage                          | V <sub>INL</sub>    |                          |       |                      | 0.8             | V     |
| Input current                              | I <sub>IN</sub>     |                          |       |                      | 1               | μA    |
| Input capacitance <sup>(7)</sup>           | C <sub>IN_D</sub>   |                          |       | 2                    |                 | pF    |
| Digital Output                             |                     |                          |       |                      |                 |       |
| Output high voltage                        | V <sub>OH</sub>     | I <sub>LOAD</sub> = 1mA  | 3.1   |                      |                 | V     |
| Output low voltage                         | V <sub>OL</sub>     | I <sub>LOAD</sub> = 1mA  |       |                      | 1               | V     |
| Floating output capacitance <sup>(7)</sup> | C <sub>OUT</sub>    |                          |       | 2                    |                 | pF    |
| Floating output current <sup>(7)</sup>     | I <sub>OL</sub>     |                          |       |                      | 1               | μA    |
| Power Supply Characteristics               |                     |                          |       |                      |                 |       |
| Power supply voltage                       | V <sub>DD</sub>     |                          |       | 3.3                  |                 | V     |
| Static normal mode current                 | I <sub>DDS</sub>    |                          |       | 0.73                 |                 | mA    |
| Operation normal mode current              | I <sub>DDOP</sub>   |                          |       | 1.3                  | 1.8             | mA    |
| Sleep mode current                         | I <sub>SD</sub>     | SCLK off                 |       | 36                   |                 | μA    |
|                                            |                     | SCLK on                  |       | 120                  |                 | μA    |
| Operational normal mode power consumption  | P <sub>OP</sub>     |                          |       | 4.3                  |                 | mW    |
| Sleep power consumption                    | P <sub>SD</sub>     | SCLK off                 |       | 120                  |                 | μW    |
|                                            |                     | SCLK on                  |       | 400                  |                 | μW    |
| AC Electrical Characteristics              |                     |                          |       |                      |                 |       |
| Clock frequency                            | f <sub>SCLK</sub>   |                          |       |                      | 20              | MHz   |
| SCLK duty cycle                            |                     |                          |       | 50%                  |                 |       |
| Throughput rate                            | f <sub>SAMPLE</sub> |                          |       |                      | 1               | MHz   |

## ELECTRICAL CHARACTERISTICS (MDC97477)

$V_{DD} = 3.3V$ ,  $V_{CS}$ ,  $V_{SCLK} = 0V$  to  $3.3V$  <sup>(4)</sup>,  $f_{SCLK} = 20MHz$ ,  $f_{SAMPLE} = 1MSPS$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$  <sup>(5)</sup>, unless otherwise noted.

| Parameter                                  | Symbol              | Conditions               | Min  | Typ   | Max             | Units |
|--------------------------------------------|---------------------|--------------------------|------|-------|-----------------|-------|
| Dynamic Characteristics                    |                     |                          |      |       |                 |       |
| Signal to noise ratio                      | SNR                 | f <sub>IN</sub> = 120kHz | 61   | 61.8  |                 | dBFS  |
| Signal-to-(noise and distortion) ratio     | SINAD               | f <sub>IN</sub> = 120kHz | 60.8 | 61.8  |                 | dBFS  |
| Total harmonic distortion                  | THD                 | f <sub>IN</sub> = 120kHz |      | -80   |                 | dB    |
| Spurious free dynamic range                | SFDR                | f <sub>IN</sub> = 120kHz |      | 83    |                 | dB    |
| Static Characteristics                     |                     |                          |      |       |                 |       |
| No missing codes                           |                     |                          | 10   |       |                 | Bits  |
| Integral nonlinearity                      | INL                 |                          | -0.4 |       | +0.4            | LSB   |
| Differential nonlinearity                  | DNL                 |                          | -0.5 | ±0.14 | +0.4            | LSB   |
| Gain error <sup>(6)</sup>                  | GE                  |                          | -2.8 |       | +2.7            | LSB   |
| Offset error <sup>(6)</sup>                | V <sub>OFF</sub>    |                          | -4.2 |       | +4              | LSB   |
| Analog Input                               |                     |                          |      |       |                 |       |
| Input voltage range                        | V <sub>IN</sub>     |                          | 0    |       | V <sub>DD</sub> | V     |
| DC leakage current                         | I <sub>L</sub>      |                          |      |       | 1               | µA    |
| Input capacitance <sup>(7)</sup>           | C <sub>IN_A</sub>   |                          |      | 14    |                 | pF    |
| Digital Input                              |                     |                          |      |       |                 |       |
| Input high voltage                         | V <sub>INH</sub>    |                          | 2.4  |       |                 | V     |
| Input low voltage                          | V <sub>INL</sub>    |                          |      |       | 0.8             | V     |
| Input current                              | I <sub>IN</sub>     |                          |      |       | 1               | µA    |
| Input capacitance <sup>(7)</sup>           | C <sub>IN_D</sub>   |                          |      | 2     |                 | pF    |
| Digital Output                             |                     |                          |      |       |                 |       |
| Output high voltage                        | V <sub>OH</sub>     | I <sub>LOAD</sub> = 1mA  | 3.1  |       |                 | V     |
| Output low voltage                         | V <sub>OL</sub>     | I <sub>LOAD</sub> = 1mA  |      |       | 0.4             | V     |
| Floating output capacitance <sup>(7)</sup> | C <sub>OUT</sub>    |                          |      | 2     |                 | pF    |
| Floating output current <sup>(7)</sup>     | I <sub>OL</sub>     |                          |      |       | 1               | µA    |
| Power Supply Characteristics               |                     |                          |      |       |                 |       |
| Power supply voltage                       | V <sub>DD</sub>     |                          |      | 3.3   |                 | V     |
| Static normal mode current                 | I <sub>DDs</sub>    |                          |      | 0.73  |                 | mA    |
| Operation normal mode current              | I <sub>DDOP</sub>   |                          |      | 1.3   | 1.8             | mA    |
| Sleep mode current                         | I <sub>SD</sub>     | SCLK off                 |      | 36    |                 | µA    |
|                                            |                     | SCLK on                  |      | 120   |                 | µA    |
| Operational normal mode power consumption  | P <sub>OP</sub>     |                          |      | 4.3   |                 | mW    |
| Sleep power consumption                    | P <sub>SD</sub>     | SCLK off                 |      | 120   |                 | µW    |
|                                            |                     | SCLK on                  |      | 400   |                 | µW    |
| AC Electrical Characteristics              |                     |                          |      |       |                 |       |
| Clock frequency                            | f <sub>SCLK</sub>   |                          |      |       | 20              | MHz   |
| SCLK duty cycle                            |                     |                          |      | 50%   |                 |       |
| Throughput rate                            | f <sub>SAMPLE</sub> |                          |      |       | 1               | MHz   |

## ELECTRICAL CHARACTERISTICS (MDC97478)

$V_{DD} = 3.3V$ ,  $V_{CS}$ ,  $V_{SCLK} = 0V$  to  $3.3V$  <sup>(4)</sup>,  $f_{SCLK} = 20MHz$ ,  $f_{SAMPLE} = 1Mps$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$  <sup>(5)</sup>, unless otherwise noted.

| Parameter                                  | Symbol      | Conditions        | Min   | Typ  | Max      | Units   |
|--------------------------------------------|-------------|-------------------|-------|------|----------|---------|
| <b>Dynamic Characteristics</b>             |             |                   |       |      |          |         |
| Signal to noise ratio                      | SNR         | $f_{IN} = 120kHz$ | 48.8  | 49.9 |          | dBFS    |
| Signal-to-(noise and distortion) ratio     | SINAD       | $f_{IN} = 120kHz$ | 48.6  | 49.9 |          | dBFS    |
| Total harmonic distortion                  | THD         | $f_{IN} = 120kHz$ |       | -72  | -63      | dB      |
| Spurious free dynamic range                | SFDR        | $f_{IN} = 120kHz$ |       | 69   |          | dB      |
| <b>Static Characteristics</b>              |             |                   |       |      |          |         |
| No missing codes                           |             |                   | 8     |      |          | Bits    |
| Integral nonlinearity                      | INL         |                   | -0.19 |      | +0.15    | LSB     |
| Differential nonlinearity                  | DNL         |                   | -0.17 |      | +0.15    | LSB     |
| Gain error <sup>(6)</sup>                  | GE          |                   | -1.84 |      | +1.93    | LSB     |
| Offset error <sup>(6)</sup>                | $V_{OFF}$   |                   | -1.18 |      | +1.18    | LSB     |
| <b>Analog Input</b>                        |             |                   |       |      |          |         |
| Input voltage range                        | $V_{IN}$    |                   | 0     |      | $V_{DD}$ | V       |
| DC leakage current                         | $I_L$       |                   |       |      | 1        | $\mu A$ |
| Input capacitance <sup>(7)</sup>           | $C_{IN\_A}$ |                   |       | 14   |          | pF      |
| <b>Digital Input</b>                       |             |                   |       |      |          |         |
| Input high voltage                         | $V_{INH}$   |                   | 2.4   |      |          | V       |
| Input low voltage                          | $V_{INL}$   |                   |       |      | 0.8      | V       |
| Input current                              | $I_{IN}$    |                   |       |      | 1        | $\mu A$ |
| Input capacitance <sup>(7)</sup>           | $C_{IN\_D}$ |                   |       | 2    |          | pF      |
| <b>Digital Output</b>                      |             |                   |       |      |          |         |
| Output high voltage                        | $V_{OH}$    | $I_{LOAD} = 1mA$  | 3.1   |      |          | V       |
| Output low voltage                         | $V_{OL}$    | $I_{LOAD} = 1mA$  |       |      | 0.4      | V       |
| Floating output capacitance <sup>(7)</sup> | $C_{OUT}$   |                   |       | 2    |          | pF      |
| Floating output current <sup>(7)</sup>     | $I_{OL}$    |                   |       |      | 1        | $\mu A$ |
| <b>Power Supply Characteristics</b>        |             |                   |       |      |          |         |
| Power supply voltage                       | $V_{DD}$    |                   |       | 3.3  |          | V       |
| Static normal mode current                 | $I_{DDs}$   |                   |       | 0.73 |          | mA      |
| Operation normal mode current              | $I_{DDOP}$  |                   |       | 1.3  | 1.8      | mA      |
| Sleep mode current                         | $I_{SD}$    | SCLK off          |       | 36   |          | $\mu A$ |
|                                            |             | SCLK on           |       | 120  |          | $\mu A$ |
| Operational normal mode power consumption  | $P_{OP}$    |                   |       | 4.3  |          | mW      |
| Sleep power consumption                    | $P_{SD}$    | SCLK off          |       | 120  |          | $\mu W$ |
|                                            |             | SCLK on           |       | 400  |          | $\mu W$ |

## ELECTRICAL CHARACTERISTICS (MDC97478) (continued)

$V_{DD} = 3.3V$ ,  $V_{CS}$ ,  $V_{SCLK} = 0V$  to  $3.3V$  <sup>(4)</sup>,  $f_{SCLK} = 20MHz$ ,  $f_{SAMPLE} = 1MSPS$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$  <sup>(5)</sup>, unless otherwise noted.

| Parameter                            | Symbol       | Conditions | Min | Typ | Max | Units |
|--------------------------------------|--------------|------------|-----|-----|-----|-------|
| <b>AC Electrical Characteristics</b> |              |            |     |     |     |       |
| Clock frequency                      | $f_{SCLK}$   |            |     |     | 20  | MHz   |
| SCLK duty cycle                      |              |            |     | 50% |     |       |
| Throughput rate                      | $f_{SAMPLE}$ |            |     |     | 1   | MHz   |

### Notes:

- 4) Tested with an SPI interface from 0V to 3.3V. Functional from 0V to 5V.
- 5) Production tested at 25°C.
- 6) The offset error and gain errors are based on the relationship between the ADC output code and ADC input voltage ( $V_{IN}$ ). See the ADC Conversion Result section on page 15 for more information.
- 7) Values confirmed by engineering characterization.



## TIMING CHARACTERISTICS <sup>(8)</sup> <sup>(9)</sup> <sup>(10)</sup>

$V_{DD} = 3.3V$ ,  $V_{CS}$ ,  $V_{SCLK} = 0V$  to  $3.3V$  <sup>(4)</sup>,  $f_{SCLK} = 20MHz$ ,  $f_{SAMPLE} = 1MSPS$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$  <sup>(5)</sup>, unless otherwise noted.

| Parameter                                                 | Symbol        | Conditions | Min                   | Typ                   | Max | Units   |
|-----------------------------------------------------------|---------------|------------|-----------------------|-----------------------|-----|---------|
| SCLK period                                               | $t_{SCLK}$    |            | 50                    |                       |     | ns      |
| Conversion time                                           | $t_{ON}$      |            |                       | $16 \times t_{SCLK}$  |     | ns      |
| Quiet time                                                | $t_{QUIET}$   |            | 50                    |                       |     | ns      |
| Minimum $\overline{CS}$ pulse width                       | $t_1$         |            | 10                    |                       |     | ns      |
| $\overline{CS}$ to SCLK set-up time                       | $t_2$         |            | 10                    |                       |     | ns      |
| Delay from $\overline{CS}$ until SDATA tri-state disabled | $t_3$         |            |                       |                       | 20  | ns      |
| Data access time after SCLK falling edge                  | $t_4$         |            |                       |                       | 40  | ns      |
| SCLK low pulse width                                      | $t_5$         |            | $0.4 \times t_{SCLK}$ |                       |     | ns      |
| SCLK high pulse width                                     | $t_6$         |            | $0.4 \times t_{SCLK}$ |                       |     | ns      |
| SCLK to data valid hold time                              | $t_7$         |            | 5                     |                       |     | ns      |
| SCLK falling edge to SDATA high impedance                 | $t_8$         |            | 5                     |                       |     | ns      |
| Wake-up time from sleep mode                              | $t_{WAKEUP}$  |            |                       | 50                    |     | $\mu s$ |
| Power-up wait time                                        | $t_{PUWAIT}$  |            | 200                   |                       |     | $\mu s$ |
| Wait time before normal operation after power-up          | $t_{CLKWAIT}$ |            |                       | $200 \times t_{SCLK}$ |     | ns      |

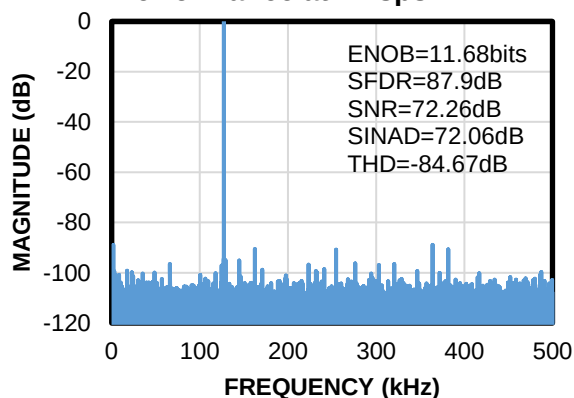
### Notes:

- 8) For  $t_{SCLK}$ ,  $t_{ON}$ ,  $t_{QUIET}$ , and  $t_1$ – $t_8$ , see Figure 2 on page 13.
- 9) For  $t_{PUWAIT}$  and  $t_{CLKWAIT}$ , see Figure 12 on page 17.
- 10) Timing characteristics are guaranteed by engineering characterization.

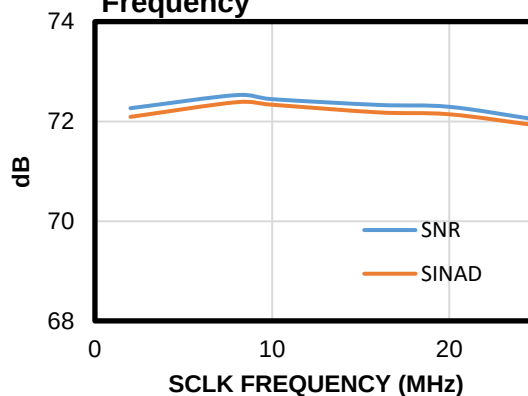
# TYPICAL CHARACTERISTICS

$V_{DD} = 3.3V$ ,  $V_{CS}$ ,  $V_{SCLK} = 0V$  to  $3.3V$  <sup>(4)</sup>,  $f_{SCLK} = 20MHz$ ,  $f_{SAMPLE} = 1Mps$ ,  $f_{IN} = 120kHz$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted.

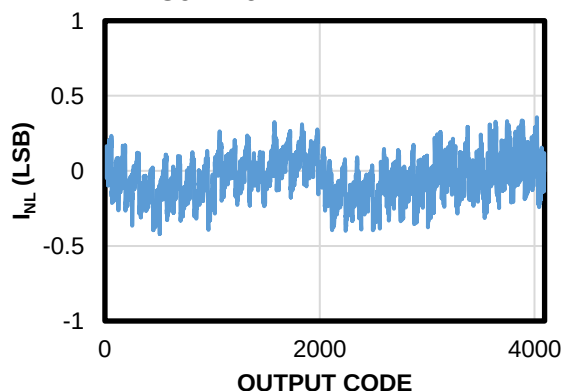
**MDC97476 Dynamic Performance at 1Mps**



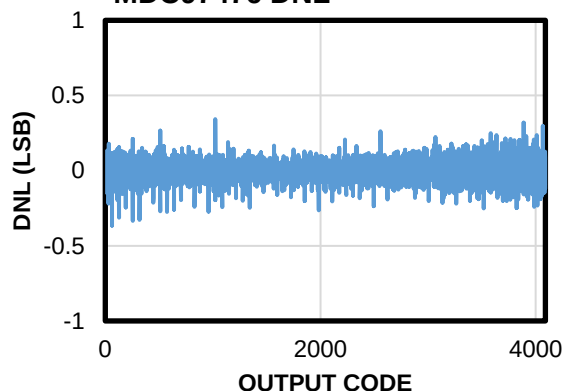
**MDC97476 Dynamic Performance vs. SCLK Frequency**



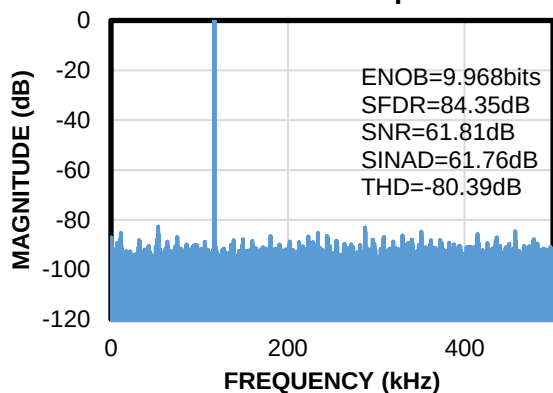
**MDC97476 INL**



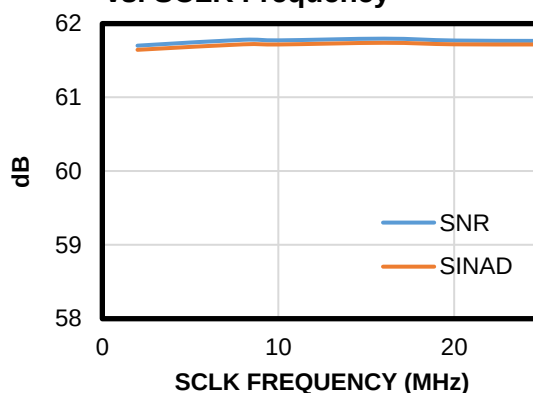
**MDC97476 DNL**



**MDC97477 Dynamic Performance at 1Mps**

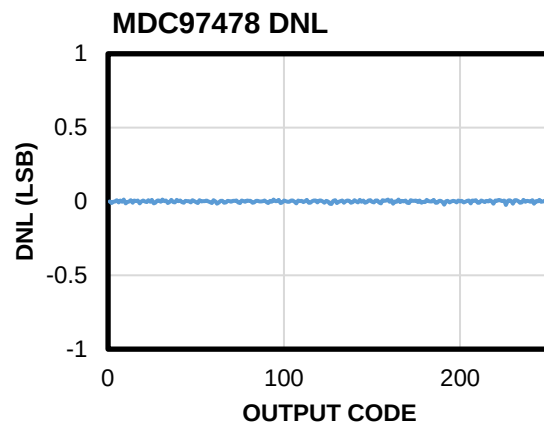
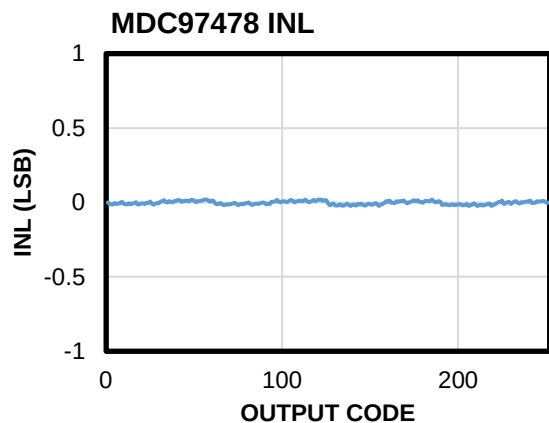
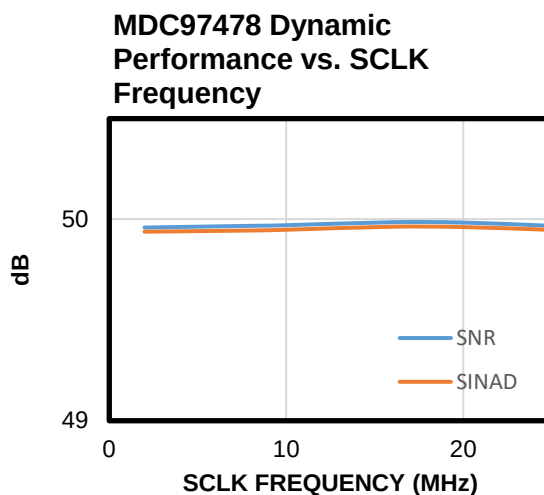
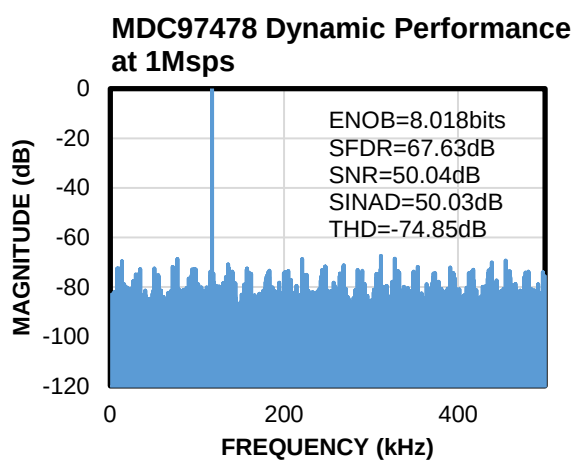
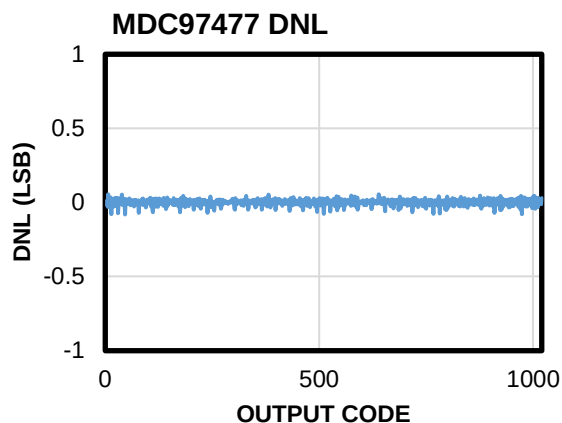
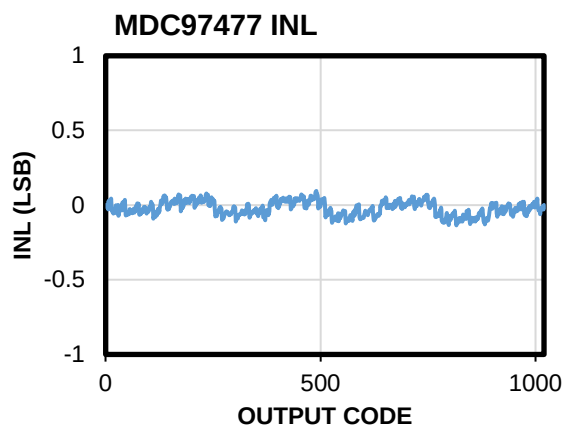


**MDC97477 Dynamic Performance vs. SCLK Frequency**



# TYPICAL CHARACTERISTICS (continued)

$V_{DD} = 3.3V$ ,  $V_{CS}$ ,  $V_{SCLK} = 0V$  to  $3.3V^{(4)}$ ,  $f_{SCLK} = 20MHz$ ,  $f_{SAMPLE} = 1Mps$ ,  $f_{IN} = 120kHz$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted.



## FUNCTIONAL BLOCK DIAGRAM

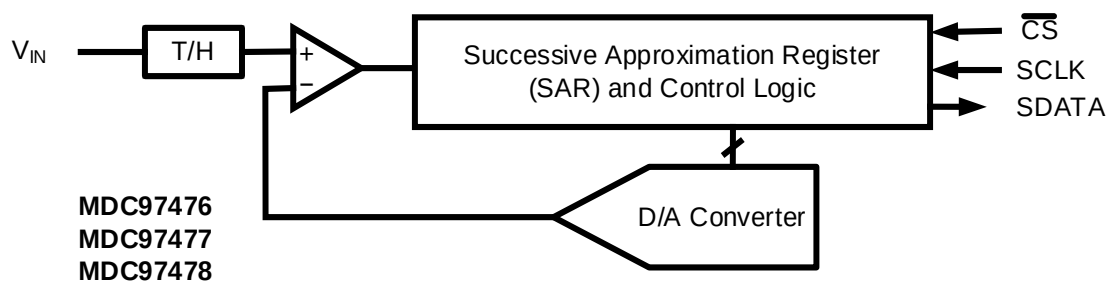


Figure 1: Functional Block Diagram

## OPERATION

The MDC97476, MDC97477, and MDC97478 are 12-bit, 10-bit, and 8-bit (respectively), fast, micropower, single-supply, successive-approximation analog-to-digital converters (SAR ADCs). These devices operate from a single 3.3V supply and are capable of throughput rates of 1MSPS with a 20MHz input clock.

Each device provides an on-chip, track-and-hold ADC and a serial interface in a tiny TSOT-23-6 package. The serial clock input accesses data from the device and provides the clock source for the SAR. The analog input range between 0V and the VDD pin's voltage ( $V_{DD}$ ). There is no on-chip reference, and no external reference is required for the ADC. The reference for the MDC97476/7/8 is derived from the power supply, which provides the widest dynamic input range.

Figure 1 on page 12 shows that there are four input/output (I/O) pins. VIN is the analog input signal pin.  $\overline{CS}$  is chip select, which is used to start the conversion process. SCLK is the input clock, which controls the serial data interface's timing. SDATA is the serial data output pin, which outputs the conversion result.

The falling edge of  $\overline{CS}$  initiates the end of the signal tracking phase and the start of the conversion process. Meanwhile, the SDATA pin transitions from tri-state to logic low.

At the thirteenth rising edge of SCLK after  $\overline{CS}$  goes low, the ADC transitions from the hold phase to the track phase. The SDATA pin goes

into tri-state mode either at the 16th falling edge of SCLK after  $\overline{CS}$  goes low, or at the rising edge of  $\overline{CS}$ . After SDATA outputs all data and goes back to tri-state, the ADC must wait for the minimum quiet time ( $t_{QUIET}$ ) before starting a new conversion. This means that the next falling edge of  $\overline{CS}$  cannot happen until  $t_{QUIET}$  has elapsed (see Figure 2).

To read a complete sample from the MDC97476/7/8,  $\overline{CS}$  must remain low for at least 16 SCLK cycles. SDATA is clocked out on the falling edges of SCLK. SDATA outputs four leading zeroes first, followed by 12 (MDC97476), 10 (MDC97477), or 8 (MDC97478) data bits. The order begins with the most significant bit (MSB) first. After the data bits:

- The MDC97476's SDATA pin goes into tri-state mode.
- The MDC97477's SDATA pin clocks out two trailing zeros and then goes into tri-state mode.
- The MDC97478's SDATA pin clocks out four trailing zeros and then goes into tri-state mode.

The  $\overline{CS}$  pin's falling edge should only occur when SCLK is high. Figure 2 shows the detailed timing diagram for the MDC97476. Figure 3 on page 14 shows the detailed timing diagram for the MDC97477. Figure 4 on page 14 shows the detailed timing diagram for the MDC97478.

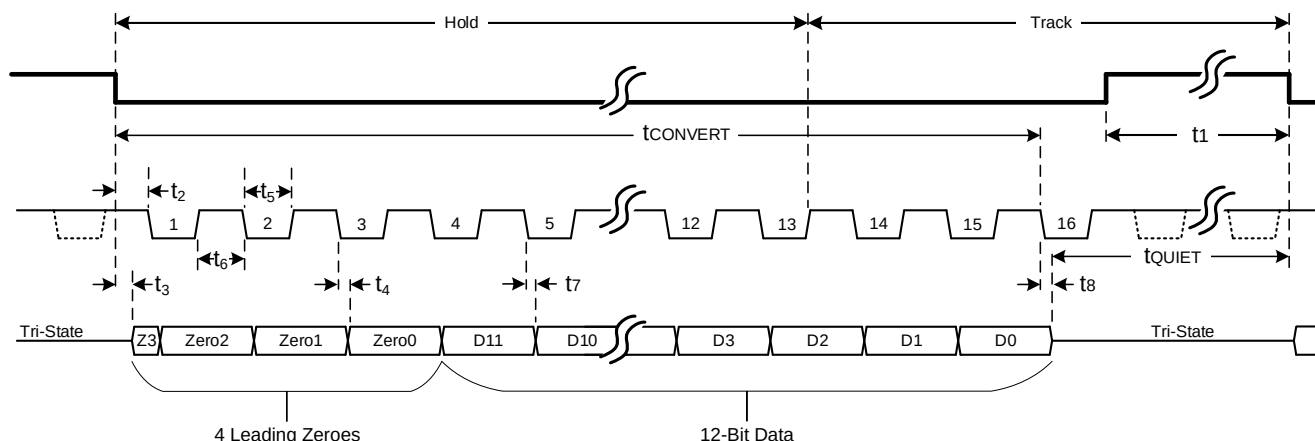


Figure 2: MDC97476 Serial Interface Timing Diagram

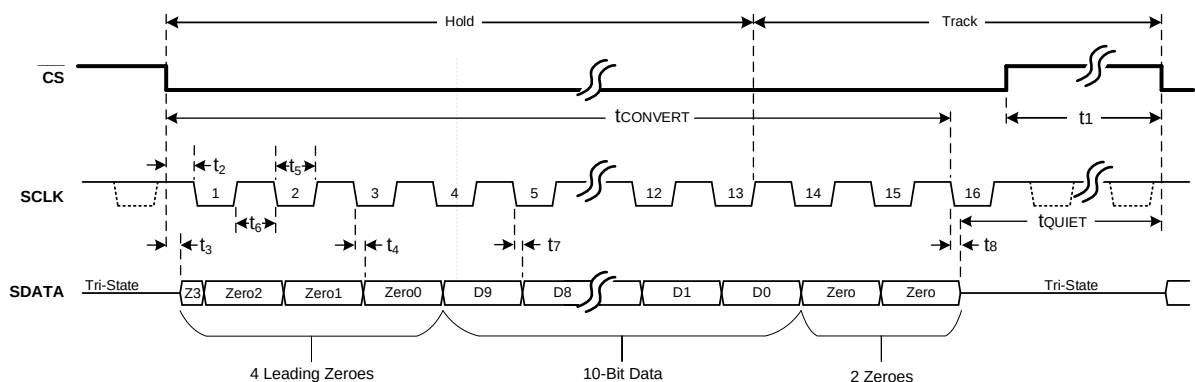


Figure 3: MDC97477 Serial Interface Timing Diagram

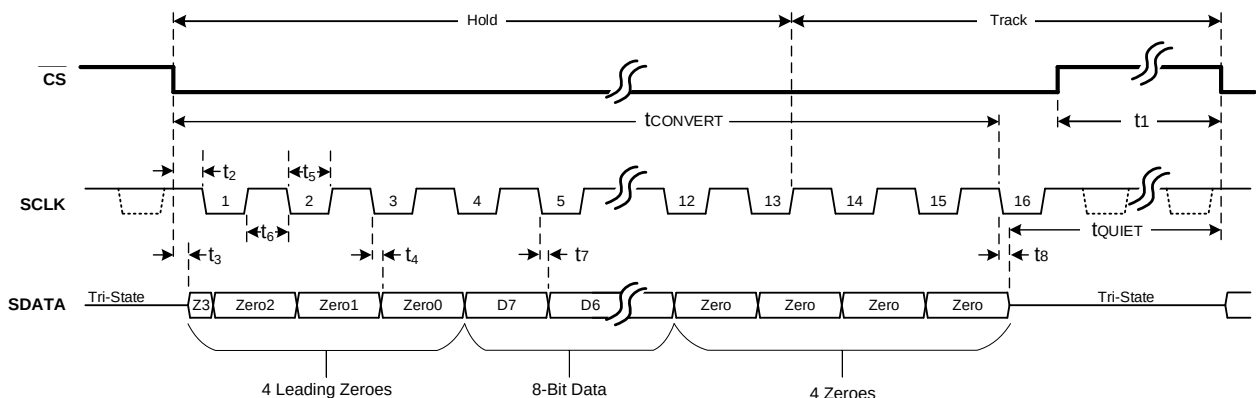


Figure 4: MDC97478 Serial Interface Timing Diagram

### Device Functional Stages

The MDC97476/7/8 is a fast, micropower, single-supply, SAR ADC with charge redistribution digital-to-analog converters (DACs).

Figure 5 shows a simplified schematic of the device in the hold phase. In this phase, SW2 is

open, and the sampling capacitor is connected to ground via SW1, maintaining the sampled voltage at the comparator's input. The control logic then controls the capacitive DAC to add or subtract charge from the sampling capacitor until the comparator is balanced.

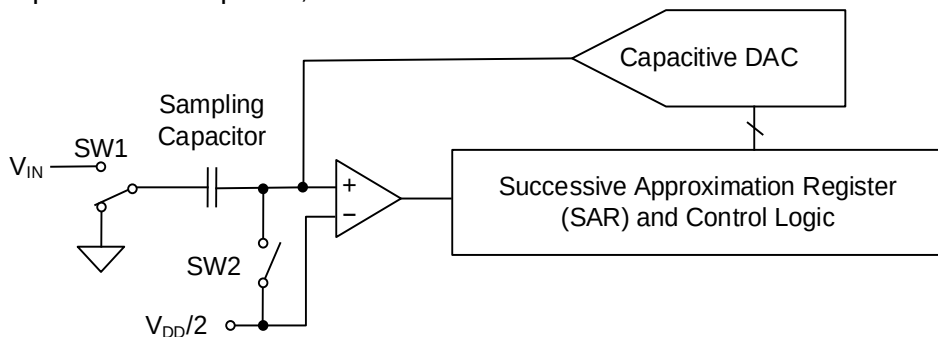


Figure 5: Hold Phase

After the comparator is balanced, the control code applied to the DAC is the digital value of the analog input voltage. The device can then move into track phase (see Figure 6 on page 15). In

track phase, SW2 is closed, the comparator is balanced, and SW1 connects the sampling capacitor to VIN, which stores the input voltage on the sampling capacitor.



The MDC97476/7/8's output coding is straight binary. Code transitions occur at integer least significant bit (LSB) values, such as 1 LSB, 2 LSB, and so on.

- The LSB size for the MDC97476 is  $V_{DD} / 4096$ .

- The LSB size for the MDC97477 is  $V_{DD} / 1024$ .
- The LSB size for the MDC97478 is  $V_{DD} / 256$ .

Figure 7 shows an ideal transfer characteristic.



The MDC97476/7/8 transfer function slightly varies from the ideal in a predictable fashion. After the conversion completes, the conversion result is sent out as `Adc_Code`. The relationship between `Adc_Code` and the ADC input voltage ( $V_{IN}$ ) can be calculated with Equation (1) for the

MDC97476, Equation (2) for the MDC97477, and Equation (3) for the MDC97478:

$$V_{IN} = \frac{V_{DD}}{4096} \times (\text{Adc\_Code} + 38 - 89 \times \frac{\text{Adc\_Code} - 1}{4094}) \quad (1)$$

$$V_{IN} = \frac{V_{DD}}{1024} \times (\text{Adc\_Code} + 8.7 - 21.5 \times \frac{\text{Adc\_Code} - 1}{1022}) \quad (2)$$

$$V_{IN} = \frac{V_{DD}}{256} \times (\text{Adc\_Code} + 2.13 - 5.35 \times \frac{\text{Adc\_Code} - 1}{254}) \quad (3)$$

## Analog Input

Figure 8 shows an equivalent circuit for the MDC97476/7/8 input pin (VIN). The analog input voltage must always be kept between (GND - 300mV) and (VDD + 300mV). Two diodes (DES1 and DES2) provide ESD protection for the analog input. The capacitor (CPIN) in Figure 8 represents the input pin capacitance, with a typical value of 2pF. The resistor (RON) represents the lumped

pm resistance of the track and hold switch, and it has a typical value of 125Ω. The capacitor (CSAMPLING) represents the ADC sampling capacitor, and it has a typical value of 14pF.

In applications where harmonic distortion and signal-to-noise ratio are critical, the MDC97476/7/8 should be driven by a low-impedance source. A band-pass or low-pass filter is helpful to reduce harmonics and noise, improving THD and SNR performance.

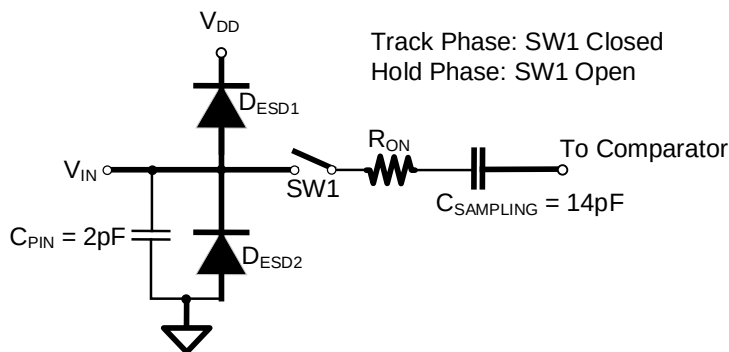


Figure 8: Equivalent Analog Input Circuit

## Digital Inputs

ESD protection circuits are also used for the digital inputs and the output, which means that the digital inputs and output share the same voltage limitations as the analog input.

## Modes of Operation

By controlling CS during conversion, the MDC97476/7/8 can go into two possible modes: normal mode and sleep mode. The device enters normal mode when the CS signal goes low, or it enters sleep mode when CS pulled high before the tenth falling edge of SCLK after CS is pulled low.

Choosing different modes can optimize the power dissipation/throughput rate ratio for different application requirements.

## Normal Mode

To keep the device in normal mode continuously, CS must be kept low until after the tenth falling edge of SCLK after the start of a conversion. Note that a conversion is initiated by bringing CS low.

The MDC97476/7/8 can obtain the highest throughput performance by staying in normal mode, as there is no wake-up delay.

If CS is pulled high after the tenth falling edge and before the sixteenth falling edge, the device stays in normal mode, but the current conversion is aborted, and SDATA goes into tri-state.

If CS remains low for more than 16 SCLK clock cycles, SDATA returns to tri-state at the sixteenth SCLK falling edge (see Figure 9).

A new conversion can be initiated after tQUIET has elapsed by bringing CS low again.

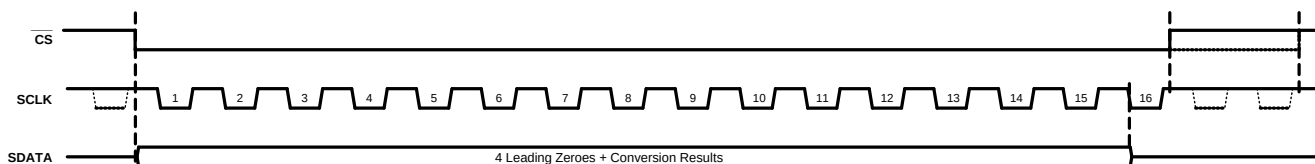


Figure 9: Normal Mode Operation



## Sleep Mode

Sleep mode is intended to reduce power consumption in applications that either sample discontinuously, or with a slow throughput rate. When the MDC97476/7/8 is in sleep mode, most of the analog circuitry is turned off.

Figure 10 shows how the device enters sleep mode. When  $\overline{CS}$  is pulled high after the second falling edge and before the tenth falling edge, the conversion is interrupted, and device enters sleep mode. The current conversion is aborted, and SDATA enters tri-state. If  $\overline{CS}$  is pulled high before the second falling edge of SCLK, the device stays in normal mode; this prevents noise on the  $\overline{CS}$  line from accidentally changing the mode.

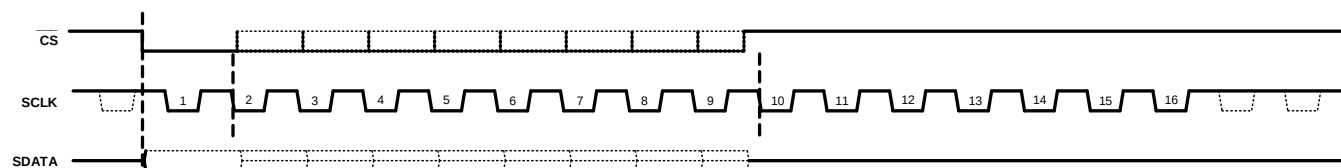


Figure 10: Entering Sleep Mode

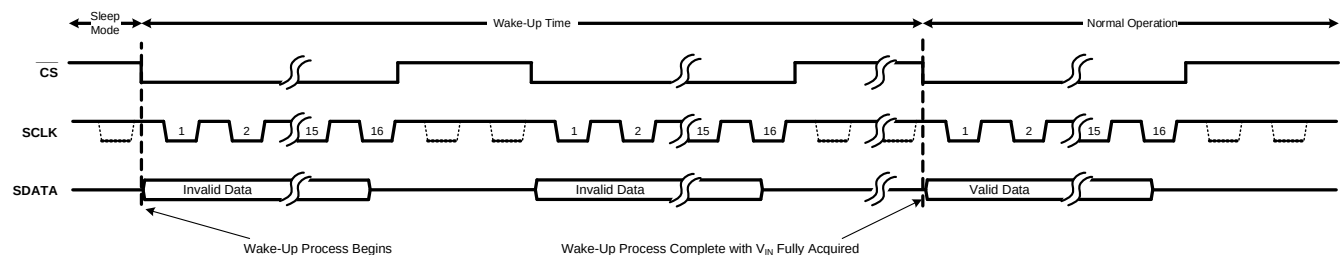


Figure 11: Entering Normal Mode

## Power-Up Sequence

For the power-up sequence, the first step is for  $V_{DD}$  to ramp up and stabilize. Next, wait at least 200 $\mu$ s ( $t_{PUWAIT}$ ). Lastly, wait at least 200 cycles ( $t_{CLKWAIT}$ ) of stable SCLK to allow the MDC97476/7/8 to fully power up.  $t_{CLKWAIT}$  is equivalent to 10 dummy samples operating  $\overline{CS}$

and SCLK in normal operation. During  $t_{CLKWAIT}$ ,  $\overline{CS}$  can be either high or low. It is recommended to keep  $\overline{CS}$  high or operate  $\overline{CS}$  in the same manner as in normal operation.

Figure 12 shows the detailed power-up timing sequence.

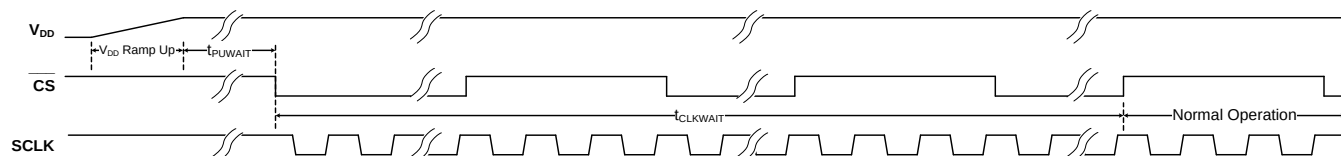


Figure 12: Power-Up Sequence

## APPLICATION INFORMATION

### Layout Guidelines

The reference voltage is critical for optimal ADC performance. A noisy reference voltage affects SNR and SINAD performance. Since the MDC97476/7/8 uses  $V_{DD}$  as its reference voltage,  $V_{DD}$  must be treated carefully.

A uniform ground plane and a dedicated  $V_{DD}$  plane are recommended for the MDC97476/7/8.

The decoupling capacitors should have a low ESR/ESL. For the best performance, place the capacitors next to the VDD and GND pins, and on the same side of the PCB as the chip.

## TYPICAL APPLICATION CIRCUIT

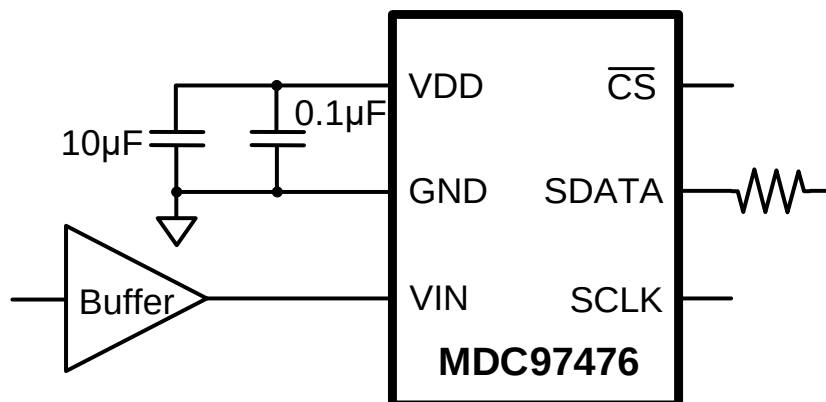
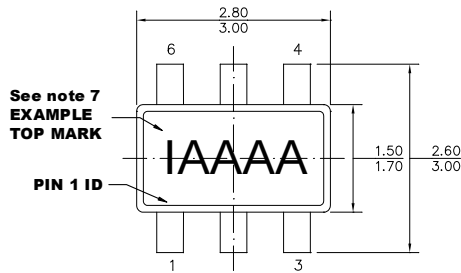


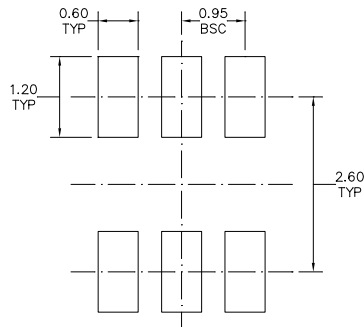
Figure 13: Typical Application Circuit

## PACKAGE INFORMATION

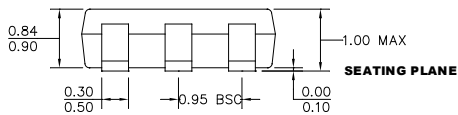
### TSOT-23-6



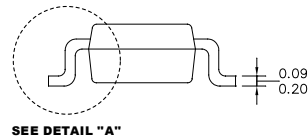
**TOP VIEW**



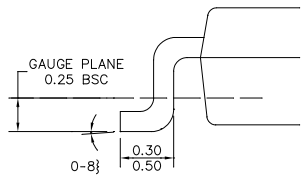
**RECOMMENDED LAND PATTERN**



**FRONT VIEW**



**SIDE VIEW**

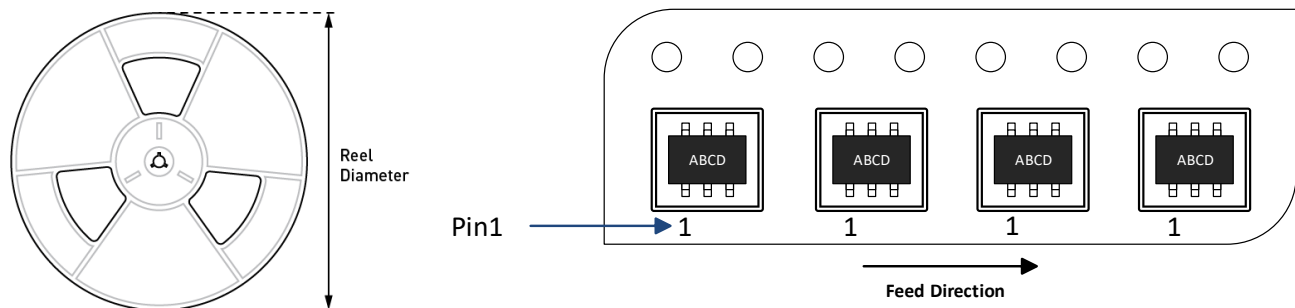


**DETAIL "A"**

#### NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
- 5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AB.
- 6) DRAWING IS NOT TO SCALE.
- 7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

## CARRIER INFORMATION



| Part Number  | Package Description | Quantity/ Reel | Quantity/ Tube | Quantity/ Tray | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch |
|--------------|---------------------|----------------|----------------|----------------|---------------|--------------------|--------------------|
| MDC97476GJ-Z | TSOT-23-6           | 3000           | N/A            | N/A            | 7in           | 8mm                | 4mm                |
| MDC97477GJ-Z |                     |                |                |                |               |                    |                    |
| MDC97478GJ-Z |                     |                |                |                |               |                    |                    |

## REVISION HISTORY

| Revision # | Revision Date | Description     | Pages Updated |
|------------|---------------|-----------------|---------------|
| 1.0        | 2/3/2026      | Initial Release | -             |

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