MagAlpha MA736

8-Bit to 12.5-Bit, 3µs Low-Latency, Ultra-Small, Contactless Digital Angle Sensor

DESCRIPTION

The MA736 is a MagAlpha digital angle sensor that detects the absolute angular position of a permanent magnet, typically a diametrically magnetized cylinder on a rotating shaft. Its ultra-small UTQFN package makes it an ideal solution for space-constrained applications. Fast data acquisition and processing provide accurate angle measurements from static angle measurement to high-speed rotation. The digital filtering is adjustable to optimize control loop performance when used in servo motor applications.

This sensor supports a wide range of magnetic field strengths and spatial configurations. Both end-of-shaft and side-shaft (off-axis mounting) configurations are supported.

The MA736 detects the strength of the magnetic field, and includes configurable thresholds that can be used for diagnostic purposes. An on-chip, non-volatile memory (NVM) provides storage for configuration parameters, such as the reference zero-angle and magnetic field detection thresholds. It is also possible to configure the MA736 with volatile registers without accessing the NVM.

The MA736 is available in a UTQFN-14 (2mmx2mm) package.

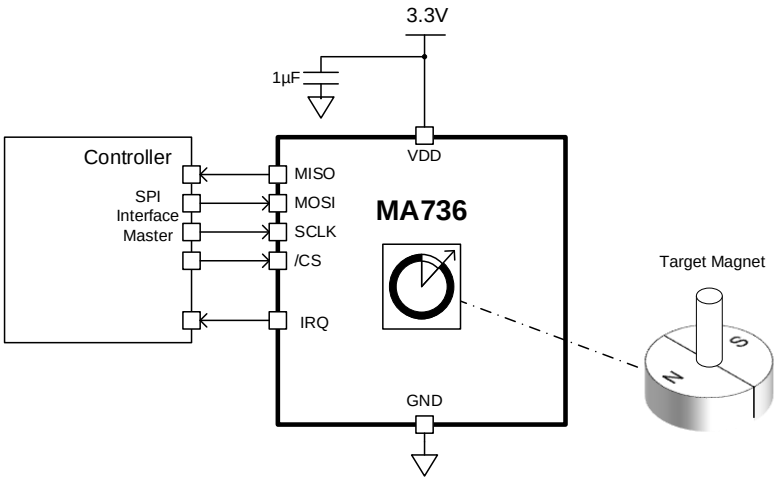
FEATURES

- Configurable 8-Bit to 12.5-Bit ±3σ Resolution Absolute Angle Encoder
- 3µs of Latency at Constant Rotation Speed
- SPI Serial Interface for Digital Angle Readout and Chip Configuration
- Configurable Magnetic Field Strength Detection for Diagnostic Checks
- Non-Volatile Memory (NVM) Read/Write Command Extends Memory Life
- 3.3V, 11mA Supply Current
- -40°C to +125°C Operating Temperature
- 0rmp to 60,000rpm Rotation
- Interrupt Out when Angle Change Is Detected
- Available in an Ultra-Small UTQFN-14 (2mmx2mm) Package

APPLICATIONS

- General-Purpose Angle Measurement
- High-Resolution Angle Encoders
- Automotive Position Sensing
- Robotics

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MA736GGU	UTQFN-14 (2mmx2mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MA736GGU-Z).

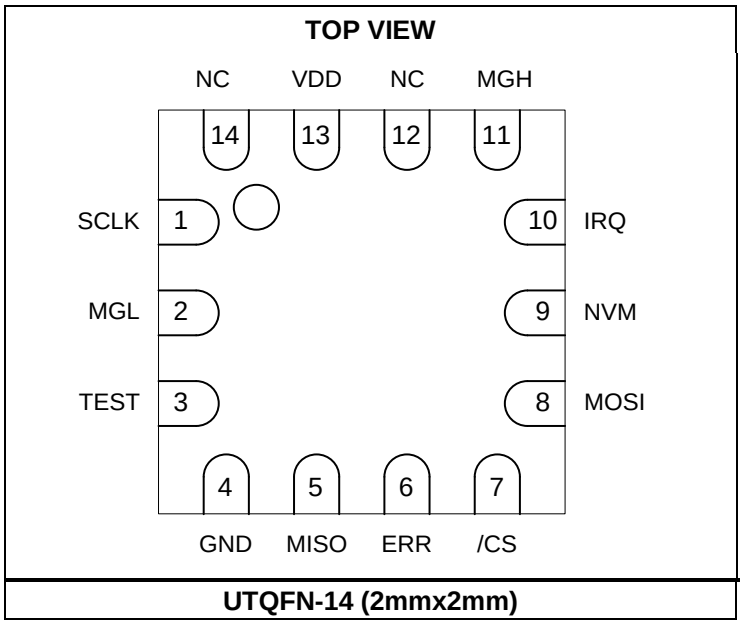
TOP MARKING

MVY

LLLL

MV: Product code of MA736GGU
Y: Year code
LLLL: Lot number

PACKAGE REFERENCE



UTQFN-14 (2mmx2mm)

PIN FUNCTIONS

Pin #	Name	Description
1	SCLK	**Clock (SPI).** The SCLK pin is an internal pull-down resistor input. (1)
2	MGL	**Digital output.** The MGL pin is a digital output that indicates the field strength below the MGLT level.
3	TEST	**Factory use only.** Connect the TEST pin to ground.
4	GND	**Supply ground.**
5	MISO	**Data output (SPI).** The MISO pin is an output, and is pulled down when the /CS pin is logic 1 (i.e. SPI is inactive). (2)
6	ERR	**Error flag.** The ERR pin is an active high output.
7	/CS	**Chip select (SPI).** The /CS pin is an internal, active-low, pull-up resistor input. (1)
8	MOSI	**Data input (SPI).** The MOSI pin is an internal pull-down resistor input. (1)
9	NVM	**Non-volatile memory (NVM).** The NVM pin is an output that indicates whether the chip is busy accessing the NVM.
10	IRQ	**Interrupt on angle change.** The IRQ pin is an output that indicates whether the angle change has exceeded the defined threshold.
11	MGH	**Digital output.** This MGH pin is a digital output that indicates the field strength above the MGHT level.
12	NC	**Not connected.** The NC pin is not connected internally.
13	VDD	**3.3V supply.** Bypass the VDD pin to ground using a 1µF capacitor.
14	NC	**Not connected.** The NC pin is not connected internally.

Notes:

1) Can be configured to a high-impedance (Hi-Z) state via the SPI-PULL register.
2) Can be configured to a Hi-Z state via the TRI-STATE register.

ABSOLUTE MAXIMUM RATINGS (3)

Supply voltage (V_{DD}) .....-0.5V to +4.6V
Input pin voltage (V_{IN}) .....-0.5V to +6V
Output pin voltage (V_{OUT}) .....-0.5V to +4.6V
Continuous power dissipation (T_A = 25°C) (4) 2W
Junction temperature .....160°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±2kV
Charged device model (CDM) ..... ±750V

Thermal Resistance (5)	***θJA***	***θJC***
UTQFN-14 (2mmx2mm)	90	20 °C/W

Notes:

3) Exceeding these ratings may damage the device.
4) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{DD} = 3.3V, 45mT < B < 100mT, T_A = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Recommended Operating Conditions						
Supply voltage	V_{DD}		3	3.3	3.6	V
Supply current	I_{DD}	T_A = -40°C to +125°C		11	12.5	mA
Operating temperature	T_A		-40		+125	°C
Applied magnetic field (6)	B		30	60		mT
Absolute Output – Serial						
Resolution (±3σ) (6)		Filter window, τ = 4μs, at 25°C	7.2		8	bits
		Filter window, τ = 1ms, at 25°C	10.2		11.5	bits
		Filter window, τ = 4ms, at 25°C	11.6		12.5	bits
Noise RMS (6)		Filter window, τ = 4μs, at 25°C	0.2		0.4	deg
		Filter window, τ = 1ms, at 25°C	0.02		0.05	deg
		Filter window, τ = 4ms, at 25°C	0.01		0.02	deg
Resolution drift in temperature				-0.003		bits/°C
Refresh rate (6)			850	980	1100	kHz
Data output length			16		16	bits
Response Time						
Start-up time (6)		Filter window, τ = 4μs			0.6	ms
		Filter window, τ = 1ms			16	ms
		Filter window, τ = 4ms			65	ms
Latency		Constant speed propagation delay		3		μs
Filter cutoff frequency	f_{CUTOFF}	Filter window, τ = 4μs		95		kHz
		Filter window, τ = 1ms		380		Hz
		Filter window, τ = 4ms		95		Hz
Accuracy						
INL accuracy		T_A = 25°C, at room temperature across the entire field range		0.7		deg
		T_A = -40°C to +125°C, across the entire temperature range and the entire field range		1.1		deg
Output Drift						
Temperature-induced drift		At room temperature		0.01		deg/°C
Temperature-induced variation		T_A = 25°C to 85°C		0.5		deg
		T_A = 25°C to 125°C		0.7		deg
Magnetic field induced				0.01		deg/mT
Voltage supply induced				0.35		deg/V

GENERAL CHARACTERISTICS

V_{DD} = 3.3V, 45mT < B < 100mT, T_A = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Magnetic Field Detection Thresholds						
Accuracy				5		mT
Hysteresis	MagHys			6		mT
Temperature drift				-600		ppm/°C
Digital I/O						
Input high voltage	V_{IN_HIGH}		2.5	3.3	5.5	V
Input low voltage	V_{IN_LOW}		-0.3	0	+0.8	V
Output low voltage (6)	V_{OUT_LOW}	I_{OUT_LOW} = 4mA		0	0.4	V
Output high voltage (6)	V_{OUT_HIGH}	I_{OUT_HIGH} = 4mA	2.4	3.3		V
Pull-up resistance	R_{PU}	V_{IN} = 0V	46	66	97	kΩ
Pull-down resistance	R_{PD}	V_{IN} = 3.3V	25	35	97	kΩ
Rising edge slew rate	t_{RISING}	C_{LOAD} = 50pF		0.7		V/ns
Falling edge slew rate	$t_{FALLING}$	C_{LOAD} = 50pF		0.7		V/ns

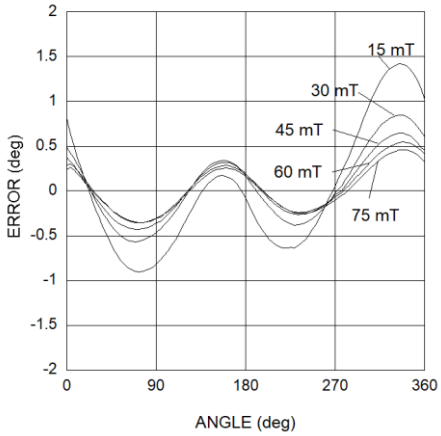
Note:

6) Guaranteed by design and characterization.

TYPICAL CHARACTERISTICS

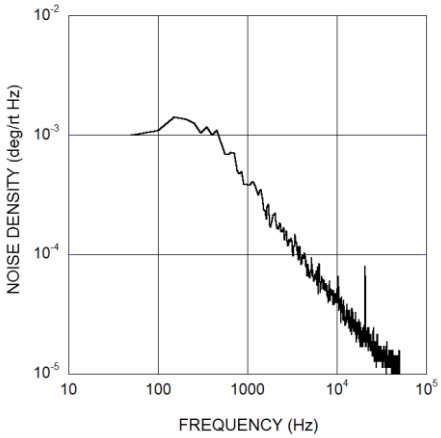
V_{DD} = 3.3V, T_A = 25°C, unless otherwise noted.

Error vs. Angle



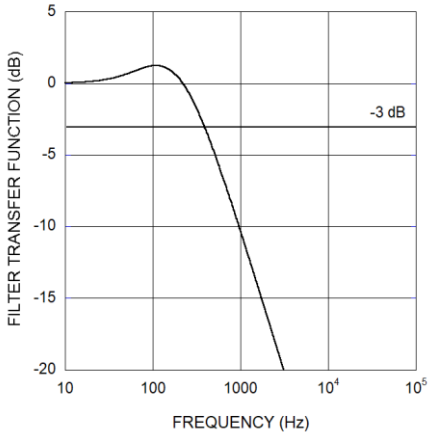
Noise Density vs. Frequency

Magnetic field = 50mT,
τ = 1024µs

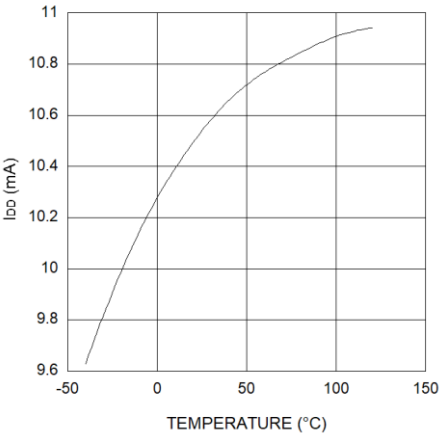


Filter Transfer Function vs. Frequency

τ = 1024µs



Supply Current vs. Temperature



FUNCTIONAL BLOCK DIAGRAM

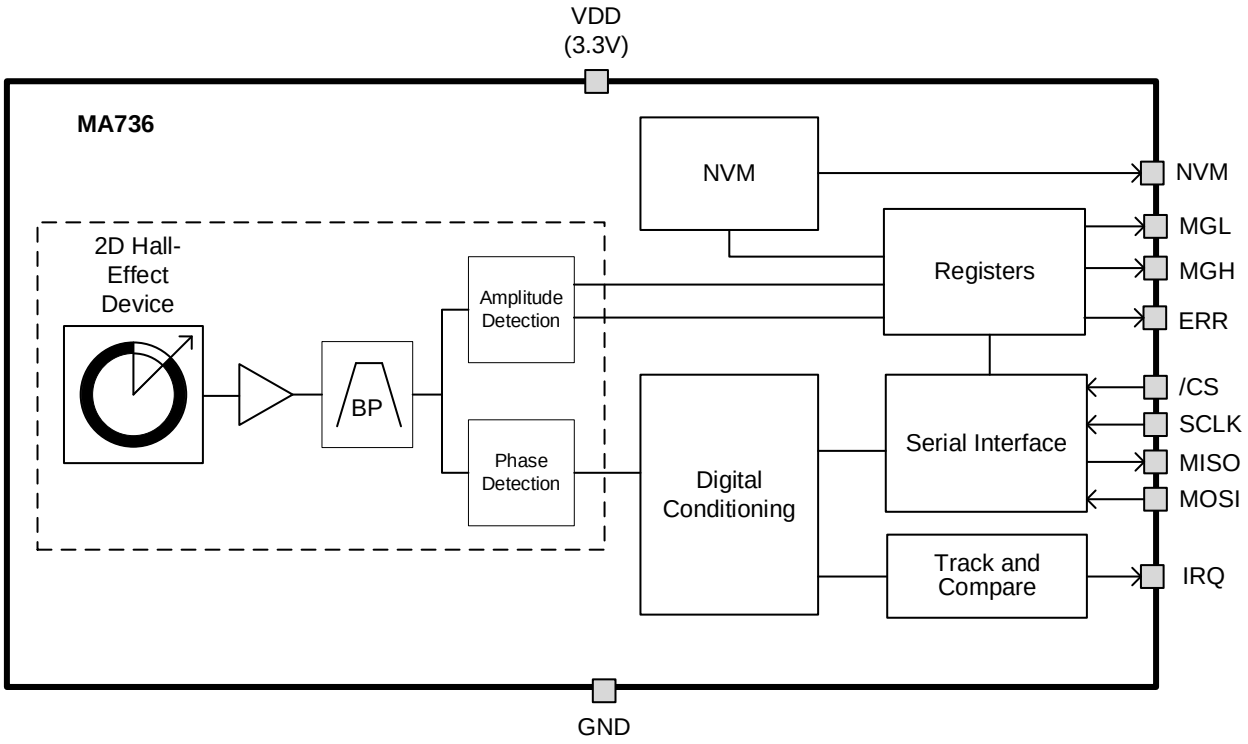


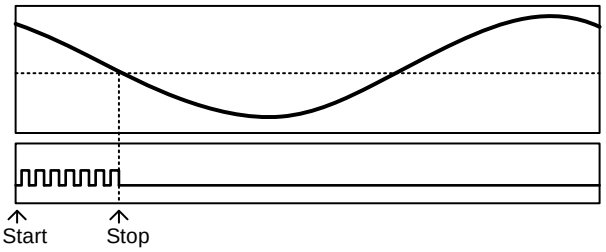
Figure 1: Functional Block Diagram

OPERATION

Sensor Front End

The magnetic field is detected with integrated Hall devices located in the center of the package. The angle is measured using MPS's proprietary SpinAxis™ method, which digitizes the direction of the field directly without complex arctangent computations or feedback loop-based circuits (interpolators).

The SpinAxis™ method is based on phase detection, and generates a sinusoidal signal with a phase that represents the angle of the magnetic field. The angle is then obtained by a time-to-digital converter, which measures the time between the zero crossing of the sinusoidal signal and the edge of a constant waveform (see Figure 2). The time-to-digital is outputted from the front end to the digital conditioning block.



Sine Waveform (Top)
Clock of Time-to-Digital Converter (Bottom)

Figure 2: Phase Detection Method

The output of the front end delivers a digital number proportional to the angle of the magnetic field at a rate of 1MHz in a straightforward, open-loop manner.

Digital Filtering

The front-end signal is further treated to achieve the final resolution. This treatment does not add any latency in steady conditions. The filter transfer function can be calculated with Equation (1):

$$H(s) = \frac{1+2\tau s}{(1+\tau s)^2} \quad (1)$$

Where τ is the filter time constant (see Table 15 on page 21).

Sensor Magnet Mounting

The MA736's sensitive area (where the Hall devices are placed) is confined within a region less than 100µm wide, and has multiple integrated Hall devices. This volume is located horizontally and vertically within 50µm of the center of the UTQFN package. The sensor detects the angle of the magnetic field projected in a plane parallel to the package's upper surface. This means that the only relevant magnetic field is the in-plane component (X and Y components) in the mid-point of the package.

By default, when looking at the top of the package, the angle increases while the magnetic field rotates clockwise. Figure 3 shows the zero angle of the non-configured sensor, where the plus sign (+) indicates the sensitive point. Both the rotation direction and the zero angle can be configured.

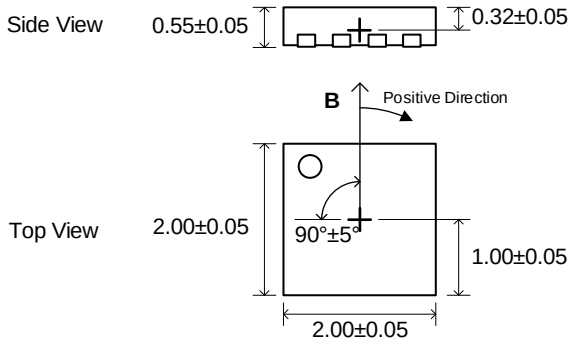


Figure 3: Detection Point and Default Positive Direction

This type of detection provides flexibility for the angular encoder design. The sensor requires only the magnetic vector to lie within the sensor plane with a field amplitude of at least 30mT. The MA736 can work with fields smaller than 30mT, but the linearity and resolution performance may deviate from the specifications.

The most straightforward mounting method is to place the MA736 sensor on the rotation axis of a permanent magnet (e.g. a diametrically magnetized cylinder) (see Figure 4).

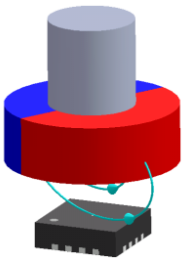


Figure 4: End-of-Shaft Mounting

The recommended magnet is a Neodymium alloy (N35) cylinder with dimensions of Ø5x3mm, inserted into an aluminum shaft with a 1.5mm air gap between the magnet and the sensor (surface of package). For good linearity, position the sensor with a precision of 10% of the magnet's radius.

If the end-of-shaft position is not available, the sensor can be positioned away from the rotation axis of a cylinder or ring magnet (see Figure 5).

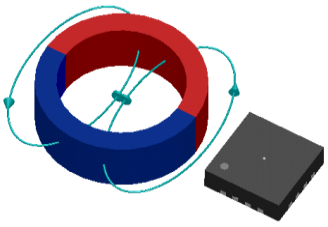


Figure 5: Side-Shaft Mounting

In this case, the magnetic field angle is not directly proportional to the mechanical angle. The MA736 can be adjusted to compensate for this effect and recover the linear relationship between the mechanical angle and the sensor output. With multiple pole pair magnets, the MA736 indicates multiple rotations for each mechanical turn.

Electrical Mounting and Power Supply Decoupling

It is recommended to place a 1µF decoupling capacitor close to the sensor with a low-impedance path to GND (see Figure 6).

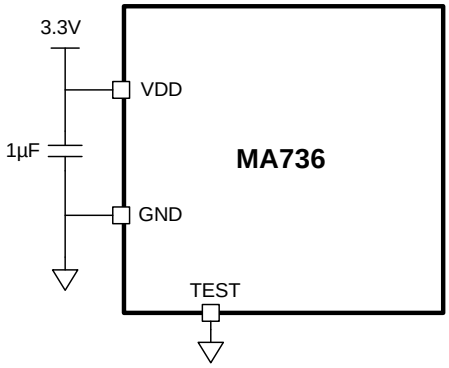


Figure 6: Supply Decoupling Connection

Serial Interface

The sensor supports the serial peripheral interface (SPI) standard for angle reading and register configuration.

SPI

The SPI is a four-wire, synchronous, serial communication interface. The MA736 supports SPI Mode 3 and Mode 0 (see Table 1 and Table 2).

Table 1: SPI Specification

	Mode 0	Mode 3
SCLK Idle State	Low	High
Data Capture	On SCLK rising edge	
Data Transmission	On SCLK falling edge	
CS Idle State	High	
Data Order	MSB first	

Table 2: SPI Standard

	Mode 0	Mode 3
CPOL	0	1
CPHA	0	1
Data Order (DORD)	0 (MSB first)	

The SPI mode (0 or 3) is detected automatically by the sensor, and does not require additional action from the user. There is no minimum clock rate. Real-world data rates depend on the PCB layout quality and signal trace length. Figure 8, and Table 3 on page 11 show the SPI timing diagram and communication.

All commands to the MA736 (whether for writing or reading register content) must be transferred through the SPI MOSI pin, and must be 16 bits long. See the SPI Communication section on page 12 for details.

SPI Signal Routing on a PCB

For a reliable data transfer via the SPI bus between the sensor (slave) and the controller (master), take extra care with the PCB design, especially the SCLK line. The steps below are recommended:

- Properly shield all SPI signals with a GND plane on both sides of each trace, as well as a GND plane underneath the SPI traces.
- Place vias along the SPI traces to connect the top and bottom GND planes.
- To reduce EMI, route the SCLK signal away from the other SPI signals and noise sources. The distance should be at least 3 times the SCLK trace width.

- Place an RC low-pass filter on SCLK, and close to the sensor. It is recommended to use a 200Ω serial resistor with a 10pF shunt capacitor to create a filter with a cutoff frequency of about 80MHz (see Figure 7).
- Use a star topology for the GND connection. Keep the GND trace short and direct as possible to avoid ground loops.
- Place RC low-pass filters on the MISO and MOSI signals. The filter on MOSI should be close to the controller; the filter on MISO should close to the sensor. It is recommended to use a 200Ω resistor with a 10pF capacitor.
- Avoid significant trace length mismatch between the SPI signals, especially between the MISO, MOSI, and SCLK signals. Design the PCB such that the trace lengths are equal for similar propagation delay.
- If possible, avoid vias on the SCLK signal.

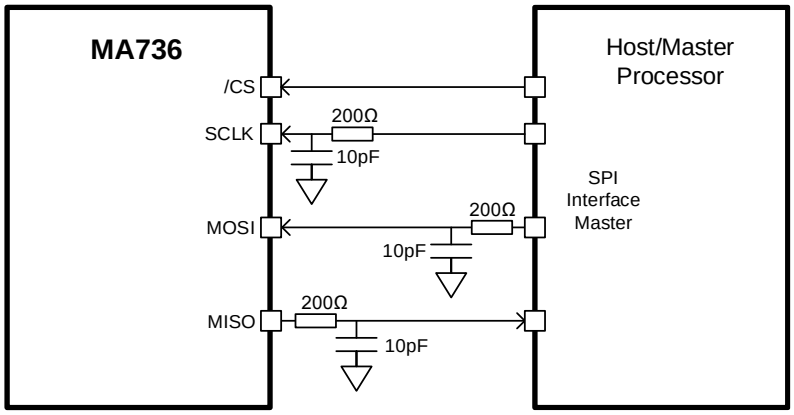


Figure 7: Example of RC Low-Pass Filter on SPI Signals

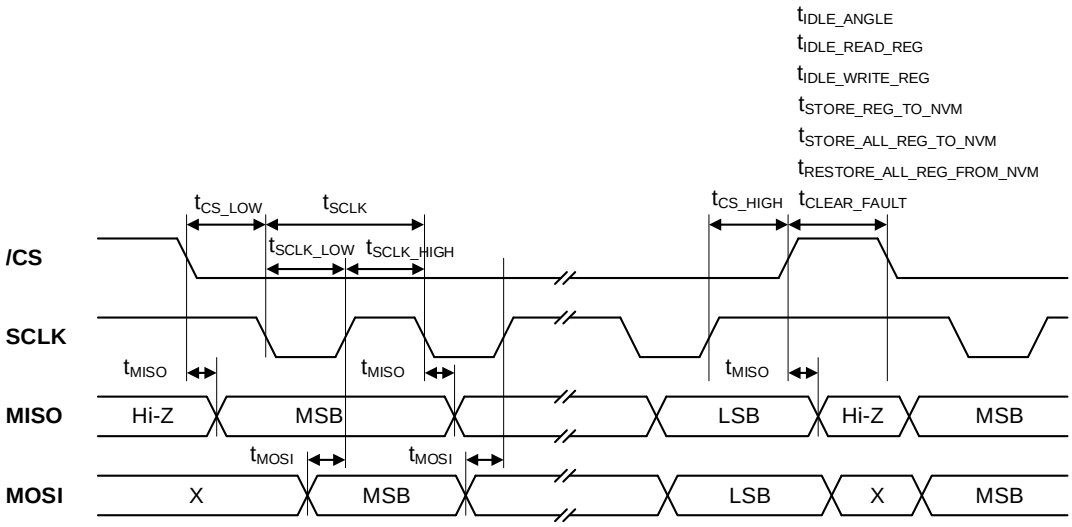


Figure 8: SPI Timing Diagram (Mode 3)

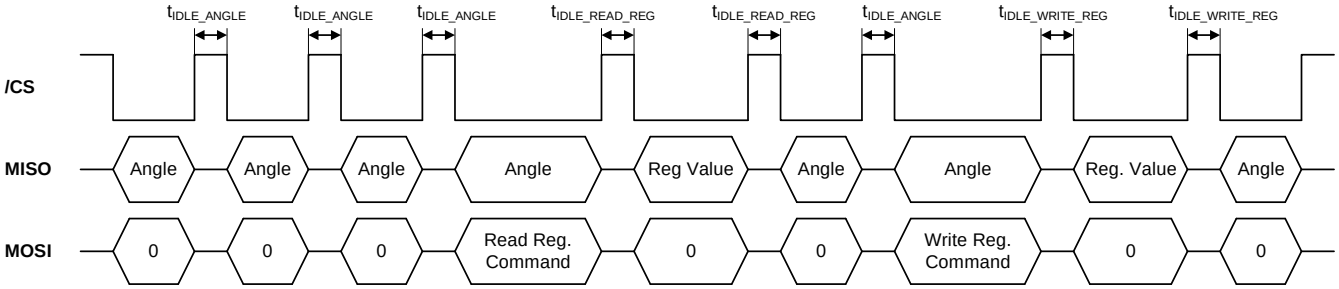


Figure 9: Minimum Idle Time

Table 3: SPI Timing

Parameter (7)	Description	Min	Max	Unit
t_{IDLE_ANGLE}	Idle time between two subsequent angle transmissions	120	-	ns
$t_{IDLE\_READ\_REG}$	Idle time before and after a register readout	120	-	ns
$t_{IDLE\_WRITE\_REG}$	Idle time before and after a register write	120	-	ns
$t_{STORE\_REG\_TO\_NVM}$	Time required to store a single register to the NVM	23	-	ms
$t_{STORE\_ALL\_REG\_TO\_NVM}$	Time required to store all registers to the NVM	704	-	ms
$t_{RESTORE\_ALL\_REG\_FROM\_NVM}$	Time required to restore all registers from the NVM	240	-	µs
t_{CLEAR_FAULT}	Time required to clear the error flags (register 26)	40	-	ns
t_{CSL}	Time between /CS falling edge and SCLK falling edge	120	-	ns
t_{SCLK}	SCLK period	40	-	ns
t_{SCLK_LOW}	Low level of the SCLK signal	20	-	ns
t_{SCLK_HIGH}	High level of the SCLK signal	20	-	ns
t_{CS_HIGH}	Time between the SCLK rising edge and the /CS rising edge	20	-	ns
t_{MISO}	SCLK falling edge to data output valid	-	15	ns
t_{MOSI}	Data input valid to the SCLK reading edge	15	-	ns

Note:

7) Guaranteed by design.

SPI Communication

The MA736 supports the following types of SPI operation:

- Read angle
- Read register
- Write register
- Store a single register value to the non-volatile memory (NVM)
- Store all register values to the NVM
- Restore all register values from the NVM
- Clear error flags

SPI Read Angle

New data is transferred into the output buffer every 1µs. The master device triggers the reading by pulling /CS low.

If a trigger event is detected, then the data remains in the output buffer until the /CS signal is de-asserted (see Table 4).

Table 4: Sensor Data Timing

Event	Action
/CS falling edge	Starts reading and freezes the output buffer
/CS rising edge	Releases the output buffer

Figure 10 shows a diagram of a full SPI angle reading.

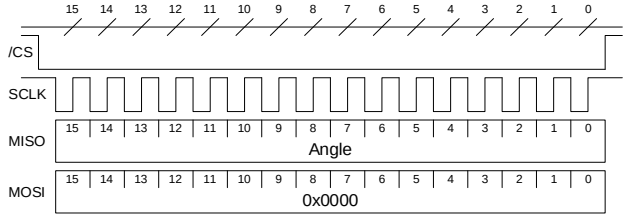


Figure 10: Full 16-Bit SPI Angle Reading

Figure 11 shows a partial SPI angle reading.

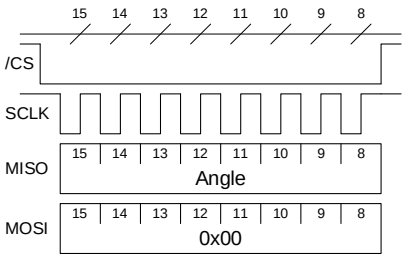


Figure 11: Partial 8-Bit SPI Angle Reading

A full angle reading requires 16 clock pulses. The sensor MISO line returns:

	MSB															LSB
MISO	*Angle[15:0]*															
MOSI	*0*															

If less resolution is desired, then the angle can be read by sending even fewer clock counts (since the MSB is first) (see Figure 11).

If the reading cycle is shorter than the refresh time, the MA736 continues sending the same data until the data refreshes. See the General Characteristics section on page 4 for details on the refresh rate.

SPI Read Register

A read register operation consists of two 16-bit frames. The first frame sends a read request, which contains the 3-bit read command (010) followed by the 5-bit register address. The last 8 bits of the frame should all be set to 0. The second frame returns the 8-bit register value (MSB byte) with an 8-bit angle value.

The first 16-bit SPI frame (read request) is:

	MSB															LSB
MISO	*Angle[15:0]*															
	Command			*Reg. Address*												
MOSI	*0*	*1*	*0*	*A_4*	*A_3*	*A_2*	*A_1*	*A_0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*

The second 16-bit SPI frame (response) is:

	Reg. Value															
MISO	*Angle[15:8]*								*V_7*	*V_6*	*V_5*	*V_4*	*V_3*	*V_2*	*V_1*	*V_0*
	MSB															*LSB*
MOSI	*0*															

For example, to determine the value of the magnetic level high flag (MGH) and low flag (MGL), read register 27 (bit[6], bit[7]) by sending the following first frame:

	MSB															LSB
MISO	*Angle[15:0]*															
	Command			*Reg. Address*												
MOSI	*0*	*1*	*0*	*1*	*1*	*0*	*1*	*1*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*

In the second frame, the MA736 replies:

	Reg. Value															
MISO	*Angle[15:8]*								*MGH*	*MGL*	*X*	*X*	*X*	*X*	*X*	*X*
	MSB															*LSB*
MOSI	*0*															

Figure 12 shows a complete transmission.

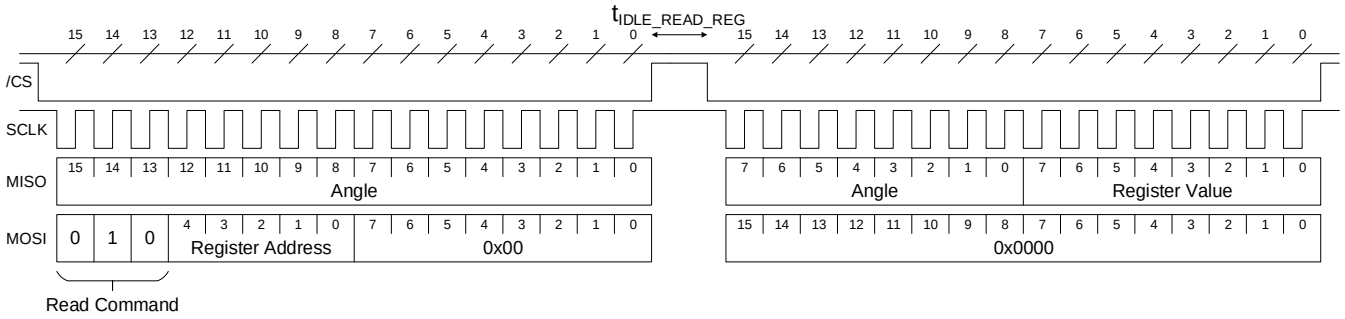


Figure 12: Read Register Operation with Two 16-Bit Frames

SPI Write Register

A write register operation consists of two 16-bit frames. The first frame sends a write request, which contains the 3-bit write command (100), followed by the 5-bit register address and the 8-bit value (MSB first). The second frame returns the newly written register value (acknowledge) with an 8-bit angle value.

The first 16-bit SPI frame (write request) is:

	MSB														LSB
MISO	Angle[15:0]														

	Command			Reg. Address					Reg. Value							
MOSI	1	0	0	A_4	A_3	A_2	A_1	A_0	V_7	V_6	V_5	V_4	V_3	V_2	V_1	V_0

The second 16-bit SPI frame (response) is:

	Reg. Value								
MISO	Angle[15:8]	V_7	V_6	V_5	V_4	V_3	V_2	V_1	V_0

	MSB														LSB
MOSI	0														

The readback register content can be used to verify the register configuration.

For example, to set the value of the output rotation direction (RD) to counterclockwise (RD = 1), write register 9 by sending the following first frame:

	MSB														LSB
MISO	Angle[15:0]														

	Command			Reg. Address					Reg. Value							
MOSI	1	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0

Then send the second frame. If the register is written correctly, the reply is:

	Reg. Value								
MISO	Angle[15:8]	1	0	0	0	0	0	0	0

	MSB														LSB
MOSI	0														

Figure 13 shows a complete transmission overview.

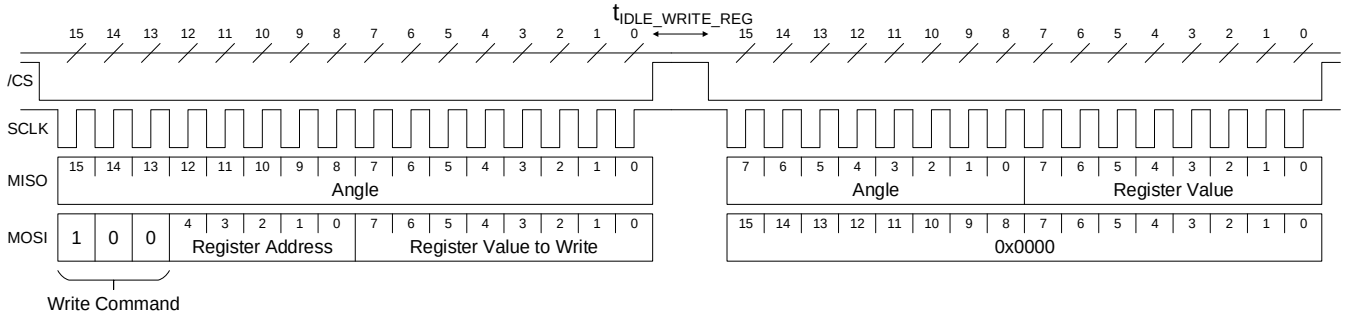


Figure 13: Write Register Operation with Two 16-Bit Frames

Non-Volatile Memory (NVM) Operation

The MA736 contains a non-volatile memory (NVM) to store the chip configuration during shutdown. The values stored in the NVM are loaded to the sensor's registers automatically during start-up. It is possible to manually restore the NVM values to the registers via the Restore All Registers from the NVM SPI command.

The registers can be copied to the NVM using either of two SPI commands:

1. Store a Single Register to the NVM
2. Store All Registers to the NVM

The desired configuration should be written to the registers via the write register commands first, and then the store commands can save one or all of the registers to the NVM.

Commands are ignored if the NVM is busy executing a previously received command.

To check whether the NVM is available and ready to receive a new command, observe the NVM pin level:

- High: NVM is busy
- Low: NVM is available and ready to receive new commands

SPI Store a Single Register to the NVM

The current value of a specific register can be stored in the NVM. Commands are ignored if the NVM is busy executing a previously received command (see Figure 14).

SPI Store All Registers to the NVM

The user can store the current value of all registers in the NVM (see Figure 15).

Commands are ignored if the NVM is busy executing a previously received command.

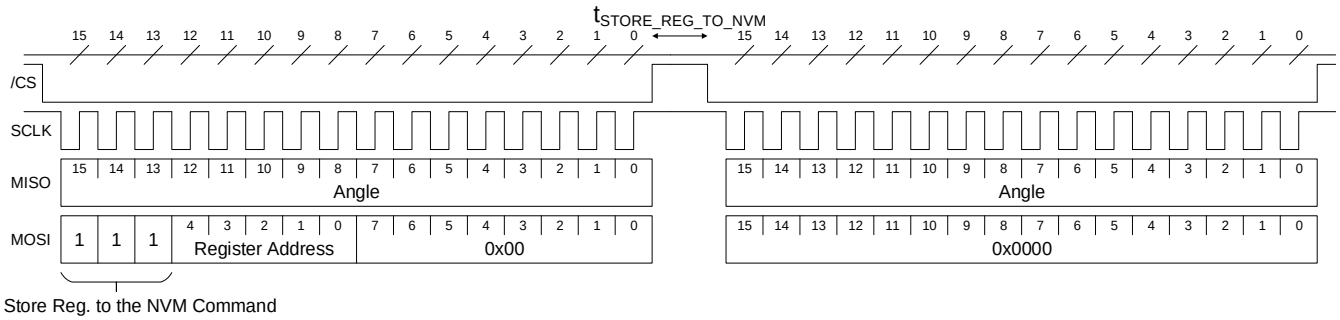


Figure 14: Store a Single Register to the NVM Operation with Two 16-Bit Frames

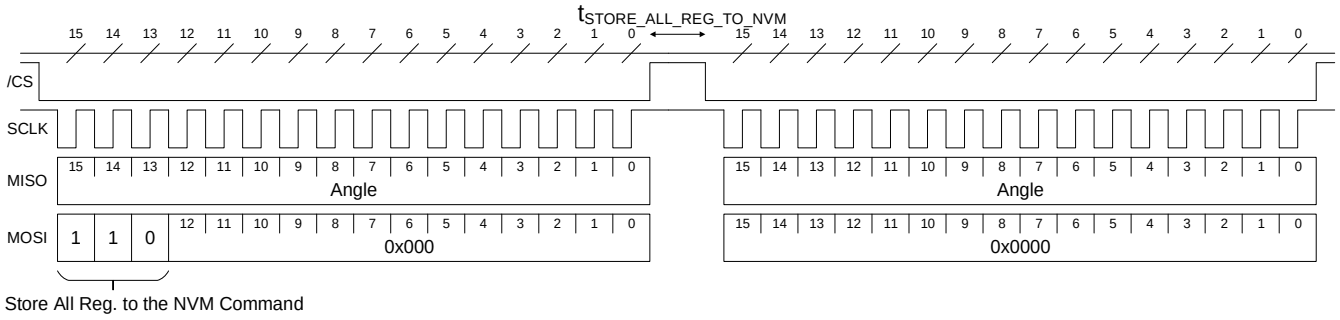


Figure 15: Store All Registers to the NVM Operation with Two 16-Bit Frames

SPI Restore All Registers from the NVM

The user can restore the value of all registers from the NVM. This operation is done automatically during start-up (see Figure 16 on page 15). Commands are ignored if the NVM is busy executing a previously received command.

SPI Clear Error Flags

The error flags on the ERR pin and in register 26 can be cleared using the SPI Clear Error Flags command (see Figure 17 on page 15).

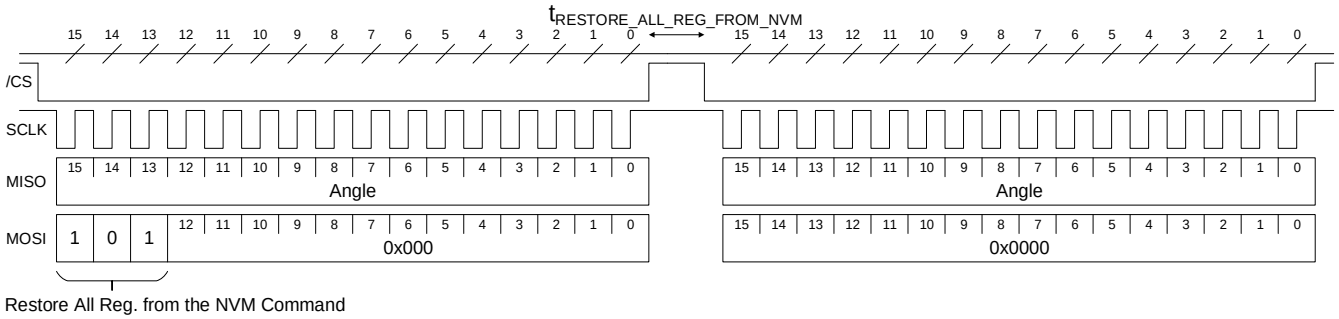


Figure 16: Restore All Registers from the NVM Operation with Two 16-Bit Frames

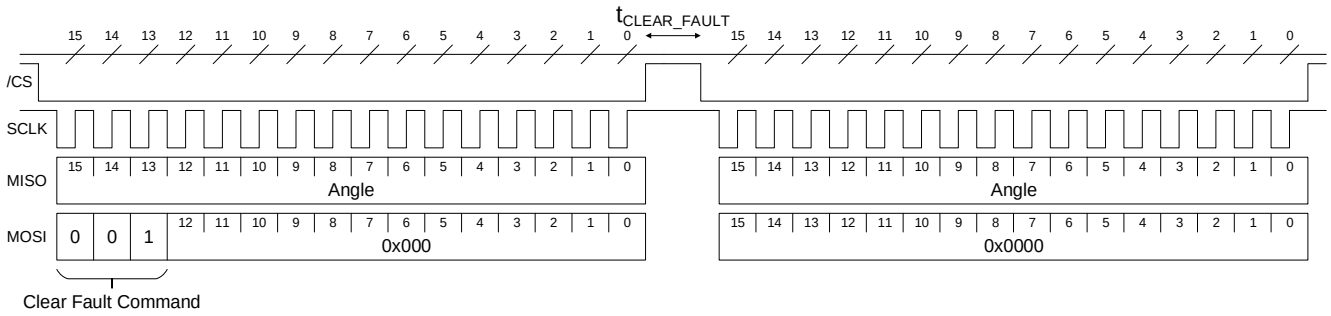


Figure 17: Clear Error Flags Operation with Two 16-Bit Frames

Table 5 shows a summary of all SPI commands.

Table 5: SPI Commands

Command Name	Command Bits[15:13]	Register Address Required?	Register Value Required?	Returned Value
Read Angle	000	No	No	16-bit angle
Read Register	010	Yes	No	8-bit angle + register value
Write Register	100	Yes	Yes	8-bit angle + register value
Store Single Register to the NVM	111	Yes	No	16-bit angle
Store All Registers to the NVM	110	No	No	16-bit angle
Restore All Registers from the NVM	101	No	No	16-bit angle
Clear Error Flags	001	No	No	16-bit angle

REGISTER MAP

Table 6: Register Map

# of Registers	Hex	Binary	Read/ Write	Bit[7] (MSB)	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0] (LSB)
0	0x0	00000	R/W	Z[7:0]							
1	0x1	00001	R/W	Z[15:8]							
2	0x2	00010	R/W	BCT[7:0]							
3	0x3	00011	R/W	-	-	-	-	-	-	ETY	ETX
6	0x6	00110	R/W	MGLT[3:0]			MGHT[3:0]			-	MG
7	0x7	00111	R/W	IRQM	RAR	HYST[5:0]					
8	0x8	01000	R/W	THR[7:0]							
9	0x9	01001	R/W	RD	-	-	-	-	-	-	-
10	0xA	01010	R/W	REF[7:0]							
13	0xD	01101	R/W	TRI-STATE	-	-	-	-	-	SPI-PULL	-
14	0xE	01110	R/W	FW[3:0]				-	-	-	-
26	0x1A	11010	R	-	-	-	-	ERR-PAR	ERR-MEM	ERR-NVM	-
27	0x1B	11011	R	MGH	MGL	-	-	-	-	-	-

Table 7: Factory Default Values

# of Registers	Hex	Binary	Read/ Write	Bit[7] (MSB)	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0] (LSB)
0	0x0	00000	R/W	0	0	0	0	0	0	0	0
1	0x1	00001	R/W	0	0	0	0	0	0	0	0
2	0x2	00010	R/W	0	0	0	0	0	0	0	0
3	0x3	00011	R/W	0	0	0	0	0	0	0	0
6	0x6	00110	R/W	0	0	0	1	1	1	0	1
7	0x7	00111	R/W	1	0	0	0	0	0	1	1
8	0x8	01000	R/W	0	1	0	0	0	0	0	0
9	0x9	01001	R/W	0	0	0	0	0	0	0	0
10	0xA	01010	R/W	0	1	0	0	0	0	0	0
13	0xD	01101	R/W	0	0	0	0	0	0	1	0
14	0xE	01110	R/W	1	0	1	0	0	0	0	0

Table 8: Configuration Parameters

Parameters	Symbol	# of Bits	Description	See Table
Zero setting	Z	16	Sets the zero position	9
Bias current trimming	BCT	8	For side-shaft configuration, reduces the bias current of the X or Y Hall device	11
Enable trimming X	ETX	1	Biased current trimmed in the X-direction Hall device	12
Enable trimming Y	ETY	1	Biased current trimmed in the Y-direction Hall device	12
Enable magnetic field threshold	MG	1	Activates the magnetic field threshold detection	-
Magnetic field high threshold	MGHT	3	Sets the field strength high threshold	14
Magnetic field low threshold	MGLT	3	Sets the field strength low threshold	14
IRQ mode	IRQM	1	IRQ pin in logic or latched mode	19
Reference auto-refresh	RAR	1	IRQ pin, automatically updates the reference (REF) during each detection change	18
Hysteresis	HYST	6	Hysteresis of the IRQ signal in logic mode	20
Threshold	THR	8	IRQ signal detection threshold	16
Rotation direction	RD	1	Determines the sensor positive direction	10
Reference	REF	8	IRQ pin, reference position	17
Filter window	FW	4	Size of the digital filter window	15
SPI input pin configuration	SPI-PULL	1	Sets the /CS, MOSI, and SCLK internal circuits	22
SPI output pin configuration	TRI-STATE	1	Sets the MISO internal circuit	23

REGISTER SETTINGS

Zero Setting

The zero position of the MA736 (a_0) can be configured with 16 bits of resolution. The angle streamed out by the part (a_{OUT}) can be calculated with Equation (2):

$$a_{OUT} = a_{RAW} - a_0 \quad (2)$$

Where a_{RAW} is the raw angle provided by the MA736 front end.

The parameter Z[15:0], is the zero-angle position coded on 16 bits (see Table 9).

Table 9: Zero-Setting Parameter

Z[15:0]	Zero Position a_0 (deg)
0	0
1	0.005
2	0.011
…	…
65534	359.989
65535	359.995

Rotation Direction

By default, when looking at the top of the package, the angle increases while the magnetic field rotates clockwise (CW) (see Figure 18).

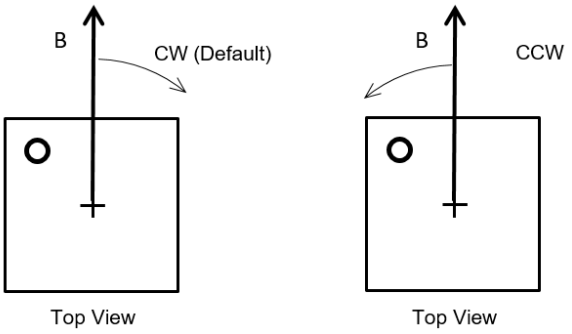


Figure 18: Positive Rotation Direction of the Magnetic Field

Table 10 shows the rotation direction parameter.

Table 10: Rotation Direction Parameter

RD	Positive Direction
0	Clockwise (CW)
1	Counterclockwise (CCW)

Bias Current Trimming (BCT) Settings

Side-Shaft

When the MA736 is mounted on the side of the magnet, the relationship between the field angle and the mechanical angle is no longer directly linear. This effect is related to the fact that the tangential magnetic field is typically smaller than the radial field. The field ratio (*k*) can be determined with Equation (3):

$$k = B_{RAD} / B_{TAN} \quad (3)$$

Where B_{RAD} is the maximum radial tangential magnetic field, and B_{TAN} is the maximum tangential magnetic field (see Figure 19).

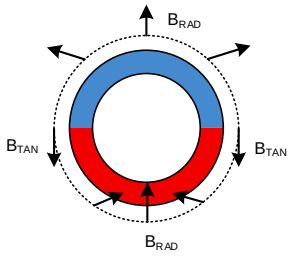


Figure 19: Side-Shaft Field

The *k* ratio depends on the magnet geometry and the distance to the sensor. Having a *k* ratio other than 1 results in the sensor output response not being linear with respect to the mechanical angle. Note that the error curve has the shape of a double sinewave (see Figure 20).

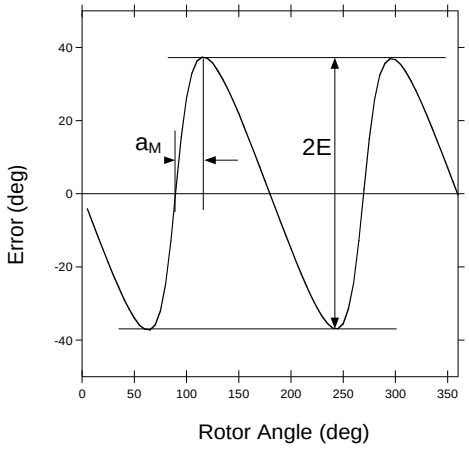


Figure 20: Error Curve in Side-Shaft Configuration with (BCT = 0)

E is the amplitude of this error.

The X-axis or the Y-axis bias currents can be reduced to recover an equal Hall signal for all angles to suppress the error. The ETX and ETY parameters control the direction in which sensitivity is reduced. The current reduction is set by the parameter bias current trimming register (BCT[7:0]), which is an integer between 0 and 255.

In side-shaft configurations (i.e. the sensor center is located beyond the magnet outer diameter), $k > 1$. If k is known, BCT can be calculated with Equation (4):

$$BCT[7:0] = 258\left(1-\frac{1}{k}\right) \quad (4)$$

Figure 21 shows the optimal BCT value for a particular k ratio.

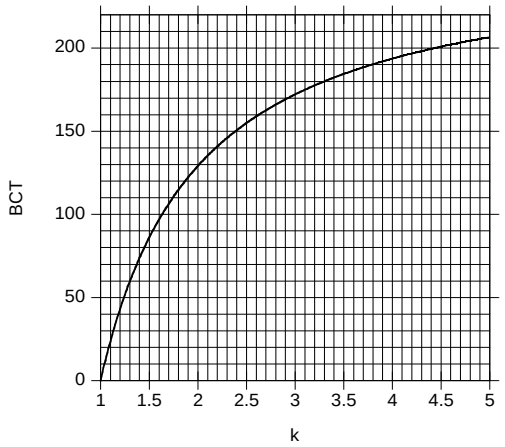


Figure 21: Relationship between the *k* Ratio and the Optimal BCT to Recover Linearity

Table 11 shows typical BCT settings.

Table 11: Typical BCT Settings

E (deg)	Magnet Ratio (*k*)	BCT[7:0]
0	1	0
11.5	1.5	86
19.5	2	129
25.4	2.5	155
30	3	172
33.7	3.5	184
36.9	4	194
39.5	4.5	201
41.8	5	207

Determining k

The k ratio can be deduced from the error curve obtained with the default BCT setting (BCT = 0). Rotate the magnet more than one revolution and record the device's output. Then plot the error curve (the output minus the real mechanical position vs. the real mechanical position) and extract the two parameters: the maximum error (E) and the position of this maximum with respect to a zero crossing a_M (see Figure 21). k can be calculated with Equation (5):

$$k = \frac{\tan(E + a_M)}{\tan(a_M)} \quad (5)$$

The k parameter can also be obtained from a graph (see Figure 22).

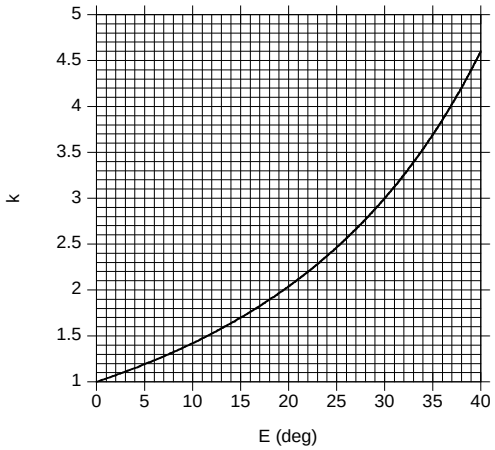


Figure 22: Relationship between the Error Measured with BCT = 0 and the Magnet Ratio *k*

Sensor Orientation

The dot marked on the package indicates whether the radial field is aligned with sensor coordinate X or Y (see Figure 23).

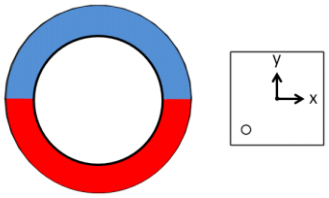


Figure 23: Package Top View with X- and Y-Axes

Determine which axis should be reduced based on the qualitative field distribution around a ring (see Figure 19 on page 18). For example, Figure 23 shows an arrangement in which the field along the sensor Y direction is tangential and

weaker. The X-axis should be reduced (ETX = 1 and ETY = 0). If both ETX and ETY are set to 1, then the current bias is reduced in both directions the same way (i.e. without side-shaft correction) (see Table 12 and Table 13).

Table 12: ETX Trimming Direction Parameter

ETX	Enable Trimming of the X-Axis
0	Disabled
1	Enabled

Table 13: ETY Trimming Direction Parameter

ETY	Enable Trimming of the Y-Axis
0	Disabled
1	Enabled

This reduces the sinusoidal signal and modifies the magnetic field thresholds (see Figure 2 on page 8).

Magnetic Field Thresholds

The magnetic flags (MGL and MGH) indicate whether the magnetic field at the sensor position is out of the range defined by the lower and upper magnetic field thresholds (MGLT and MGHT, respectively) (see Figure 24).

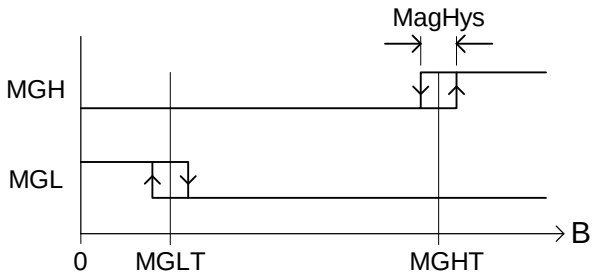


Figure 24: MGH and MGL Signals as a Function of the Field Strength

MagHys is the typical hysteresis on the signals MGH and MGL (6mT). The MGLT and MGHT thresholds are coded on 3 bits and stored in register 6 (see Table 14).

Table 14: Register 6

Register 6							
Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
MGLT			MGHT			-	MG

The 3-bit values of MGLT and MGHT correspond to the magnetic field (see Table 15).

Table 15: MGLT and MGHT Binary to mT Relationship

MGLT or MGHT (9)	Field Threshold in mT (8) (10)	
	From Low to High Magnetic Field	From High to Low Magnetic Field
000	26	20
001	41	35
010	56	50
011	70	64
100	84	78
101	98	92
110	112	106
111	126	120

Notes:

8) Valid for V_{DD} = 3.3V. If V_{DD} ≠ 3.3V, then the field threshold is scaled by the factor V_{DD} / 3.3V.
9) MGLT can have a larger value than MGHT.
10) If ETX = 1 and ETY = 1, then the field thresholds can be increased by increasing BCT.

The MGL and MGH alarm flags can be read via register 27 (bit[6] and bit[7]). Their logic state is also given at digital output pins 2 and 11.

To read the MGL and MGH flags via the SPI, send the 8-bit read command to register 27:

Command			*Reg. Address*					*MSB*			*Value*				*LSB*
0	*1*	*0*	*1*	*1*	*0*	*1*	*1*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*

The MA736 response with the register 27 content in the next transmission:

R[7:0]							
MGH	**MGL**	x	x	x	x	x	x

Filter Window (FW)

The filter window (FW) determines the resolution (defined as the ±3σ noise interval). Figure 25 shows the resolution for different window sizes (FW) and magnetic fields (B).

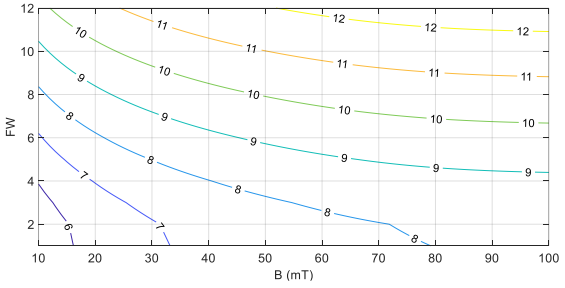


Figure 25: Resolution as a Function of the Magnetic Field and Window Size

Since FW modifies the filter time constant (τ), it has an impact on the output bandwidth. The cutoff frequency (f_{CUTOFF}) is the upper limit of the bandwidth. f_{CUTOFF} can be calculated with Equation (6):

$$f_{CUTOFF} = 0.38 / T \quad (6)$$

Table 16 shows the time constant for each window.

Table 16: Filter Window Size

Window Size FW[3:0]	τ (µs)	f_{CUTOFF} (Hz)
0	1	380 000
1	2	190 000
2	4	95 000
3	8	47 500
4	16	23 750
5	32	11 875
6	64	5 940
7	128	2 970
8	256	1 480
9	512	740
10 (default)	1024	380
11	2048	190
12	4096	95
13	4096	95
14	4096	95
15	4096	95

The time constant (τ) is the parameter entered in the transfer function (1). This allows the user to accurately model the system and analyze the stability of a control loop.

Angle Change Interrupt (IRQ)

Pin 10 indicates when the angle changes with respect to a reference angle. The reference can be a fixed value, or can be automatically updated during each IRQ event.

Threshold

The threshold for defining a change is a relative angle controlled by the parameter THR.

THR is coded on 8 bits (see Table 17). If THR is greater than 180, then the IRQ flag is disabled.

Table 17: IRQ Threshold

THR[7:0]	Threshold (deg)
0	0
1	1.41
2	2.81
…	…
64	90 (default)
…	…
127	178.59
128	180 (IRQ flag only at 180)
129	181.41 (no IRQ flag)
…	…
255	358.59 (no IRQ flag)

Reference

The change is defined in relationship to a reference angle. This angle is controlled by the parameter REF. If the angle distance to REF exceeds the threshold, then the IRQ pin goes high. REF is an absolute angle coded on 8 bits (see Table 18).

Table 18: Change Detection Fixed Reference

REF[7:0]	Reference (deg)
0	0
1	1.41
2	2.81
…	…
64	90 (default)
…	…
255	358.59

REF can be a fixed value, or can be updated automatically during each crossing of the threshold. Incremental change can also be detected. Use the reference auto-refresh bit (RAR) to select the reference type (see Table 19).

Table 19: Reference Auto-Refresh Mode

RAR	Reference
0 (default)	Remains fixed
1	Updated automatically

If RAR is set to 0, then REF remains fixed at the default value or the user value.

If RAR is set to 1, then REF is updated automatically each time the threshold is crossed (see Figure 26).

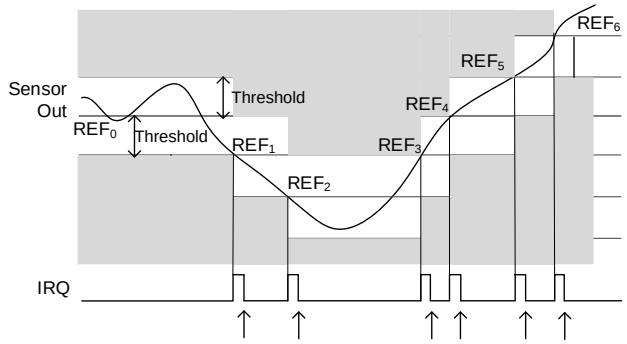


Figure 26: IRQ Motion Profile Signal Response if RAR = 1 and IRQM = 0 (Arrows = SPI Readings)

The user value is replaced by the updated REF value, which is the sensor output value at the moment the threshold was crossed.

IRQ Mode (IRQM)

The IRQ pin can be set to logic level or latch-off mode via the IRQM bit in register 7 (see Table 20).

Table 20: IRQ Pin Mode Parameter

IRQM	Mode
0	Latch off
1 (default)	Logic level

In latch-off mode, the IRQ pin resets at the first SCLK rising edge of some SPI commands (e.g. Read Angle, Store Registers to the NVM, Restore Registers from the NVM, and Clear Status Byte). The IRQ flag does not reset when writing or reading the registers.

In logic-level mode, the IRQ signal is updated every 1µs, and reflects the status of the condition (e.g. the relationship between the angle output value, angle threshold, and angle reference) in real time (see Figure 27).

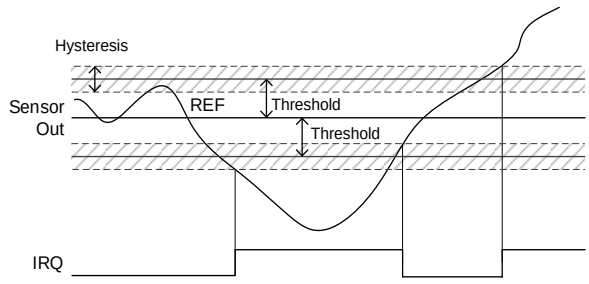


Figure 27: IRQ Signal in Logic-Level Mode when Hysteresis is Applied

In this mode, the IRQ signal status is not reset once the SPI reads the angle. To avoid multiple transitions around the threshold, set an amount of hysteresis via HYST[5:0] in register 7. The hysteresis can be calculated with Equation (7):

$$\text{Hysteresis} = \frac{11.25°}{64} \text{ HYST[5:0]} \quad (7)$$

HYST[5:0] is 3 by default, which means the hysteresis is set to 0.53° (see Table 21).

Table 21: IRQ Pin Hysteresis Setting

HYST[5:0]	HYST (deg)
000000	0
…	…
111111	11.07

HYST[5:0] affects the hysteresis of the IRQ pin, regarless of whether IRQM is 0 or 1.

If RAR and IRQM are both set to 1, then the IRQ pin resets immediately after being set, which generates a short pulse.

Error Flags

Register 26 contains information about the sensor's operational integrity, detailed below.

ERRPAR

When using 17-bit communication on the SPI bus, the SPI write register command sent by the controller to the sensor can be checked for parity (unlike the other commands). The controller sends a parity bit on the MOSI line after the 16-bit command. The sensor checks the parity of the 17-bit command. If the parity is not even, then the data to be written to the register is discarded and the ERRPAR is set to 1.

ERRMEM

If an SPI write register command is sent while the NVM is busy (e.g. the NVM pin is high), then the ERRMEM bit is set to 1. To avoid raising the ERRMEM flag, the user should ensure that no SPI write is sent while the NVM pin is high (set to 1). It is also recommended to check that the register value returned by the SPI write register command matches the desired written value (see the SPI Write Register section on page 13).

ERRNVM

Restoring register values from the NVM is secured by a cyclic redundancy check (CRC) algorithm. If the generated CRC result does not

match the stored value, the ERRNVM bit is set to 1. If any error flag is asserted, then the ERR pin is set to 1. Send the SPI Clear Error Flags command to cleat the error flags and ERR pin.

SPI Pin Configuration

The SPI input pins (/CS, SCLK, and MOSI) are configured as pull-up/pull-down by default.

If required, the SPI inputs can be set to a high-impedance (Hi-Z) state via the SPI-PULL register (see Table 22). When the internal pin impedance is high, it is recommended to externally pull SCLK and MOSI to GND, and to pull /CS to VDD to avoid any voltage buildup and inadvertent programming when the SPI interface is idle (i.e. /CS is high). Figure 28 shows the SPI input pins' internal circuits.

For the values of R_{PD} and R_{PU}, see the General Characteristics table on page 5.

Table 22: SPI Input Pins Circuit

SPI-PULL	SPI Input Pins	
	/CS	SCLK, MOSI
0	Hi-Z	Hi-Z
1 (default)	Pull-up	Pull-down

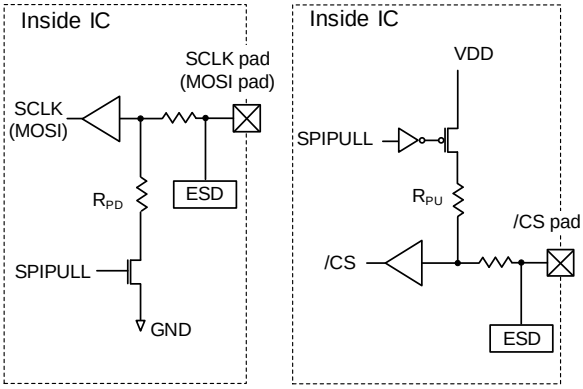


Figure 28: SPI Input Pins Circuit in the IC

The SPI output pin (MISO) is configured to push-pull when SPI active, and is configured to pull-down by default when the SPI interface is idle. MISO can be configured to a Hi-Z state when SPI idle via the TRI-STATE register (see Table 23), which allows connecting multiple devices on the same bus. Figure 29 shows the MISO pin's internal circuit.

Table 23: SPI Output Pin Circuit

TRI-STATE	SPI Output Pin
	MISO
0 (default)	Pull-down when idle
1	Hi-Z when idle

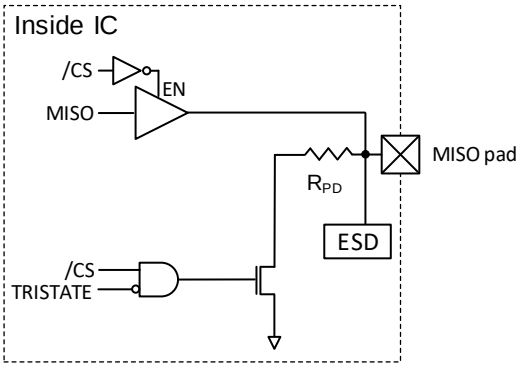


Figure 29: MISO Pin Circuit in the IC

TYPICAL APPLICATION CIRCUIT

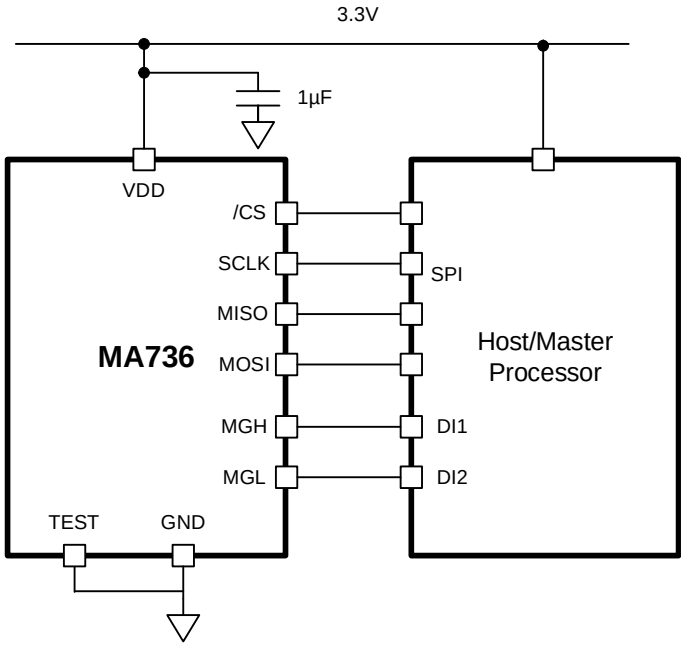


Figure 30: Typical Application Circuit Using the SPI Interface and MGH/MGL Signals

APPENDIX A: DEFINITIONS

Resolution (3σ noise level) The smallest angle increment distinguishable from the noise. The resolution is measured by computing 3 x σ (the standard deviation in degrees) taken across 1,000 data points at a constant position. The resolution in bits is can be calculated with $\log_2(360 / 6\sigma)$.

Refresh Rate The rate at which new data points are stored in the output buffer.

Latency The time elapsed between when the data is ready to be read and when the shaft passes that position. The lag in degrees is (latency x *v*). Where *v* is the angular velocity in deg/s.

Start-Up Time The time until the sensor delivers valid data, beginning at start-up.

Integral Nonlinearity (INL) The maximum deviation between the average sensor output (at a fixed position) and the true mechanical angle (see Figure A1).

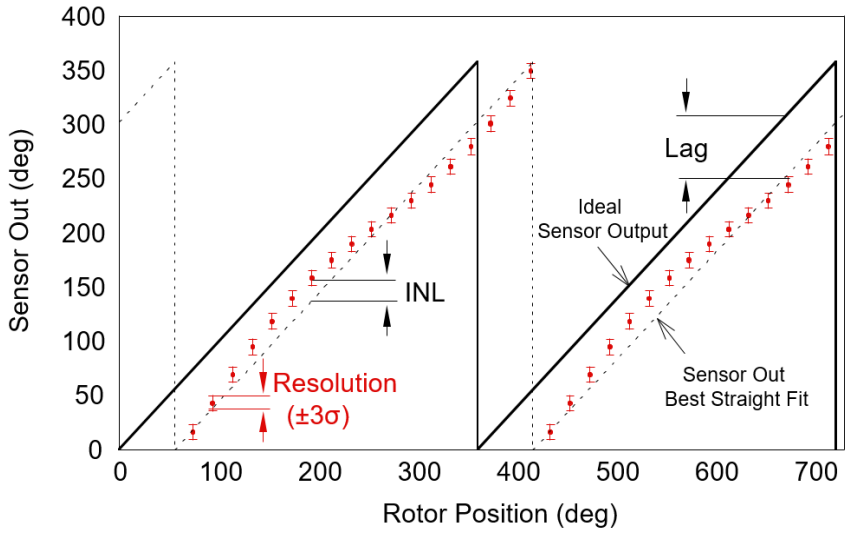


Figure A1: Resolution, INL, Lag

INL can be obtained from the error curve ($err_{(a)} = out_{(a)} - a$). Where $out_{(a)}$ is the average across 1,000 sensor outputs and *a* is the mechanical angle indicated by a high-precision encoder (<0.001°). Then INL is then calculated with Equation (A1):

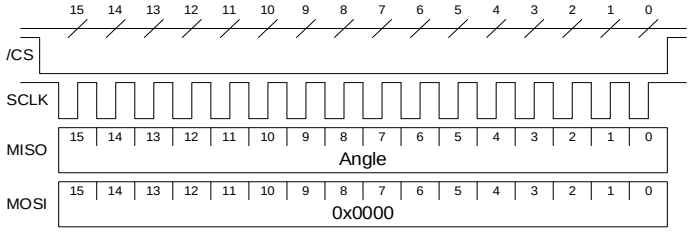
$$INL = \frac{\max(err_{(a)}) - \min(err_{(a)})}{2} \quad (A1)$$

Drift The angle variation rate when one parameter is changed (e.g. temperature, V_{DD}) and all the others remain constant (including the shaft angle).

APPENDIX B: SPI COMMUNICATION CHEAT SHEET

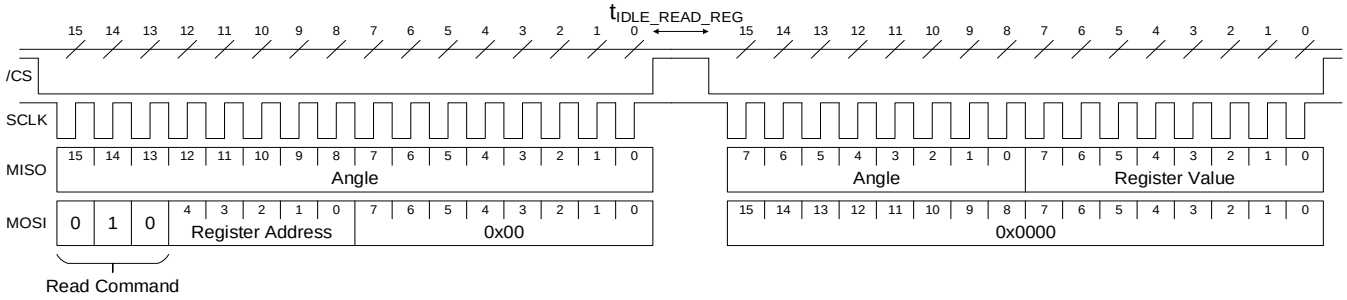
Read Angle

See the SPI Read Angle section on page 12.



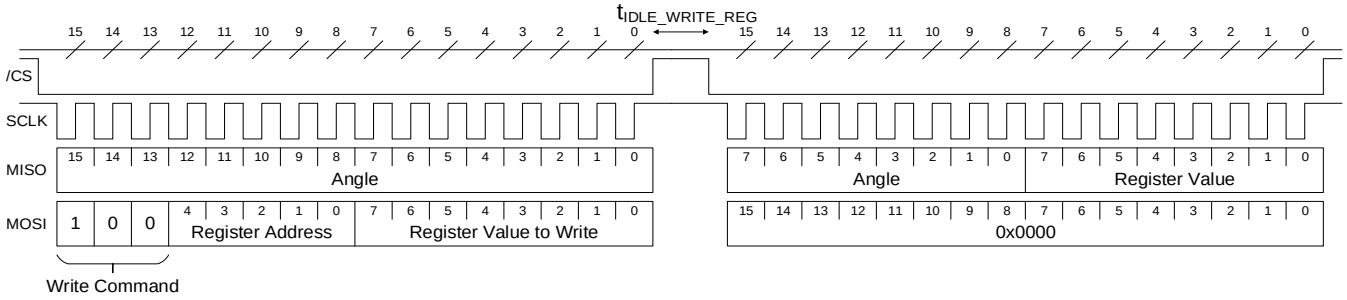
Read Register

See the SPI Read Register section on page 12.



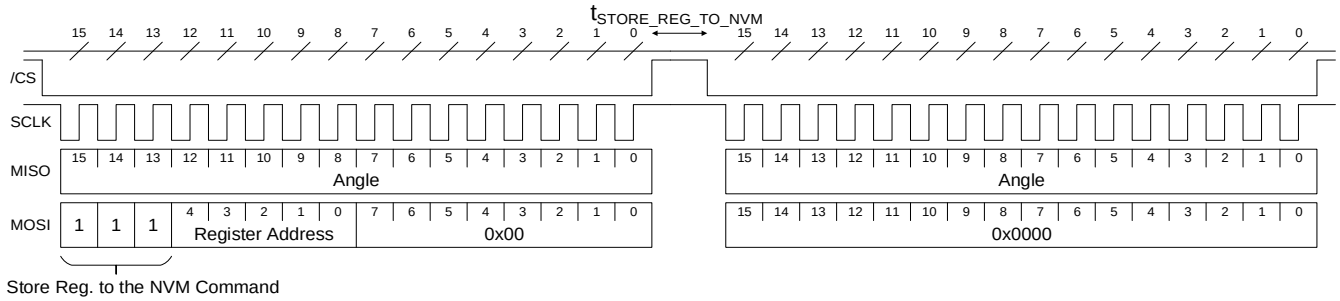
Write Register

See the SPI Write Register section on page 13.



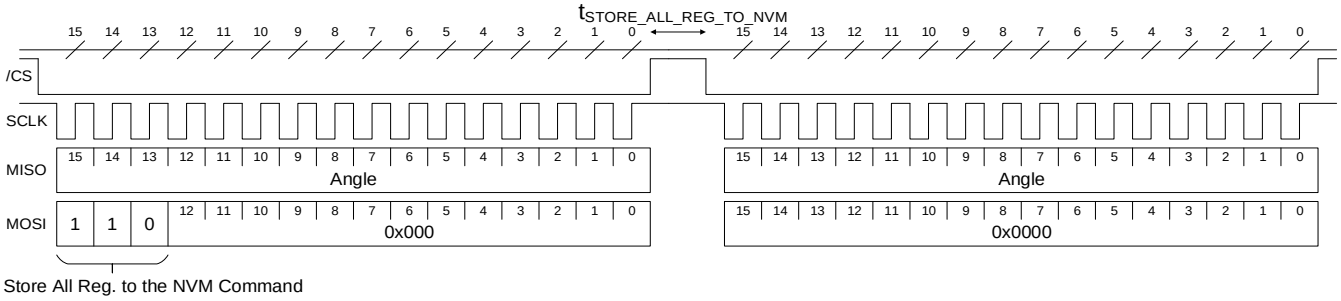
Store a Single Register to the NVM

See the SPI Store a Single Register to the NVM section on page 14.



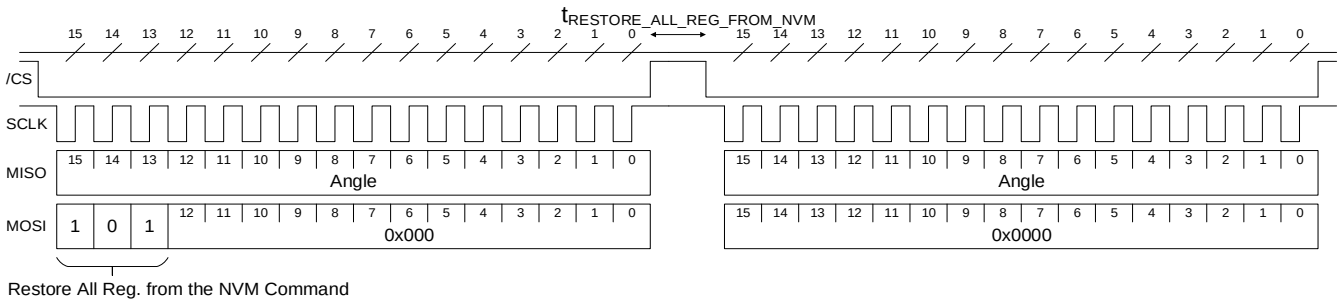
Store All Registers to the NVM

See the SPI Store All Registers to the NVM section on page 14.



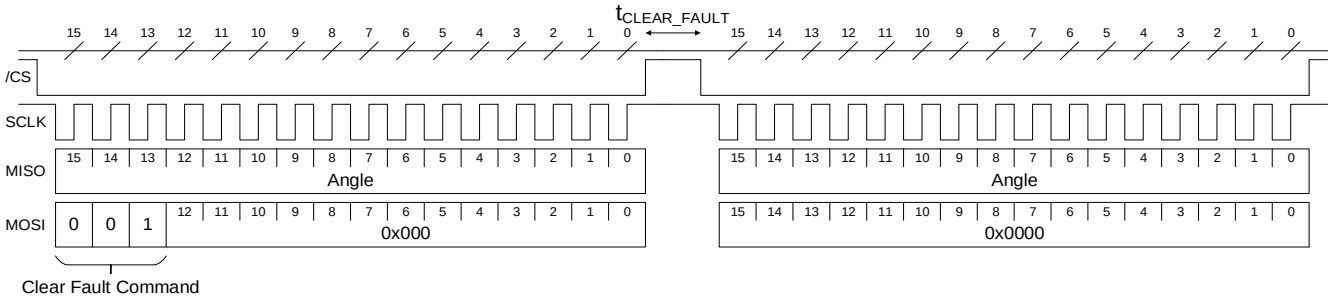
Restore All Registers from the NVM

See the SPI Restore All Registers from the NVM section on page 14.



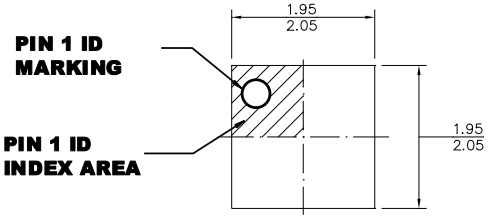
Clear Error Flags

See the SPI Clear Error Flags section on page 14.

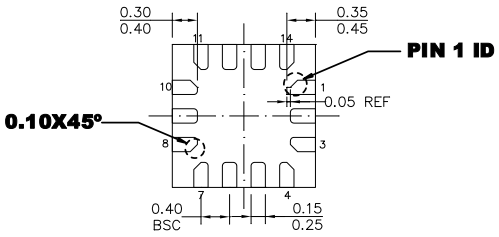


PACKAGE INFORMATION

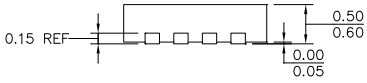
UTQFN-14 (2mmx2mm)



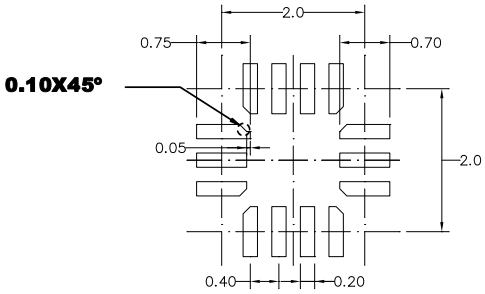
TOP VIEW



BOTTOM VIEW



SIDE VIEW

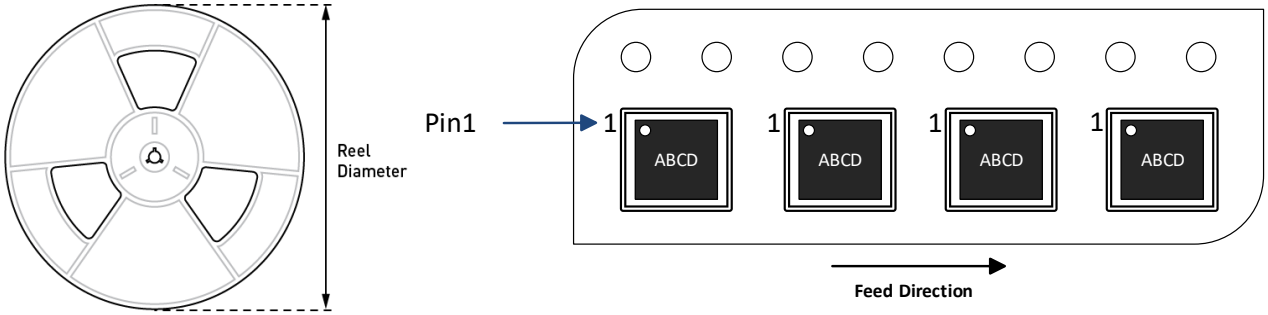


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MA736GGU-Z	UTQFN-14 (2mmx2mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	4/26/2022	Initial Release	-
1.1	1/30/2023	Added SPI pin configuration information	3, 16–17, 23
		Updated note numbers	3–5, 11, 20
		Updated figure number	24
1.2	3/20/2025	Updated the following in Table 6: • Updated the name of the MGLT[2:0] bits to MGLT[3:0], and changed the bits position from bits[7:6] to bits[7:5] • Updated the name of the MGHT[2:0] bits to MGHT[3:0], and changed the bits position from bits[5:4] to bits[4:2]	16
		Corrected the numbering of Table 4	12
		Added MG to the Bit[0] column in Table 14	20