HR1002A

Enhanced LLC Controller with Robust Adaptive Dead-Time Adjustment and Capacitive Mode Protection

DESCRIPTION

The HR1002A is an enhanced LLC controller that provides robust adaptive dead-time adjustment (ADTA) and capacitive mode protection (CMP), as well as improved functional surge performance.

ADTA automatically inserts a dead time between the two complimentary gate outputs. This is ensured by keeping the outputs off while sensing the dV/dt current of the half-bridge switching node. ADTA simplifies the design and provides lower EMI, as well as higher efficiency.

The HR1002A incorporates capacitive mode protection, which prevents potentially destructive capacitive mode switching if the output is shorted or is severely overloaded. This feature protects the MOSFET during abnormal conditions to provide a robust converter.

The HR1002A has a configurable oscillator that sets both the maximum and minimum switching frequencies. To prevent excessive inrush current, it starts up at a configured maximum switching frequency and decays until the control loop takes over.

The HR1002A enters a controlled burst mode under light-load conditions to minimize power consumption and tighten the output regulation.

Full protection features include two-level over-current protection (OCP) with external latched shutdown, auto-recovery, brown-in and brownout, capacitive mode protection (CMP), and over-temperature protection (OTP).

The HR1002A requires minimal external components, and is available in an SOIC16-15 package.

FEATURES

- Over-Current Protection (OCP) with Configurable Delay for Enhanced Surge Performance
- Adaptive Dead-Time Adjustment (ADTA)
- Capacitive Mode Protection (CMP)
- 50% Duty Cycle, Variable Frequency Control for Resonant Half-Bridge Converter
- 600V High-Side Gate Driver with Integrated Bootstrap Diode, High-Accuracy Oscillator, and High dV/dt Immunity
- Operates Up to 600kHz
- Two-Level Over-Current Protection (OCP): Frequency Shift and Latched Shutdown with Configurable Duration
- Latched Disable Input for Easy Protection
- Remote On/Off Control and Brownout Protection through BO
- Configurable Burst Mode Operation under Light-Load Conditions
- Nonlinear Soft Start for Monotonic Output Voltage Rising
- Available in an SOIC16-15 Package

APPLICATIONS

- LCD and PDP TVs
- Desktop PCs and Servers
- Telecom SMPSs
- AC/DC Adapters, Open-Frame SMPSs
- Power Tools
- Video Game Consoles
- Electronic Lighting Ballasts

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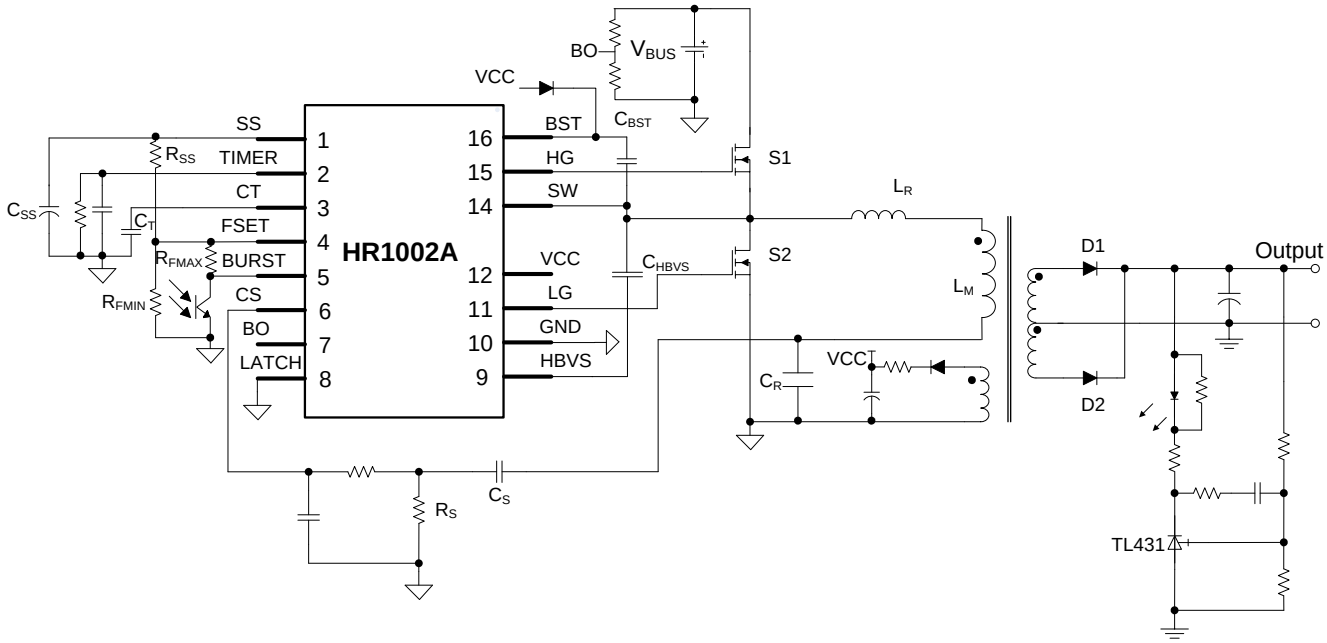
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
HR1002AGSE	SOIC16-15	*See Below*	2

* For Tape & Reel, add suffix –Z (e.g. HR1002AGSE–Z).

TOP MARKING

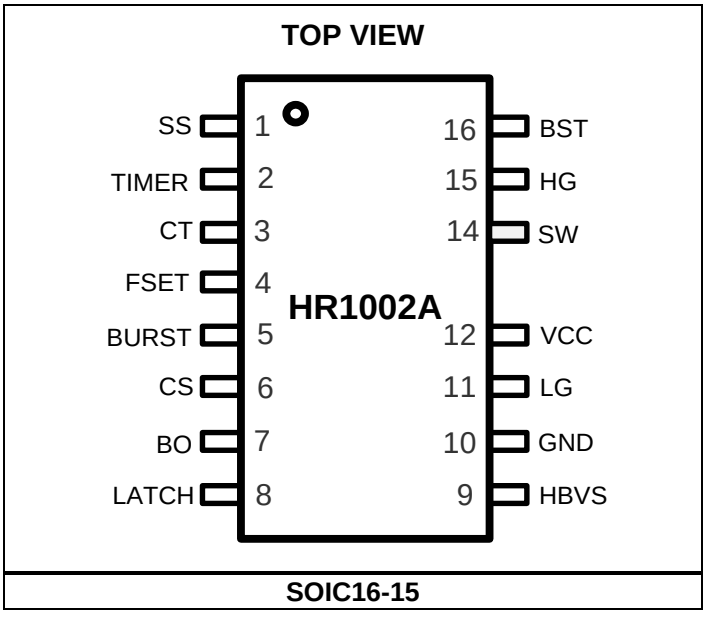
MPSYYWW

HR1002A

LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
HR1002A: Part number
LLLLLLLLL: Lot number

PACKAGE REFERENCE



SOIC16-15

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PIN FUNCTIONS

Pin #	Name	Description
1	SS	**Soft start.** Connect an external capacitor between SS and GND, and a resistor from SS to FSET to set the maximum oscillator frequency and the time constant for the frequency shift during start-up. An internal switch discharges the capacitor when the chip turns off to guarantee a soft start. The chip can shut down due to VCC < V_{CCL}, BO < V_{BO-OFF}, BO > $V_{BO-CLAMP}$, LATCH > V_{LATCH}, CS > V_{CS-OCP}, TIMER > $V_{TIMER-FMAX}$, CMP is triggered and lasts longer than the set delay time (t_{DMAX}, typically 1.5µs), or thermal shutdown.
2	TIMER	**Period between over-current protection (OCP) and shutdown.** Connect a capacitor and a resistor from TIMER to GND to set both the maximum duration from an over-current condition before the IC stops switching, and the delay before the IC resumes switching. Whenever the voltage on the CS pin (V_{CS}) exceeds V_{CS-OCR}, an internal current source (I_{TIMER}) charges the capacitor. An external resistor discharges this capacitor slowly. If the voltage on TIMER reaches $V_{TIMER-FMAX}$, the soft-start capacitor discharges completely, raising its switching frequency to its maximum value. I_{TIMER} remains on. When the voltage exceeds $V_{TIMER-SD}$, the IC stops switching, the internal current source turns off, and the voltage decays. The IC enters soft start when the voltage drops below $V_{TIMER-R}$. This converter works intermittently with very low average input power under short-circuit conditions.
3	CT	**Time setting.** An internal current source configured by an external network connected to FSET charges and discharges a capacitor on CT. This determines the converter's switching frequency.
4	FSET	**Switching frequency setting.** FSET provides a precise 2V reference. A resistor connected from FSET to GND defines a current that sets the minimum oscillator frequency. Connect the phototransistor of an optocoupler to FSET through a resistor to close the feedback loop that modulates the oscillator frequency, which regulates the converter's output voltage. The value of this resistor sets the maximum operating frequency. An RC series connected from FSET to GND sets the frequency shift at start-up to prevent excessive inrush current.
5	BURST	**Burst mode operation threshold.** BURST senses the voltage related to the feedback control, which is compared to an internal reference (V_{BURST}). If the voltage on BURST is below this reference, the IC enters an idle state and reduces its quiescent current. If the feedback drives BURST above V_{BURST} + $V_{BURST-HYS}$ (typically 30mV), the chip resumes switching and does not soft start. This function enables burst mode operation when the load falls below a configured level, determined by connecting an appropriate resistor to the optocoupler to FSET (see the Functional Block Diagram section on page 16). Connect BURST to FSET if burst mode is not used.

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PIN FUNCTIONS *(continued)*

Pin #	Name	Description
6	CS	**Half-bridge current sense.** CS uses a current-sense resistor or a capacitive divider to sense the primary current. CS has the following functions: Over-current regulation: If the voltage exceeds V_{CS-OCR}, the soft-start capacitor on SS discharges internally. The frequency increases, limiting the power throughout. During an output short circuit, this normally results in a nearly constant peak primary current. TIMER limits the duration of this condition. Over-current protection (OCP): If the current continues to rise despite the frequency increase when $V_{CS} > V_{CS-OCP}$, SS is discharged continuously. Over-current protection (OCP) is not triggered until $V_{SS} < V_{SS-OCP}$. If $V_{CS} > V_{CS-OCP}$ once V_{SS} drops below V_{SS-OCP}, OCP is triggered in latch mode. Once this happens, the IC supply voltage must be cycled to restart the HR1002A. The latch is removed once V_{CC} drops below the UVLO threshold. This prevents OCP from mistriggering in surge tests or other transient tests. Capacitive mode protection (CMP): Once LG turns off, V_{CS} is compared to the V_{CSNR} CMP threshold. If $V_{CS} > V_{CSNR}$, HG is blocked from turning on until the slope is detected or the CMP timer is complete. Once HG turns off, V_{CS} is compared to the V_{CSPR} CMP threshold. If $V_{CS} < V_{CSPR}$, the low-side gate is blocked from turning on until the slope is detected or the CMP timer is completed. If a capacitive mode status is detected, SS is not discharged immediately, and there is a delay (t_{DMAX}, typically 1.5µs). After the blanking delay, SS is discharged if the fault condition in capacitive mode remains. This prevents noise on CS. Connect CS to GND if the CMP function is not used.
7	BO	**Input voltage sense and brown-in/brownout protection.** If the voltage on BO exceeds V_{BO-ON}, the IC enables the gate driver. If the voltage on BO is below V_{BO-OFF}, the IC is disabled.
8	LATCH	**IC latch-off.** When the voltage on LATCH exceeds V_{LATCH}, the IC shuts down and lowers its biased current almost to its pre start-up level. LATCH is reset when the voltage on VCC is discharged below its under-voltage lockout (UVLO) threshold. Connect LATCH to GND if the function is not used.
9	HBVS	**Half-bridge dV/dt sense.** To detect the dV/dt of the half-bridge, a high-voltage capacitor is connected between SW and HBVS. The dV/dt current through HVBS adaptively adjusts the dead time between the high-side gate and the low-side gate.
10	GND	**Ground.** GND is the current return for both the low-side gate driver and the IC bias.
11	LG	**Low-side gate driver output.** The driver is capable of a 0.8A source/sink peak current to drive the lower MOSFET of the half-bridge. LG is pulled to GND during under-voltage lockout (UVLO).
12	VCC	**Supply voltage.** VCC supplies both the IC bias and the low-side gate driver. Use a small bypass capacitor (e.g. 0.1µF) to reduce the noise.
14	SW	**High-side switch source.** SW is the current return for the high-side gate drive current. SW requires careful consideration when designing the PCB layout to avoid large spikes below ground.
15	HG	**High-side floating gate driver output**. HG is capable of a 0.8A source/sink peak current to drive the upper MOSFET of the half-bridge. Connect an internal resistor to SW to ensure that HG does not float during UVLO.
16	BST	**Bias for the floating voltage supply of the high-side gate driver.** Connect a bootstrap capacitor between BST and SW. This capacitor is charged by an internal bootstrap diode driven in phase with the low-side gate driver. It is recommended to connect an external bootstrap diode between VCC and BST for a fast set-up of the high-side gate driver's supply. This is especially useful for start-up, or if the device restarts after a fault condition.

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ABSOLUTE MAXIMUM RATINGS (1)

BST voltage .....-0.3V to +618V
SW voltage .....-3V to +600V
Max voltage slew rate of SW 50V/ns
Supply voltage (V_{CC}) .....Self-limited
Sink current of HBVS..... ±65mA
Voltage on HBVS.....-0.3V to self-limit
FSET source current..... 2mA
LG voltage rating .....-0.3V to VCC
CS voltage .....-3V to +6V
Other analog inputs and outputs.....-0.3V to +6V
Continuous power dissipation (T_A = 25°C) (2)
P_{IC} 1.56W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) for all pins..... ±2kV
Charged device model (CDM):
For BST, HG and SW..... ±2kV
All other pins..... ±4kV

Recommended Operating Conditions (3)

Supply voltage (V_{CC}) .....13V to 15.5V
Analog inputs and outputs .....-0.3V to +6V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (4)	***θ_{JA}***	***θ_{JC}***	
SOIC16-15	80	35	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{CC} = 13V, C_{HG} = C_{LG} = 1nF, CT = 470pF, R_{FSET} = 12kΩ, T_J = -40°C to +125°C, min and max values guaranteed by characterization, typical value tested under 25°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units
IC Supply Voltage (VCC)						
VCC operating range			8.9		15.5	V
VCC high threshold, IC switch on	V_{CCH}		10.3	11	11.7	V
VCC low threshold, IC switch off	V_{CCL}		7.5	8.2	8.9	V
Hysteresis	V_{CC-HYS}		2.3	2.8		V
IC Supply Current (VCC)						
Start-up current	$I_{START-UP}$	Before the device turns on, V_{CC} = V_{CCH} - 0.2V		250	320	μA
Quiescent current	I_{Q1}	Device on, BURST < V_{BURST}, R_{FSET} = 12kΩ, f_{SW} = 60kHz		1.2	1.5	mA
	I_{Q2}	Device on, BURST < V_{BURST}, R_{FSET} = 3.57kΩ, f_{SW} ≈ 200kHz		1.42	1.8	mA
Operating current	I_{CC}	Device on, BURST short with FSET		3	5	mA
Residual consumption	I_{FAULT}	VCC < V_{CCL} or LATCH > V_{LATCH} or CS > V_{CS-OCP} or TIMER > $V_{TIMER-SD}$ or BO < V_{BO-OFF} or BO > $V_{BO-CLAMP}$ or OTP is triggered	240	350	420	μA
High-Side Floating Gate Driver Supply (BST and SW)						
BST leakage current	I_{LK-BST}	V_{BST} = 600V, T_J = 25°C			14	μA
SW leakage current	I_{LK-SW}	V_{SW} = 582V, T_J = 25°C			14	μA
Current Sense (CS)						
Input bias current	I_{CS}	V_{CS} = 0V to V_{CS-OCP}			2	μA
Frequency shift threshold	V_{CS-OCR}		0.9	1	1.1	V
OCP threshold	V_{CS-OCP}		1.41	1.5	1.59	V
Current polarity comparator reference when HG turns off	V_{CSPR}		50	85	131	mV
Current polarity comparator reference when LG turns off	V_{CSNR}		-131	-85	-50	mV
Line Voltage Sensing (BO)						
Start-up threshold voltage	V_{BO-ON}		2.15	2.3	2.4	V
Shutdown threshold voltage	V_{BO-OFF}		1.72	1.81	1.9	V
Clamp level	$V_{BO-CLAMP}$		5.1	5.5	5.9	V
Latch-Off Function (LATCH)						
Input bias current (V_{LATCH} = 0V to V_{LATCH})	I_{LATCH}				1	μA
LATCH threshold	V_{LATCH}		1.72	1.85	1.95	V

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ELECTRICAL CHARACTERISTICS *(continued)*

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Parameter	Symbol	Condition	Min	Typ	Max	Units
Oscillator						
Output duty cycle	D	T_J = 25°C	48	50	52	%
		T_J = -40 to +125°C	47	50	53	%
Maximum operation frequency	f_{OSC}	CT ≤ 150pF, R_{FSET} ≤ 2kΩ, dead time = 300ns	580			kHz
CT peak value	V_{CFP}		3.54	3.8	3.94	V
CT valley value	V_{CFV}		0.79	0.9	0.95	V
CT hysteresis	V_{CT_HYS}		2.7	2.85	3	V
Voltage reference at FSET	V_{REF}		1.87	2	2.05	V
First LG delay time	$t_{LG_DELAY_1ST}$		1	2.2	3.5	µs
Dead time	t_{DMIN}	C_{HBVS} = 5pF (typical)	180	235	290	ns
	t_{DMAX}		1.3	1.5	2	µs
Timer for CMP	t_{CMP}		35	52	80	µs
Half-Bridge Voltage Sense (HBVS)						
Voltage clamp	$V_{HBVS-CLAMP}$		7	7.6	8.2	V
Minimum voltage change rate that can be detected	dV_{MIN}/dt	C_{HBVS} = 5pF (typical)			180	V/µs
Turn-on delay	t_{ON-D}	Slope finish to turn-on delay	70	100	150	ns
Soft-Start Function (SS)						
Discharge resistance	R_{SS}	V_{CS} > V_{CS-OCR}	110	130	150	Ω
Threshold for OCP latch	V_{SS-OCP}	V_{CS} > V_{CS-OCP}	1.64	1.73	1.82	V
Standby Function (BURST)						
Disable threshold	V_{BURST}		1.17	1.23	1.28	V
Hysteresis	V_{BURST_HYS}			30	100	mV
Delayed Shutdown (TIMER)						
Charge current	I_{TIMER}	V_{TIMER} = 0V, V_{CS} = 1.05V, T_J = 25°C	80	130	180	µA
Threshold for forced operation at maximum frequency	$V_{TIMER-FMAX}$		1.8	2	2.1	V
Shutdown threshold	$V_{TIMER-SD}$		3.2	3.5	3.7	V
Restart threshold	$V_{TIMER-R}$		0.21	0.28	0.35	V
Low-Side Gate Driver (LG, Referenced to GND)						
Peak source current (5)	$I_{LG-SOURCE-PK}$			0.75		A
Peak sink current (5)	$I_{LG-SINK-PK}$			0.87		A
Sourcing resistor	$R_{LG-SOURCE}$	I_{SOURCE} = 0.01A, T_J = 25°C	4.3	5.5	6.7	Ω
Sinking resistor	$R_{LG-SINK}$	I_{SINK} = 0.01A, T_J = 25°C	1.6	2.8	4	Ω
Fall time	t_{LG-F}			30	45	ns
Rise time	t_{LG-R}			30	45	ns
UVLO saturation		V_{CC} = 0 to V_{CCH}, I_{SINK} = 2mA			1	V

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{CC} = 13V, C_{HG} = C_{LG} = 1nF, CT = 470pF, R_{FSET} = 12kΩ, T_J = -40°C to +125°C, min and max values guaranteed by characterization, typical value tested under 25°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units
High-Side Gate Driver (HG, Referenced to SW)						
Peak source current (5)	$I_{HG-SOURCE-PK}$			0.74		A
Peak sink current (5)	$I_{HG-SINK-PK}$			0.87		A
Sourcing resistor	$R_{HG-SOURCE}$	I_{SOURCE} = 0.01A, T_J = 25°C	4.3	5.5	6.7	Ω
Sinking resistor	$R_{HG-SINK}$	I_{SINK} = 0.01A, T_J = 25°C	1.6	2.8	4	Ω
Fall time	t_{HG-F}			30	45	ns
Rise time	t_{HG-R}			30	45	ns
Thermal Shutdown						
Thermal shutdown threshold (5)				150		°C
Thermal shutdown recovery threshold (5)				120		°C

Note:

5) Guaranteed by design.

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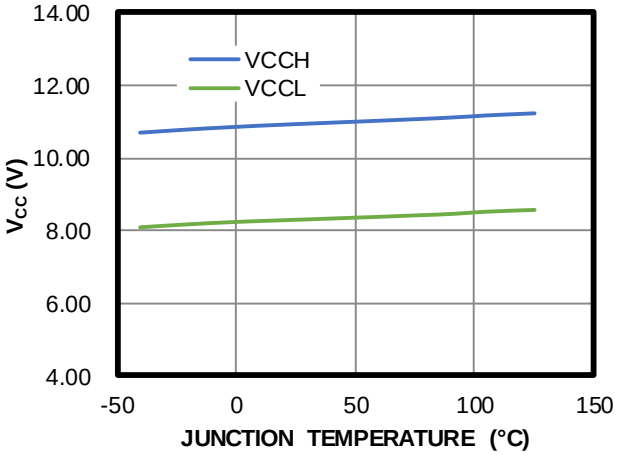
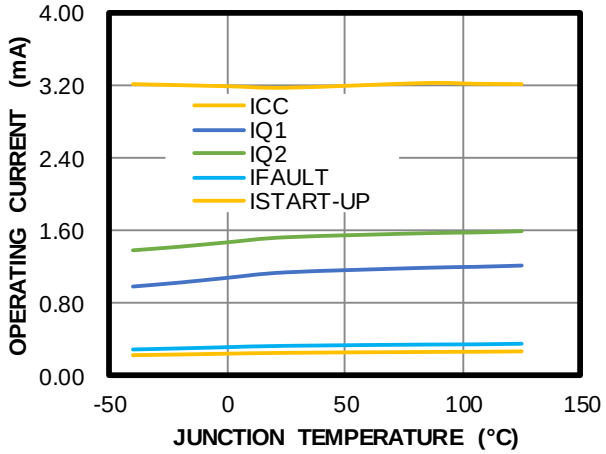
TYPICAL CHARACTERISTICS

V_{CC} = 13V, C_{HG} = C_{LG} = 1nF, C_T = 470pF, R_{FSET} = 12kΩ, T_J = -40°C to +125°C, unless otherwise noted.

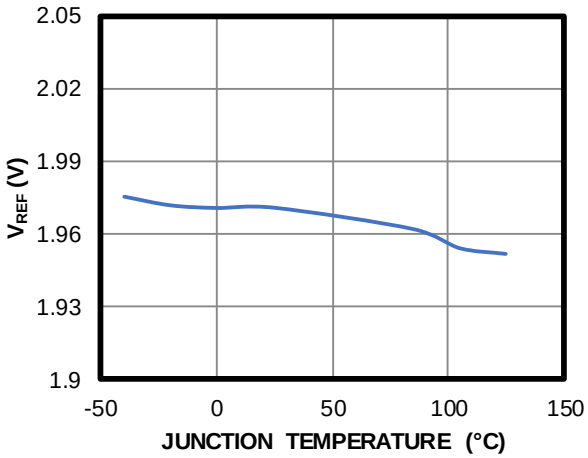
V_{CC} vs. Junction Temperature



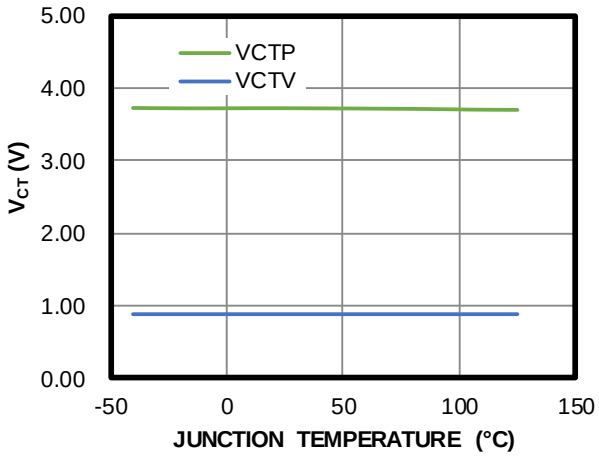
Operating Current vs. Junction Temperature



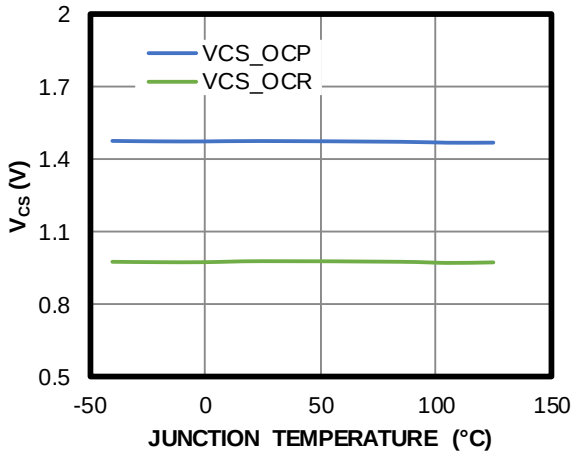
Reference Voltage vs. Junction Temperature



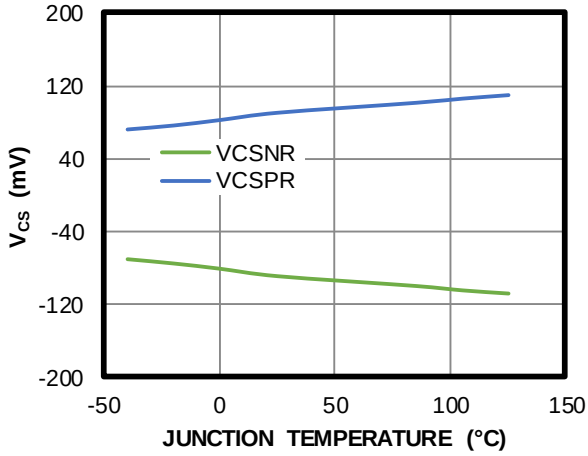
CT Voltage vs. Junction Temperature



Current-Sense Threshold vs. Junction Temperature



Current Polarity Reference vs. Junction Temperature



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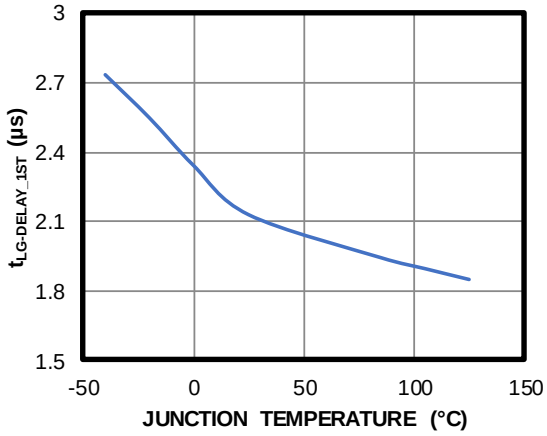
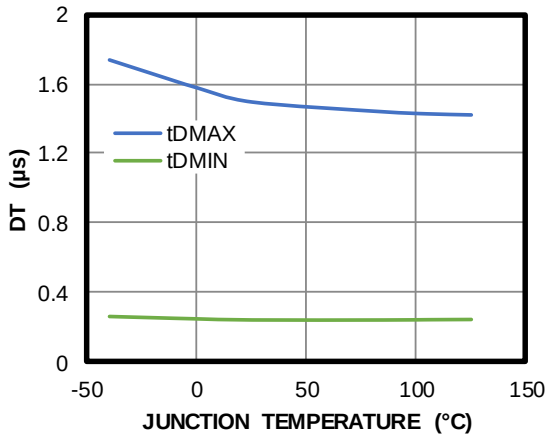
TYPICAL CHARACTERISTICS *(continued)*

V_{CC} = 13V, C_{HG} = C_{LG} = 1nF, C_T = 470pF, R_{FSET} = 12kΩ, T_J = -40°C to +125°C, unless otherwise noted.

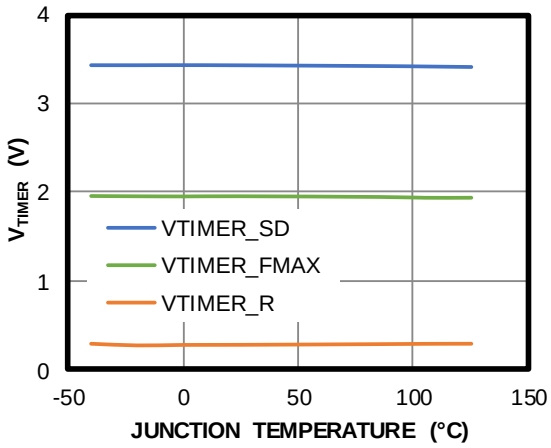
First LG Delay vs. Junction Temperature



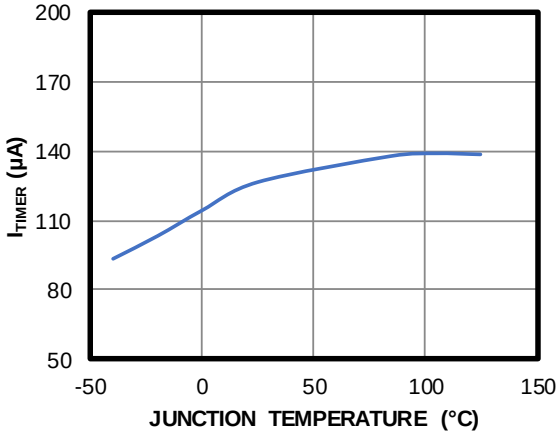
Dead Time vs. Junction Temperature



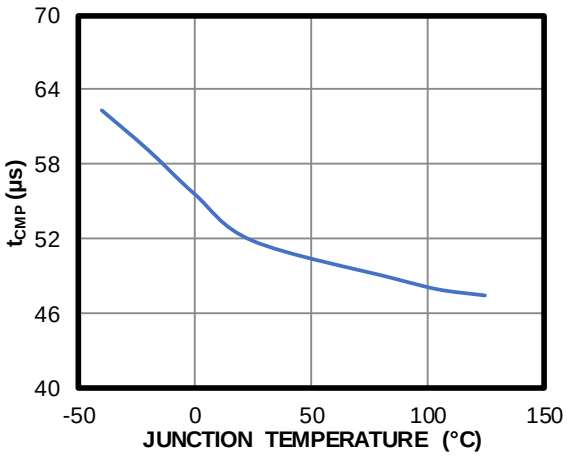
TIMER Threshold vs. Junction Temperature



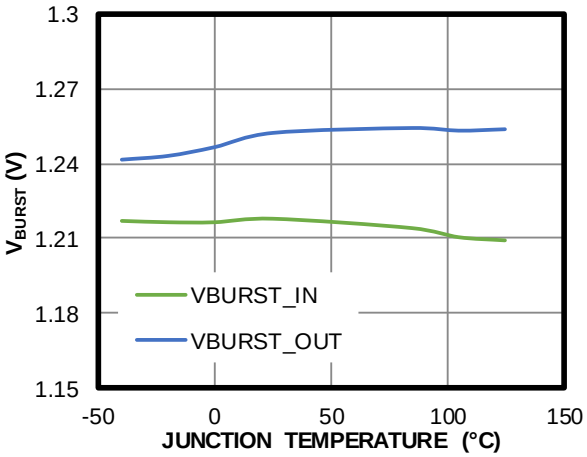
TIMER Charge Current vs. Junction Temperature



CMP Timer vs. Junction Temperature



BURST Threshold vs. Junction Temperature



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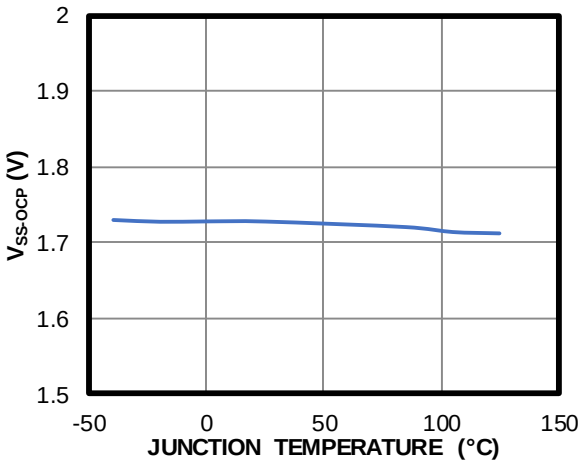
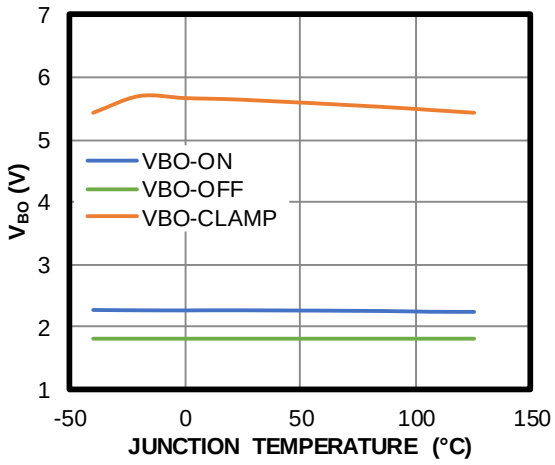
TYPICAL CHARACTERISTICS *(continued)*

V_{CC} = 13V, C_{HG} = C_{LG} = 1nF, C_T = 470pF, R_{FSET} = 12kΩ, T_J = -40°C to +125°C, unless otherwise noted.

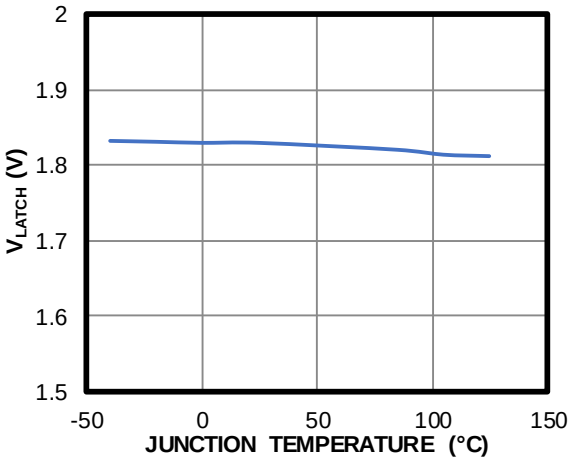
SS Level for OCP vs. Junction Temperature



BO Threshold vs. Junction Temperature



LATCH Threshold vs. Junction Temperature



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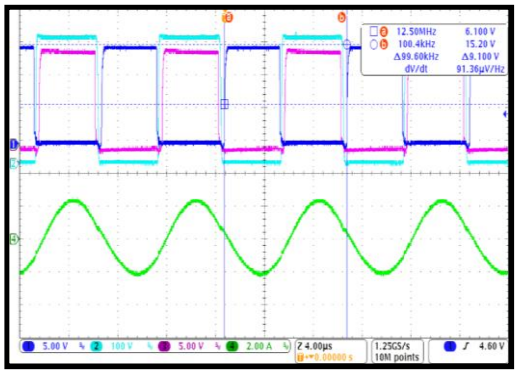
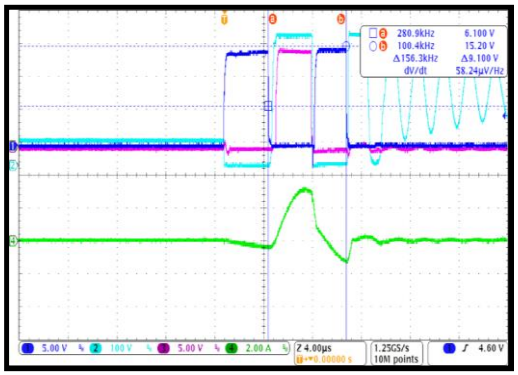
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are generated using the evaluation board (see Figure 26 on page 32). V_{AC} = 230V, V_{OUT} = 12V, I_{OUT} = 20A, T_A = 25°C, unless otherwise noted.

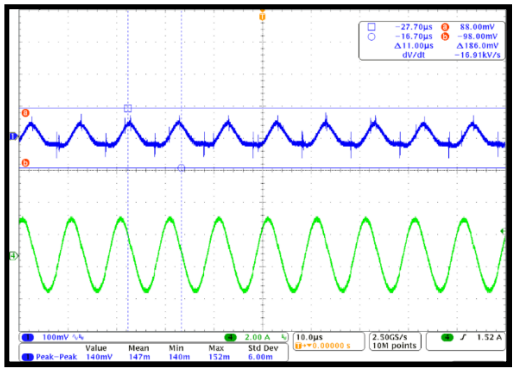
Steady State
Full load



Steady State
No load



Output Ripple
Full load



Output Ripple
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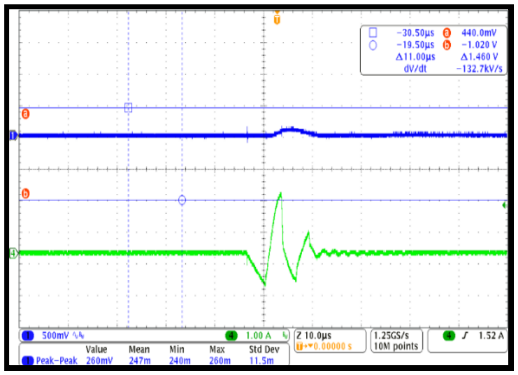
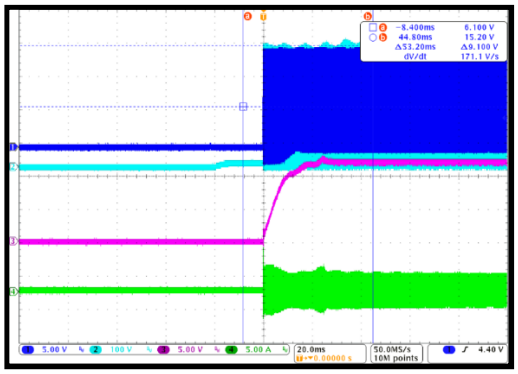


Start-Up
Full load



Start-Up
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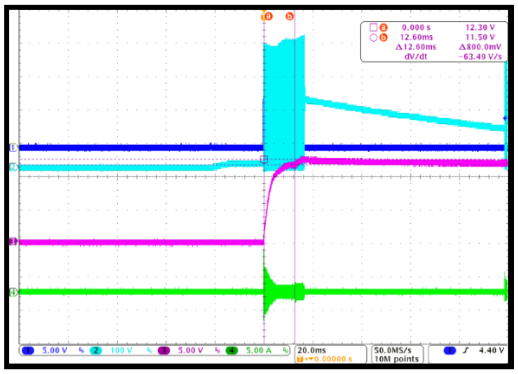

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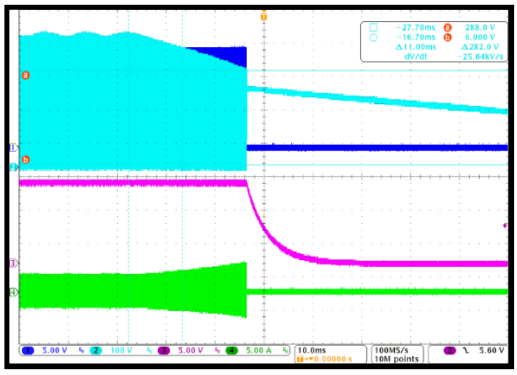
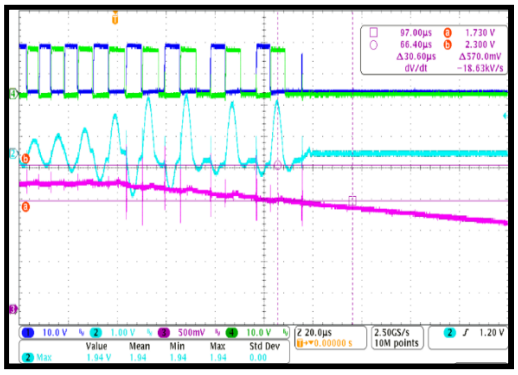
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are generated using the evaluation board (see Figure 26 on page 32). V_{AC} = 230V, V_{OUT} = 12V, I_{OUT} = 20A, T_A = 25°C, unless otherwise noted.

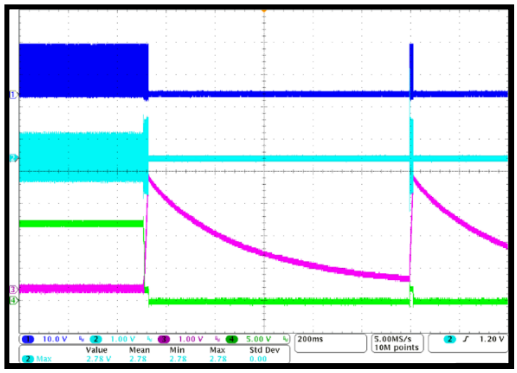
Shutdown
Full load



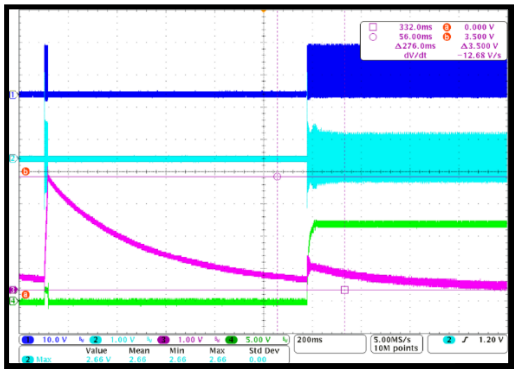
Short-Circuit Protection
Latch-off mode



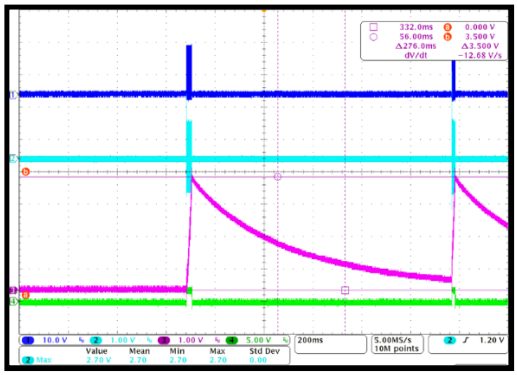
Over-Current Protection Entry
Full load



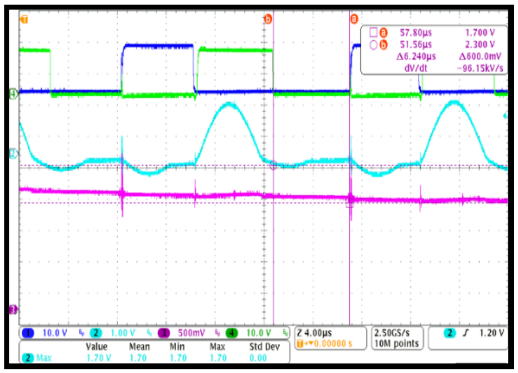
Over-Current Protection Recovery
Full load



Short then Start
Full load



Capacitive Mode Protection
Short circuit



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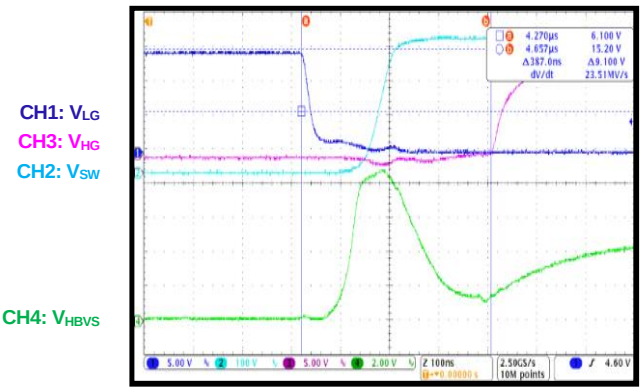
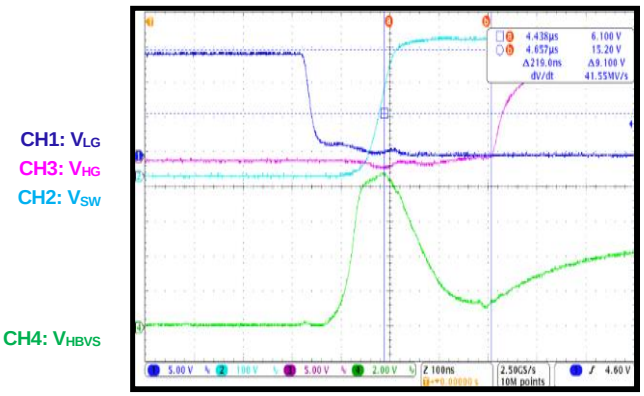
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are generated using the evaluation board (see Figure 26 on page 32). V_{AC} = 230V, V_{OUT} = 12V, I_{OUT} = 20A, T_A = 25°C, unless otherwise noted.

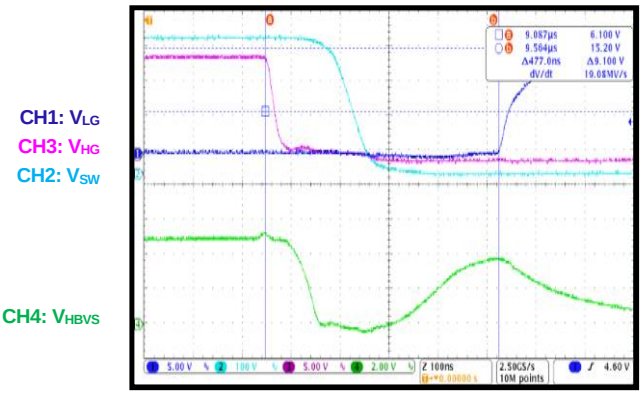
Dead Time When LG Turns Off



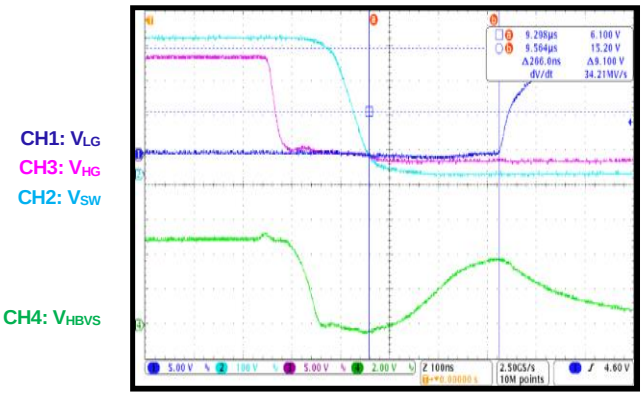
Delay Time When LG Turns Off



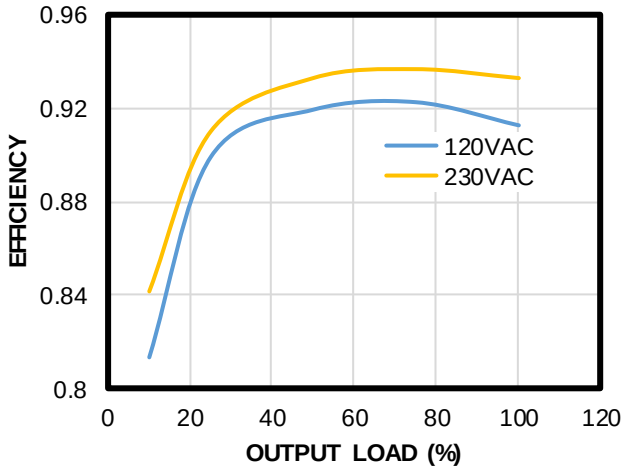
Dead Time When HG Turns Off



Delay Time When HG Turns Off



Efficiency



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FUNCTIONAL BLOCK DIAGRAM

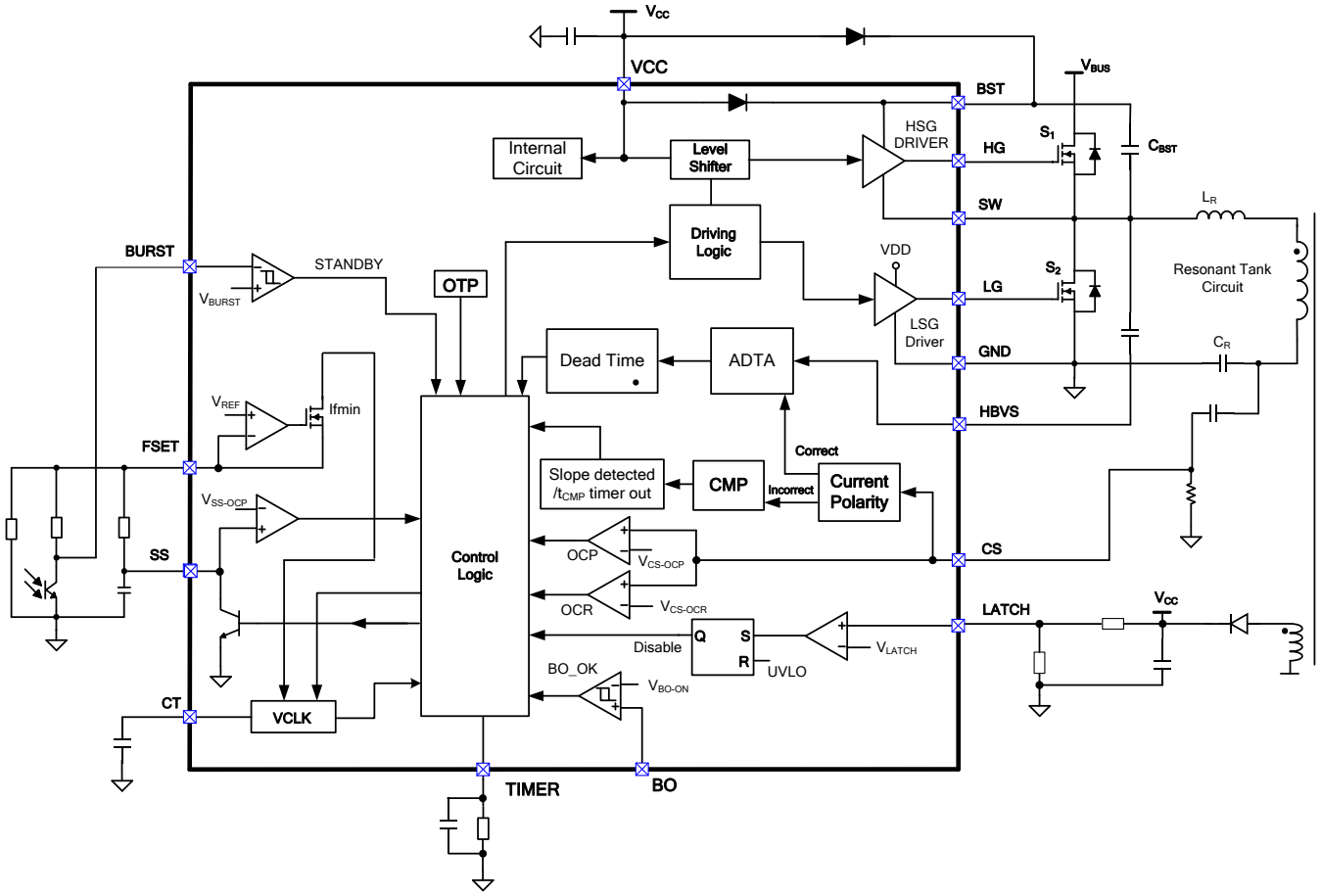

Figure 1: Functional Block Diagram

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OPERATION

Oscillator

Figure 2 shows the oscillator block diagram. A modulated current charges and discharges the CT capacitor repeatedly between its peak valley thresholds, which determines the oscillator frequency.

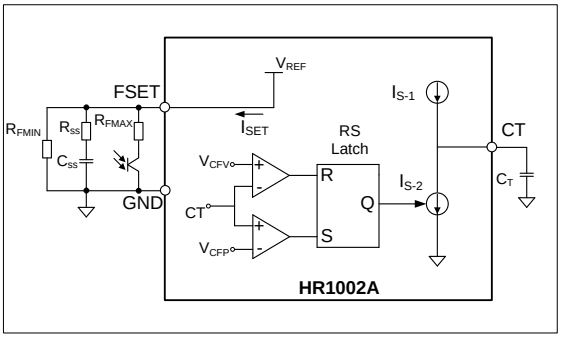

Figure 2: Oscillator Block Diagram

FSET sets the CT charge current, with I_{S-1} being equal to I_{SET}. When CT passes its peak threshold (V_{CFP}), the RS latch is set, and a discharge current source (I_{S-2}) that equals 2 times I_{SET} is enabled. The difference between these two currents forces CT to have equal charging and discharging values. If the voltage on the CT capacitor falls below its valley threshold (V_{CFV}, hysteresis $V_{CT_HYS} = V_{CFP} - V_{CFV}$), the flip-flop is reset and I_{S-2} turns off. This starts a new switching cycle. Figure 3 shows the oscillator's detailed waveform.

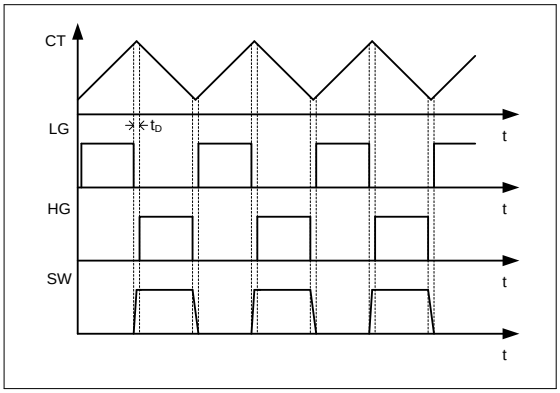

Figure 3: CT Waveform and Gate Signal

An RC network that is externally connected to FSET determines the normal switching frequency and the soft-start switching frequency.

The resistor from FSET to GND (R_{FMIN}) contributes to the maximum resistance of the external RC network when the phototransistor is not conducting. This sets the FSET minimum source current, which defines the minimum switching frequency.

During normal operation, the phototransistor adjusts the current flowing through R_{FMAX} to modulate the frequency for output voltage regulation. If the phototransistor is saturated, the current through R_{FMAX} is at its maximum, which sets the frequency at its maximum.

An RC connected in series between FSET and GND shifts the frequency at start-up. See the Soft Start (SS) section below for more details.

Calculate the minimum and maximum frequencies with Equation (1) and Equation (2), respectively:

$$f_{MIN} \approx \frac{1}{V_{CT_HYS} \times C_T \times R_{FMIN}} \quad (1)$$

$$f_{MAX} \approx \frac{R_{FMIN} + R_{FMAX}}{V_{CT_HYS} \times C_T \times R_{FMIN} \times R_{FMAX}} \quad (2)$$

It is recommended to use a CT capacitor (≤330pF) for the best overall temperature performance. Estimate the values of R_{FMIN} and R_{FMAX} with Equation (3) and Equation (4), respectively:

$$R_{FMIN} = \frac{1}{V_{CT_HYS} \times C_T \times f_{MIN}} \quad (3)$$

$$R_{FMAX} = \frac{R_{FMIN}}{\frac{f_{MAX}}{f_{MIN}} - 1} \quad (4)$$

Soft Start (SS)

For the resonant half-bridge converter, the power delivered is inversely proportional to its switching frequency. To ensure that the converter starts or restarts with a safe current level, soft start forces a high initial switching frequency until the frequency is controlled by the closed loop.

Soft start is achieved using an external RC series circuit (see Figure 4).

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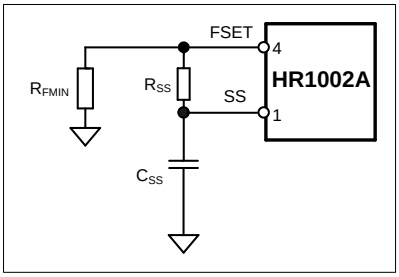

Figure 4: Soft-Start Block

When start-up begins, the SS voltage is 0V, so the soft-start resistor (R_{SS}) is in parallel to R_{FMIN}. R_{FMIN} and R_{SS} determine the initial frequency (f_{START}), which can be calculated with Equation (5):

$$f_{START} = \frac{R_{FMIN}+R_{SS}}{V_{CT_HYS} \times C_T \times R_{FMIN} \times R_{SS}} \quad (5)$$

During start-up, C_{SS} charges until its voltage reaches the reference voltage (V_{REF}), and the current through R_{SS} decays to 0A. This period takes about 5 times the (R_{SS} x C_{SS}) value. During this period, the switching frequency changes following an exponential curve. Initially, the C_{SS} charge reduces the frequency relatively quickly, but the rate gradually decreases.

After soft start, the switching frequency is dominated by the feedback loop to regulate the output voltage. With soft start, the current of the resonant tank gradually increases during start-up.

Calculate R_{SS} with Equation (6):

$$R_{SS} = \frac{R_{FMIN}}{\frac{f_{START}}{f_{MIN}} - 1} \quad (6)$$

Estimate C_{SS} with Equation (7):

$$C_{SS} = \frac{3 \times 10^{-3}}{R_{SS}} \quad (7)$$

Select the initial frequency (f_{START}) to be at least four times greater than f_{MIN}. When selecting C_{SS}, there is a tradeoff between the desired soft start operation and over-current protection (OCP) speed. See the Over-Current Protection (OCP) section on page 21 for more details.

Adaptive Dead-Time Adjustment (ADTA)

When operating in inductive mode, the soft switching of the power MOSFETs results in high efficiency for the resonant converter. A fixed dead time may result in hard switching under light loads, especially if the magnetizing inductance (L_M) is too large. A dead time that is too long may lead to zero-voltage switching (ZVS) loss. In addition, the current may change polarity during the dead time, resulting in capacitive mode switching. Adaptive dead-time control adjusts the dead time automatically by detecting the dV/dt of the half-bridge's switching node (SW).

The HR1002A incorporates an intelligent adaptive dead-time adjustment (ADTA) logic circuit, which detects SW's dV/dt and inserts a proper dead time automatically. For the external circuit, connect a capacitor (C_{HBVS}, typically 5pF) between SW and HBVS to sense dV/dt. Figure 5 shows the simplified ADTA block diagram.

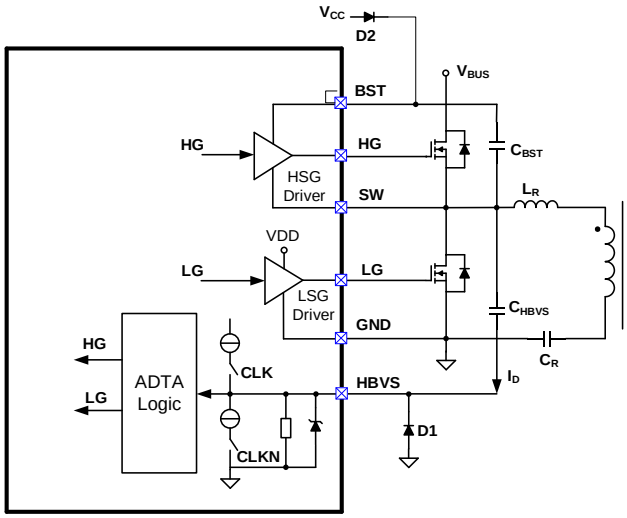

Figure 5: ADTA Block Diagram

Figure 6 shows the operation waveform for ADTA.

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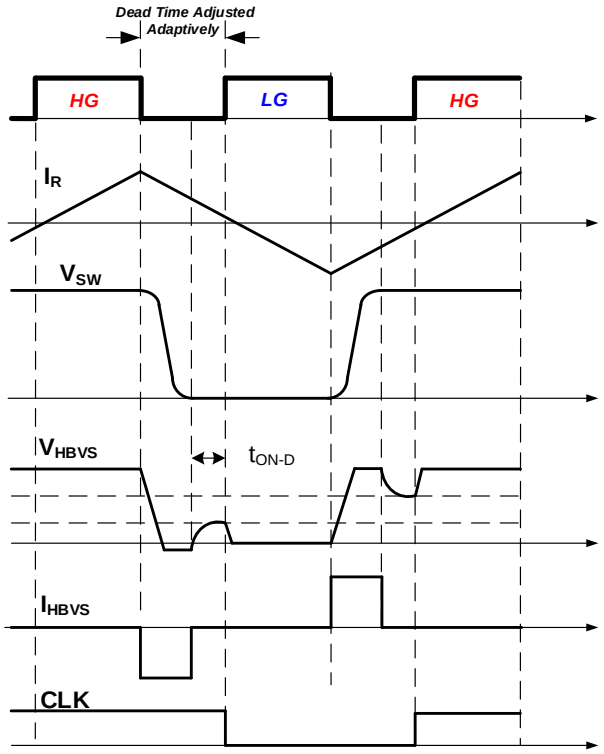

Figure 6: Operation Waveform of ADTA

When HG switches off, the SW voltage swings from high to low due to the resonant tank current (I_R). Accordingly, this negative dV/dt pulls current from HBVS via C_{HBVS}. If the dV/dt current exceeds the internal comparison current, the voltage on HBVS (V_{HBVS}) is pulled down and clamped at 0V. When SW stops slewing and the differential current stops, V_{HBVS} starts to ramp up. LG turns on after a delay (minimum dead time). The dead time is the time between HG turning off and LG turning on.

When LG switches off, the SW voltage swings from low to high, and a positive dV/dt current is detected via C_{HBVS}. The dead time between LG turning off and HG turning on is maintained automatically by sensing the dV/dt current.

To avoid damaging HBVS, C_{HBVS} should be selected carefully. Keep the dV/dt current below 65mA. I_{HBVS} can be calculated with Equation (8):

$$I_{HBVS} = \left| C_{HBVS} \times \frac{dV}{dt} \right| < 65mA \quad (8)$$

If C_{HBVS} is too low to sense the dV/dt, the minimum voltage change rate (dV_{MIN}/dt) must be accounted for to ensure a proper C_{HBVS} value.

First, calculate the peak magnetizing current (I_M) with Equation (9):

$$I_M = \frac{V_{BUS}}{8 \times L_M \times f_{MAX}} \quad (9)$$

Estimate C_{HBVS} with Equation (10):

$$C_{HBVS} > 5pF \times \frac{dV_{MIN}}{dt} \times \frac{2 \times C_{OSS}}{I_M} \quad (10)$$

Where C_{OSS} is the output capacitance of MOSFET, and dV_{MIN}/dt is 180V/μs. Leave a margin that is 2 to 3 times greater than the calculated capacitance for C_{HBVS} due to design and component tolerance.

Figure 7 shows a possible dead time using ADTA logic. Note that there are three types of dead times: the minimum dead time (t_{DMIN}), maximum dead time (t_{DMAX}), and adjusted dead time (t_D), which is between t_{DMIN} and t_{DMAX}.

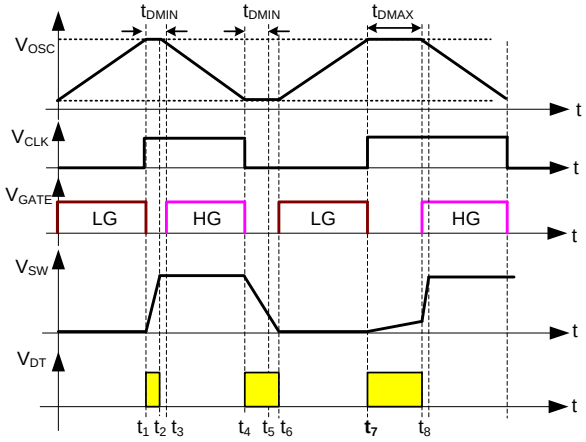

Figure 7: Dead Time in ADTA

ADTA logic sets t_{DMIN} to 235ns. If the SW transition time is shorter than t_{DMIN}, the logic does not let the gate turn on, which prevents shoot-through between the low-side and high-side MOSFETs. A maximum dead time (t_{DMAX}, typically 1.5μs) forces the gate to turn on, preventing duty cycle losses or soft switching.

ADTA adjusts the dead time automatically and ensures ZVS, which enables more flexibility when selecting the MOSFET and L_M. ADTA also prevents hard switching if the design does not carefully account for light-load or no-load conditions.

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Under light-load conditions, the switching frequency goes high and the magnetizing current goes low, which risks hard switching that can lead to thermal or reliability issues.

If HBVS is not connected, the internal circuit cannot detect the differential current from HBVS, so the dead time remains fixed at the maximum dead time (t_{DMAX}).

If V_{HBVS} is pulled down too low by the negative current from C_{HBVS}, the dead time from HG turning off to LG turning on may be too long. To clamp HBVS at lower negative voltage and ensure an optimal dead time, connect a Schottky diode (D1) (such as BAT54) from GND to HBVS.

Capacitive Mode Protection (CMP)

When the resonant HB converter output is subject to overload or short circuit conditions, the converter may run into a capacitive region. In capacitive mode, the voltage applied to the resonant tank causes the resonant tank's current to lag. Under this condition, the body diode of only one MOSFET is conducting. To prevent the device from failing, the other MOSFET should not be turned on. Figure 8 shows the functional block diagram for capacitive mode protection (CMP).

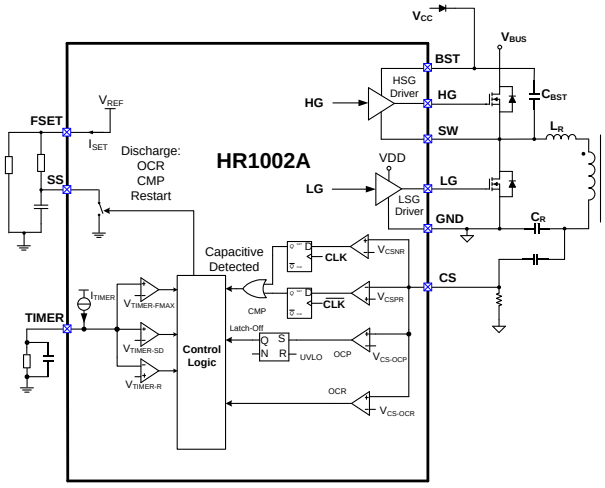

Figure 8: CMP and OCP Block Diagram

Figure 9 shows the operating current principles of CMP. CSPOS and CSNEG stand for the current polarity, which is generated by comparing the voltage on CS with the internal V_{CSNR} and V_{CSPR} voltage references.

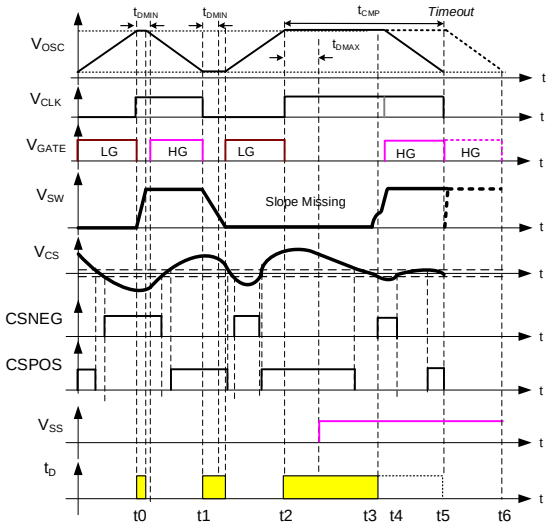

Figure 9: Operating Principles of CMP

t0: At t0, LG turns off and CSNEG is high. This means the current is flowing in the correct direction and converter operates in inductive mode.

t1: At t1, HG turns off and CSPOS is high. This means that the current is flowing in the correct direction and converter operates in inductive mode.

t2: At t2, LG turns off for the second time. CSNEG is low, indicating that the current is flowing in the wrong direction (the low-side MOSFET body diode is conducting), and the converter is operating in capacitive mode.

SW does not go high until the current returns to the correct polarity. DT stays high and V_{OSC} is stopped, preventing the other MOSFET from turning on. This prevents capacitive switching.

t3: At t3, the current returns to the correct polarity, and the other MOSFET turns on after the dV/dt current is detected.

Between t2 and t5, the correct current polarity cannot be detected, meaning there is so little current that SW cannot be pulled up or down.

Eventually, the timer (t_{CMP}) for CMP expires, and the other MOSFET is forced to turn on (see Figure 11).

If capacitive mode operation is detected, the V_{SS} control signal goes high, turning on an internal transistor to discharge C_{SS} after a blanking delay of t_{DMAX} (typically 1.5µs). This causes the frequency to increase quickly to limit

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the output power. The V_{SS} control is reset, and soft start is activated when the first low-side gate driver is switched off after CMP. The switching frequency decreases smoothly until the control loop takes over.

Figure 10 shows CMP behavior when the output is shorted. The current polarity goes in the wrong direction when LG switches off. The CMP logic detects this capacitive mode immediately and prohibits HG from turning on, which prevents destructive capacitive switching. Once the current (I_R) returns to the correct polarity, SW ramps up, the dV/dt current is detected, and HG turns on once the ZVS condition is met.

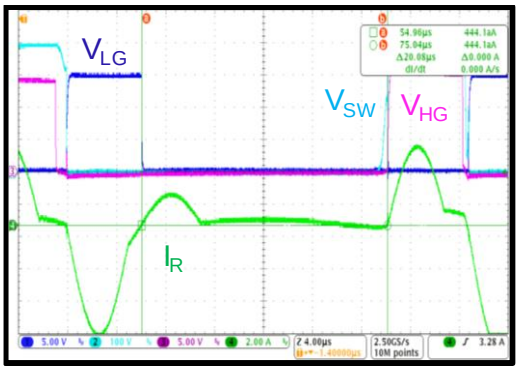

Figure 10: Capacitive Mode Protection Waveform

Over-Current Protection (OCP)

The HR1002A provides two levels of over-current protection (see Figure 11).

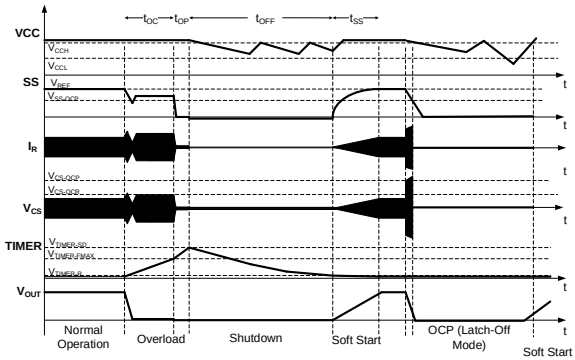

Figure 11: OCP Timing Sequence

The first level of protection occurs when the voltage on the CS pin (V_{CS}) exceeds V_{CS-OCR}. This is followed by two actions. First, the internal transistor connected between SS and GND turns on for at least 10µs, which discharges C_{SS}. This creates a sharp increase on the oscillator frequency, reducing the energy transferred to the output. Second, an internal current source (I_{TIMER}) turns on to charge the capacitor on TIMER (C_{TIMER}), ramping the TIMER voltage.

If V_{CS} drops below V_{CS-OCR} before the TIMER voltage (V_{TIMER}) reaches $V_{TIMER-FMAX}$, both C_{SS} discharging and C_{TIMER} charging are stopped. The converter resumes normal operation.

t_{OC} is the time for V_{TIMER} to rise from 0V to $V_{TIMER-FMAX}$. t_{OC} is also a delay time for over-current regulation. There is not a simple relationship between t_{OC} and C_{TIMER}. Select C_{TIMER} based on experimental results. Based on experiments, C_{TIMER} may increase the operating time by 100ms.

If V_{CS} still exceeds V_{CS-OCR} after V_{TIMER} reaches $V_{TIMER-FMAX}$, C_{SS} is discharged completely. Simultaneously, I_{TIMER} continues to charge C_{TIMER} until V_{TIMER} reaches $V_{TIMER-SD}$, and then turns off all gate drivers.

Calculate the time for V_{TIMER} to rise from $V_{TIMER-FMAX}$ to $V_{TIMER-SD}$ (t_{OP}) with Equation (11):

$$t_{OP} = 10^4 \times C_{TIMER} \quad (11)$$

The IC maintains the condition until V_{TIMER} decreases to $V_{TIMER-R}$, and then the IC restarts. Calculate this time period with Equation (12):

$$t_{OFF} = R_{TIMER} \times C_{TIMER} \times \ln\frac{V_{TIMER-SD}}{V_{TIMER-R}} \approx 2.5 \times R_{TIMER} \times C_{TIMER} \quad (12)$$

The second level of over-current protection is triggered when V_{CS} reaches V_{CS-OCP}. Typically, this condition occurs when V_{CS} continues to rise during a short circuit. Once V_{CS} reaches V_{CS-OCP}, the HR1002A does not stop switching immediately, and C_{SS} is continuously discharged by an internal transistor. If V_{CS} remains above V_{CS-OCP} until V_{SS} drops below V_{SS-OCP}, the IC shuts down and latches off (see Figure 12).

While V_{SS} is dropping, the converter resumes normal operation if V_{CS} falls below V_{CS-OCR}. This is a particular characteristic of the HR1002A, and prevents instantaneous interference on CS to trigger any protection if the converter experiences a surge or other transient waves. Once this is triggered, it does not reset until VCC drops below the under-voltage lockout (UVLO) threshold.

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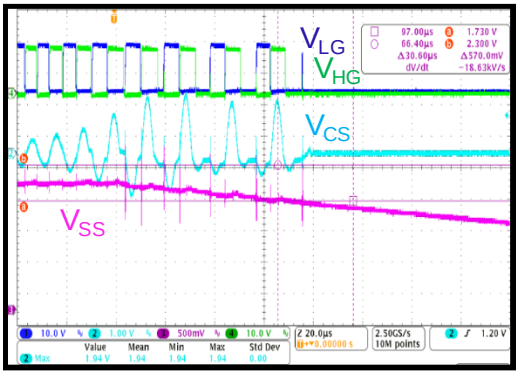

Figure 12: SCP Waveform

OCP limits the energy transferred from the primary side to the secondary side during an overload or short-circuit condition. Excessive power consumption due to high continuous currents can damage the secondary-side windings and rectifiers. TIMER provides additional protection to reduce the average power consumption. When OCP is triggered (except when V_{CS} > V_{CS-OCP}), the converter enters a hiccup-like protection mode that operates intermittently.

Current Sensing

There are two current-sensing methods: lossless current sensing and current sensing with a current-sense resistor.

Generally, lossless current sensing is used in high-power applications (see Figure 13).

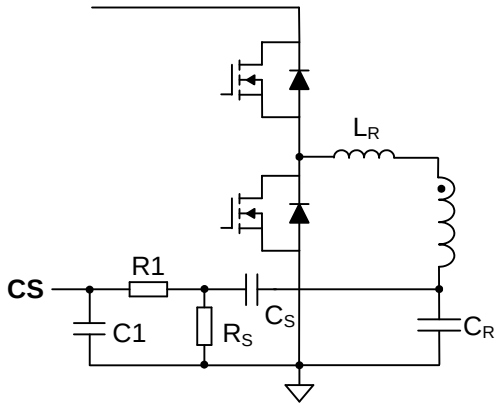

Figure 13: Current Sensing with a Lossless Network

To design a lossless current sensing network, estimate C_S with Equation (13):

$$C_S \le \frac{C_R}{100} \quad (13)$$

Calculate R_S with Equation (14):

$$R_S < \frac{V_{CS-OCR}}{I_{RPK}} \times (1 + \frac{C_R}{C_S}) \quad (14)$$

Where I_{RPK} is the peak current of the resonant tank at a low input voltage and full load. Calculate I_{RPK} with Equation (15):

$$I_{RPK} = \sqrt{(\frac{N_{PS} \times V_O}{4 \times L_M \times f_{SW}})^2 + (\frac{I_O \times \pi}{2 \times N_{PS}})^2} \quad (15)$$

Where N_{PS} is the turns ratio of the transformer, I_O is the output current, V_O is the output voltage, f_{SW} is the switching frequency, and L_M is the magnetizing inductance.

For capacitive mode detection under no-load or light-load conditions, R_S should fulfill the condition estimated with Equation (16):

$$R_S > \frac{|V_{CSPR}|}{I_M} \times (1 + \frac{C_R}{C_S}) \quad (16)$$

Under some conditions, especially if a large L_M is used, it can be difficult to fulfill both Equation (14) and Equation (16). The IC operates without CMP functionality under light loads if it is not restricted by the calculations from Equation (16).

The R1 and C1 network attenuates the switching noise on CS. The time constant should be about 100ns.

An alternate solution uses a current-sense resistor placed in series with the resonant tank (see Figure 14). This method simplifies the design but results in power loss on the current-sense resistor.

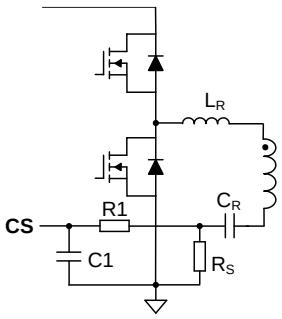

Figure 14: Current Sensing with a Current-Sense Resistor

Calculate the value of the current-sense resistor with Equation (17):

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$$R_S = \frac{V_{CS-OCR}}{I_{RPK}} \quad (17)$$

Input Voltage Sensing (BI/BO)

The HR1002A stops switching if the input voltage drops below a specified value, and restarts when the input voltage returns to normal. This function guarantees that the resonant half-bridge converter always operates within the specified input voltage range. The IC senses the voltage on the BO pin (V_{BO}) through the tap of a resistor divider connected to the rectified AC voltage or the PFC output.

Figure 15 shows the line-sensing internal block diagram.

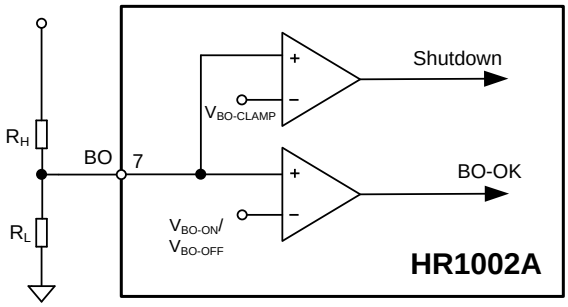

Figure 15: Input Voltage Sensing Block

If V_{BO} exceeds V_{BO-ON}, the IC provides the gate driver outputs. The IC does not stop the gate driver until V_{BO} drops below V_{BO-OFF}.

For the half-bridge's minimum operation input voltage ($V_{BUS-MIN}$), select a value for R_H that can sufficiently reduce power consumption at no load. Then calculate R_L with Equation (18):

$$R_L = R_H \times \frac{V_{BO-OFF}}{V_{BUS-MIN} - V_{BO-OFF}} \quad (18)$$

For additional protection, the IC shuts down when V_{BO} exceeds the internal clamp voltage ($V_{BO-CLAMP}$). When V_{BO} is between V_{BO-ON} and $V_{BO-CLAMP}$, the IC operates normally.

Burst Mode Operation

Under light-load or no-load conditions, the maximum frequency limits the resonant half-bridge switching frequency. To control the output voltage and limit power consumption, the HR1002A enables compatible converters to operate in burst mode. This greatly reduces the average switching frequency, which reduces the average residual magnetizing current and associated losses.

Operating in burst mode requires setting the BURST pin. If the voltage on BURST (V_{BUR}) drops below the internal threshold (V_{BURST}), the HR1002A shuts down the HG and LG outputs, leaving only the 2V reference voltage on FSET and SS to retain the previous state and minimize the power consumption. When V_{BUR} exceeds V_{BURST} by 30mV ($V_{BURST-HYS}$), the HR1002A resumes normal operation.

Based on the burst mode operating principle, BURST must be connected to the feedback loop. Figure 16 shows a typical circuit connecting BURST to the feedback signal for narrow input voltage range applications.

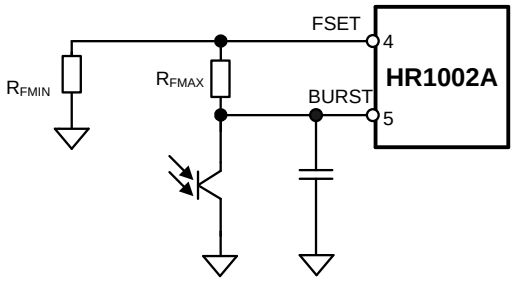

Figure 16: Burst Mode Operation Set-Up

In addition to setting the oscillator maximum frequency at start-up, R_{FMAX} determines the maximum burst mode frequency. After confirming f_{MAX}, calculate R_{FMAX} with Equation (19):

$$R_{FMAX} = \frac{3}{8} \times \frac{R_{FMIN}}{\frac{f_{MAX}}{f_{MIN}} - 1} \quad (19)$$

f_{MAX} corresponds to a load point (P_{BURST}), where the peak current flowing through the transformer is too low to cause audible noise.

As a property of the resonant circuit, the input voltage determines the switching frequency. This means P_{BURST} has a large variance across the wide input voltage range. To stabilize P_{BURST} across the input range, use a circuit to insert the input voltage signal into the feedback loop (see Figure 17).

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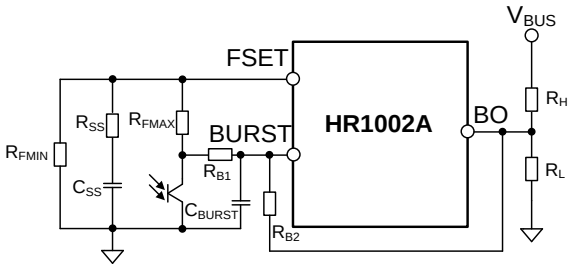

Figure 17: Burst Mode Set-Up for a Wide Input Voltage Range

R_{B1} and R_{B2} in Figure 19 correct against the wide input voltage range. Select both resistors based on experimental results. The total resistance of R_{B1} and R_{B2} should exceed R_H to minimize the effect on V_{BO}. During burst mode, when the load is below P_{BURST}, the switching frequency is clamped at the maximum frequency. The output voltage must exceed the setting value, which increases the current flowing through the optocoupler. Therefore, the voltage on R_{FMAX} rises due to the increased phototransistor current. Then V_{BUR} drops below V_{BURST}, triggering the gate signal to turn off. Until the output voltage falls below the setting value, the current flow through the optocoupler decreases, causing V_{BUR} to rise. When V_{BUR} exceeds V_{BURST} + 30mV ($V_{BURST-HYS}$), the IC restarts to generate the gate signal. The IC operates in this mode under no-load or light-load conditions to decrease average power consumption.

Latch-Off

The HR1002A provides a simple latch-off function through LATCH. Applying an external voltage over V_{LATCH} causes the IC to enter a latched shutdown. After the IC is latched, its consumption drops (see the residual current in the Electrical Characteristics section on page 5). Resetting the IC requires dropping V_{CC} below the under-voltage lockout (UVLO) threshold (see Figure 18).

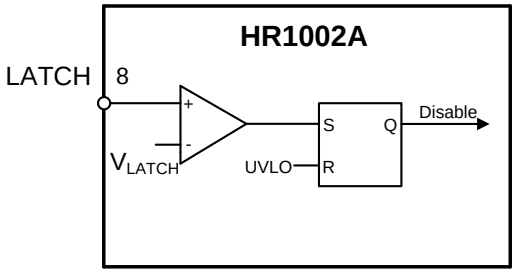

Figure 18: Latch-Off Function Block

High-Side Gate Driver (HG)

The external BST capacitor provides energy to the high-side gate driver (HG). An integrated bootstrap diode charges this capacitor through VCC. This diode allows the BST capacitor to charge when the low-side MOSFET (S_1) turns on (see Figure 1 on page 16).

To provide enough gate driver energy (considering the BST capacitor charge time), use a 100nF to 470nF capacitor for the BST capacitor. It is recommended to use an external diode connecting VCC to BST for fast start-up, especially when using a large BST capacitor (≥330nF).

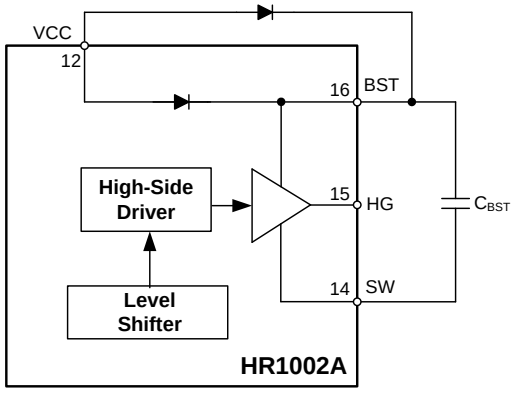

Figure 19: High-Side Gate Driver

Low-Side Gate Driver (LG)

The low-side gate driver (LG) provides the gate driver signal for the external low-side MOSFET (S_1) (see Figure 1 on page 16). The maximum voltage on LG is 16V. Under certain conditions, a large voltage spike occurs on LG due to oscillations from the long gate driver wire, the MOSFET parasitic capacitance, or the small gate driver resistor. This voltage spike is dangerous for LG, so it is recommended to place a 15V Zener diode close to LG and GND (see Figure 20).

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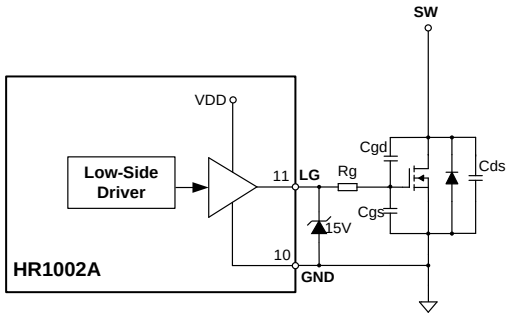

Figure 20: Low-Side Gate Driver

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APPLICATION INFORMATION

The HR1002A is designed to minimize power loss and achieve a suitable peak gain that ensures a wider input voltage range. The conduction and switching losses are related to the magnetizing inductance (L_M). The following design methodology is based on the achievable peak gain, as well as h and Q combinations. h is the ratio for L_M, L_R is the resonant inductance, and Q is the quality factor.

Frequency Domain Analysis of LLC-SRC

First-harmonic approximation (FHA) is normally used to simplify calculations by assuming that the input-output power transfer is due to first order harmonics of the fundamental Fourier series of the currents and voltages. Figure 21 shows the LLC-SRC circuit simplified via FHA.

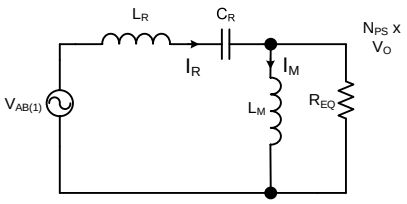

Figure 21: Simplified LLC-SRC Circuit

The fundamental of the Fourier component analysis of the input voltage can be calculated with Equation (20):

$$V_{ab(1)} = \frac{2}{\pi} \times V_{IN} \times \sin(2\pi \times f_{SW} \times t) \quad (20)$$

Where V_{IN} is the input voltage of LLC's half-bridge.

The circuit on secondary side of transformer can be reflected to primary side. The equivalent resistance (R_{EQ}) can be calculated with Equation (21):

$$R_{EQ} = N_{PS}^2 \times \frac{8}{\pi^2} \times R_L \quad (21)$$

Where R_L is the load impedance, estimated with Equation (22):

$$R_L = \frac{V_O}{I_O} \quad (22)$$

Based on the simplified circuit of LLC topology, the voltage gain of the output and input can be calculated with Equation (23):

$$M(h,Q,f_N) = \frac{1}{\sqrt{(1+\frac{1}{h}-\frac{1}{h \times f_N^2})^2 + Q^2 \times (f_N - \frac{1}{f_N})^2}} \quad (23)$$

Where the parameters are defined below.

The inductor ratio (h) can be calculated with Equation (24):

$$h = \frac{L_M}{L_R} \quad (24)$$

The normalized frequency (f_N) can be estimated with Equation (25):

$$f_N = \frac{f_{SW}}{f_R} \quad (25)$$

The quality factor (Q) can be calculated with Equation (26):

$$Q = \frac{\sqrt{L_R / C_R}}{R_{EQ}} \quad (26)$$

There are three resonant components in the LLC-SRC topology, which lead to two inherent resonant frequencies: f_R and f_M.

The first resonant frequency (f_R) can be calculated with Equation (27):

$$f_R = \frac{1}{2\pi \times \sqrt{L_R \times C_R}} \quad (27)$$

The second resonant frequency (f_M) can be estimated with Equation (28):

$$f_M = \frac{1}{2\pi \times \sqrt{(L_R + L_M) \times C_R}} \quad (28)$$

A benefit of LLC-SRC is that it can achieve ZVS not only when $f_{SW} \geq f_R$, but also when $f_M < f_{SW} < f_R$. Figure 22 shows a gain curve with different h and Q combinations. The voltage gain is always 1 when $f_N = 1$. This means that the switching frequency is equal to the series resonant frequency, calculated with Equation (29):

$$f_{SW} = f_R \quad (29)$$

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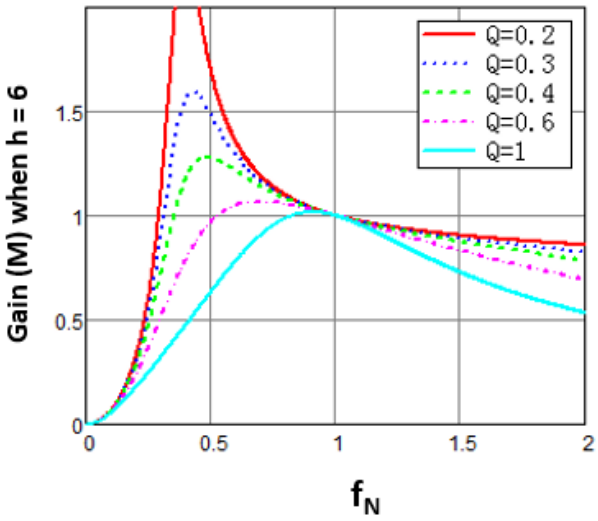

Figure 22: Gain Curve vs. h and Q

Setting the Transformer Turning Ratio

Generally, the LLC-SRC switching frequency is designed at the resonant frequency (f_R), at the normal input voltage to optimize efficiency.

Due to unit gain at the resonant frequency (f_R), the turn ratio only depends on the input and output voltages. Calculate turn ratio for half-bridge applications with Equation (30):

$$N_{PS} = \frac{V_{IN_DC_NOM} / 2}{V_O} \quad (30)$$

Calculate the turn ratio for full-bridge applications with Equation (31):

$$N_{PS} = \frac{V_{IN_DC_NOM}}{V_O} \quad (31)$$

Where V_O is the output voltage, and $V_{IN_DC_NOM}$ is the typical DC input voltage.

Setting the Maximum and Minimum Gain

The maximum and minimum gain can be estimated with Equation (32) and Equation (33), respectively:

$$M_{MAX} = \frac{V_{O_MAX} \times N_{PS}}{V_{IN_DC_MIN} / 2} \quad (32)$$

$$M_{MIN} = \frac{V_{O_MIN} \times N_{PS}}{V_{IN_DC_MAX} / 2} \quad (33)$$

Where V_{O_MAX} is the maximum output voltage, V_{O_MIN} is the minimum output voltage, $V_{IN_DC_MAX}$ is the maximum input voltage, and $V_{IN_DC_MIN}$ is the minimum input voltage.

Setting h and Q

Each gain curve has a peak gain (see Figure 22). Figure 23 illustrates the peak gain with different h and Q combinations. Depending on the required maximum peak, select the optimal h and Q combination. Note that a higher h provides a higher magnetizing inductance (L_M), which results in higher efficiency.

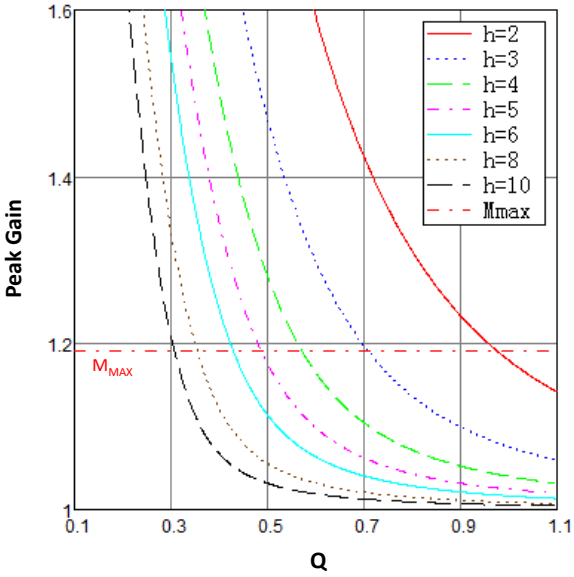

Figure 23: Peak Gain vs. h and Q

Setting L_R, C_R, and L_M

Other parameters can be calculated once the values for h and Q are set. C_R can be calculated with Equation (34):

$$C_R = \frac{1}{2\pi \times f_R \times R_{EQ} \times Q} \quad (34)$$

L_R can be estimated with Equation (35):

$$L_R = \frac{1}{(2\pi \times f_R)^2 \times C_R} \quad (35)$$

The magnetizing inductance (L_M) can be calculated with Equation (36):

$$L_M = h \times L_R \quad (36)$$

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Setting the Maximum Magnetizing Inductance

To ensure the ZVS turn-on condition, the MOSFET junction capacitor should be discharged during the maximum dead time. The discharge current equals the peak magnetizing current, which is inversely proportional to L_M. This relationship is expressed with Equation (37):

$$\frac{I_M}{2} \times t_{DEAD} = 2 \times C_{EQ} \times V_{IN} \quad (37)$$

Where I_M is the peak magnetizing current during dead time, t_{DEAD} is the dead time, C_{EQ} is the MOSFET's equivalent output capacitance, and V_{IN} is the input of the LLC stage. I_M can be estimated with Equation (38):

$$I_M = \frac{V_{IN}}{8 \times L_M \times f_{MAX}} \quad (38)$$

The conditions that L_M must satisfy in a half-bridge topology can be estimated with Equation (39):

$$L_M < \frac{t_{DEAD}}{16 \times C_{EQ} \times f_{MAX}} = \frac{t_{DMAX}}{16 \times C_{EQ} \times f_{MAX}} \quad (39)$$

TRANSFORMER DESIGN

Setting the RMS Value

The primary-side RMS current can be estimated with Equation (40):

$$I_{RMS_PRI} = \frac{V_O \times \sqrt{4\pi^2 + N_{PS}^4 \times R_L^2 \times \frac{T_R^2}{L_M^2}}}{4\sqrt{2} \times N_{PS} \times R_L} \quad (40)$$

Where $T_R = 1/f_R$.

The primary-side peak current (I_{PK_PRI}) can be estimated with Equation (41):

$$I_{PK_PRI} = \sqrt{2} \times I_{RMS_PRI} \quad (41)$$

The secondary-side RMS current can be calculated with Equation (42):

$$I_{RMS_SEC} = \sqrt{3} \frac{V_O \times \sqrt{12\pi^4 + \frac{5\pi^2 - 48}{L_M^2} N_{PS}^4 \times R_L^2 \times T_R^2}}{24\pi \times R_L} \quad (42)$$

The transformer's total RMS current (I_{RMS_T}) includes the current through the primary side and the current reflected from the secondary side. The total RMS current can be calculated with Equation (43):

$$I_{RMS_T} = I_{RMS_PRI} + \frac{I_{RMS_SEC}}{N_{PS}} \quad (43)$$

Selecting the Core Size

Select an optimal core that considers the specific output power value at the operating frequency (typically ferrite for most applications). The core area product (AP) is the core's magnetic cross-section area multiplied by the window area available for winding. AP provides an initial estimate of the core size for a given application. A rough indication of the required A_E x A_W (cm^4) size can be estimated with Equation (44):

$$AP_T = \left(\frac{L_M \times I_{PK_PRI} \times I_{RMS_T} \times 10^4}{B_{MAX} \times K_U \times K_J}\right)^{\frac{4}{3}} \ cm^4 \quad (44)$$

Where K_U is winding factor (typically 0.2 to 0.3), K_J is the current-density coefficient (typically $600A/cm^2$), and B_{MAX} is the flux density. B_{MAX} should be between 0.1T and 0.3T for a ferrite core, which is based on the tradeoff between core loss and winding loss.

Selecting the Primary Side and Secondary Side Turns

With a defined core size, the turns of the secondary side can be calculated with Equation (45):

$$N_S = \frac{V_O}{4 \times f_R \times B_{MAX} \times A_E} \quad (45)$$

Where V_O is the output voltage, B_{MAX} is the allowable flux density (generally selected according to the core loss), and A_E is the effective area cross sectional core,

The primary winding (N_P) can be estimated with Equation (46):

$$N_P = N_{PS} \times N_S \quad (46)$$

Selecting the Wire Size

After the winding turns are determined, select

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the wire size to minimize the winding conduction loss. The winding loss depends on the RMS current value, transformer structure, and the wire's length and cross section.

Determine the wire size through the winding RMS current.

The required wire size for the primary and secondary side can be calculated with Equation (47) and Equation (48), respectively:

$$S_{PRI} = \frac{I_{RMS_PRI}}{K_J} \quad (47)$$

$$S_{SEC} = \frac{I_{RMS_SEC}}{K_J} \quad (48)$$

Due to the skin effect and proximity effect of the conductor, the diameter of the wire should be below (2 x Δd) (where Δd is the skin-effect depth). Δd can be calculated with Equation (49):

$$\Delta d = \sqrt{\frac{1}{\pi \times f_s \times \mu_0 \times \sigma}} \quad mm \quad (49)$$

Where μ_0 is the vacuum's permeability ($4\pi x10^{-7}$H/m), and σ is the wire's conductivity (e.g. for copper wires, σ is typically $6x10^7$S/m).

If the required winding size exceeds Δd, use multiple strands of thinner wire or Litz wire to minimize the AC resistance. The effective cross-section area of multiple wire strands or the Litz wire must meet the requirement set by the current density.

After determining the wire size, determine whether the window area with the selected core can accommodate the windings.

Calculate the window area required by each winding and include the area for inter-winding insulation, bobbin, and spaces existing between the turns. Select a fill factor (the winding area to the whole window area of the core) below 1 due to the inter-winding insulation and spaces between turns. For the best results, select a fill factor no greater than 30%. Use smaller fill factors for transformers with multiple outputs.

Compare the total window area required to the available window area of a selected core based on these considerations. If the required window area exceeds the selected core area, either reduce the wire size or select a larger core. Note that reducing the wire size increases the copper loss of the transformer.

Air Gap

Using the selected core and winding turns, calculate the air gap of the core with Equation (50):

$$l_{G_TR} = \frac{\mu_0 \times N_P^2 \times A_E}{L_M} \quad (50)$$

Selecting the Inductor

The AP solution can be used to select an inductor. AP_L can be estimated with Equation (51):

$$AP_L = \left(\frac{L_R \times I_{PK_PRI} \times I_{RMS_PRI} \times 10^4}{B_{MAX} \times K_U \times K_J}\right)^{\frac{4}{3}} \quad cm^4 \quad (51)$$

With the defined core size, estimate the turns of the inductor with Equation (52):

$$N_L = \frac{L_R \times I_{PK_PRI}}{B_{MAX} \times A_E} \quad (52)$$

The required wire size for the inductor should be equal to S_{PRI}.

The air gap of the inductor's core can be calculated with Equation (53):

$$l_{G_LR} = \frac{\mu_0 \times N_L^2 \times A_E}{L_R} \quad (53)$$

Setting the Maximum and Minimum Switching Frequencies

The minimum and maximum switching frequencies can be based on the gain curve (see Figure 24). The red gain curve is the full load Q curve, and the blue gain curve is the light-load Q curve (e.g. a 20% load). The intersection between the maximum gain requirement (M_{MAX}) and full-load Q curve generate the minimum frequency (f_{MIN}). The intersection between the minimum gain requirement (M_{MIN}) and light-load Q curve generate the maximum frequency (f_{MAX}).

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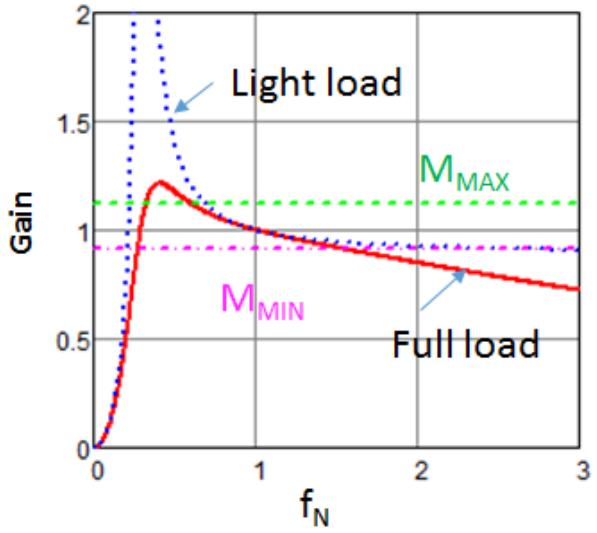

Figure 24: Frequency Range vs. Gain Curve

C_T should be selected (typically 330pF with ±5% capacitance tolerance) depending on the maximum source current capability (2mA). Design R_{FMIN} and R_{FMAX} such that the selected oscillator frequency can cover the regulatory range, from the minimum frequency (minimum input and maximum load), to the maximum frequency (maximum input and minimum load).

Using the minimum frequency, R_{FMIN} can be calculated with Equation (54):

$$R_{FMIN} = \frac{1}{3 \times C_T \times f_{MIN}} \quad (54)$$

R_{FMAX} determines the maximum frequency, and when the controller enters burst mode operation at the minimum load.

R_{FMAX} can be estimated with Equation (55):

$$R_{FMAX} = \frac{3}{8} \times \frac{R_{FMIN}}{\frac{f_{MAX}}{f_{MIN}} - 1} \quad (55)$$

Calculate R_{SS} with Equation (56):

$$R_{SS} = \frac{R_{FMIN}}{\frac{f_{START}}{f_{MIN}} - 1} \quad (56)$$

Estimate C_{SS} with Equation (57):

$$C_{SS} = \frac{3 \times 10^{-3}}{R_{SS}} \quad (57)$$

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PCB Layout Guidelines

The PCB layout is critical for stable operation and EMI performance. If the layout is not properly designed, the device can malfunction due to noise coupling. For the best results, refer to Figure 25 and follow the guidelines below:

1. Make the high-current loop as small as possible.
2. Do not place the IC in a power loop.
3. Make the areas of high dV/dt junctions (e.g. the drain of the external primary MOSFET) as small as possible. Place the IC and control circuits far away from these areas.
4. Separate the reference ground of the IC and control signals circuit from the ground of the power loop. Then connect this signal ground to the ground of the output capacitor with a single-point junction.
5. Connect the VCC-GND capacitor close to the IC.
6. Connect the following capacitors and resistors close to the IC: R_{SS}, C_{SS}, C_T, R_{FMIN}, R_{FMAX}, C_{BURST}, C_{BO}, and C_1.
7. Connect the slope-sensing capacitor C_{HBVS} close to the HBVS pin.
8. Connect the feedback and ground of the optocoupler to the HR1002A with two separate wires in parallel.
9. If the PFC stage is connected to a cascading DC/DC stage, separate both GNDs with an output capacitor, so that the GND noises do not interfere with one another.

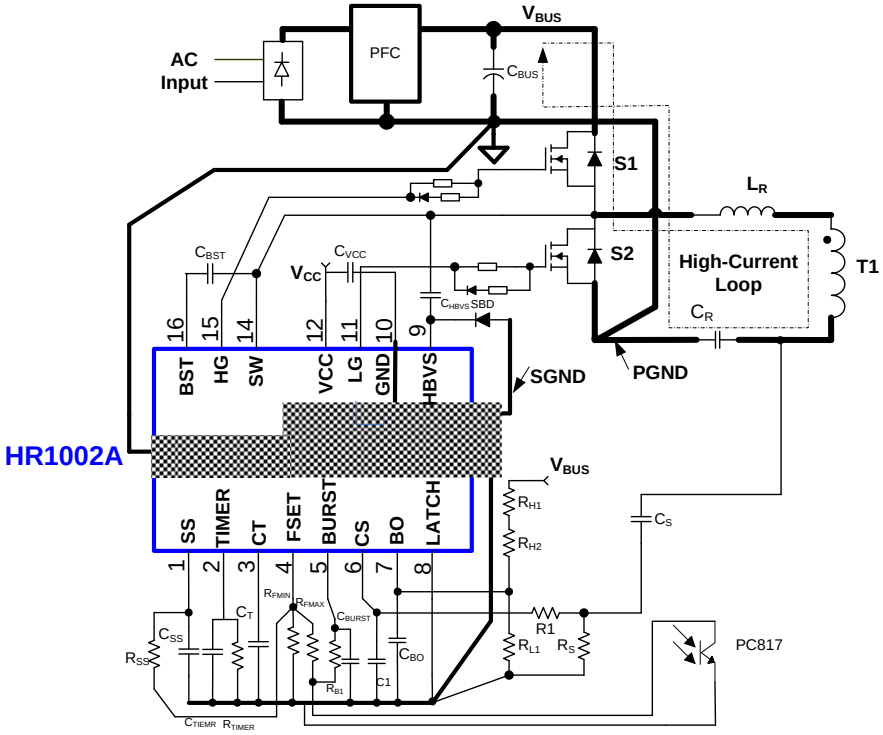

Figure 25: Recommended PCB Layout

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DESIGN EXAMPLE

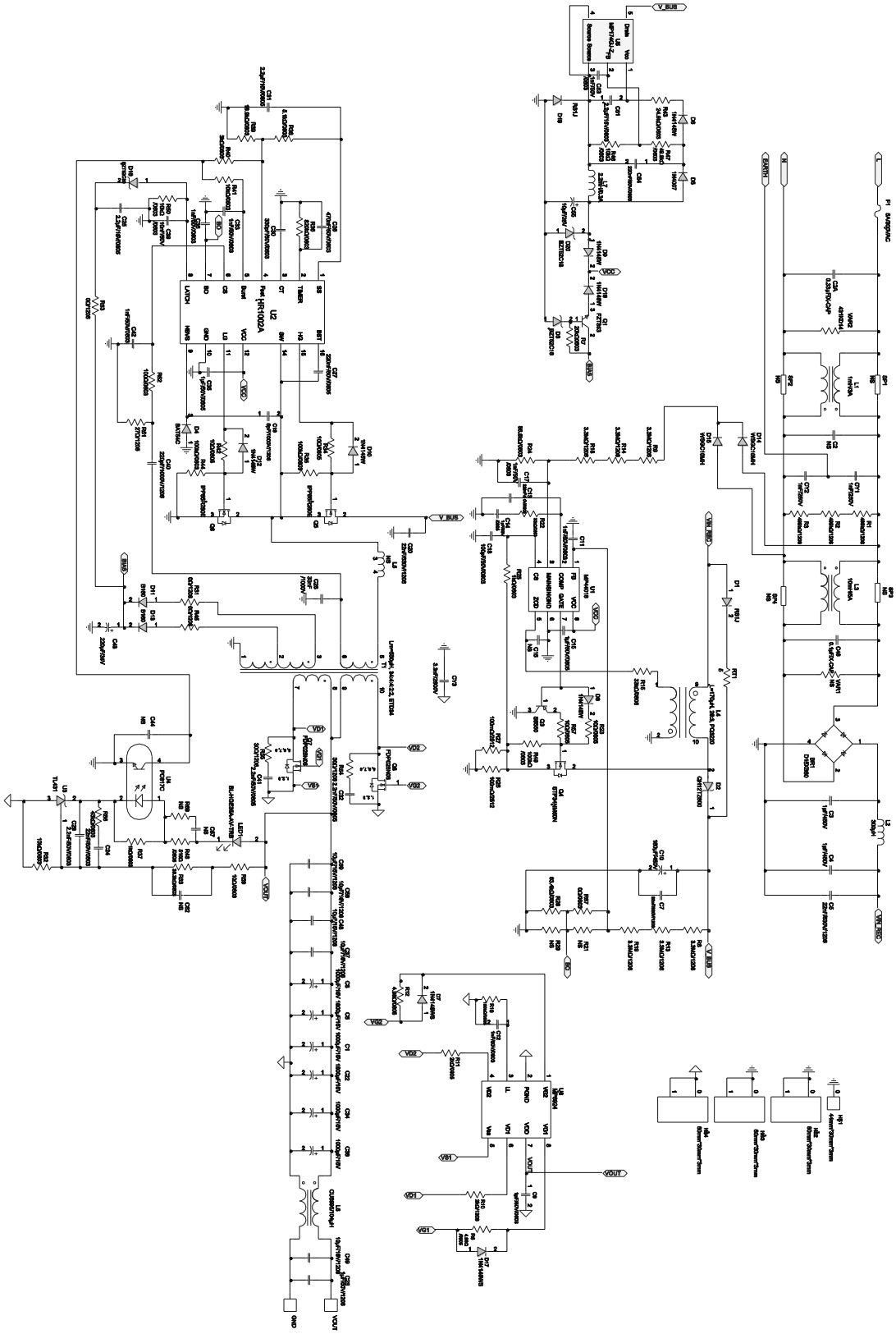

Figure 26: Design Example for a 12V/20A Output

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CONTROL FLOWCHART

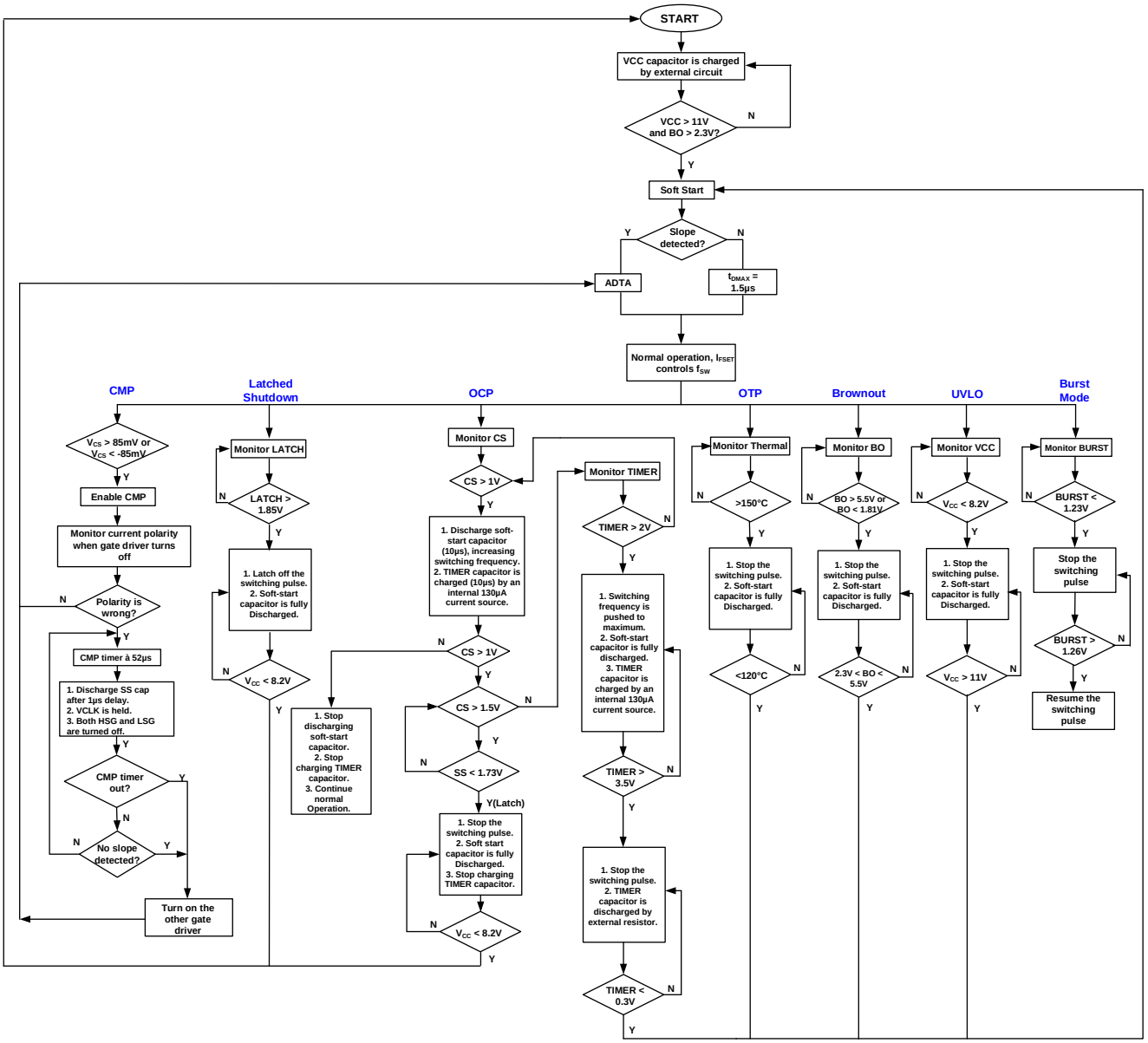

Figure 27: Control Flowchart

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TYPICAL APPLICATION CIRCUIT

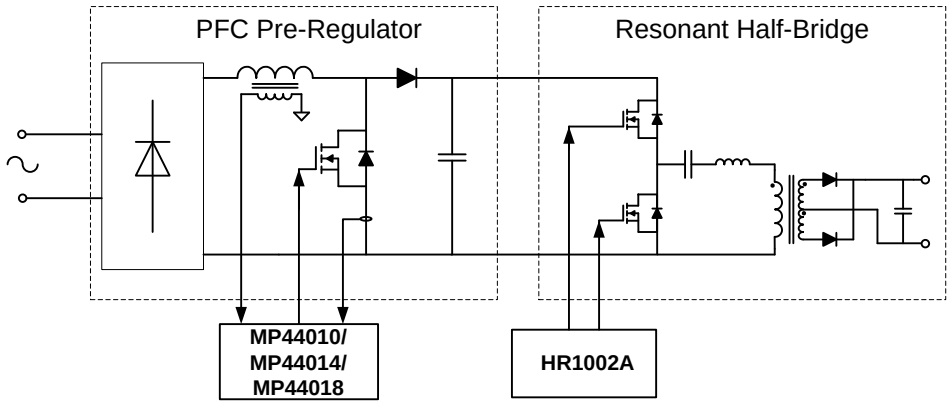

Figure 28: HR1002A Typical Application Circuit

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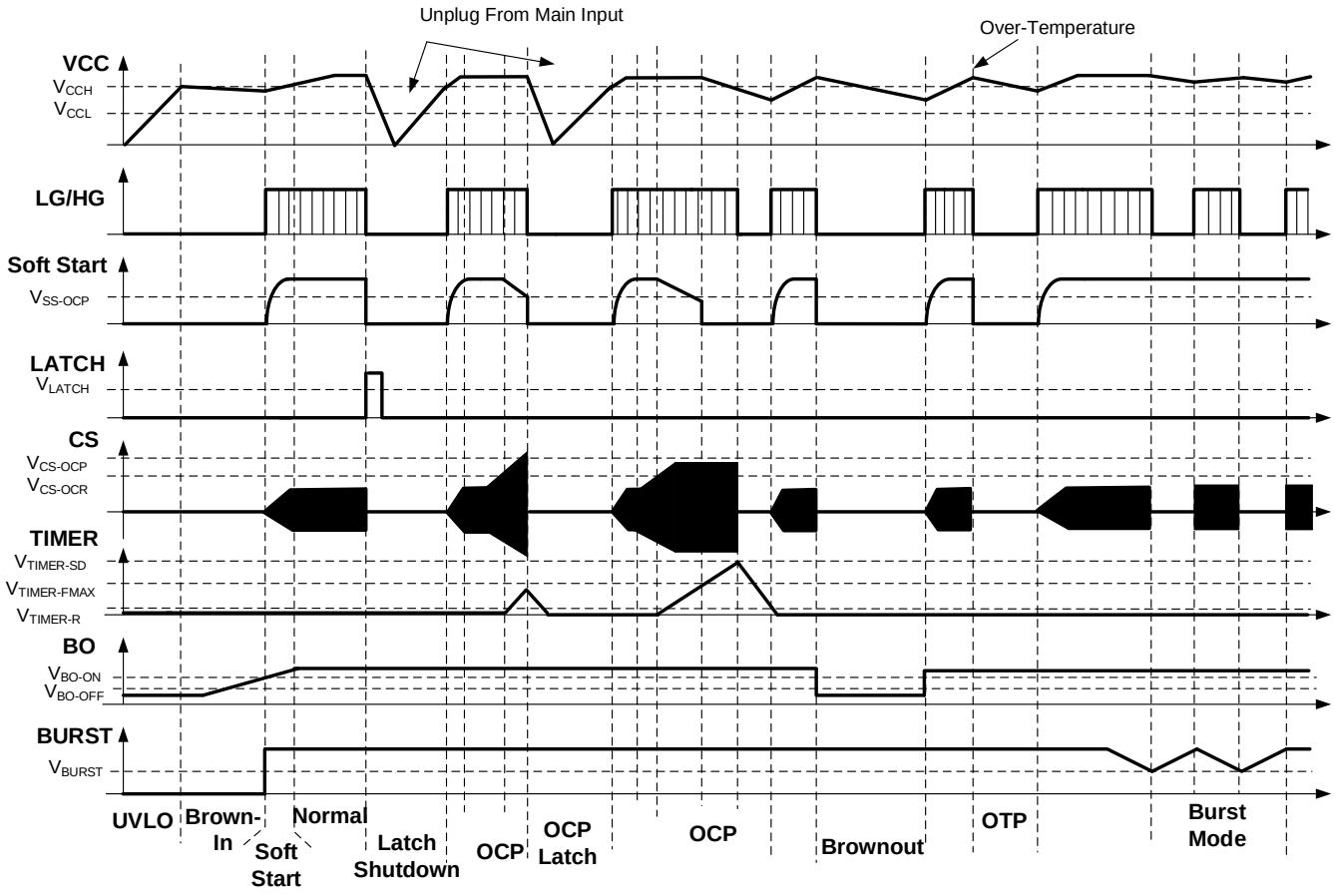
SYSTEM TIMING



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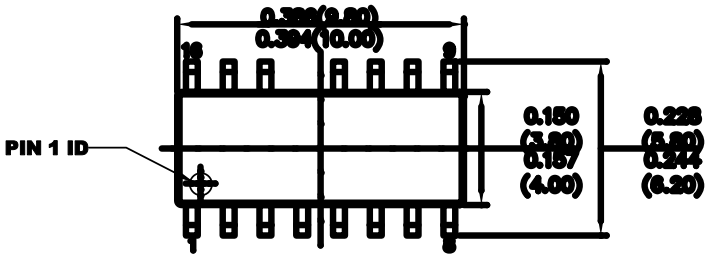
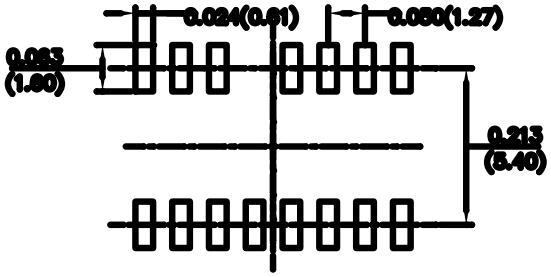
PACKAGE INFORMATION

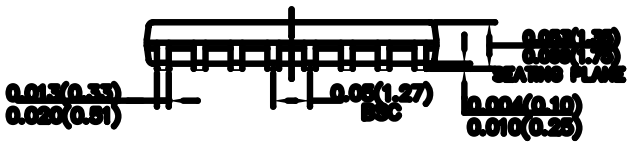
SOIC16-15



TOP VIEW

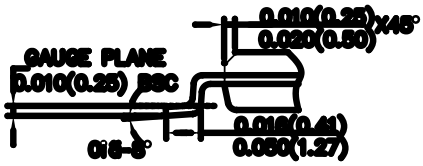


RECOMMENDED LAND PATTERN



FRONT VIEW

SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BC.
6) DRAWING IS NOT TO SCALE.

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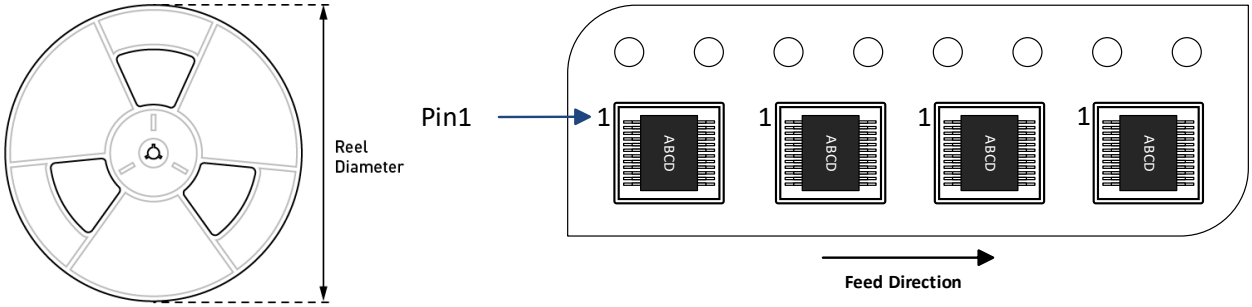
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
HR1002AGSE –Z	SOIC16-15	2500	50	N/A	13in	16mm	8mm

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Revision History

Revision #	Revision Date	Description	Pages Updated
1.0	10/13/2020	Initial Release	-

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