DESCRIPTION
The HFC0511 is a fixed-frequency, current-mode controller with internal slope compensation specifically designed for medium-power, offline, flyback, switch-mode power supplies. The HFC0511 is a highly efficient green-mode controller. At light loads, the controller freezes the peak current and reduces its switching frequency down to 27kHz to achieve excellent light-load efficiency. At very light loads, the controller enters burst mode to achieve very low standby power consumption.

The HFC0511 offers frequency jittering to help dissipate energy generated by the conducted noise.

The HFC0511 employs an over-power compensation function to narrow the difference of the over-power protection point between the low line and high line.

The HFC0511 also has an X-cap discharge function to discharge the X-capacitor when the input is unplugged. This helps lower the power at no load.

Full protection features include thermal shutdown, VCC under-voltage lockout (UVLO), overload protection (OLP), over-voltage protection (OVP), and brown-out protection.

The HFC0511 is available in a SOIC8-7A package.

FEATURES
• Fixed-Frequency, Current-Mode Control with Internal Slope Compensation
• Frequency Foldback down to 27kHz at Light Load
• Burst Mode for Low Standby Power Consumption, Meeting EuP Lot 6
• Frequency Jitter to Reduce EMI Signature
• X-Cap Discharge Function
• Adjustable Over-Power Compensation
• Internal High-Voltage Current Source
• VCC Under-Voltage Lockout (UVLO) with Hysteresis
• Brown-Out Protection on HV
• Overload Protection with Programmable Delay
• Thermal Shutdown (Auto- Restart with Hysteresis)
• Latch-Off for External Over-Voltage Protection (OVP) and Over-Temperature Protection (OTP) on TIMER
• Latch-Off for VCC Over-Voltage Protection (OVP)
• Short-Circuit Protection (SCP)
• Programmable Soft Start (SS)
• Available in a SOIC8-7A Package

APPLICATIONS
• AC/DC Power for Small and Large Appliances
• AC/DC Adapters for Notebook Computers, Tablets, and Smart Phones
• Offline Battery Chargers
• LCD TVs and Monitors

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TYPICAL APPLICATION

Input
85 ~ 265 Vac

Output

T1

HV

FB

CS

GND

HFC0511

DRV

VCC

TYPICAL APPLICATION

HFC0511 – FIXED-FREQUENCY FLYBACK CONTROLLER W/ ULTRA-LOW NO LOAD POWER CONSUMPTION

TYPICAL APPLICATION

HFC0511

8

6

5

4

3

2

1

TIMER

HV

FB

CS

GND

DRV

VCC

HFC0511

Output

T1

Input
85 ~ 265 Vac
ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Part Number*</th>
<th>Package</th>
<th>Top Marking</th>
</tr>
</thead>
<tbody>
<tr>
<td>HFC0511GS</td>
<td>SOIC8-7A</td>
<td>See Below</td>
</tr>
</tbody>
</table>

* For Tape & Reel, add suffix –Z (e.g. HFC0511GS–Z)

TOP MARKING

HFC0511

LLLLLLLL

MPSYWW

HFC0511: First seven digits of the part number
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

PACKAGE REFERENCE

TOP VIEW

![Diagram of SOIC8-7A package with pin numbers and labels]

- TIMER 1
- FB 2
- CS 3
- GND 4
- O 8 (HV)
- 6 (VCC)
- 5 (DRV)

SOIC8-7A
ABSOLUTE MAXIMUM RATINGS (1)
HV ............................................. -0.7V to 700V
VCC, DRV to GND ...................... -0.3V to 30V
FB, TIMER, CS to GND ............... -0.3V to 7V
Continuous power dissipation (T_A = +25°C) (2) ........................................... 1.3W
Junction temperature ................. 150°C
Lead temperature ..................... 260°C
Storage temperature ................. -60°C to +150°C
ESD capability human body model (except HV and DRV) ................................... 4.0kV
ESD capability human body model (DRV) ........................................................... 3.5kV
ESD capability human body model (HV) ... 1.0kV
ESD capability for machine mode .......... 400V

Recommended Operation Conditions (3)
Operating junction temp. (T_J) ... -40°C to +125°C
Operating VCC range .................... 9V to 24V

Thermal Resistance (4) θJA θJC
SOIC8-7A..................................... 96........ 45 ... °C/W

NOTES:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θJA, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A)/θJA. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.
### ELECTRICAL CHARACTERISTICS

VCC = 18V, Tj = -40°C ~ 125°C, min and max values are guaranteed by characterization, typical value is tested under 25°C, unless otherwise specified.

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<tr>
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<th>Typ</th>
<th>Max</th>
<th>Unit</th>
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</thead>
<tbody>
<tr>
<td>Start-Up Current Source (HV)</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Supply current from HV</td>
<td>I_{HV, 400}</td>
<td>VCC = 12V, V_{HV} = 400V</td>
<td>1.5</td>
<td>2.8</td>
<td>3.9</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>I_{HV, 120}</td>
<td>VCC = 12V, V_{HV} = 120V</td>
<td>1.5</td>
<td>2.7</td>
<td>3.7</td>
<td>mA</td>
</tr>
<tr>
<td>Leakage current from HV</td>
<td>I_{Lk, 400}</td>
<td>VCC increases to 18V, then decreases to 14V, V_{HV} = 400V</td>
<td>1</td>
<td>16</td>
<td>28</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>I_{Lk, 200}</td>
<td>VCC increases to 18V, then decreases to 14V, V_{HV} = 200V</td>
<td>1</td>
<td>13</td>
<td>25</td>
<td>µA</td>
</tr>
<tr>
<td>Break-down voltage</td>
<td>V_{BR}</td>
<td>T_j = 25°C</td>
<td>700</td>
<td>790</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Supply Voltage Management (VCC)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>VCC increasing level at which the current source turns off</td>
<td>VCC_{OFF}</td>
<td>12.5</td>
<td>15.5</td>
<td>18</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VCC decreasing level above which soft start takes place if HV &gt; HV_{ON}</td>
<td>VCC_{SS}</td>
<td>10.5</td>
<td>12</td>
<td>13</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VCC hysteresis for brown-in detection</td>
<td>VCC_{OFF} - VCC_{SS}</td>
<td>1.35</td>
<td>3.5</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VCC decreasing level at which the current source turns on</td>
<td>VCC_{ON}</td>
<td>7.3</td>
<td>8.5</td>
<td>9.6</td>
<td>V</td>
<td></td>
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<tr>
<td>VCC UVLO hysteresis</td>
<td>VCC_{OFF} - VCC_{ON}</td>
<td>5</td>
<td>7</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VCC recharge level when protection takes place</td>
<td>VCC_{PRO}</td>
<td>4.9</td>
<td>5.5</td>
<td>6.2</td>
<td>V</td>
<td></td>
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<tr>
<td>VCC decreasing level at which the latch-off phase ends</td>
<td>VCC_{LATCH}</td>
<td>2.5</td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Internal IC consumption</td>
<td>I_{CC}</td>
<td>V_{FB} = 2V, C_{L} = 1nF, VCC = 12V</td>
<td>0.9</td>
<td>1.8</td>
<td>2.7</td>
<td>mA</td>
</tr>
<tr>
<td>Internal IC consumption, latch-off phase</td>
<td>I_{CC_{LATCH}}</td>
<td>VCC = VCC_{OFF} - 1V, T_j = 25°C</td>
<td>520</td>
<td>700</td>
<td>880</td>
<td>µA</td>
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<tr>
<td>Voltage on the VCC above which the controller latches off (OVP)</td>
<td>V_{OVP}</td>
<td>24</td>
<td>26.5</td>
<td>28.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Blanking duration on the OVP comparator</td>
<td>T_{OVP}</td>
<td>60</td>
<td></td>
<td></td>
<td>µs</td>
<td></td>
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<tr>
<td>Brown-Out</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>HV turn-on threshold voltage</td>
<td>HV_{ON}</td>
<td>V_{HV} going up, T_j = 25°C</td>
<td>95</td>
<td>107</td>
<td>119</td>
<td>V</td>
</tr>
<tr>
<td>HV turn-off threshold voltage</td>
<td>HV_{OFF}</td>
<td>V_{HV} going down, T_j = 25°C</td>
<td>86</td>
<td>97</td>
<td>110</td>
<td>V</td>
</tr>
<tr>
<td>Brown-out hysteresis</td>
<td>ΔHV</td>
<td>T_j = 25°C</td>
<td>6.5</td>
<td>10</td>
<td>13.5</td>
<td>V</td>
</tr>
<tr>
<td>Timer duration for line cycle dropout</td>
<td>T_{HV}</td>
<td>C_{TIMER} = 47nF</td>
<td>40</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>Oscillator</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Oscillator frequency</td>
<td>f_{OSC}</td>
<td>V_{FB} &gt; 1.85V, T_j = 25°C</td>
<td>125</td>
<td>130</td>
<td>135</td>
<td>kHz</td>
</tr>
<tr>
<td>Frequency jittering amplitude, in percentage of f_{OSC}</td>
<td>A_{jitter}</td>
<td>V_{FB} &gt; 1.85V, T_j = 25°C</td>
<td>±5</td>
<td>±6.5</td>
<td>±8.3</td>
<td>%</td>
</tr>
<tr>
<td>Frequency jittering entry level</td>
<td>V_{FB, JITTER}</td>
<td></td>
<td>1.95</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Frequency jittering modulation period</td>
<td>T_{jitter}</td>
<td>C_{TIMER} = 47nF</td>
<td>3.7</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
</tbody>
</table>
**ELECTRICAL CHARACTERISTICS (continued)**

VCC = 18V, TJ = -40°C ~ 125°C, min and max values are guaranteed by characterization, typical value is tested under 25°C, unless otherwise specified.

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<th>Unit</th>
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</thead>
<tbody>
<tr>
<td><strong>Current Sense</strong></td>
<td></td>
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<tr>
<td>Current-limit point</td>
<td>V\textsubscript{ILIM}</td>
<td></td>
<td>0.93</td>
<td>1</td>
<td>1.07</td>
<td>V</td>
</tr>
<tr>
<td>Short-circuit protection point</td>
<td>V\textsubscript{SCP}</td>
<td></td>
<td>1.3</td>
<td>1.47</td>
<td>1.63</td>
<td>V</td>
</tr>
<tr>
<td>Current limitation when frequency folds back</td>
<td>V\textsubscript{FOLD}</td>
<td>V\textsubscript{FB} = 1.85V</td>
<td>0.63</td>
<td>0.68</td>
<td>0.73</td>
<td>V</td>
</tr>
<tr>
<td>Current limitation when entering burst</td>
<td>V\textsubscript{IBURL}</td>
<td>V\textsubscript{FB} = 0.7V</td>
<td></td>
<td>0.11</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Current limitation when leaving burst</td>
<td>V\textsubscript{IBURH}</td>
<td>V\textsubscript{FB} = 0.8V</td>
<td></td>
<td>0.15</td>
<td></td>
<td>V</td>
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<tr>
<td>Leading edge blanking for V\textsubscript{ILIM}</td>
<td>T\textsubscript{LEB1}</td>
<td></td>
<td>350</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Leading edge blanking for V\textsubscript{SCP}</td>
<td>T\textsubscript{LEB2}</td>
<td></td>
<td>270</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Slope of the compensation ramp</td>
<td>S\textsubscript{RAMP}</td>
<td></td>
<td>18</td>
<td>25</td>
<td>32</td>
<td>mV/\mu s</td>
</tr>
<tr>
<td><strong>Feedback (FB)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Internal pull-up resistor</td>
<td>R\textsubscript{FB}</td>
<td></td>
<td>11.5</td>
<td>14</td>
<td>17</td>
<td>k\Omega</td>
</tr>
<tr>
<td>Internal pull-up voltage</td>
<td>V\textsubscript{DD}</td>
<td></td>
<td>4.3</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V\textsubscript{FB} to internal current set point division ratio</td>
<td>K\textsubscript{FB1}</td>
<td>V\textsubscript{FB} = 2V</td>
<td>2.55</td>
<td>2.8</td>
<td>3.05</td>
<td>--</td>
</tr>
<tr>
<td>V\textsubscript{FB} to internal current set point division ratio</td>
<td>K\textsubscript{FB2}</td>
<td>V\textsubscript{FB} = 3V</td>
<td>2.8</td>
<td>3.1</td>
<td>3.4</td>
<td>--</td>
</tr>
<tr>
<td>FB decreasing level at which the controller enters burst mode</td>
<td>V\textsubscript{BURL}</td>
<td></td>
<td>0.63</td>
<td>0.7</td>
<td>0.77</td>
<td>V</td>
</tr>
<tr>
<td>FB increasing level at which the controller leaves burst mode</td>
<td>V\textsubscript{BURH}</td>
<td></td>
<td>0.72</td>
<td>0.8</td>
<td>0.88</td>
<td>V</td>
</tr>
<tr>
<td><strong>Overload Protection (OLP)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FB level at which the controller enters the OLP after a dedicated time</td>
<td>V\textsubscript{OLP}</td>
<td></td>
<td>3.7</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Time duration before OLP when FB reaches protection point</td>
<td>T\textsubscript{OLP}</td>
<td>C\textsubscript{TIMER} = 47nF</td>
<td>40</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td><strong>Over-Power Compensation</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V\textsubscript{HV} to I\textsubscript{OPC} ratio</td>
<td>K\textsubscript{OPC}</td>
<td></td>
<td>0.45</td>
<td></td>
<td></td>
<td>\mu A/V</td>
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<tr>
<td>Current out of CS</td>
<td>I\textsubscript{OPC}</td>
<td>V\textsubscript{HV} = 120V, V\textsubscript{FB} = 2.5V</td>
<td>0</td>
<td></td>
<td></td>
<td>\mu A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V\textsubscript{HV} = 155V, V\textsubscript{FB} = 2.5V</td>
<td>13</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>V\textsubscript{HV} = 310V, V\textsubscript{FB} = 2.5V</td>
<td>85</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>V\textsubscript{HV} = 380V, V\textsubscript{FB} = 2.5V, TJ = 25°C</td>
<td>80</td>
<td>109</td>
<td>138</td>
<td></td>
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<tr>
<td>FB voltage below which compensation is removed</td>
<td>V\textsubscript{OPC(OFF)}</td>
<td></td>
<td>0.55</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>FB voltage above which compensation is applied fully</td>
<td>V\textsubscript{OPC(ON)}</td>
<td></td>
<td>2.2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td><strong>Frequency Foldback</strong></td>
<td></td>
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</tr>
<tr>
<td>FB voltage threshold below which frequency foldback starts</td>
<td>V\textsubscript{FB(FOLD)}</td>
<td></td>
<td>1.8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Minimum switching frequency</td>
<td>F\textsubscript{OSC(min)}</td>
<td>TJ = 25°C</td>
<td>21</td>
<td>27</td>
<td>33</td>
<td>kHz</td>
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<tr>
<td>FB voltage threshold below which frequency foldback ends</td>
<td>V\textsubscript{FB(FOLDE)}</td>
<td></td>
<td>1.0</td>
<td></td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>
ELECTRICAL CHARACTERISTICS (continued)
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<tbody>
<tr>
<td>Latch-Off Input (Integration in TIMER)</td>
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<tr>
<td>Threshold below which controller is latched</td>
<td>V_TIMER(LATCH)</td>
<td></td>
<td>0.7</td>
<td>1</td>
<td>1.3</td>
<td>V</td>
</tr>
<tr>
<td>Blanking duration on latch detection</td>
<td>T_LATCH</td>
<td></td>
<td></td>
<td></td>
<td>12</td>
<td>μs</td>
</tr>
<tr>
<td>DRV Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>Driver voltage high level</td>
<td>V_high</td>
<td>C_L = 1nF, VCC = 12V</td>
<td>10.3</td>
<td>V</td>
<td></td>
<td></td>
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<tr>
<td>Driver voltage clamp level</td>
<td>V_Clamp</td>
<td>C_L = 1nF, VCC = 24V</td>
<td>13.4</td>
<td>V</td>
<td></td>
<td></td>
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<tr>
<td>Driver voltage low level</td>
<td>V_LOW</td>
<td>C_L = 1nF, VCC = 24V</td>
<td>16</td>
<td>mV</td>
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<td></td>
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<tr>
<td>Driver voltage rise time</td>
<td>T_R</td>
<td>C_L = 1nF, VCC = 16V</td>
<td>13</td>
<td>ns</td>
<td></td>
<td></td>
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<tr>
<td>Driver voltage fall time</td>
<td>T_F</td>
<td>C_L = 1nF, VCC = 16V</td>
<td>23</td>
<td>ns</td>
<td></td>
<td></td>
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<tr>
<td>Driver pull-up resistance</td>
<td>R_Pull-up</td>
<td>C_L = 1nF, VCC = 16V</td>
<td>8</td>
<td>Ω</td>
<td></td>
<td></td>
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<tr>
<td>Driver pull-down resistance</td>
<td>R_Pull-down</td>
<td>C_L = 1nF, VCC = 16V</td>
<td>10</td>
<td>Ω</td>
<td></td>
<td></td>
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<tr>
<td>Thermal Shutdown</td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal shutdown threshold</td>
<td></td>
<td></td>
<td>(5)</td>
<td>150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Thermal shutdown hysteresis</td>
<td></td>
<td></td>
<td>(5)</td>
<td>25</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

NOTE:
5) This parameter is guaranteed by design.
## PIN FUNCTIONS

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>TIMER</td>
<td>Timer. TIMER combines soft start, frequency jittering, and timer functions for overload protection (OLP), brown-out protection, and X-cap discharging. The HFC0511 can be latched off by pulling TIMER low.</td>
</tr>
<tr>
<td>2</td>
<td>FB</td>
<td>Feedback. Use a pull-down optocoupler to control the output regulation.</td>
</tr>
<tr>
<td>3</td>
<td>CS</td>
<td>Current sense. CS senses the primary-side current for current-mode operation and provides a mean for over-power compensation adjustment.</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>IC ground.</td>
</tr>
<tr>
<td>5</td>
<td>DRV</td>
<td>Drive signal output.</td>
</tr>
<tr>
<td>6</td>
<td>VCC</td>
<td>Power supply.</td>
</tr>
<tr>
<td>8</td>
<td>HV</td>
<td>High-voltage current source. HV includes brown-out and X-cap discharge functions.</td>
</tr>
</tbody>
</table>
TYPICAL CHARACTERISTICS

Supply Current from HV vs. Temperature

Leakage Current from HV vs. Temperature

Internal IC Consumption vs. Temperature

Break-Down Voltage vs. Temperature

VCC Current-Source Turn-Off Level, Rising vs. Temperature

VCC Threshold for HV Turn-On Detection, Falling vs. Temperature

VCC Current Source Turn-On Level, Falling vs. Temperature

Voltage above VCC where the Controller Latches Off (OVP) vs. Temperature

VCC Hysteresis for HV Turn-On Detection vs. Temperature
TYPICAL CHARACTERISTICS (continued)

VCC Recharge Level where Protection Occurs vs. Temperature

VCC Decreasing Level when Latch-Off Phase Ends vs. Temperature

HV Turn-On Threshold vs. Temperature

HV Turn-Off Threshold vs. Temperature

Oscillator Frequency vs. Temperature

Frequency Jitter Amplitude in Percentage of fosc vs. Temperature

Minimum Switching Frequency vs. Temperature

Slope of the Compensation Ramp vs. Temperature

Current Limit vs. Temperature
TYPICAL CHARACTERISTICS (continued)

- **Short-Circuit Protection Level** vs. Temperature
- **Leading Edge Blanking for $V_{ILM}$** vs. Temperature
- **Leading Edge Blanking for $V_{SCP}$** vs. Temperature
- **FB Level (Falling) at which Controller Enters Burst Mode** vs. Temperature
- **FB Level (Rising) at which Controller Exits Burst Mode** vs. Temperature
- **FB Level at which Controller Enters OLP after Blanking Time** vs. Temperature
- **FB Internal Pull-Up Resistor** vs. Temperature
- **FB Internal Pull-Up Voltage** vs. Temperature
TYPICAL PERFORMANCE CHARACTERISTICS

\( V_{IN} = 230\,V_{AC} \), \( V_{OUT} = 19\,V \), \( I_{OUT} = 2.35\,A \), unless otherwise noted.

**Input Power Start-Up**

230\,V_{AC} Full Load

**Input Power Shutdown**

230\,V_{AC} Full Load

**Output Ripple**

Output Ripple

**SCP Entry**

SCP Entry

SCP Recovery

SCP Power-On

**OLP Entry**

OLP Entry

OLP Recovery

OLP Power-On
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 230\text{V}_{AC}, V_{OUT} = 19\text{V}, I_{OUT} = 2.35\text{A}, T_A = 25^\circ\text{C}$, unless otherwise noted.
**Figure 1: Functional Block Diagram**
OPERATION

The HFC0511 incorporates all necessary features for building a reliable switch-mode power supply. The HFC0511 is a fixed-frequency, current-mode controller with internal slope compensation. At light loads, the controller freezes the peak current and reduces its switching frequency down to 27kHz to minimize switching losses. When the output power falls below a given level, the controller enters burst mode. The HFC0511 also has excellent EMI performance due to frequency jittering. The HFC0511’s high level of integration requires very few external components.

Fixed Frequency with Jitter

Frequency jitter reduces EMI by spreading the energy over the jitter frequency range. Figure 2 shows the circuit of the frequency jittering.

A controlled current source (fixed at 2.72µA when \( V_{FB} = 2V \)) charges the internal \( C_{OSC} \) capacitor. Comparing the capacitor voltage to the TIMER voltage determines the switching frequency. Frequency jitter is accomplished by varying \( V_{TIMER} \) between 3.2V and 2.8V (see Figure 3). Determine \( T_{jitter} \) with Equation (1):

\[
T_{jitter} = 2 \times \frac{C_{TIMER} \times (3.2V - 2.8V)}{10\mu A} \tag{1}
\]

Figure 2: Frequency Jitter Circuit

Figure 3: Frequency Jitter

Frequency Foldback

The HFC0511 implements frequency foldback at light load to improve overall efficiency.

When the load decreases to a given level (1.0V < \( V_{FB} < 1.8V \)), the controller freezes the peak current (as measured on CS, typically 0.7V) while reducing its switching frequency to 27kHz. This reduces switching loss. If the load continues to decrease, the peak current decreases with 27kHz of fixed frequency to avoid audible noise. Figure 4 shows the frequency vs. \( V_{FB} \) and peak current (\( V_{CS} \)) vs. \( V_{FB} \).

Figure 4: Frequency and Peak Current (\( V_{CS} \)) vs. \( V_{FB} \)

Current-Mode Operation with Slope Compensation

The feedback voltage (\( V_{FB} \)) controls the primary peak current. When the peak current reaches the level determined by \( V_{FB} \), DRV turns off. The controller can also be used in continuous conduction mode (CCM) with a wide input voltage range because of its internal slope compensation (typically 25mV/µs), avoiding sub-harmonic oscillations above a 50% duty cycle.
High Voltage Start-Up Current Source with Brown-Out Detection

At start-up, the internal high-voltage current source from HV supplies the IC. The IC turns off the current source once VCC reaches VCCOFF (typically 15.5V) and detects the voltage on HV. Once the HV voltage exceeds HV_ON before VCC drops down to VCC_SS (typically 12V), the controller begins switching. If the HV voltage does not exceed HV_ON, the system treats this as a brown-out and latches DRV low. When VCC drops to VCC_PRO (typically 5.5V), the high-voltage current source turns on to recharge VCC. The auxiliary transformer winding supplies the IC after the controller starts switching. If VCC falls below VCC_ON (typically 8.5V), the switching pulse stops, and the current source turns on again. Figure 5 shows the typical VCC under-voltage lockout (UVLO) waveform.

![Figure 5: VCC Under-Voltage Lockout](image_url)

The VCC lower threshold UVLO drops from VCC_ON to VCC_PRO under fault conditions such as overload protection (OLP), short-circuit protection (SCP), brown-out, and over-temperature protection (OTP).

Soft Start (SS)

Soft start is externally programmable with a capacitor on TIMER. As this capacitor charges from 1V to 1.75V with 1/4 of the normal charge current, the peak-current limit threshold increases gradually from 0.25V to 1V while increasing the switching frequency gradually. Figure 6 shows the typical soft-start waveform. The TIMER capacitor determines the start-up duration as shown in Equation (2):

\[ T_{\text{Soft-start}} = \frac{C_{\text{TIMER}} \cdot (1.75V - 1V)}{10/4 \mu A} \]  

**Burst Mode**

To minimize power dissipation in no load or light load, the HFC0511 employs burst-mode operation. As the load decreases, \( V_{FB} \) decreases. The IC enters burst mode when \( V_{FB} \) drops below the lower threshold \( V_{BURL} \) (typically 0.7V), stopping output switching. Then the output voltage starts to drop, which causes \( V_{FB} \) to increase again. Once \( V_{FB} \) exceeds \( V_{BURH} \) (typically 0.8V), switching resumes. Burst mode enables and disables MOSFET switching alternately, thereby reducing no-load or light-load switching losses.

**Adjustable Over-Power Compensation**

An offset current proportional to the input voltage is added to the current sense voltage. By choosing the value of the resistor to be in series with CS, the amount of compensation can be adjusted to the application for a more accurate output power limit at the total input range. Figure 7 and Figure 8 show the compensation current relation to FB and the peak voltage on HV respectively.

![Figure 7: Compensation Current vs. FB and HV Voltage](image_url)
HFC0511 – FIXED-FREQUENCY FLYBACK CONTROLLER W/ ULTRA-LOW NO LOAD POWER CONSUMPTION

Short-Circuit Protection (SCP)

The HFC0511 employs short-circuit protection (SCP) if \( V_{\text{CS}} \) reaches \( V_{\text{SCP}} \) (typically 1.47V) after a reduced leading-edge blanking time (\( T_{\text{LEB2}} \)). Once the fault disappears, the power supply resumes operation.

Thermal Shutdown

To prevent thermal damage, the HFC0511 stops switching when the temperature exceeds 150°C. Once the temperature drops below 125°C, the power supply resumes operation. During thermal shutdown, the VCC UVLO lower threshold drops from 8.5V to 5.5V.

VCC Over-Voltage Protection (OVP)

The HFC0511 enters a latched fault condition if VCC rises above \( V_{\text{OVP}} \) (typically 26.5V) for 60µs. The controller remains fully latched until VCC drops below \( V_{\text{CC}}(\text{LATCH}) \) (typically 2.5V), such as when the power supply is unplugged from the main input and is plugged in again. This situation usually occurs when the optocoupler fails, which results in the loss of output voltage regulation.

TIMER Latch-Off for OVP and OTP

Pulling TIMER below \( V_{\text{TIMER(LATCH)}} \) (typically 1V) for 12µs can latch off the IC. This function can be used for external over-voltage protection (OVP) and OTP.

X-Cap Discharge Function

X-capacitors are typically positioned across a power supply’s input terminals to filter differential mode EMI noise. These components pose a potential hazard since they can store unsafe levels of voltage energy after the AC line is disconnected. Generally, resistors in parallel with the X-caps provide a discharge path to meet safety standards, but these discharge resistors produce a constant loss while the AC is connected and contribute to no-load and standby input power consumption.
HV acts as a smart X-cap discharger. When AC voltage is applied, the internal high-voltage current source turns off to block HV current, and the IC monitors the HV voltage. When removing the AC voltage, the IC turns off the high-voltage current source after about 32 TIMER cycles to discharge the X-cap energy. The first discharge duration is 16 cycles. After the first discharge, the IC turns off the current source for 16 cycles to detect whether the input is plugged into the AC line again. If the AC input remains disconnected, the IC turns on the current source for 48 cycles to discharge again, and then turn off for 16 cycles to detect repeatedly until the voltage on the X-cap drops to VCC. Once the reconnected AC input is detected, the high-voltage current source remains off until VCC drops to VCCPRO (5.3V), and then restarts the system by recharging VCC. Figure 10 shows the discharge function waveforms.

This approach provides an intelligent discharge path for the X-cap, eliminating power loss from the external discharge resistors.

Clamped Driver
DRV is clamped at VClamp (typically 13.4V) when VCC exceeds 16V, allowing for the use of any standard MOSFET.

Leading-Edge Blanking
An internal leading-edge blanking (LEB) unit containing two LEB times is employed between the CS and the current comparator input to prevent premature switching pulse termination due to parasitic capacitances (see Figure 11). During the blanking time, the current comparator is disabled and cannot turn off the external MOSFET.

![Figure 11: Leading-Edge Blanking](image_url)

This is a diagram showing the timing of LEB times.

**Figure 10: X-Cap Discharger**

This diagram illustrates the discharge function waveforms.
APPLICATION INFORMATION

VCC Capacitor Selection

Figure 12 shows the start-up circuit. The values of R1 and C1 determine the system start-up delay time. A larger R1 or C1 increases the start-up delay.

![Start-Up Circuit Diagram]

Figure 12: Start-Up Circuit

The VCC duration (from VCCOFF to VCCSS) for brown-out detection should exceed half of the input period. Estimate a value for the VCC capacitor with Equation (3):

\[
C_{VCC} > \frac{I_{CC(noswitch)} \cdot 0.5 \cdot T_{input}}{VCC_{OFF} - VCC_{SS}} \tag{3}
\]

Where \(I_{CC(noswitch)}\) is the internal consumption (close to \(I_{CCLATCH}\), and \(T_{input}\) is the period of the AC input. For most applications, choose a VCC capacitor value that exceeds 10μF.

A higher R1 value decreases the current of the internal high-voltage current source, especially at a low-input condition. Ensure that the practical supply current from HV is not smaller than the corresponding internal IC consumption current, which is the same as \(I_{CCLATCH}\). For the universal input range, R1 should be smaller than 80kΩ. 20kΩ is generally recommended.

Primary-Side Inductor Design (\(L_m\))

With internal slope compensation, the HFC0511 can support CCM when the duty cycle exceeds 50%. Set a ratio (\(K_P\)) of the primary inductor’s ripple current amplitude vs. the peak current value to \(0 < K_P \leq 1\), where \(K_P = 1\) for discontinuous conduction mode (DCM). Figure 13 shows the relevant waveforms.

A larger inductor leads to a smaller \(K_P\), which can reduce RMS current, but increases transformer size. An optimal \(K_P\) value is between 0.6 and 0.8 for the universal input range and 0.8 to 1 for a 230VAC input range.

![Typical Primary-Current Waveform]

Figure 13: Typical Primary-Current Waveform

The input power (\(P_{in}\)) at the minimum input can be estimated with Equation (4):

\[
P_{in} = \frac{V_O \cdot I_O}{\eta} \tag{4}
\]

Where \(V_O\) is the output voltage, \(I_O\) is the rated output current, and \(\eta\) is the estimated efficiency, which is generally between 0.75 and 0.85 depending on the input range and output application.

For CCM at minimum input, the converter duty cycle can be calculated with Equation (5):

\[
D = \frac{(V_O + V_F) \cdot N + V_{in(min)}}{(V_O + V_F) \cdot N + V_{in(min)}} \tag{5}
\]

Where \(V_F\) is the secondary diode’s forward voltage, \(N\) is the transformer turn ratio, and \(V_{in(min)}\) is the minimum voltage on the bulk capacitor.

The MOSFET turn-on time can be calculated with Equation (6):

\[
T_{on} = D \cdot T_s \tag{6}
\]

Where \(T_s\) is the switching period.

The average value of the primary current is calculated with Equation (7):

\[
I_{av} = \frac{P_{in}}{V_{in(min)}} \tag{7}
\]
The peak value of the primary current is calculated with Equation (8):

\[ I_{\text{peak}} = \frac{I_{\text{av}}}{1 - K_p \cdot D} \]  

(8)

The ripple value of the primary current is calculated with Equation (9):

\[ I_{\text{ripple}} = K_p \cdot I_{\text{peak}} \]  

(9)

The valley value of the primary current is calculated with Equation (10):

\[ I_{\text{valley}} = (1 - K_p) \cdot I_{\text{peak}} \]  

(10)

The inductance \( L_m \) can be estimated with Equation (11):

\[ L_m = \frac{V_{\text{in(min)}} \cdot T_{\text{on}}}{T_{\text{ripples}}} \]  

(11)

**Current-Sense Resistor**

Figure 14 shows the peak-current comparator logic and the subsequent waveform.

When the sum of the sensing resistor voltage and the slope compensator reaches \( V_{\text{peak}} \), the comparator goes high to reset the RS flip-flop, and DRV is pulled down to turn off the MOSFET. The maximum current limit (\( V_{\text{limit}} \), as measured by \( V_{\text{CS}} \)) is 0.95V. The slope compensator (\( V_{\text{slope}} \)) is ~25mV/µs. Given a certain margin, use 0.95\( \times V_{\text{limit}} \) as \( V_{\text{peak}} \) at full load. Then the voltage on the sensing resistor can be obtained with Equation (12):

\[ V_{\text{sense}} = 95\% \cdot V_{\text{limit}} - V_{\text{slope}} \cdot T_{\text{on}} \]  

(12)

Then calculate the value of the sense resistor with Equation (13):

\[ R_{\text{sense}} = \frac{V_{\text{sense}}}{I_{\text{peak}}} \]  

(13)

Select the current sense resistor with an appropriate power rating. Then calculate the sense resistor power loss with Equation (14):

\[ P_{\text{sense}} = \left[ \frac{\left( I_{\text{peak}} + I_{\text{valley}} \right)^2}{2} + \frac{1}{12} \left( I_{\text{peak}} - I_{\text{valley}} \right)^2 \right] \cdot D \cdot R_{\text{sense}} \]  

(14)

**Low-Pass Filter on CS**

A small capacitor connected to the CS with \( R_{\text{series}} \) forms a low-pass filter for noise filtering when the MOSFET turns on and off (see Figure 15).

The low-pass filter’s \( RxC \) constant should not exceed 1/3 of the leading-edge blanking period for SCP (\( T_{\text{LEB2}} \), typically 270ns), otherwise the filtered sensed voltage cannot reach the SCP point (1.45V) to trigger SCP if an output short circuit occurs.
Over-Power Compensation (OPC)
The HFC0511 uses an over-power compensation function (OPC) by drawing current from CS. OPC minimizes the OLP difference caused by a different input voltage. The offset current is proportional to the input peak voltage sensed by HV.

Supposing that the resistor in the current sensing loop is \( R_{\text{series}} \), and the input voltage is 220V\(_{\text{AC}}\), calculate the compensation voltage on CS with Equation (15):

\[
V_{\text{comp}} = R_{\text{series}} \cdot I_{\text{opc - 310V}} \quad (15)
\]

The compensation criterion is making the FB voltage under full-load condition similar whether in high line or low line.

**Jitter Period**

Frequency jitter is an effective method to reduce EMI by dissipating energy. The \( n \)^\text{th} order harmonic noise bandwidth is calculated with Equation (16):

\[
B_{T_n} = n \cdot (2 \cdot f_j + f_{\text{jitter}}) \quad (16)
\]

Where \( f_j \) is the frequency jitter amplitude.

If \( B_{T_n} \) exceeds the resolution bandwidth (RBW) of the spectrum analyzer (200Hz for noise frequency less than 150kHz, 9kHz for noise frequency between 150kHz to 30MHz), the spectrum analyzer receives less noise energy.

The capacitor on TIMER determines the period of the frequency jitter. A 10\( \mu \text{A} \) current source charges the capacitor. When the TIMER voltage reaches 3.2V, another 10\( \mu \text{A} \) current source discharges the capacitor to 2.8V. This charging and discharging cycle repeats.

Equation (2) describes the jitter period in theory. A smaller \( f_{\text{jitter}} \) is more effective for EMI reduction. However, the measurement bandwidth requires that \( f_{\text{jitter}} \) be large compared to the spectrum analyzer RBW for effective EMI reduction. \( f_{\text{jitter}} \) should also be less than the control-loop-gain crossover frequency to avoid disturbing the output voltage regulation. Simultaneously consider the practical application when selecting the TIMER capacitor. A capacitor that is too large may cause the start-up to fail at full load because of the long soft start-up duration shown in Equation (3).

However, a TIMER capacitor that is too small causes the TIMER period to become smaller, so the TIMER count capability is overloaded, and some logic problems may occur. For most applications, a \( f_{\text{jitter}} \) value between 200Hz and 400Hz is recommended.

**X-Cap Discharge Time**

Figure 10 shows the X-cap discharger waveforms. The maximum discharge time occurs at a high-line input with no-load condition. The maximum discharge delay time is calculated with Equation (17):

\[
T_{\text{delay}} = 32 \cdot T_{\text{jitter}} \quad (17)
\]

The X-cap is discharged from a high-voltage constant current source \( (I_{HV - 120V}, \text{ typically } 2.5mA) \) into HV. The current-source discharge time for the X-cap to drop to 37% of the peak voltage can be estimated with Equation (18):

\[
T_{\text{discharge}} = \frac{C_X \cdot 63\% \cdot \sqrt{2} \cdot V_{\text{ac(max)}}}{I_{HV - 120V}} \quad (18)
\]

Where \( C_X \) is the X-cap capacitance, and \( V_{\text{AC(max)}} \) is the maximum AC input RMS value.

The first discharging period is 16\( \times T_{\text{jitter}} \), with a subsequent period equal to 48\( \times T_{\text{jitter}} \). Then the discharge sections times can be calculated approximately with Equation (19):

\[
n = \frac{T_{\text{discharge}} - 16 \cdot T_{\text{jitter}}}{48 \cdot T_{\text{jitter}}} + 1 \quad (19)
\]

For every discharge section, there is a certain period \( (16\times T_{\text{jitter}}) \) for detection as shown in Equation (20):

\[
T_{\text{detect}} = 16 \cdot T_{\text{jitter}} \cdot (n - 1) \quad (20)
\]

As a result, the total discharge time is determined with Equation (21):

\[
T_{\text{total}} = T_{\text{delay}} + T_{\text{discharge}} + T_{\text{detect}} \quad (21)
\]

The total discharge time is relative to \( T_{\text{jitter}} \), which is dependent on \( C_{\text{TIMER}} \). For example, if \( C_{\text{TIMER}} \) is 47\( \text{nF} \), and \( T_{\text{jitter}} \) is 3.7ms, the X-cap discharge margin is 1s due to the X-cap value tolerance (\( \pm 10\% \) typically). It is recommended to select an X-cap less than 3.3\( \mu \text{F} \).
Though the X-cap has been discharged, it may still retain a high voltage on the bulk capacitor. For safety, make sure it is released before debugging the board.

**Ramp Compensation**

When adopting peak current control, subharmonic oscillation occurs when \( D > 0.5 \) in CCM. The HFC0511 is equipped with internal ramp compensation to solve this problem. \( \alpha \) is calculated with Equation (22):

\[
\alpha = \frac{D_{\text{max}} \cdot V_{\text{in(min)}} \cdot R_{\text{sense}} - m_a}{(1-D_{\text{max}}) \cdot L_m \cdot V_{\text{in(min)}}} \cdot R_{\text{sense}} + m_a
\]  

Where \( m_a = 18 \text{mV/\mu s} \) is the minimum internal slope value of the compensation ramp, \( \frac{V_{\text{in(min)}} \cdot R_{\text{sense}}}{L_m} \) is the slew rate of the primary-side sensed by the CS resistor, and \( \frac{D_{\text{max}} \cdot V_{\text{in(min)}} \cdot R_{\text{sense}}}{(1-D_{\text{max}}) \cdot L_m} \) is the slew rate of the equivalent secondary-side voltage sensed by the CS resistor respectively. For stable operation, \( \alpha \) must be less than 1.

**PCB Layout Guidelines**

Efficient PCB layout is critical for stable operation, good EMI performance, and good thermal performance. For best results, refer to Figure 16 and follow the guidelines below.

1) Minimize the power stage loop area including the input loop (C1 - T1 - Q1 - R11/R12/R13 - C1), the auxiliary winding loop (T1 - D4 - R4 - C3 - T1), and the output loop (T1 - D6 - C10 - T1).

2) Keep the input loop GND and control circuit separate.
   *Only connect them at C1.*

3) Connect the Q1 heat sink to the primary GND plane to improve EMI.

4) Place the control circuit capacitors (such as those for FB, CS, and VCC) close to the IC to decouple noise.

**Design Example**

Table 1 is a design example of the HFC0511 for power adapter applications.

<table>
<thead>
<tr>
<th>Table 1: Design Example</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{\text{IN}} )</td>
</tr>
<tr>
<td>( V_{\text{OUT}} )</td>
</tr>
<tr>
<td>( I_{\text{OUT}} )</td>
</tr>
</tbody>
</table>
TYPICAL APPLICATION CIRCUIT

Figure 17: Typical Application
FLOW CHART

Figure 18: Control Flow Chart

UVLO, brown-out, OTP & OLP is auto restart, OVP on VCC and Latch-off on TIMER are latch mode.

Release from the latch condition, need to unplug from the main input.

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EVOLUTION OF THE SIGNALS IN PRESENCE OF FAULTS

Figure 19: Signal Evolution in the Presence of Faults
PACKAGE INFORMATION

SOIC8-7A

HFC0511 – FIXED-FREQUENCY FLYBACK CONTROLLER W/ ULTRA-LOW NO LOAD POWER CONSUMPTION

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NOTE:
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2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING SHALL BE 0.004" INCHES MAX.
5) JEDEC REFERENCE IS MS-012.
6) DRAWING IS NOT TO SCALE