**DESCRIPTION**

HFC0500 is a fixed-frequency current-mode controller with internal slope compensation. It is specifically designed for the medium-power, offline, flyback, switch-mode power supplies. HFC0500 is a green-mode highly efficient controller. At light loads, the controller freezes the peak current and reduces its switching frequency down to 25kHz to offer excellent light-load efficiency. At very light loads, the controller enters burst mode to achieve very low standby power consumption.

HFC0500 offers frequency jittering to help dissipate energy generated by conducted noise.

HFC0500 employs overpower compensation function to narrow the difference of over power protection point between low line and high line.

HFC0500 also has X-cap discharge function to discharge the X-cap when the input is unplugged. This aids in lowering no load power.

HFC0500 features multiple protections that include thermal shutdown (TSD), VCC under-voltage lockout (UVLO), overload protection (OLP), over-voltage protection (OVP), and brown-out protection.

HFC0500 is available in an SOIC8-7A package.

**FEATURES**

- Fixed-frequency current-mode control with internal slope compensation
- Frequency foldback down to 25kHz at light loads
- Burst mode for low standby power consumption, meeting EuP Lot 6
- Frequency jitter to reduce EMI signature
- X-cap discharge function
- Adjustable overpower compensation
- Internal high-voltage current source
- VCC under-voltage lockout with hysteresis (UVLO)
- Brown-out protection on HV
- Overload protection with programmable delay
- Thermal shutdown (auto-restart with hysteresis)
- Latch-off for external over-voltage protection (OVP) and over-temperature protection (OTP) on TIMER
- Latch-off for Vcc over voltage protection
- Short-circuit protection
- Programmable soft start

**APPLICATIONS**

- AC/DC power for small and large appliances
- AC/DC adapters for notebook computers, tablets, and smart phones
- Offline battery chargers
- LCD TVs and monitors

*All MPS parts are lead-free, halogen free, and adhere to the RoHS directive. For MPS green status, please visit MPS website under Quality Assurance.*

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TYPICAL APPLICATION

Input 85~265 Vac

HFC0500

8
6
5
4
3
2
1 TIMER

HV

FB

CS

GND

HFC0500

6
5
VCC

DRV

Output T1

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ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Part Number*</th>
<th>Package</th>
<th>Top Marking</th>
</tr>
</thead>
<tbody>
<tr>
<td>HFC0500GS</td>
<td>SOIC8-7A</td>
<td>See Below</td>
</tr>
</tbody>
</table>

* For Tape & Reel, add suffix –Z (e.g. HFC0500GS–Z);

TOP MARKING

HFC0500
LLLLLLLLL
MPSYWW

HFC0500: first seven digits of the part number;
LLLLLLLL: lot number;
MPS: MPS prefix;
Y: year code;
WW: week code;

PACKAGE REFERENCE

```
<table>
<thead>
<tr>
<th>TIMER</th>
<th>1</th>
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<th>3</th>
<th>4</th>
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<th>6</th>
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<td>HV</td>
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<td>VCC</td>
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<td>DRV</td>
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</tbody>
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TOP VIEW
**ABSOLUTE MAXIMUM RATINGS**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
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<tbody>
<tr>
<td>HV</td>
<td>-0.7V to 700V</td>
</tr>
<tr>
<td>VCC, DRV to GND</td>
<td>-0.3V to 30V</td>
</tr>
<tr>
<td>FB, TIMER, CS to GND</td>
<td>-0.3V to 7V</td>
</tr>
</tbody>
</table>

Continuous Power Dissipation (TA = +25°C) \( \leq 1.3 \text{W} \)

Junction Temperature \( \leq 150°C \)

Lead Temperature \( \leq 260°C \)

Storage Temperature \( -60°C \) to \( +150°C \)

ESD Capability Human Body Model (except HV and DRV) \( \geq 4.0 \text{kV} \)

ESD Capability Human Body Model (DRV) \( \geq 3.5 \text{kV} \)

ESD Capability Human Body Model (HV) \( \geq 1.8 \text{kV} \)

ESD capability for Machine Mode \( \geq 400 \text{V} \)

**Thermal Resistance**

<table>
<thead>
<tr>
<th>Package</th>
<th>( \theta_{JA} )</th>
<th>( \theta_{JC} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>SOIC8-7A</td>
<td>96°C/W</td>
<td>45°C/W</td>
</tr>
</tbody>
</table>

**Notes:**

1) Exceeding these ratings may damage the device.

2) The maximum allowable power dissipation is a function of the maximum junction temperature \( T_J \) (MAX), the junction-to-ambient thermal resistance \( \theta_{JA} \), and the ambient temperature \( T_A \). The maximum allowable continuous power dissipation at any ambient temperature is calculated by \( P_D \) (MAX) = \( (T_J \) (MAX) - \( T_A \))/\( \theta_{JA} \). Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.

3) The device is not guaranteed to function outside of its operating conditions.

4) Measured on JESD51-7, 4-layer PCB.
## Electrical Characteristics

$V_{CC}=18V$, $T_J=-40°C$ ~ $125°C$, Min & Max are guaranteed by characterization, typical is tested under $25°C$, unless otherwise specified.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
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<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Start-up Current Source (HV)</strong></td>
<td>$I_{HV,400}$</td>
<td>$V_{CC}= 12V$, $V_{HV}=400V$</td>
<td>1.5</td>
<td>2.8</td>
<td>5</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>$I_{HV,120}$</td>
<td>$V_{CC}= 12V$, $V_{HV}=120V$</td>
<td>1.5</td>
<td>2.7</td>
<td>5</td>
<td>mA</td>
</tr>
<tr>
<td><strong>Leakage Current from HV</strong></td>
<td>$I_{LK,400}$</td>
<td>$V_{CC}$ increases to $18V$ then decreases to $14V$, $V_{HV}=400V$</td>
<td>1</td>
<td>16</td>
<td>25</td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td>$I_{LK,200}$</td>
<td>$V_{CC}$ increases to $18V$ then decreases to $14V$, $V_{HV}=200V$</td>
<td>1</td>
<td>13</td>
<td>22</td>
<td>μA</td>
</tr>
<tr>
<td><strong>Break Down Voltage</strong></td>
<td>$V_{BR}$</td>
<td>$T_J = 25°C$</td>
<td>700</td>
<td>790</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td><strong>Supply Voltage Management ($V_{CC}$)</strong></td>
<td><strong>VCC Increasing Level at which the Current Source Turns-Off</strong></td>
<td>$V_{CCOFF}$</td>
<td>12.5</td>
<td>15.5</td>
<td>18</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td><strong>VCC Decreasing Level above which Soft Start Takes Place if HV&gt;HVON</strong></td>
<td>$V_{CCSS}$</td>
<td>10.5</td>
<td>12</td>
<td>13</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td><strong>VCC Hysteresis for Brown-in Detection</strong></td>
<td>$V_{CCOFF} - V_{CCSS}$</td>
<td>1.35</td>
<td>3.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td><strong>VCC Decreasing Level at which the Current Source Turns-On</strong></td>
<td>$V_{CCON}$</td>
<td>7.3</td>
<td>8.5</td>
<td>9.6</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td><strong>VCC UVLO Hysteresis</strong></td>
<td>$V_{CCOFF} - V_{CCON}$</td>
<td>5</td>
<td>7</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td><strong>VCC Re-charge Level when Protection Takes Place</strong></td>
<td>$V_{CCPRO}$</td>
<td>4.9</td>
<td>5.5</td>
<td>6.2</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td><strong>VCC Decreasing Level at which the Latch off Phase Ends</strong></td>
<td>$V_{CCLATCH}$</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
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<tr>
<td></td>
<td><strong>Internal IC Consumption</strong></td>
<td>$I_{CC}$</td>
<td>$V_{FB}=2V, C_L=1nF, V_{CC}=12V$</td>
<td>1.1</td>
<td>1.8</td>
<td>2.7</td>
</tr>
<tr>
<td></td>
<td><strong>Internal IC Consumption, Latch off Phase</strong></td>
<td>$I_{CCLATCH}$</td>
<td>$V_{CC}=V_{CCOFF}-1V, T_J=25°C$</td>
<td>520</td>
<td>700</td>
<td>880</td>
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<tr>
<td></td>
<td><strong>Voltage on the VCC above which the Controller Latches off (OVP)</strong></td>
<td>$V_{OVP}$</td>
<td></td>
<td>24</td>
<td>26.5</td>
<td>28.5</td>
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<td></td>
<td><strong>Blanking Duration on the OVP Comparator</strong></td>
<td>$T_{OVP}$</td>
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<td>60</td>
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</table>
### ELECTRICAL CHARACTERISTICS (continued)

$V_{CC}=18V$, $T_J=-40^\circ C$ ~$125^\circ C$, Min & Max are guaranteed by characterization, typical is tested under $25^\circ C$, unless otherwise specified.

<table>
<thead>
<tr>
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<th>Min</th>
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<th>Max</th>
<th>Unit</th>
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<tbody>
<tr>
<td><strong>Brown-out</strong></td>
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<tr>
<td>HV Turn on Threshold Voltage</td>
<td>$HV_{ON}$</td>
<td>$V_{HV}$ going up,$T_J=25^\circ C$</td>
<td>95</td>
<td>107</td>
<td>119</td>
<td>V</td>
</tr>
<tr>
<td>HV Turn off Threshold Voltage</td>
<td>$HV_{OFF}$</td>
<td>$V_{HV}$ going down,$T_J=25^\circ C$</td>
<td>86</td>
<td>97</td>
<td>110</td>
<td>V</td>
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<tr>
<td>Brown-out Hysteresis</td>
<td>$\Delta HV$</td>
<td>$T_J=25^\circ C$</td>
<td>7.5</td>
<td>10</td>
<td>12.5</td>
<td>V</td>
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<tr>
<td>Timer Duration for Line Cycle Drop-out</td>
<td>$T_{HV}$</td>
<td>$C_{TIMER}=47nF$</td>
<td>40</td>
<td></td>
<td></td>
<td>ms</td>
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<tr>
<td><strong>Oscillator</strong></td>
<td></td>
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<tr>
<td>Oscillator Frequency</td>
<td>$f_{OSC}$</td>
<td>$V_{FB}&gt;1.85V,T_J=25^\circ C$</td>
<td>62</td>
<td>65</td>
<td>68</td>
<td>kHz</td>
</tr>
<tr>
<td>Frequency Jittering Amplitude, in Percentage of $f_{OSC}$</td>
<td>$A_{jitter}$</td>
<td>$V_{FB}&gt;1.85V,T_J=25^\circ C$</td>
<td>±5</td>
<td>±6.5</td>
<td>±8.3</td>
<td>%</td>
</tr>
<tr>
<td>Frequency jittering entry level</td>
<td>$V_{FB_JITTER}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V</td>
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<tr>
<td>Frequency Jittering Modulation Period</td>
<td>$T_{jitter}$</td>
<td>$C_{TIMER}=47nF$</td>
<td>3.7</td>
<td></td>
<td></td>
<td>ms</td>
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<tr>
<td><strong>Current Sense</strong></td>
<td></td>
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<tr>
<td>Current Limit Point</td>
<td>$V_{ILIM}$</td>
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<td>0.93</td>
<td>1</td>
<td>1.07</td>
<td>V</td>
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<td>Short Circuit Protection Point</td>
<td>$V_{SCP}$</td>
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<td>1.3</td>
<td>1.47</td>
<td>1.63</td>
<td>V</td>
</tr>
<tr>
<td>Current limitation when frequency foldback</td>
<td>$V_{FOLD}$</td>
<td>$V_{FB}=1.85V$</td>
<td>0.63</td>
<td>0.68</td>
<td>0.73</td>
<td>V</td>
</tr>
<tr>
<td>Current limitation when entry Burst</td>
<td>$V_{IBURL}$</td>
<td>$V_{FB}=0.7V$</td>
<td>0.11</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Current limitation when leave Burst</td>
<td>$V_{IBURH}$</td>
<td>$V_{FB}=0.8V$</td>
<td>0.15</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Leading Edge Blanking for $V_{ILIM}$</td>
<td>$T_{LEB1}$</td>
<td></td>
<td>350</td>
<td></td>
<td>ns</td>
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<tr>
<td>Leading Edge Blanking for $V_{SCP}$</td>
<td>$T_{LEB2}$</td>
<td></td>
<td>270</td>
<td></td>
<td>ns</td>
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<tr>
<td>Slope of the Compensation Ramp</td>
<td>$S_{RAMP}$</td>
<td></td>
<td>18</td>
<td>25</td>
<td>32</td>
<td>mV/µs</td>
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<tr>
<td><strong>Feedback (FB)</strong></td>
<td></td>
<td></td>
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<tr>
<td>Internal Pull-up Resistor</td>
<td>$R_{FB}$</td>
<td></td>
<td>11.5</td>
<td>14</td>
<td>16.5</td>
<td>kΩ</td>
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<tr>
<td>Internal Pull-up Voltage</td>
<td>$V_{DD}$</td>
<td></td>
<td>4.3</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{FB}$ to Internal Current Setpoint Division Ratio</td>
<td>$K_{FB1}$</td>
<td>$V_{FB}=2V$</td>
<td>2.55</td>
<td>2.8</td>
<td>3.05</td>
<td>--</td>
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<tr>
<td>$V_{FB}$ to Internal Current Setpoint Division Ratio</td>
<td>$K_{FB2}$</td>
<td>$V_{FB}=3V$</td>
<td>2.8</td>
<td>3.1</td>
<td>3.4</td>
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</tr>
<tr>
<td>FB Decreasing Level at which the Controller Enters the Burst Mode</td>
<td>$V_{BURL}$</td>
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<td>0.63</td>
<td>0.7</td>
<td>0.77</td>
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<td>FB Increasing Level at which the Controller Leaves the Burst Mode</td>
<td>$V_{BURH}$</td>
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<td>0.72</td>
<td>0.8</td>
<td>0.88</td>
<td>V</td>
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</tbody>
</table>
### ELECTRICAL CHARACTERISTICS (continued)

$V_{CC}=18\text{V}$, $T_J=-40^\circ\text{C} \sim 125^\circ\text{C}$, Min & Max are guaranteed by characterization, typical is tested under $25^\circ\text{C}$, unless otherwise specified.

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<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Over Load Protection</td>
<td>$V_{OLP}$</td>
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<td></td>
<td>3.7</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$T_{OLP}$</td>
<td>$C_{\text{TIMER}}=47\text{nF}$</td>
<td>40</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>Over Power Compensation</td>
<td>$K_{\text{OPC}}$</td>
<td></td>
<td>0.45</td>
<td></td>
<td></td>
<td>$\mu\text{A/V}$</td>
</tr>
<tr>
<td>Current out of CS</td>
<td>$I_{\text{OPC}}$</td>
<td>$V_{\text{HV}}=120\text{V}, V_{\text{FB}}=2.5\text{V}$</td>
<td>0</td>
<td></td>
<td></td>
<td>$\mu\text{A}$</td>
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<tr>
<td></td>
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<td>$V_{\text{HV}}=155\text{V}, V_{\text{FB}}=2.5\text{V}$</td>
<td>13</td>
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<td>$V_{\text{HV}}=310\text{V}, V_{\text{FB}}=2.5\text{V}$</td>
<td>85</td>
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<td>$V_{\text{HV}}=380\text{V}, V_{\text{FB}}=2.5\text{V}, T_J=25^\circ\text{C}$</td>
<td>90</td>
<td>119</td>
<td>148</td>
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<td>$V_{\text{OPC(OFF)}}$</td>
<td>0.55</td>
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<td>V</td>
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<td></td>
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<td>$V_{\text{OPC(ON)}}$</td>
<td>2.2</td>
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<td>V</td>
</tr>
<tr>
<td>Frequency Foldback</td>
<td>$V_{\text{FB(\text{FOLD})}}$</td>
<td></td>
<td>1.8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$F_{\text{OSC(min)}}$</td>
<td>$T_J=25^\circ\text{C}$</td>
<td>21</td>
<td>25</td>
<td>30</td>
<td>kHz</td>
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<tr>
<td></td>
<td>$V_{\text{FB(\text{FOLDE})}}$</td>
<td></td>
<td>1.0</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Latch-off Input (Integration in TIMER)</td>
<td>$V_{\text{TIMER(LATCHE)}}$</td>
<td></td>
<td>0.7</td>
<td>1</td>
<td>1.3</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$T_{\text{LATCH}}$</td>
<td></td>
<td>12</td>
<td></td>
<td></td>
<td>$\mu\text{s}$</td>
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### ELECTRICAL CHARACTERISTICS (continued)

V_{CC}=18V, \ T_J=-40^\circ C\sim 125^\circ C, \ Min & Max are guaranteed by characterization, typical is tested under 25^\circ C, unless otherwise specified.

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<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRV Voltage</td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Driver Voltage High Level</td>
<td>V_{high}</td>
<td>C_L=1nF, V_{CC}=12V</td>
<td>10.3</td>
<td>V</td>
<td></td>
<td></td>
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<tr>
<td>Driver Voltage Clamp Level</td>
<td>V_{clamp}</td>
<td>C_L=1nF, V_{CC}=24V</td>
<td>13.4</td>
<td>V</td>
<td></td>
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<tr>
<td>Driver Voltage Low Level</td>
<td>V_{low}</td>
<td>C_L=1nF, V_{CC}=24V</td>
<td>16</td>
<td>mV</td>
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<tr>
<td>Driver Voltage Rise Time</td>
<td>T_R</td>
<td>C_L=1nF, V_{CC}=16V</td>
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<td>ns</td>
<td></td>
<td></td>
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<tr>
<td>Driver Voltage Fall Time</td>
<td>T_F</td>
<td>C_L=1nF, V_{CC}=16V</td>
<td>23</td>
<td>ns</td>
<td></td>
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</tr>
<tr>
<td>Driver Pull-up Resistance</td>
<td>R_{pull-up}</td>
<td>C_L=1nF, V_{CC}=16V</td>
<td>8</td>
<td>\Omega</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Driver Pull-down Resistance</td>
<td>R_{pull-down}</td>
<td>C_L=1nF, V_{CC}=16V</td>
<td>10</td>
<td>\Omega</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Notes:

5) This parameter is guaranteed by design.
## PIN FUNCTIONS

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>TIMER</td>
<td>Timer. This pin combines the soft start, frequency jittering, along with the timer functions for OLP, brown-out protection, and X-cap discharge. The IC can be latched off by pulling this pin low.</td>
</tr>
<tr>
<td>2</td>
<td>FB</td>
<td>Feedback. Use a pull-down opto-coupler to control output regulation.</td>
</tr>
<tr>
<td>3</td>
<td>CS</td>
<td>Current Sense. Senses the primary side current for current-mode operation, and provides a means for over power compensation adjustment.</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>IC Ground.</td>
</tr>
<tr>
<td>5</td>
<td>DRV</td>
<td>Drive Signal Output.</td>
</tr>
<tr>
<td>6</td>
<td>VCC</td>
<td>Power Supply.</td>
</tr>
<tr>
<td>8</td>
<td>HV</td>
<td>High-Voltage Current Source. Includes brown-out and X-cap discharge functions.</td>
</tr>
</tbody>
</table>
TYPICAL CHARACTERISTICS

Supply Current from HV vs. Temperature
$V_{CC}=6V, V_{HV}=400V$

Leakage Current from HV vs. Temperature
$V_{CC}=14V, V_{HV}=400V$

Internal IC Consumption vs. Temperature

Break-Down Voltage vs. Temperature

$V_{CC}$ Current-Source Turn-off Level, Rising vs. Temperature

$V_{CC}$ Threshold for HV Turn-On Detection, Falling vs. Temperature

$V_{CC}$ Current Source Turn-On Level, Falling vs. Temperature

Voltage above $V_{CC}$ where the Controller Latches off (OVP) vs. Temperature

$V_{CC}$ Hysteresis for HV Turn-On Detection vs. Temperature
TYPICAL CHARACTERISTICS (continued)

- **V\textsubscript{CC} Recharge Level where Protection Occurs vs. Temperature**
- **V\textsubscript{CC} Decreasing Level when Latch-off Phase Ends vs. Temperature**
- **HV Turn-on Threshold vs. Temperature**

- **HV Turn-off Threshold vs. Temperature**
- **Oscillator Frequency vs. Temperature**
- **Frequency Jitter Amplitude in Percentage of f\textsubscript{osc} vs. Temperature**

- **Minimum Switching Frequency vs. Temperature**
- **Slope of the Compensation Ramp vs. Temperature**
- **Current Limit vs. Temperature**
TYPICAL CHARACTERISTICS (continued)

- Short Circuit Protection Level vs. Temperature
- Leading Edge Blanking for \( V_{ILIM} \) vs. Temperature
- Leading Edge Blanking for \( V_{SCP} \) vs. Temperature
- FB Level (Falling) at Which Controller Enters Burst Mode vs. Temperature
- FB Level (Rising) at Which Controller Exits Burst Mode vs. Temperature
- FB Level at Which Controller Enters OLP after Blanking Time vs. Temperature
- FB Internal Pull-up Resistor vs. Temperature
- FB Internal Pull-up Voltage vs. Temperature
TYPICAL PERFORMANCE CHARACTERISTIC

Vin=230VAC, Vout=19V, Iout=2.35A, unless otherwise noted.

Input Power Start Up
230VAC Full Load

Input Power Shut Down
230VAC Full Load

Output Ripple

SCP Entry

SCP Recovery

SCP Power On

OLP Entry

OLP Recovery

OLP Power On

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TYPICAL PERFORMANCE CHARACTERISTIC (continued)

$V_{IN}=230V_{AC}$, $V_{OUT}=19V$, $I_{OUT}=2.35A$, $T_{A}=25^\circ C$, unless otherwise noted.

**OVP**

- No Load
  - $V_{OC}$: 200V/div.
  - $V_{CC}$: 10V/div.
  - $V_{FB}$: 1V/div.
  - $V_{OUT}$: 10V/div.

- Full Load
  - $V_{OC}$: 200V/div.
  - $V_{CC}$: 10V/div.
  - $V_{FB}$: 1V/div.
  - $V_{OUT}$: 100V/div.

- No Load
  - $V_{FB}$: 1V/div.
  - $V_{CC}$: 5V/div.
  - $V_{OC}$: 2V/div.
  - $V_{OUT}$: 100V/div.

- Full Load
  - $V_{FB}$: 1V/div.
  - $V_{CC}$: 5V/div.
  - $V_{OC}$: 2V/div.
  - $V_{OUT}$: 100V/div.

Brown-in

- 400ms/div.

Brown-Out

- 400ms/div.

**OTP**

- 2s/div.

**X-Cap Discharge**

- 265$V_{AC}$, Full Load
  - $V_{IN}$: 100V/div.
  - 200ms/div.

** Conducted EMI**

- 230$V_{AC}$, L Wire
  - 150kHz to 30MHz

- 230$V_{AC}$, N Wire
  - 150kHz to 30MHz
TYPICAL PERFORMANCE CHARACTERISTIC (continued)

Vin=230VAC, Vout=19V, Iout=2.35A, Ta=25°C, unless otherwise noted.

No Load Power Consumption

<table>
<thead>
<tr>
<th>Vin (VAC/Hz)</th>
<th>85/60</th>
<th>115/60</th>
<th>230/50</th>
<th>265/50</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin (mW)</td>
<td>73.63</td>
<td>67.31</td>
<td>72.37</td>
<td>78.86</td>
</tr>
</tbody>
</table>
OPERATION

HFC0500 incorporates all the necessary features to build a reliable switch-mode power supply. It is a fixed-frequency current-mode controller with internal slope compensation. At light loads, the controller freezes the peak current and reduces its switching frequency down to 25kHz to minimize switching losses. When the output power falls below a given level, the controller enters burst mode. It also has excellent EMI performance due to frequency jittering.

Its high level of integration requires very few external components.

Figure 1: Functional Block Diagram
Fixed-Frequency with Jitter

Frequency jitter reduces EMI by spreading the energy over the jitter frequency range. Figure 2 shows the circuit of frequency jittering.

\[ f_s = \frac{1}{14pF \cdot V_{\text{TIMER}} / 2.72\mu A + 0.2\mu s} \quad (1) \]

\[ T_{\text{jitter}} = 2 \cdot \frac{C_{\text{TIMER}} \cdot (3.2V - 2.8V)}{10\mu A} \quad (2) \]

Figure 3: Frequency Jitter

Frequency Foldback

The HFC0500 implements frequency foldback at light load condition to improve overall efficiency. When the load decreases to a given level (1.0V < VFB < 1.8V), the controller freezes the peak current (as measured on CS, typically 0.7V) while reducing its switching frequency to 25kHz. This reduces the switching loss. If the load continues to decrease, the peak current decreases with 25kHz fixed frequency to avoid audible noise. Figure 4 shows the frequency vs. VFB and peak current vs. VFB.

Current-Mode Operation with Slope Compensation

VFB controls the primary-peak current. When the peak current reaches the level determined by VFB, DRV turns off. The controller can also be used in continuous conduction mode (CCM) with a wide input voltage range because of its internal slope compensation (25mV/µs, typical), avoiding sub-harmonic oscillations above 50% duty cycle.

High Voltage Startup Current Source with Brown-Out Detection

At start up, the internal high-voltage current source from HV supplies the IC. The IC turns off the current source as soon as VCC reaches VCCOFF (15V, typical), and detects the voltage on HV. Once the HV voltage exceeds HVON before VCC drops down to VCCSS (12V, typical), the controller starts switching. Otherwise the system treats the condition as a brown-out and
latches DRV low. When \( V_{CC} \) drops to \( V_{CCPRO} \) (5.3V, typical), the high-voltage current source turns on to recharge \( V_{CC} \). The auxiliary transformer winding supplies the IC after the controller starts switching. If \( V_{CC} \) falls below \( V_{CCON} \) (8.0V, typical), the switching pulse stops and the current source turns on again. Figure 5 shows the typical \( V_{CC} \) under-voltage lockout waveform.

![Figure 5: VCC Under-Voltage Lockout](image)

The \( V_{CC} \) lower threshold UVLO drops from 8V to 5.3V under fault conditions, such as OLP, SCP, brown-out, and OTP.

**Soft Start**

Soft start is externally programmable with a capacitor on TIMER. As this capacitor charges from 1V to 1.75V with 1/4 the normal charge current, the peak current limit threshold gradually increases from 0.25V to 1V while gradually increasing the switching frequency. Figure 6 shows the typical soft-start waveform. The TIMER capacitor determines the start-up duration as follow equation (3).

\[
T_{\text{Soft-start}} = \frac{C_{\text{TIMER}}(1.75V - 1V)}{10 / 4\mu A} \tag{3}
\]

![Figure 6: Soft-Start](image)

**Burst Mode**

To minimize power dissipation in no load or light load, HFC0500 employs burst-mode operation. As the load decreases, \( V_{FB} \) decreases. The IC will enter burst-mode when \( V_{FB} \) drops below the lower threshold \( V_{BURL} \) (0.7V, typical), stopping output switching. At this point, the output voltage starts to drop, which causes \( V_{FB} \) to increase again. Once \( V_{FB} \) exceeds \( V_{BURH} \) (0.8V, typical), switching resumes. Burst mode alternately enables and disables MOSFET switching, thereby reducing no load or light load switching losses.

**Adjustable Over Power Compensation**

An offset current which is proportional to the input voltage is added to current sense voltage. By choosing the value of the resistor in series with the CS, the amount of compensation can be adjusted to the application for more accurate output power limit at total input range. Figure 7 and Figure 8 show the compensation current relation to FB and peak voltage on HV respectively.

![Figure 7: Compensation Current vs. FB and HV Voltage](image)
Timer-Based Over-Load Protection

In a flyback converter, if the switching frequency is fixed, maximum output power is limited by the peak current. The output voltage drops below the set value when the output power exceeds the power limit. This reduces the current through the opto-coupler, pulling $V_{FB}$ high.

When $FB$ is higher than $V_{OLP}$ (3.7V, typical) which is considered as an error flag, the timer begins to count. If the error flag is removed during the count, the timer resets. If the timer count reaches 17, OLP triggers. This timer duration avoids triggering OLP during the power supply start-up or short load transients. Figure 9 shows OLP function.

Timer-Based Brown-Out Protection

The brown-out protection block is similar to the OLP block. When the HV voltage drops below $HV_{OFF}$ (98V, typical) which is considered as an error flag, the timer starts to count. Once the HV voltage is higher than $HV_{OFF}$, the timer resets. When the timer counts to 17, brown-out protection triggers and the switching stops.

Short-Circuit Protection (SCP)

The HFC0500 has short-circuit protection if $V_{CS}$ reaches $V_{SCP}$ (1.45V, typical) after a reduced leading-edge blanking time ($T_{LEB2}$). As soon as the fault disappears, the power supply resumes operation.

Thermal Shutdown (TSD)

To prevent any thermal damage, HFC0500 stops switching when the temperature exceeds 150°C. As soon as the temperature drops below 125°C, the power supply resumes operation. During TSD, the $V_{CC}$ UVLO lower threshold drops from 8.0V to 5.3V.

$V_{CC}$ Over-Voltage Protection (OVP)

The HFC0500 enters latched fault condition if $V_{CC}$ goes above $V_{OVP}$ (26.5V, typical) for 60µs. The controller stays fully latched until $V_{CC}$ drops below $V_{CC\text{LATCH}}$ (2.5V, typical), i.e. when the user unplugs the power supply from the main input and re-plugs it. The situation usually happens when the opto-coupler fails, which results in the loss of output voltage regulation.

TIMER Latch-Off for OVP and OTP

Pulling TIMER down lower than $V_{\text{TIMER(LATCH)}}$ (1V, typical) for 12µs can also latch off the IC. This function can be used for external OVP and OTP etc.

X-Cap Discharge Function

X capacitors are typically positioned across a power supply’s input terminals to filter differential mode EMI noise. These components pose a potential hazard because they can store unsafe levels of voltage energy after the AC line is disconnected. Generally, resistors in parallel to the X-cap provide a discharge path to meet safety standards, but these discharge resistors produce a constant loss while the AC is connected, and contribute to no-load and standby input power consumption.
The HFC0500's HV acts as a smart X-cap discharger. When the AC voltage is applied, the internal high-voltage current source turns off to block HV current and the IC monitors the HV voltage. When removing the AC voltage, the IC turns on the high-voltage current source after about 32 TIMER cycles to discharge the X-cap energy. The first discharge duration is 16 cycles. After the first discharge, the IC turns off the current source for 16 cycles to detect whether the input is re-plugged to the AC line. If the AC input remains disconnected, the IC turns on the current source for 48 cycles to discharge again, and then off for 16 cycles to re-detect repeatedly until the voltage on X-cap drops to V_{CC}. Once the reconnected AC input is detected, the high-voltage current source remains off until V_{CC} drops to V_{CC PRO} (5.3V), and then restarts the system by recharging Vcc. Figure 10 shows the discharge function waveforms.

This approach provides an intelligent discharge path for the X-cap, eliminating the power loss form external discharge resistors.

**Clamped Driver**

DRV is clamped at V_{Clamp} (13.4V, typical) when V_{CC} exceeds 16V, allowing the use of any standard MOSFET.

**Leading-Edge Blanking**

An internal leading-edge blanking (LEB) unit containing two LEB times is employed between the CS and the current comparator input to avoid premature switching pulse termination due to parasitic capacitances. During the blanking time, the current comparator is disabled and can not turn off the external MOSFET. Figure 11 shows the LEB waveform.
APPLICATION INFORMATION

VCC Capacitor Selection

Figure 12: Start-Up Circuit

Figure 12 shows the start-up circuit. The values of R1 and C1 determine the system start-up delay time: a larger R1 or C1 increases the start-up delay. The VCC duration (from VCC,OFF to VCC,SS) for brown-out detection should exceed half of the input period, equation (4) provides an estimated value for the VCC capacitor, where \( I_{CC(noswitch)} \) is the internal consumption (close to \( I_{CC latch} \)), and \( T_{input} \) is period of the AC input. For most applications, choose a VCC capacitor value that exceeds 10\( \mu \)F.

\[
C_{VCC} > \frac{I_{CC(noswitch)} \cdot 0.5 \cdot T_{input}}{VCC_{OFF} - VCC_{SS}} \quad (4)
\]

A higher value R1 decreases the current of internal high-voltage current source especially at low input condition. It is necessary to make sure the practical supply current from HV is not smaller than the corresponding internal IC consumption current which is the same as \( I_{CLATCH} \). Thus for universal input range R1 should be smaller than 80k and 20k is generally recommended.

Primary-Side Inductor Design (\( L_m \))

With internal slope compensation, HFC0500 supports CCM when the duty cycle exceeds 50%. Set a ratio \( (K_F) \) of the primary inductor’s ripple current amplitude vs. the peak current value to 0<\( K_F \)≤1, where \( K_F=1 \) for DCM. Figure 13 shows the relevant waveforms. A larger inductor leads to a smaller \( K_F \), which can reduce RMS current but increase transformer size. An optimal \( K_F \) value is between 0.6 and 0.8 for the universal input range and 0.8 to 1 for 230VAC input range.

\[
D = \frac{(V_D + V_F) \cdot N}{(V_D + V_F) \cdot N + V_{in(min)}} \quad (6)
\]

Where:
- \( V_D \) is the output voltage, \( I_O \) is the rated output current, \( \eta \) is the estimated efficiency, generally it is between 0.75 and 0.85 depending on the input range and output application.
- For CCM at minimum input, the converter duty cycle is:

\[
D = \frac{(V_D + V_F) \cdot N}{(V_D + V_F) \cdot N + V_{in(min)}} \quad (6)
\]

Where:
- \( V_F \) is the secondary diode’s forward voltage,
- \( N \) is the transformer turn ratio, and
- \( V_{in(min)} \) is the minimum voltage on bulk capacitor.

The MOSFET turn-on time is:

\[
T_{on} = D \cdot T_s \quad (7)
\]

Where \( T_s \) is the frequency jitter’s dominant switching period, \( \frac{1}{T_s} = f_s = 65kHz \).

The average, peak, ripple and valley values of the primary current are described as follows:

\[
I_{av} = \frac{P_n}{V_{in(min)}} \quad (8)
\]

\[
I_{peak} = \frac{I_{av}}{\left(1 - \frac{K_F}{2}\right) \cdot D} \quad (9)
\]
The following equation estimates \( L_m \) as:

\[
L_m = \frac{V_{\text{in(min)}} \cdot T_{\text{on}}}{I_{\text{ripples}}}
\]  

(12)

Current-Sense Resistor

A small capacitor connected to the CS with \( R_{\text{series}} \) forms a low-pass filter for noise filtering when the MOSFET turns on and off, as showed in Figure 15. The low-pass filter’s \( R \times C \) constant should not exceed 1/3 of the leading-edge blanking period for SCP (T_{LEB1}, 270ns, typical), otherwise the filtered sensed voltage cannot reach the SCP point (1.45V) to trigger SCP if an output short circuit occurs.

Over Power Compensation

HFC0500 has the over power compensation function (OPC) by drawing current from CS. The purpose of OPC is to minimize OLP difference caused by different input voltage. The offset current is proportional to the input peak voltage sensed by HV.

Suppose the resistor in current sensing loop is \( R_{\text{series}} \), and the input voltage 220Vac, then the compensation voltage on the CS can be calculated as:

\[
V_{\text{comp}} = R_{\text{series}} \cdot I_{\text{opc, 310V}}
\]  

(16)
The compensation criteria is making the FB voltage under full load condition is similar whether in high line or low line.

**Jitter Period**

Frequency jitter is an effective method to reduce EMI by dissipating energy. The $n$th-order harmonic noise bandwidth is $B_{tn} = n \cdot (2 \cdot \Delta f + f_{jitter})$, where $\Delta f$ is the frequency jitter amplitude. If $B_{tn}$ exceeds the resolution bandwidth (RBW) of the spectrum analyzer (200Hz for noise frequency less than 150 kHz, 9 kHz for noise frequency between 150 kHz to 30MHz), the spectrum analyzer receives less noise energy.

The capacitor on the TIMER determines the period of the frequency jitter. A 10µA current source charges the capacitor; when the TIMER voltage reaches 3.2V, another 10µA current source discharges the capacitor to 2.8V. This charging and discharging cycle repeats.

Equation (2) describes the jitter period in theory; a smaller $f_{jitter}$ is more effective at EMI reduction. However, the measurement bandwidth requires that $f_{jitter}$ should be large compared to spectrum analyzer RBW for effective EMI reduction. Also, $f_{jitter}$ should be less than the control-loop-gain crossover frequency to avoid disturbing the output voltage regulation. At the same time, we must consider the practical application when selected the Timer capacitor. Too large capacitor may cause failing startup at full load because of the long soft startup duration showed as equation (3). At the same time too small timer capacitor will cause timer period get smaller, so the timer count capability is overload, and some logic problem may be occurs. So for most applications, $f_{jitter}$ between 200Hz and 400Hz is recommended.

**X-Cap Discharge Time**

Figure 10 shows the X-cap discharger waveforms. The maximum discharge time occurs at a high-line input with no-load condition. The maximum discharge delay time is

$$T_{delay} = 32 \cdot T_{jitter} \quad (17)$$

The X-cap is discharged from a high-voltage constant current source ($I_{HV_{120V}}$, 2.5mA typically) into HV. The current-source discharge time for the X-cap to drop to 37% of peak voltage can be estimated by:

$$T_{discharge} = \frac{C_X \cdot 63\% \cdot \sqrt{2} \cdot V_{ac(max)}}{I_{HV_{120V}}} \quad (18)$$

Where $C_X$ is the X-cap capacitance, $V_{ac(max)}$ is the maximum AC-input RMS value.

The first discharging period is $16 \times T_{jitter}$, with subsequent period equal to $48 \times T_{jitter}$. Then the discharge sections times can approximately as:

$$n = \frac{T_{discharge} - 16 \cdot T_{jitter}}{48 \cdot T_{jitter}} + 1 \quad (19)$$

For every discharge section, there is a certain period ($16 \times T_{jitter}$) for detection as follow:

$$T_{detect} = 16 \cdot T_{jitter} \cdot (n - 1) \quad (20)$$

As a result, the total discharge time is then:

$$T_{total} = T_{delay} + T_{discharge} + T_{detect} \quad (21)$$

The total discharge time is relative to $T_{jitter}$ which is dependent on $C_{TIMER}$. For example, if $C_{TIMER}$ is 47nF and $T_{jitter}$=3.7ms, the X-cap discharge margin is 1s due to X-cap value tolerance ($\pm 10\%$ typically). It is recommended to select an X-cap less than 3.3μF.

Though the X-cap has been discharged, it may still retain a high-voltage on the bulk capacitor. For safety, make sure it is released before debugging the board.

**Ramp Compensation**

When adopting peak current control, sub harmonic oscillation will occur when $D>0.5$ in CCM. HFC0500 is equipped with internal ramp compensation to solve this problem. $\alpha$ is calculated by the following equation (22). For stable operation, $\alpha$ must be less than 1.

$$\alpha = \frac{m_a}{(1-m_a) \cdot \frac{V_{min}}{L_m} \cdot R_{sense} - m_a} - \frac{V_{min}}{L_m} \cdot R_{sense} + m_a \quad (22)$$

Where $m_a$=18mV/us, is the minimum internal slope value of the compensation ramp, $V_{min}$ is the minimum input voltage of the compensation ramp, $D_{max}$ is the maximum duty cycle, $R_{sense}$ is the sensed resistance, $L_m$ is the inductance, and $m_a$ is the slope of the ramp.
of the primary-side and equivalent secondary-side voltage sensed by CS resistor respectively.

**PCB Layout Guide**

PCB layout is very important to achieve reliable operation, good EMI performance and good thermal performance. Follow these guidelines to optimize performance:

1) Minimize the power stage loop area. This includes the input loop (C1 - T1 - Q1 – R11/R12/R13 – C1), the auxiliary winding loop (T1 – D4 – R4 – C3 – T1), and the output loop (T1 – D6 – C10 – T1).

2) The input loop GND and control circuit should be separate and only connect at C1.

3) Connecting the Q1 heat-sink to the primary GND plane to improve EMI.

4) Place the control circuit capacitors (such as those for FB, CS and VCC) close to IC to decouple noise.

**Design Example**

Below is a design example of HFC0500 for power adapter applications.

<table>
<thead>
<tr>
<th>Table 1: Design Spec.</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>VIN</strong></td>
</tr>
<tr>
<td><strong>VOUT</strong></td>
</tr>
<tr>
<td><strong>IOUT</strong></td>
</tr>
</tbody>
</table>

![PCB Layout](image)
TYPICAL APPLICATION CIRCUIT

Figure 17: Example of a Typical Application

Figure 18: Transformer Structure
### Table 2: Winding Order

<table>
<thead>
<tr>
<th>Tape (T)</th>
<th>Winding</th>
<th>Terminal Start—&gt;End</th>
<th>Wire Size (φ)</th>
<th>Turns (T)</th>
<th>Tube</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>N1</td>
<td>2—&gt;3</td>
<td>0.25mm²</td>
<td>30</td>
<td>matching with wire</td>
</tr>
<tr>
<td>1</td>
<td>N2</td>
<td>4—&gt;5</td>
<td>0.15mm²</td>
<td>7</td>
<td>matching with wire</td>
</tr>
<tr>
<td>2</td>
<td>E1</td>
<td>5—&gt;Nc</td>
<td>0.1mm²</td>
<td>Wind with tight tension across entire bobbin evenly</td>
<td></td>
</tr>
<tr>
<td></td>
<td>N3</td>
<td>P—&gt;N</td>
<td>0.5mm²(T,I,W)</td>
<td>11</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>E2</td>
<td>5—&gt;NC</td>
<td>0.1mm²</td>
<td>Wind with tight tension across entire bobbin evenly</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>N4</td>
<td>3—&gt;1</td>
<td>0.25mm²</td>
<td>30</td>
<td>matching with wire</td>
</tr>
</tbody>
</table>
FLOW CHART

UVLO, brown-out, OTP & OLP is auto restart, OVP on VCC and Latch-off on TIMER are latch mode

Release from the latch condition, need to unplug from the main input.

Figure19: Control Flow Chart
EVOLUTION OF THE SIGNALS IN PRESENCE OF FAULTS

Figure 20: Signal Evolution in the Presence of Faults
PACKAGE INFORMATION

SOIC8-7A

TOP VIEW

RECOMMENDED LAND PATTERN

FRONT VIEW

SIDE VIEW

NOTE:
1) CONTROL DIMENSION IS IN INCHES DIMENSION IN BRACKET IS IN MILLIMETERS
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING SHALL BE0.004” INCHES MAX.
5) JEDEC REFERENCE IS MS-012
6) DRAWING IS NOT TO SCALE

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