DESCRIPTION

HFC0400 is a fixed-frequency current-mode controller with built-in slope compensation. It targets medium-power, off-line, flyback, switch-mode power supplies. At light loads, the controller freezes the peak current and reduces its switching frequency down to 25kHz to offer excellent light-load efficiency.

At very light loads, the controller enters burst mode to achieve very low standby power consumption.

HFC0400 offers frequency jittering to help dissipate energy generated by conducted noise.

HFC0400 also has an X-cap discharge function to discharge the X-cap when the input is unplugged.

HFC0400 features multiple protections that include thermal shutdown (TSD), VCC under-voltage lockout (UVLO), overload protection (OLP), over-voltage protection (OVP), and brown-out protection.

HFC0400 is available in an SOIC8-7A package.

FEATURES

- Fixed-frequency current-mode control with built-in slope compensation
- Frequency foldback down to 25kHz at light loads
- Burst mode for low standby power consumption
- Frequency jitter to reduce EMI signature
- X-cap discharge function
- Internal high-voltage current source
- VCC under-voltage lockout with hysteresis (UVLO)
- Brown-out protection on HV pin
- Overload protection with programmable delay
- Thermal shutdown (auto-restart with hysteresis)
- Latch-off for external over-voltage protection (OVP) and over-temperature protection (OTP) on TIMER pin
- Short-circuit protection
- Programmable soft start

APPLICATIONS

- AC/DC adapters for notebook computers, tablets, and smartphones
- Offline battery chargers
- LCD TV s and monitors

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TYPICAL APPLICATION

![TYPICAL APPLICATION Diagram](image-url)
**ORDERING INFORMATION**

<table>
<thead>
<tr>
<th>Part Number*</th>
<th>Package</th>
<th>Top Marking</th>
</tr>
</thead>
<tbody>
<tr>
<td>HFC0400GS</td>
<td>SOIC8-7A</td>
<td>HFC0400</td>
</tr>
</tbody>
</table>

* For Tape & Reel, add suffix –Z (e.g. HFC0400GS–Z);

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**ABSOLUTE MAXIMUM RATINGS**

1. **HV Break Down Voltage** .............. –0.7V to 700V
2. **VCC, DRV to GND** ......................... –0.3V to 30V
3. **FB, TIMER, CS to GND** ................. –0.3V to 7V
4. **Continuous Power Dissipation** (T_J = 25°C) (2)

<table>
<thead>
<tr>
<th>Junction Temperature</th>
<th>150°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Shutdown</td>
<td>150°C</td>
</tr>
<tr>
<td>Thermal Shutdown Hysteresis</td>
<td>25°C</td>
</tr>
<tr>
<td>Lead Temperature</td>
<td>260°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-60°C to +150°C</td>
</tr>
<tr>
<td>ESD Capability Human Body Model (All Pins except HV)</td>
<td>4.0kV</td>
</tr>
<tr>
<td>ESD capability for Machine Mode</td>
<td>200V</td>
</tr>
</tbody>
</table>

**Recommended Operation Conditions** (3)

- Operating Junction Temp (T_J)........... -40°C to +125°C
- Operating VCC range ................. 8V to 20V

**Thermal Resistance** (4) θ_JA θ_JC

| SOIC8-7A | 96 | 45...°C/W |

**Notes:**

1. Exceeding these ratings may damage the device.
2. The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_JA, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A)θ_JA. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3. The device is not guaranteed to function outside of its operating conditions.
4. Measured on JESD51-7, 4-layer PCB.
## ELECTRICAL CHARACTERISTICS

For typical value $T_J=25^\circ C$, unless otherwise noted

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Start-up Current Source (HV)</td>
<td>$I_{HV}$</td>
<td>$V_{CC}=6V;V_{HV}=400V$</td>
<td>1.6</td>
<td>1.85</td>
<td>2.1</td>
<td>mA</td>
</tr>
<tr>
<td>Leakage Current from HV</td>
<td>$I_{HV}$</td>
<td>$V_{CC}=10V;V_{HV}=400V$</td>
<td>15</td>
<td>25</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>Break-Down Voltage</td>
<td>$V_{BR}$</td>
<td></td>
<td>700</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Supply Voltage Management (VCC)</td>
<td>$V_{CC}$</td>
<td></td>
<td>12</td>
<td>14.5</td>
<td>17</td>
<td>V</td>
</tr>
<tr>
<td>VCC Current-Source Turn-Off Level, Rising</td>
<td>$V_{CC_{OFF}}$</td>
<td></td>
<td>9.5</td>
<td>11.5</td>
<td>13.5</td>
<td>V</td>
</tr>
<tr>
<td>VCC Threshold for HV Turn-On Detection, Falling</td>
<td>$V_{CC_{SS}}$</td>
<td></td>
<td>1.5</td>
<td>1.6</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VCC Hysteresis for HV Turn-On Detection</td>
<td>$V_{CC_{OFF}} - V_{CC_{ON}}$</td>
<td></td>
<td>7.0</td>
<td>8.0</td>
<td>9.0</td>
<td>V</td>
</tr>
<tr>
<td>VCC Current-Source Turn-On Level, Falling</td>
<td>$V_{CC_{ON}}$</td>
<td></td>
<td>5.0</td>
<td>6.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VCC Re-charge Level When Protection Occurs</td>
<td>$V_{CC_{PRO}}$</td>
<td></td>
<td>4.7</td>
<td>5.3</td>
<td>5.9</td>
<td>V</td>
</tr>
<tr>
<td>VCC Decreasing Level When Latch-Off Phase Ends</td>
<td>$V_{CC_{LATCH}}$</td>
<td></td>
<td>2.5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Internal IC Consumption</td>
<td>$I_{CC}$</td>
<td>$V_{FB}=2V;C_L=1nF, V_{CC}=12V$</td>
<td>1</td>
<td>1.5</td>
<td>2</td>
<td>mA</td>
</tr>
<tr>
<td>Internal IC Consumption, Latch Off Phase</td>
<td>$I_{CC_{LATCH}}$</td>
<td>$V_{CC}=6V$</td>
<td>520</td>
<td>585</td>
<td>650</td>
<td>µA</td>
</tr>
<tr>
<td>Voltage above $V_{CC}$ Where the Controller Latches Off (OVP)</td>
<td>$V_{OVP}$</td>
<td></td>
<td>22</td>
<td>25</td>
<td>27</td>
<td>V</td>
</tr>
<tr>
<td>OVP Comparator Blanking Duration</td>
<td>$t_{OVP}$</td>
<td></td>
<td>26</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>Brown-out</td>
<td>$V_{HV}$</td>
<td>$V_{HV}$ rising</td>
<td>95</td>
<td>108</td>
<td>120</td>
<td>V</td>
</tr>
<tr>
<td>HV Turn-On Threshold</td>
<td>$V_{HV_{ON}}$</td>
<td></td>
<td>90</td>
<td>103</td>
<td>115</td>
<td>V</td>
</tr>
<tr>
<td>HV Turn-Off Threshold</td>
<td>$V_{HV_{OFF}}$</td>
<td>$V_{HV}$ falling</td>
<td>4</td>
<td>5.2</td>
<td>6.4</td>
<td>V</td>
</tr>
<tr>
<td>Brown-Out Hysteresis</td>
<td>$\Delta V_{HV}$</td>
<td></td>
<td>4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Timer Duration for Line Cycle Drop-out</td>
<td>$t_{HV}$</td>
<td>$C_{TIME}=47nF$</td>
<td>50</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>Oscillator</td>
<td>$f_{OSC}$</td>
<td></td>
<td>60</td>
<td>65</td>
<td>69.5</td>
<td>kHz</td>
</tr>
<tr>
<td>Oscillator Frequency</td>
<td>$f_{OSC}$</td>
<td></td>
<td>60</td>
<td>65</td>
<td>69.5</td>
<td>kHz</td>
</tr>
<tr>
<td>Frequency Jitter Amplitude, in Percentage of $f_{OSC}$</td>
<td>$A_{jitter}$</td>
<td></td>
<td>±6.7</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>Frequency Jitter Modulation Period</td>
<td>$t_{jitter}$</td>
<td>$C_{TIME}=47nF$</td>
<td>3.7</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>Current Sense</td>
<td>$V_{ILIM}$</td>
<td></td>
<td>0.9</td>
<td>0.95</td>
<td>1</td>
<td>V</td>
</tr>
<tr>
<td>Current Limit</td>
<td>$V_{ILIM}$</td>
<td></td>
<td>0.9</td>
<td>0.95</td>
<td>1</td>
<td>V</td>
</tr>
<tr>
<td>Short-Circuit Protection Level</td>
<td>$V_{SCP}$</td>
<td></td>
<td>1.3</td>
<td>1.45</td>
<td>1.55</td>
<td>V</td>
</tr>
<tr>
<td>Leading-Edge Blanking for $V_{ILIM}$</td>
<td>$T_{LEB1}$</td>
<td></td>
<td>350</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Leading-Edge Blanking for $V_{SCP}$</td>
<td>$T_{LEB2}$</td>
<td></td>
<td>270</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Slope of the Compensation Ramp</td>
<td>$S_{RAMP}$</td>
<td></td>
<td>20</td>
<td>25</td>
<td>30</td>
<td>mV/µs</td>
</tr>
</tbody>
</table>
### ELECTRICAL CHARACTERISTICS (continued)

For typical value $T_J=25^\circ C$, unless otherwise noted

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Feedback (FB)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Internal Pull-Up Resistor</td>
<td>$R_{FB}$</td>
<td></td>
<td>12</td>
<td>14</td>
<td>16.5</td>
<td>kΩ</td>
</tr>
<tr>
<td>Internal Pull-Up Voltage</td>
<td>$V_{DD}$</td>
<td></td>
<td></td>
<td>4.3</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{FB}$ to Internal Current Set-Point Division Ratio</td>
<td>$K_{FB}$</td>
<td></td>
<td></td>
<td>3.0</td>
<td></td>
<td>--</td>
</tr>
<tr>
<td>FB Level (Falling) at which the Controller Enters Burst Mode</td>
<td>$V_{BURL}$</td>
<td></td>
<td>0.29</td>
<td>0.32</td>
<td>0.35</td>
<td>V</td>
</tr>
<tr>
<td>FB Level (Rising) at which the Controller Exits Burst Mode</td>
<td>$V_{BURH}$</td>
<td></td>
<td>0.42</td>
<td>0.46</td>
<td>0.50</td>
<td>V</td>
</tr>
<tr>
<td><strong>Over Load Protection</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FB Level at which the Controller Enters OLP after Blanking Time</td>
<td>$V_{OLP}$</td>
<td></td>
<td>3.7</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Time Duration When FB Reaches Protection Point, Before OLP</td>
<td>$T_{OLP}$</td>
<td>$C_{TIMER}=47nF$</td>
<td></td>
<td>50</td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td><strong>Frequency Foldback</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Frequency Foldback FB Voltage Threshold, Upper Limit</td>
<td>$V_{FB(FOLD)}$</td>
<td></td>
<td>1.8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Minimum Switching Frequency</td>
<td>$f_{OSC(min)}$</td>
<td></td>
<td>21</td>
<td>25</td>
<td>30</td>
<td>kHz</td>
</tr>
<tr>
<td>Frequency Foldback FB Voltage Threshold, Lower Limit</td>
<td>$V_{FB(FOLDE)}$</td>
<td></td>
<td>1.0</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td><strong>Latch-Off Input (Integration in TIMER )</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>The Threshold below which Controller is Latched</td>
<td>$V_{TIMER(LATCH)}$</td>
<td></td>
<td>0.9</td>
<td>1</td>
<td>1.1</td>
<td>V</td>
</tr>
<tr>
<td>Blanking Duration on Latch Detection</td>
<td>$\tau_{LATCH}$</td>
<td></td>
<td>12</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td><strong>DRV Voltage</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Driver Voltage High Level</td>
<td>$V_{High}$</td>
<td>$C_L=1nF$, $V_{CC}=8.4V$</td>
<td>6.7</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$C_L=1nF$, $V_{CC}=12V$</td>
<td>10.3</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Driver Voltage-Clamp Level</td>
<td>$V_{Clamp}$</td>
<td>$C_L=1nF$, $V_{CC}=24V$</td>
<td>13.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Driver Voltage, Low Level</td>
<td>$V_{Low}$</td>
<td>$C_L=1nF$, $V_{CC}=24V$</td>
<td>16</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>Driver Voltage, Rise Time</td>
<td>$\tau_{R}$</td>
<td>$C_L=1nF$, $V_{CC}=16V$</td>
<td>13</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Driver Voltage, Fall Time</td>
<td>$\tau_{F}$</td>
<td>$C_L=1nF$, $V_{CC}=16V$</td>
<td>23</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Driver Pull-Up Resistance</td>
<td>$R_{Pull-up}$</td>
<td>$C_L=1nF$, $V_{CC}=16V$</td>
<td>8</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>Driver Pull-Down Resistance</td>
<td>$R_{Pull-down}$</td>
<td>$C_L=1nF$, $V_{CC}=16V$</td>
<td>20</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
</tbody>
</table>

---

NOT RECOMMENDED FOR NEW DESIGN

HFC0400 Rev. 1.02
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7/10/2018
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# PIN FUNCTIONS

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>TIMER</td>
<td>Timer. This pin combines the soft start, frequency jittering, and timer functions for OLP, brown-out protection, and X-cap discharge. Latch the IC by pulling this pin down.</td>
</tr>
<tr>
<td>2</td>
<td>FB</td>
<td>Feedback. Use a pull-down optocoupler to control output regulation.</td>
</tr>
<tr>
<td>3</td>
<td>CS</td>
<td>Current Sense. Senses the primary current for current-mode operation.</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>IC Ground.</td>
</tr>
<tr>
<td>5</td>
<td>DRV</td>
<td>Drive Signal Output.</td>
</tr>
<tr>
<td>6</td>
<td>VCC</td>
<td>Power Supply.</td>
</tr>
<tr>
<td>8</td>
<td>HV</td>
<td>High-Voltage Current Source. Includes brown-out and X-cap discharge functions.</td>
</tr>
</tbody>
</table>

**NOT RECOMMENDED FOR NEW DESIGN**

REFER TO HFC0500
TYPICAL CHARACTERISTICS (continued)

VCC Re-charge Level when Protection Occurs vs. Temperature

VCC Decreasing Level When Latch-off Phase Ends vs. Temperature

HV Turn-on Threshold vs. Temperature

HV Turn-off Threshold vs. Temperature

Oscillator Frequency vs. Temperature

Frequency Jitter Amplitude, in Percentage of f_{OSC} vs. Temperature

Minimum Switching Frequency vs. Temperature

Slope of the Compensation Ramp vs. Temperature

Current Limit vs. Temperature

NOT RECOMMENDED FOR NEW DESIGN
TYPICAL CHARACTERISTICS (continued)

- Short-Circuit Protection Level vs. Temperature
- Leading-Edge Blanking for VILIM vs. Temperature
- Leading Edge Blanking for VSCP vs. Temperature
- FB Level (Falling) at which the Controller Enters Burst Mode vs. Temperature
- FB Level (Rising) at which the Controller Exits Burst Mode vs. Temperature
- FB Level at which the Controller Enters OLP after Blanking Time vs. Temperature
- FB Internal Pull-up Resistor vs. Temperature
- FB Internal Pull-up Voltage vs. Temperature
TYPICAL PERFORMANCE CHARACTERISTIC

\[ V_{\text{IN}}=230\text{VAC}, \ V_{\text{OUT1}}=5\text{V}, \ I_{\text{OUT1}}=3\text{A}, \ V_{\text{OUT2}}=16\text{V}, \ I_{\text{OUT2}}=1.5\text{A}, \ T_{A}=25^\circ\text{C}, \] unless otherwise noted.
TYPICAL PERFORMANCE CHARACTERISTIC (continued)

VIN=230VAC, VOUT1=5V, IOUT1=3A, VOUT2=16V, IOUT2=1.5A, TA=25°C, unless otherwise noted.

OVP

OTP Entry

OTP Recovery

Brown-in

Brown-out

X-cap Discharge

VIN=75VAC

VIN=72VAC

VIN=265VAC, CX=0.22μF, No Load

X-cap Discharge, 
VIN=265VAC, CX=0.22μF, Full Load

Conducted EMI

1MHz 10MHz

1MHz 10MHz

EN55022Q
EN55022A
EN55022A
150kHz 30MHz
150kHz 30MHz
TYPICAL PERFORMANCE CHARACTERISTIC (continued)

$V_{IN}=230\text{VAC}$, $V_{OUT1}=5\text{V}$, $I_{OUT1}=3\text{A}$, $V_{OUT2}=16\text{V}$, $I_{OUT2}=1.5\text{A}$, $T_{A}=25^\circ\text{C}$, unless otherwise noted.

**No Load Power Consumption**

<table>
<thead>
<tr>
<th>$V_{IN}$ (VAC/Hz)</th>
<th>85/60</th>
<th>115/60</th>
<th>230/50</th>
<th>265/50</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_{IN}$ (mW)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5V/0A, 16V/0A</td>
<td>26.35</td>
<td>27.59</td>
<td>32.40</td>
<td>35.26</td>
</tr>
<tr>
<td>5V/6mA, 16V/0A</td>
<td>71.92</td>
<td>72.72</td>
<td>80.70</td>
<td>84.83</td>
</tr>
</tbody>
</table>
OPERATION

HFC0400 incorporates all the necessary features to build a reliable switch-mode power supply. It is a fixed-frequency current-mode controller with built-in slope compensation. At light loads, the controller freezes the peak current and reduces its switching frequency down to 25kHz to minimize switching losses. When the output power falls below a given level, the controller enters burst mode. It also has excellent EMI performance thanks to frequency jittering.

Its high level of integration requires very few external components.

Figure 1: Functional Block Diagram
Fixed-Frequency with Jitter

Frequency jitter reduces EMI by dissipating the energy. Figure 2 shows the circuit of frequency jittering.

![Frequency Jitter Circuit](image)

**Figure 2: Frequency Jitter Circuit**
A controlled current sourced (fixed at 2.72μA when V_FB=2V) charges the internal 14pF capacitor. Comparing the capacitor voltage to the TIMER voltage estimates the switching frequency as per equation (1). V_TIMER is a triangular wave that ranges between 2.8V and 3.2V with a charging/discharging current of 10μA. Figure 3 shows the frequency jitter, τ_jitter, as per equation (2).

\[
\begin{align*}
\tau_{\text{jitter}} &= \frac{C_{\text{TIMER}} \cdot (3.2V - 2.8V)}{10\mu A} \\
f_s &= \frac{14pF \cdot V_{\text{TIMER}}}{2.72\mu A + 0.2\mu s}
\end{align*}
\]

**Figure 3: Frequency Jitter**

Frequency Foldback

The HFC0400 implements frequency foldback at light load condition to improve overall efficiency. When the load decreases to a given level (1.33V<V_FB<2V), the controller freezes the peak current (as measured as the voltage on the CS pin, 0.67V) and reduces its switching frequency down to 25kHz which helps to reduce the switching loss. If the load continues to decrease, the peak current decreases at a 25kHz fixed frequency to avoid audible noise. Figure 4 shows the frequency vs. V_FB and peak current (V_CS) vs. V_FB.

**Figure 4: Frequency and Peak Current (V_CS) vs V_FB**

Current-Mode Operation with Slope Compensation

V_FB controls the primary-peak current. When the peak current reaches the level determined by V_FB, DRV turns off. The controller can also be used in continuous conduction mode (CCM) with a wide input voltage range because its internal synchronous slope compensation (30mV/μs) avoids sub-harmonic oscillations when the duty cycle exceeds 50%.

High Voltage Startup Current Source with Brown-Out Detection

Initially, the internal high-voltage current source drawn from the HV pin supplies the IC. The IC turns off the current source as soon as V_CC reaches 14.5V and detects the voltage on HV. Once the HV voltage exceeds HV_on before V_CC drops down to 11.5V, the controller starts switching. Otherwise the system treats the condition as a brown-out to to lock the driver.
output, causing \( V_{CC} \) to drop down to 5.3V and the high-voltage current source turns on to recharge \( V_{CC} \). The auxiliary transformer winding supplies the IC after the controller starts switching. If \( V_{CC} \) falls below 8.0V, the switching pulse stops and the current source turns on again. Figure 5 shows the typical \( V_{CC} \) under-voltage lockout waveform.

![Figure 5: VCC Under-Voltage Lockout](image)

The \( V_{CC} \) lower threshold UVLO drops from 8V to 5.3V under fault conditions, such as OLP, SOP, brown-out, OVP, and OTP.

**Soft Start**

The peak current (controlled by the TIMER voltage) gradually increases from 0.25V to 1V, as does the switching frequency, to reduce the stress on power components and to smoothly establish the output voltage as the TIMER voltage increases from 1V to 1.75V during startup. Figure 6 shows the typical soft-start waveform. The TIMER capacitor determines the startup duration as per equation (3).

\[
\tau_{\text{Soft-start}} = \frac{C_{\text{TIMER}} \cdot (1.75V - 1V)}{10/4\mu A}
\]  

**Burst Mode**

The HFC0400 enters burst-mode operation to minimize power dissipation at no load or light load. As the load decreases, \( V_{FB} \) decreases. The IC stops the switching cycle when \( V_{FB} \) drops below the lower threshold, \( V_{BRUL} = 0.32V \). The output voltage starts to drop, which causes \( V_{FB} \) to increase again. Once \( V_{FB} \) exceeds \( V_{BRUH} = 0.46V \), switching resumes. \( V_{FB} \) then rises and falls repeatedly. Burst mode alternately enables and disables MOSFET switching, thereby reducing no load or light load switching losses.

**Timer-Based Over-Load Protection**

In a flyback converter, a fixed switching frequency results in a peak-current-limited maximum output power. When the output demand exceeds the power limit, the output voltage drops below the set value. Then the current flowing through primary and secondary optocoupler falls and \( V_{FB} \) is pulled high. The HFC0400 implements a timer-based OLP block as per Figure 7.

![Figure 7: Overload Protection Block](image)
When FB exceeds 3.7V (considered an error), the timer starts to count the VQ rising edge. Removing the error flag resets the timer. If the timer reaches its completion (a count of 17), OLP triggers. This timer duration avoids triggering OLP during the power supply start-up or a load transition phase. Figure 8 shows OLP.

**Figure 8: Overload Protection**

**Timer-Based Brown-Out Protection**

The brown-out protection block is similar to the OLP block. When the HV voltage drops below HV\textsubscript{OFF} (which is an error), the timer starts to count the V\textsubscript{Q} rising edges. Once the HV voltage exceeds HV\textsubscript{OFF}, the timer resets. When the timer has counted to 17, brown-out protection triggers and the switching pulse stops.

**Short-Circuit Protection (SCP)**

The HFC0400 has short-circuit protection that senses the CS voltage and stops switching if V\textsubscript{CS} reaches 1.5V after a reduced leading-edge blanking (LEB) time. As soon as the fault disappears, the power supply resumes operation.

**Thermal Shutdown (TSD)**

To prevent from any lethal thermal damage, HFC0400 shuts down switching when the inner temperature exceeds 150°C. As soon as the inner temperature drops below 125°C, the power supply resumes operation. During TSD, the V\textsubscript{CC} UVLO lower threshold drops from 8.0V to 5.3V.

**V\textsubscript{CC} Over-Voltage Protection (OVP)**

The HFC0400 enters latched fault condition if V\textsubscript{CC} goes above 25V for 25\mu s. The controller stays fully latched until V\textsubscript{CC} drops below 2.5V, e.g. when the user power-cycles the main input.

**TIMER Latch-Off for OVP and OTP**

Pulling TIMER down below 1.0V for 12\mu s latches the HFC0400 off for external OVP and OTP etc.

**X-Cap Discharge Function**

X-caps typically filters the differential-mode EMI noise from a power supply’s input. These components pose a potential hazard because they can store unsafe levels of high-voltage energy for long after the AC line is disconnected. Resistors in parallel to the X-cap provide a discharge path to meet safety standards, but constantly dissipate power while the AC is connected, and contribute to no-load and standby input power consumption.

**Figure 9: X-Cap Discharger**

The HFC0400’s HV acts as a smart X-cap discharger. In the presence of an AC voltage, the internal high-voltage current source turns off to block HV current flow and the IC monitors the HV voltage. Upon removing the AC voltage, the IC turns on the high-voltage current source after about 32 TIMER cycles to discharge the X-cap. The first discharge duration is 16 cycles, then the IC turns off the current source for 16 cycles to detect the presence of the AC line. If the AC input remains disconnected, the IC turns on the current source for 48 cycles, then off for 16 cycles repeatedly until the voltage on X-cap drops to V\textsubscript{CC}. Upon detecting an AC input, the high-voltage current source remains off until V\textsubscript{CC}
drops to $V_{CC_{PRO}}$ (5.3V) before recharging $V_{CC}$ to restart the system. Figure 9 shows the discharge function waveforms.

This approach provides a discharge path for the X-cap, eliminating discharge resistors and reduce power loss.

**Clamped Driver**

The DRV voltage is safely clamped at 13.4V when $V_{CC}$ exceeds 16V, allowing the use of any standard MOSFET.

**Leading-Edge Blanking**

An internal leading-edge blanking (LEB) unit containing two LEB times is employed between the CS pin and the current comparator input to avoid premature switching pulse termination due to the parasitic capacitances. During the blanking time, the current comparator is disabled and can not turn off the external MOSFET. Figure 10 shows the LEB waveform.

![Figure 10: Leading-Edge Blanking](image)

$T_{LEB1}=350\,\text{ns}$

$T_{LEB2}=270\,\text{ns}$ for SCP
APPLICATION INFORMATION

VCC Capacitor Selection

![Start-Up Circuit diagram](image)

**Figure 11: Start-Up Circuit**

Figure 11 shows the start-up circuit. The values of R1 and C1 determine the system start-up delay time: a larger R1 or C1 increases the start-up delay. The VCC duration (from VCC,OFF to VCC,SS) for brown-out detection should exceed half the input period, equation (4) provides an estimated value for the VCC capacitor, where ICC(noswitch) is the internal consumption (close to ICC(charge)) and τinput is period of the AC input. For most applications, chose a VCC capacitor value that exceeds 10μF.

\[
C_{VCC} = \frac{I_{CC(noswitch)} \cdot 2.5}{VCC_{OFF} - VCC_{SS}} \tag{4}
\]

**Primary-Side Inductor Design (L_m)**

With built-in slope compensation, HFC0400 supports CCM when the duty cycle exceeds 50%. Set a ratio \(K_P\) of the primary inductor’s ripple current amplitude vs. the peak current value to \(0 < K_P \leq 1\), where \(K_P = 1\) for DCM. Figure 12 shows the relevant waveforms. A larger inductor leads to a smaller \(K_P\) leads, which can reduce RMS current but increase transformer size. An optimal \(K_P\) value is between 0.6 and 0.8 for the universal input range and 0.8 to 1 for a 230VAC input range.

![Typical Primary-Current Waveform](image)

**Figure 12: Typical Primary-Current Waveform**

The input power \(P_{in}\) at the minimum input can be estimated as

\[
P_{in} = \frac{V_O \cdot I_O}{\eta} \tag{5}
\]

Where \(V_O\) is the output voltage, \(I_O\) is the rated output current, \(\eta\) is the estimated efficiency. Generally, \(\eta\) is between 0.75 and 0.85 depending on the input range and output application.

For CCM at minimum input, the converter duty cycle is:

\[
D = \frac{(V_O + V_F) \cdot N}{(V_O + V_F) \cdot N + V_{in(min)}} \tag{6}
\]

Where:

\(V_F\) is the secondary diode’s forward voltage,

\(N\) is the transformer turn ratio, and

\(V_{in(min)}\) is the minimum voltage on bulk capacitor.

The MOSFET turn-on time is

\[
\tau_{on} = D \cdot \tau_s \tag{7}
\]

Where \(\tau_s\) is the frequency jitter’s dominant switching period, \(\frac{1}{\tau_s} = f_s = 65kHz\).

The average, peak, ripple and valley values of the primary current are described as follows:

\[
I_{av} = \frac{P_{in}}{V_{in(min)}} \tag{8}
\]

\[
I_{peak} = \frac{I_{av}}{1 - \frac{K_P}{2}} \cdot D \tag{9}
\]

\[
I_{ripple} = K_P \cdot I_{peak} \tag{10}
\]

\[
I_{valley} = (1 - K_P) \cdot I_{peak} \tag{11}
\]
The following equation estimates $L_m$ as

$$L_m = \frac{V_{in(min)} \cdot \tau_{on}}{I_{ripples}} \quad (12)$$

**Current-Sense Resistor**

A small capacitor connected to the CS pin with $R_{series}$ forms a low-pass filter for noise filtering when the MOSFET turns on and off, as shown in Figure 14. The series resistance ($R_{series}$) should not exceed 1kΩ. The low-pass filter’s $R \times C$ constant should not exceed 1/3 of the leading-edge blanking period for SCP (LEB2, 270ns), or the filtered sensed voltage won’t reach the SCP point (1.5V) to trigger SCP if an output short circuit occurs.

**Jitter Period**

Frequency jitter is an effective method to reduce EMI by dissipating energy. The nth-order harmonic noise bandwidth is $B_{Tn} = n \cdot (2 \cdot \Delta f + f_{jitter})$, where $\Delta f$ is the frequency jitter amplitude. If $B_{Tn}$ exceeds the resolution bandwidth (RBW) of the spectrum analyzer (200Hz for noise frequency less than 150 kHz, 9 kHz for noise frequency between 150kHz to 30MHz), the spectrum analyzer receives less noise energy.

The capacitor on the TIMER pin determines the period of the frequency jitter. A 10μA current source charges the capacitor; when the TIMER voltage reaches 3.2V, another 10μA current

$$P_{sense} = \left(\frac{I_{peak} + I_{valley}}{2}\right)^2 + \frac{1}{12}\left(\frac{I_{peak} - I_{valley}}{2}\right)^2 \cdot D \cdot R_{sense} \quad (15)$$

**Low-Pass Filter on CS Pin**

Figure 14: Low-Pass Filter on CS Pin

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The capacitor on the TIMER pin determines the period of the frequency jitter. A 10μA current source charges the capacitor; when the TIMER voltage reaches 3.2V, another 10μA current
source discharges the capacitor to 2.8V. This charging and discharging cycle repeats.

Equation (2) describes the jitter period. In theory, a smaller $f_{\text{jitter}}$ is more effective at EMI reduction. However, the measurement bandwidth requires that $f_{\text{jitter}}$ should be large compared to spectrum analyzer RBW for effective EMI reduction. Also, $f_{\text{jitter}}$ should be less than the control-loop-gain crossover frequency to avoid disturbing the output voltage regulation. So for most applications, select $f_{\text{jitter}}$ between 200Hz and 400Hz.

**X-Cap Discharge Time**

Figure 9 shows the X-cap discharger waveforms. The maximum discharge time occurs at a high-line input and under no-load because the energy on X-cap dissipates but won’t transfer to the bulk capacitor.

The maximum discharge delay time is

$$
\tau_{\text{delay}} = 32 \cdot \tau_{\text{jitter}}
$$

(16)

When the high-voltage current source turns on, a constant supply current ($I_{HV}$, 1.6mA typically) flows into HV. The current-source discharge time for the X-cap to drop to 37% of peak voltage can be estimated by:

$$
\tau_{\text{discharge}} = \frac{C_X \cdot 63\% \cdot \sqrt{2}}{V_{\text{ac(max)}}}
$$

(17)

Where $C_X$ is the X-cap capacitance, $V_{\text{ac(max)}}$ is the maximum AC-input RMS value.

The first discharging period is $16 \cdot \tau_{\text{jitter}}$, with subsequent period equal to $48 \cdot \tau_{\text{jitter}}$. The sections times approximately equals:

$$
n = \frac{\tau_{\text{discharge}} - 16 \cdot \tau_{\text{jitter}}}{48 \cdot \tau_{\text{jitter}}} + 1
$$

(18)

Rounding n determines the number of detecting sections, as every section is $16 \cdot \tau_{\text{jitter}}$, the detecting time is shown as follow:

$$
T_{\text{detect}} = 16 \cdot \tau_{\text{jitter}} \cdot n
$$

(19)

As a result, the total discharge time is then.

$$
\tau_{\text{total}} = \tau_{\text{delay}} + \tau_{\text{discharge}} + T_{\text{detect}}
$$

(20)

The total discharge time is relative to $\tau_{\text{jitter}}$. For example, if $C_{\text{TIMER}}$ is 47nF and $f_{\text{jitter}}=3.7ms$, the X-cap discharge margin is 1s due to X-cap value deviations (around ±10% typically), select an X-cap less than 3.3μF.

Though the X-cap has been discharged, it may still retain a high-voltage on the bulk capacitor. For safety, make sure it is released before the debugging the board.

**PCB Layout Guide**

PCB layout is important to achieve reliable operation, good EMI performance, and good thermal performance. Follow these guidelines to optimize performance.

1) Minimize the power stage switching stage loop area. This includes the input loop (C1 - T1 - Q1 - R12/R13 – C1), the auxiliary winding loop (T1 – D4 – R4 – C3 – T1), and the output loop (T1 – D6 – C10 – T1 and T1 – D7 – CT4 – T1).

2) The input loop GND and control circuit should be separate and only connect at C1.

3) Connecting the Q1 heatsink to the primary GND plane improves EMI.

4) Place the control circuit capacitors (such as those for FB, CS and VCC pins) close to IC to decouple noise.
Design Example
Below is a design example of HFC0400 for dual-output applications.

Table 1—Design Spec.

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$</td>
<td>85 to 265VAC</td>
</tr>
<tr>
<td>$V_{OUT1}$</td>
<td>5V</td>
</tr>
<tr>
<td>$I_{OUT1}$</td>
<td>3A</td>
</tr>
<tr>
<td>$V_{OUT2}$</td>
<td>16V</td>
</tr>
<tr>
<td>$I_{OUT2}$</td>
<td>1.5A</td>
</tr>
</tbody>
</table>

**Typical Application Circuit**

Input: 85-265Vac

**Figure 15: PCB Layout**

**Figure 16: Example of a Typical Application**

**Note:** This document is not recommended for new design. Refer to HFC0500.
a) Connection Diagram

b) Winding Diagram

Figure 17: Transformer Structure

Table 2—Winding Order

<table>
<thead>
<tr>
<th>Tape (T)</th>
<th>Winding</th>
<th>Margin Wall PRI side</th>
<th>Terminal Start—&gt;End</th>
<th>Margin Wall SEC side</th>
<th>Wire Size (φ)</th>
<th>Turns (T)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>N1</td>
<td>2mm</td>
<td>3—&gt;2</td>
<td>2mm</td>
<td>0.27mm*2</td>
<td>28</td>
</tr>
<tr>
<td>1</td>
<td>N6</td>
<td>2mm</td>
<td>1—&gt;NC</td>
<td>2mm</td>
<td>0.3mm*1</td>
<td>20</td>
</tr>
<tr>
<td>3</td>
<td>N4</td>
<td>2mm</td>
<td>7,8—&gt;9,10</td>
<td>2mm</td>
<td>0.33mm*12</td>
<td>3</td>
</tr>
<tr>
<td>1</td>
<td>N3</td>
<td>2mm</td>
<td>11,12—&gt;7,8</td>
<td>2mm</td>
<td>0.33mm*5</td>
<td>6</td>
</tr>
<tr>
<td>1</td>
<td>N2</td>
<td>2mm</td>
<td>5—&gt;6</td>
<td>2mm</td>
<td>0.27mm*1</td>
<td>9</td>
</tr>
<tr>
<td>2</td>
<td>N5</td>
<td>2mm</td>
<td>2—&gt;1</td>
<td>2mm</td>
<td>0.27mm*2</td>
<td>29</td>
</tr>
</tbody>
</table>
FLOW CHART

Figure 18: Control Flow Chart
Figure 19: Signal Evolution in the Presence of Faults
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HFC0400 – FIXED-FREQUENCY FLYBACK CONTROLLER WITH ULTRA-LOW NO LOAD POWER CONSUMPTION

PACKAGE INFORMATION

SOIC8-7A

NOTE:
1) CONTROL DIMENSION IS IN INCHES DIMENSION IN BRACKET IS IN MILLIMETERS
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING SHALL BE 0.004" INCHES MAX.
5) JEDEC REFERENCE IS MS-012
6) DRAWING IS NOT TO SCALE

NOT RECOMMENDED FOR NEW DESIGN