EVQ79700FS-R-00A

MPSafe™ ASIL-D 12-Channel Power Sequencer Evaluation Board, AEC-Q100 Qualified

DESCRIPTION

The EVQ79700FS-R-00A evaluation board is designed to demonstrate the capabilities of the MPQ79700FS, a 12-channel, functional safety power sequencer. The MPQ79700FS is engineered to provide precise power sequencing and safety functions for automotive advanced driver assistance systems (ADAS) and autonomous driving platforms.

The MPQ79700FS's configurability and flexibility enable design reuse across different applications and system-on-chip (SoC) generations.

The MPQ79700FS contains a crystal driver, a real-time clock (RTC) with an alarm function, a configurable watchdog that can be accessed through the I²C interface, and active-low system reset and interrupt outputs.

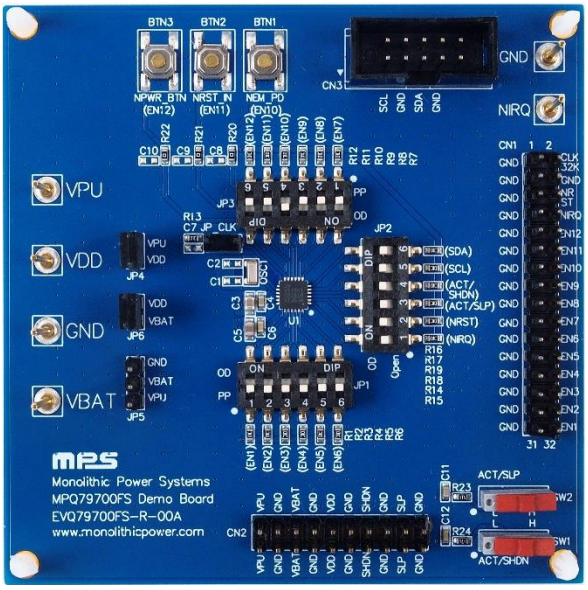
Safety mechanisms such as built-in self-test (BIST) provide high diagnostic coverage, which help the system achieve its target ASIL rating.

The EVQ79700FS-R-00A is a fully assembled and tested evaluation board. The MPQ79700FS is available in a QFN-24 (4mmx4mm) package with wettable flanks.

PERFORMANCE SUMMARY

Parameters	Conditions	Value
Supply voltage (V_{DD}) range		2.7V to 5.5V
Power-up voltage (V_{PU}) range		0.9V to V_{DD}
Backup battery voltage (V_{BAT}) range		1.85V to 5.5V
CLK32K output frequency accuracy	Nominal 32.768kHz at T_A = 25°C	±100ppm

EVQ79700FS-R-00A EVALUATION BOARD



LxWxH (8.35cmx8.35cmx1cm)

Board Number	MPS IC Number
EVQ79700FS-R-00A	MPQ79700FSGRE-0000-AEC1

QUICK START GUIDE

1. Preset the power supply between 2.7V and 5.5V, then turn off the power supply.
2. Connect the power supply terminals to:
   a. Positive (+): VDD
   b. Negative (-): GND
3. To connect jumpers on JP4, JP5, JP6, and JP_CLK, follow the steps below:
   a. Tie VPU to VDD to connect a jumper on JP4.
   b. JP5 is not connected.
   c. Tie VBAT to VDD to connect a jumper on JP6.
   d. Tie CLK32K to VPU via R13 to connect a jumper on JP_CLK.
4. To toggle the switches on JP1, JP2, and JP3, refer to Figure 4 on page 13 and follow the steps below:
   a. For JP1, toggle JP1-1, JP1-2, JP1-3, JP1-4, JP1-5, and JP1-6 to the PP silk print side.
   b. For JP2, toggle JP2-1, JP2-2, JP2-3, JP2-4, JP2-5, and JP2-6 to the OD silk print side.
   c. For JP3, toggle JP3-1, JP3-2, JP3-3, JP3-5, and JP3-6 to the PP silk print side; toggle JP3-4 to the OD silk print side.
5. Toggle SW1 to the H silk print side, and toggle SW2 to either the H or L silk print side (see Figure 4 on page 13).
6. After making the connections, turn on the power supply. The board should automatically start up. EN1–EN11 and CLK32K start up sequentially, and NRST and NRIQ de-assert. Meanwhile, EN12 remains pulled low as the default register configuration since it is not mapped in sequence.
7. To test with the connecters, CN1, CN2, and CN3, follow the steps below:
   a. CN1 is the test points of all the outputs (including EN1–EN12, NIRQ, NRST, and CLK32K). The detailed position of each output is printed on the evaluation board.
   b. CN2 is the test points of all the inputs (including VDD, VBAT, VPU, ACT/SHDN, and ACT/SLP). The detailed position of each output is printed on the evaluation board.
   c. CN3 is the interface of the EVKT-USBI2C-02, a MPS I²C evaluation kit. The EVKT-USBI2C-02 is included with product evaluation kits or can be purchased separately.
8. To evaluate the MPQ79700FS using the I²C interface, follow the steps below:
   a. Download and install Virtual Bench Pro 4.0, the MPQ79700FS's graphic user interface (GUI).
   b. Connect the EVKT-USBI2C-02 to CN3 and the computer with a ribbon cable and USB cable, respectively (see Figure 1).

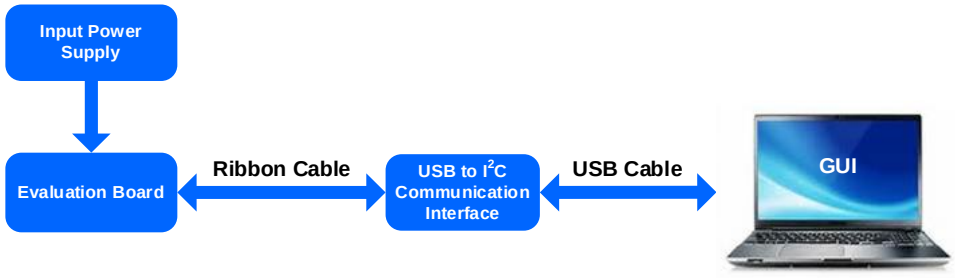


Figure 1: I²C Evaluation Kit Set-Up

c. Use the MPQ79700FS's GUI to scan for the evaluation board I²C address (3Ch default).

d. After the I²C interface is connected, evaluate the MPQ79700FS's performance including the ENx sequence order, time slot, and delay.

9. The EN10 pin's default configuration on the evaluation board is NEM_PD. Use BTN1 as the NEM_PD input.

10. To evaluate the sequence transitions, follow the steps below:

a. Toggle SW1 (ACT/SHDN) to trigger the start-up or shutdown sequence. If an external signal is used to control the ACT/SHDN pin, toggle SW1 high and apply the external signal to CN1's SHDN pin. ACT/SHDN's logic-high and logic-low thresholds are 0.84V and 0.36V, respectively.

b. To evaluate sleep mode, enable sleep mode via the I²C, then toggle SW2 (ACT/SLP) to trigger the sleep mode entry or exit sequence. If an external signal is used to control the ACT/SLP pin, toggle SW2 high and apply the external signal to CN1's SLP pin. ACT/SLP's logic-high and logic-low thresholds are 0.84V and 0.36V, respectively.

c. Use the MPQ79700FS's GUI to trigger the software shutdown sequence.

d. Use BTN1 (NEM_PD) to trigger the NEM_PD shutdown sequence. EN10's default configuration on the evaluation board is NEM_PD. If an external signal is used to control NEM_PD, apply the external signal to CN2's EN10 pin. NEM_PD (EN10)'s logic-high and logic-low thresholds are 0.84V and 0.36V, respectively.

11. If an independent pull-up voltage is applied, remove the JP4 jumper, then connect the power source's positive terminal to VPU and connect the negative terminal to GND. Set VPU between 0.9V and V_{DD}.

12. If an independent battery voltage is applied, remove the JP6 jumper, then connect the power source or the positive battery terminal to VBAT and connect the negative battery terminal to GND. Set VBAT between 1.85V and 5.5V.

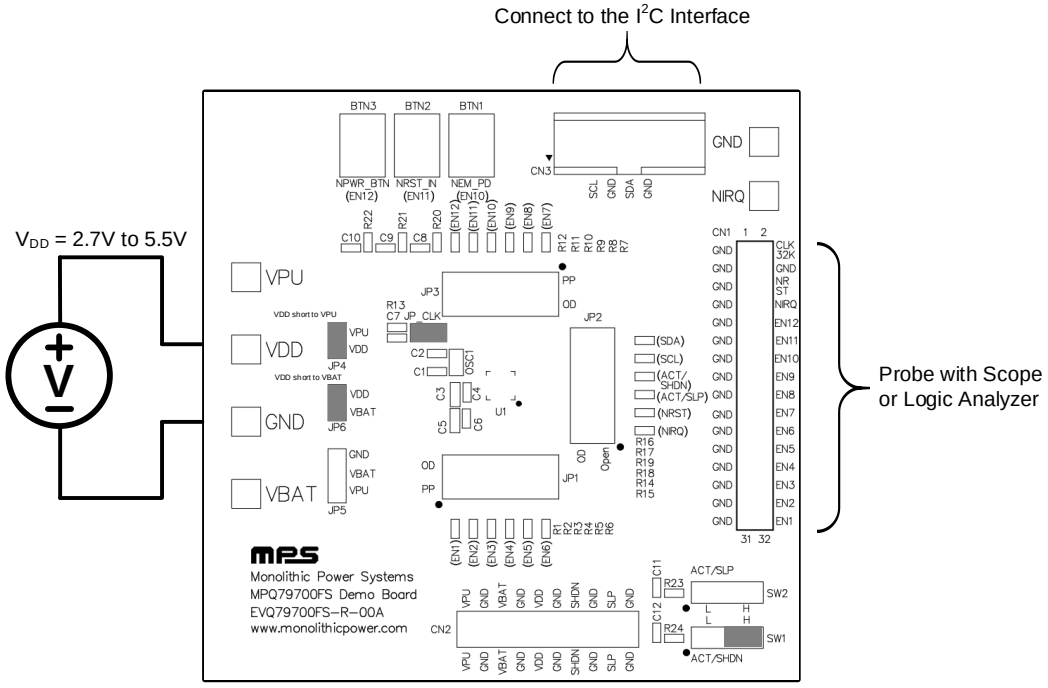


Figure 2: Measurement Equipment Set-Up

EVALUATION BOARD SCHEMATIC

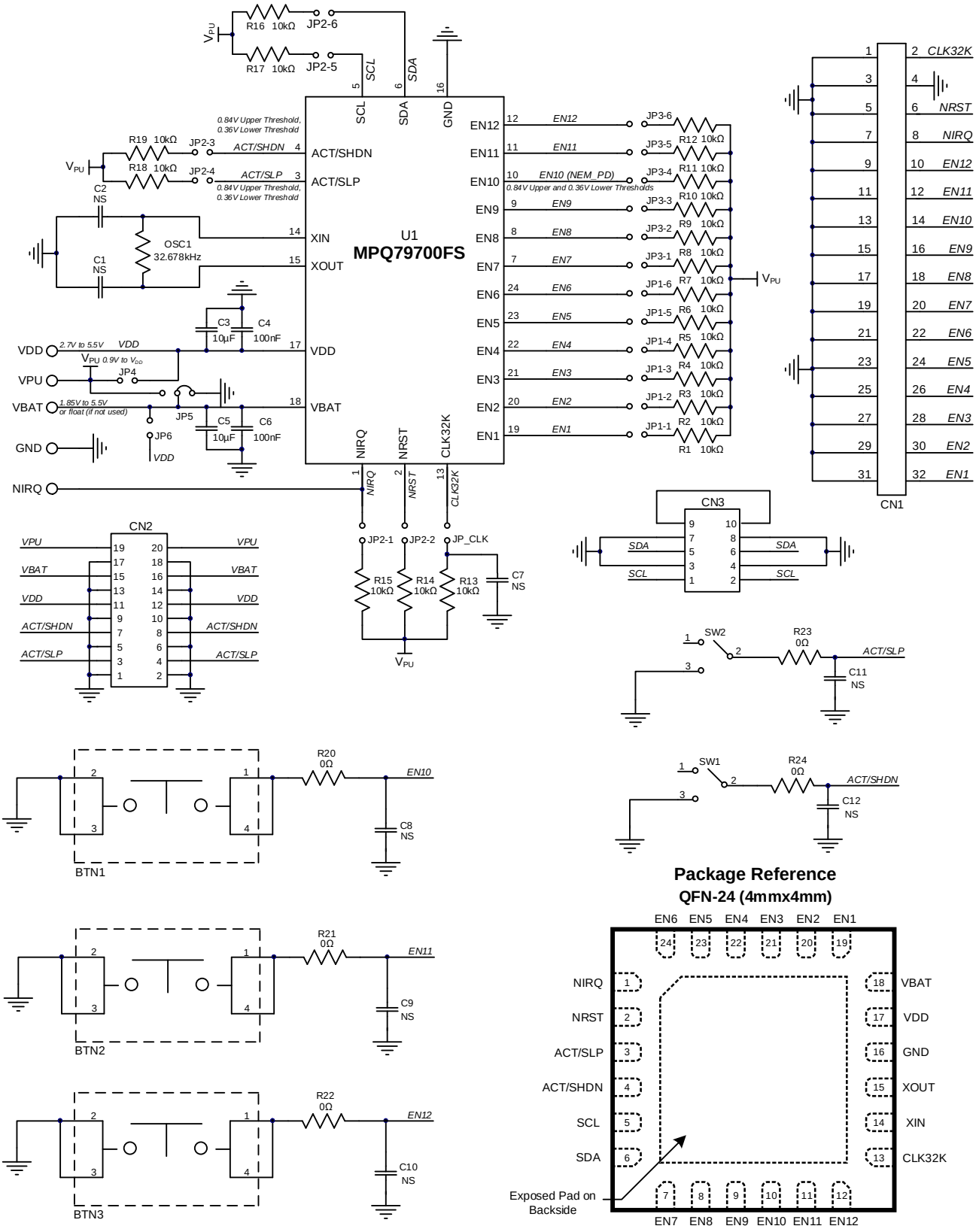


Figure 3: Evaluation Board Schematic

EVQ79700FS-R-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
3	BTN1, BTN2, BTN3	4mmx 10mmx 1.5mm	Switch push button	SMD	Custom (1)	Custom (1)
0	C1, C2	NS				
2	C3, C5	10µF	Ceramic capacitor, 10V, X7R	0805	Murata	GRM21BR71A106KE51L
2	C4, C6	100nF	Ceramic capacitor, 16V, X7R	0603	Murata	GRM188R71C104KA01D
1	C7	NS				
0	C8, C9, C10	NS				
2	C11, C12	10nF	Ceramic capacitor, 50V, X7R	0603	Murata	GRM188R71H103KA01D
1	CN1	2.54mm	180° dual pin header, 2 x 16-pin	DIP	Wurth	61303221121
1	CN2	2.54mm	180° dual pin header, 2 x 10-pin	DIP	Wurth	61302021121
1	CN3	2.54mm	Male box header, 2 x 5-pin	DIP	Wurth	612010235121
3	JP1, JP2, JP3	6-position	Compact DIP switch, SPST	SMD	Custom (1)	Custom (1)
3	JP4, JP6, JP_CLK	2.54mm	180° pin header, 2-pin	DIP	Wurth	61300211121
1	JP5	2.54mm	180° pin header, 3-pin	DIP	Wurth	61300311121
4	JP4, JP5, JP6, JP_CLK	2.54mm	Jumper, 2-pin	DIP	Wurth	60900213421
1	OSC1	32.768KHz	Crystal oscillator	SMD	NDK	NX3215SA-32.768K-STD-MUS-2
3	R20, R21, R22	0Ω	Film resistor, 5%	0603	Yageo	RC0603JR-070RL
19	R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19	10kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710KL
2	R23, R24	510Ω	Film resistor, 1%	0603	Yageo	RC0603FR-07510RL
2	SW1, SW2	SPDT	Slide switch, SPDT, opposite connection	DIP	Wurth	450301014042

EVQ79700FS-R-00A BILL OF MATERIALS *(continued)*

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
6	VPU, VDD, GND, VBAT, GND, NIRQ	1mm	Golden pin, test point	DIP	Custom (1)	Custom (1)
1	U1	MPQ79700FS	MPSafe™ ASIL-D, 12-channel power sequencer, AEC-Q100	QFN-24 (4mmx 4mm)	MPS	MPQ79700FSGRE-0000-AEC1

Note:

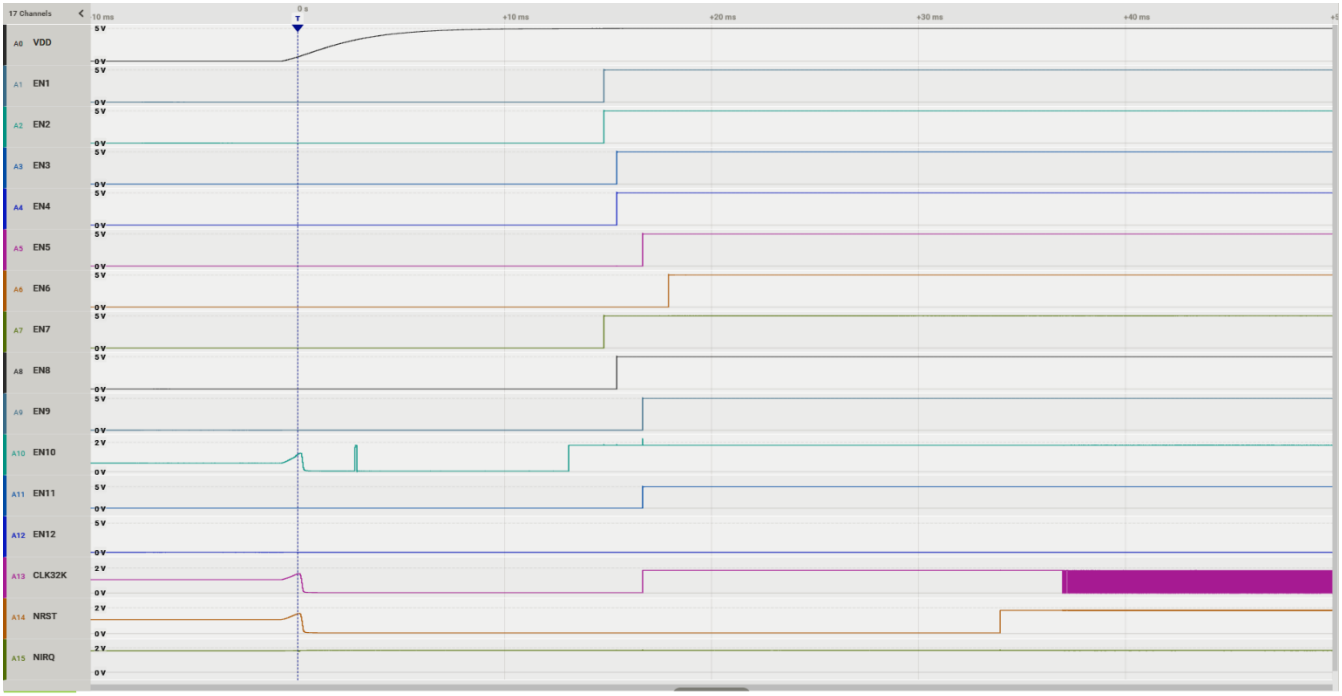
1) Contact an MPS FAE for more information regarding custom pins.

EVB TEST RESULTS

V_{DD} = 5V, V_{PU} = 1.8V, V_{BAT} = 5V, T_A = 25°C, unless otherwise noted.

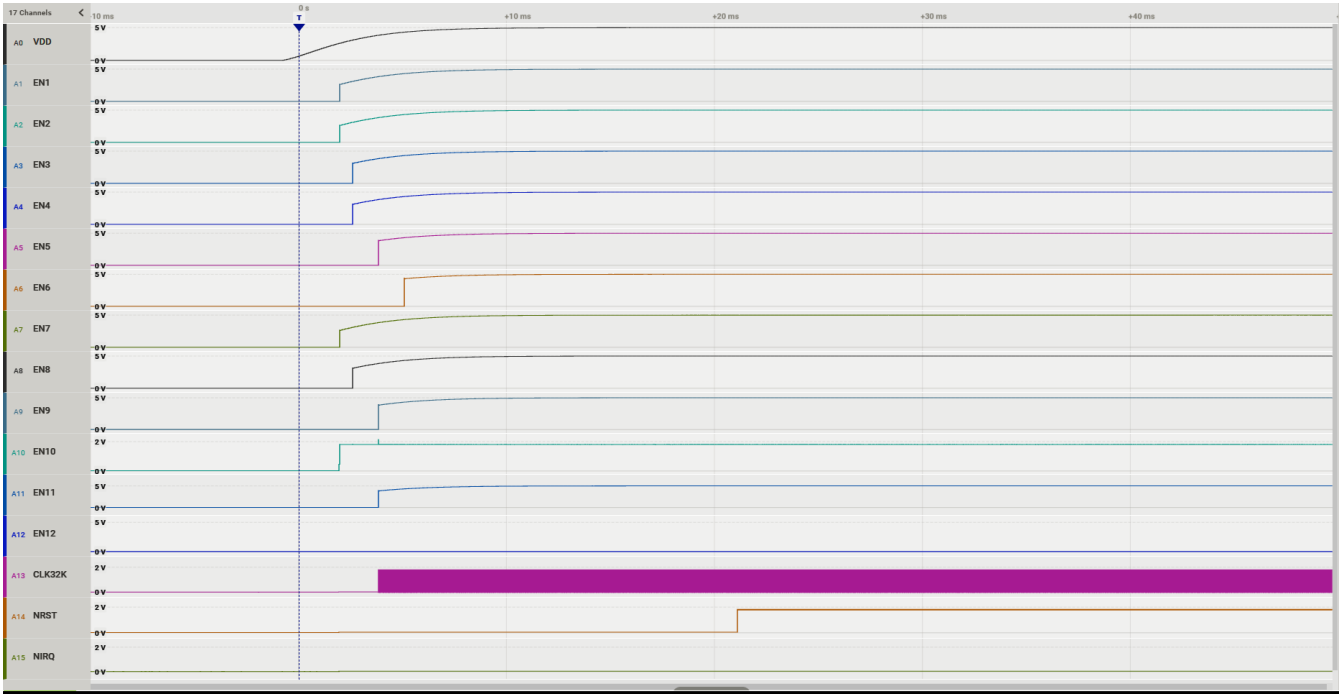
VDD Start-Up from OFF State with ACT/SHDN High

EN10 (NEM_PD) = high, ACT/SHDN = high



VDD Start-Up from BACKUP State with ACT/SHDN High

EN10 (NEM_PD) = high, ACT/SHDN = high



EVB TEST RESULTS *(continued)*

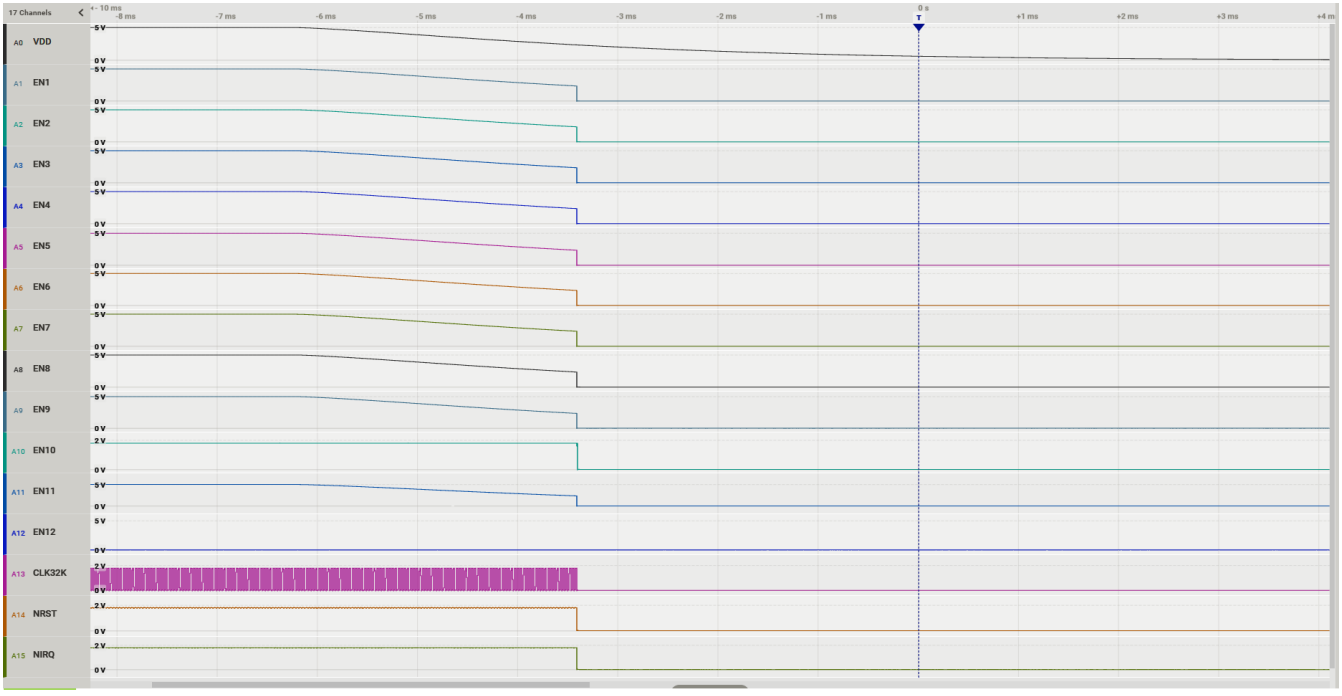
V_{DD} = 5V, V_{PU} = 1.8V, V_{BAT} = 5V, T_A = 25°C, unless otherwise noted.

Sequence 1: Power-Up from SHDN1 to ACTIVE by ACT/SHDN Control

EN10 (NEM_PD) = high

Sequence 2: VDD Emergency Power-Down from ACTIVE to BACKUP

EN10 (NEM_PD) = high, ACT/SHDN = high



EVB TEST RESULTS *(continued)*

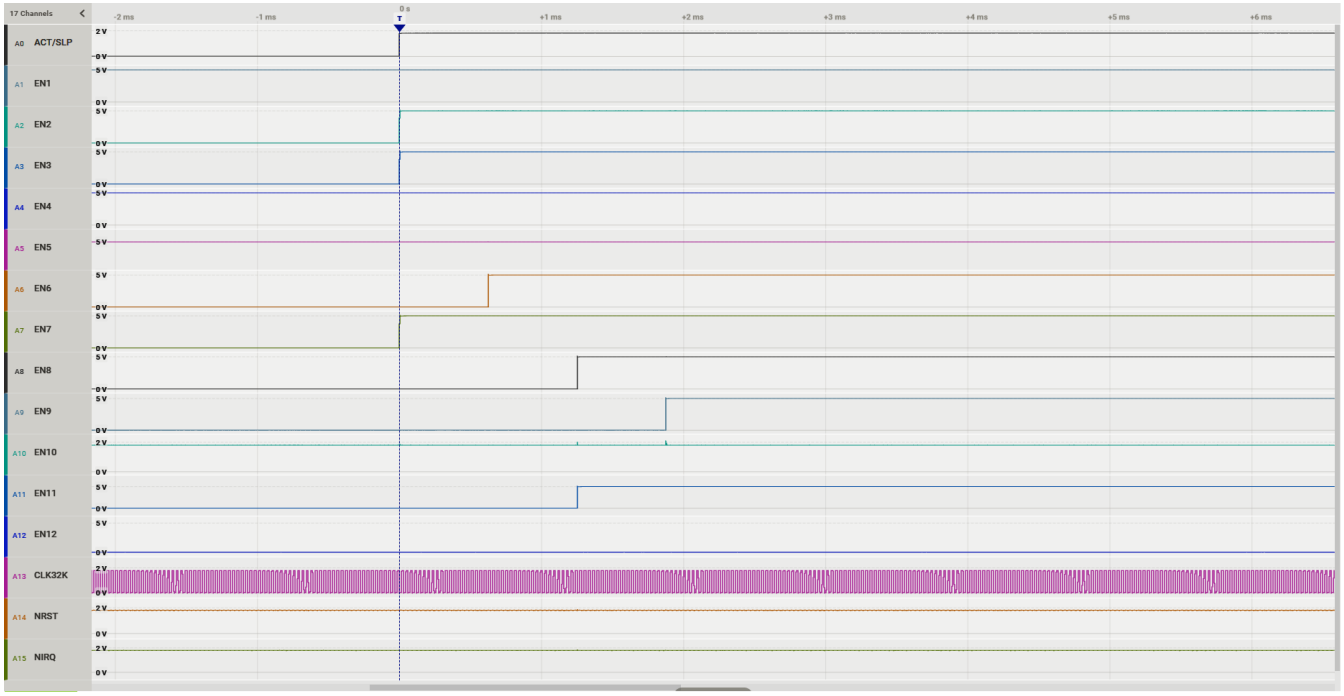
V_{DD} = 5V, V_{PU} = 1.8V, V_{BAT} = 5V, T_A = 25°C, unless otherwise noted.

Sequence 3: SLEEP Entry via ACT/SLP Control

EN10 (NEM_PD) = high, ACT/SHDN = high, register 0x28, bit[2] = 0b

Sequence 4: SLEEP Exit via ACT/SLP Control

EN10 (NEM_PD) = high, ACT/SHDN = high, register 0x28, bit[2] = 0b

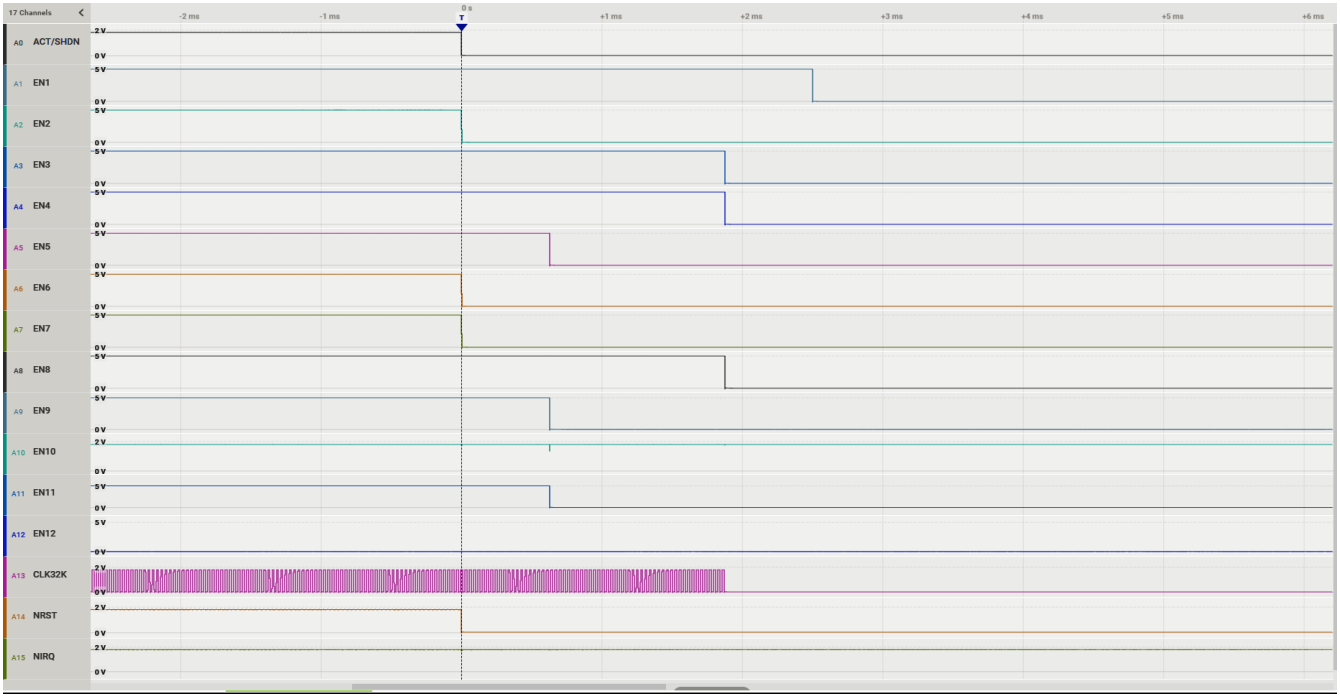


EVB TEST RESULTS *(continued)*

V_{DD} = 5V, V_{PU} = 1.8V, V_{BAT} = 5V, T_A = 25°C, unless otherwise noted.

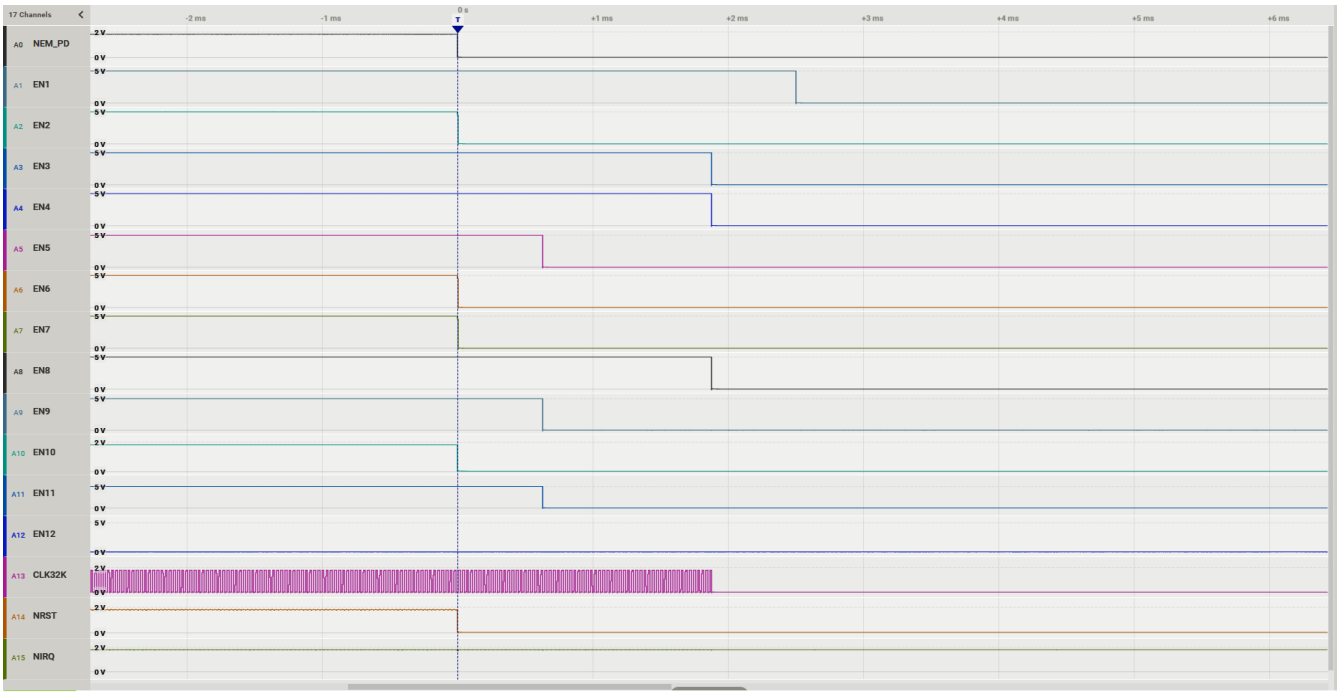
Sequence 5: Power-Down from ACTIVE to SHDN1 via ACT/SHDN Control

EN10 (NEM_PD) = high



Sequence 5: Power Down from ACTIVE to SHDN2 via NEM_PD Assertion

ACT/SHDN = high

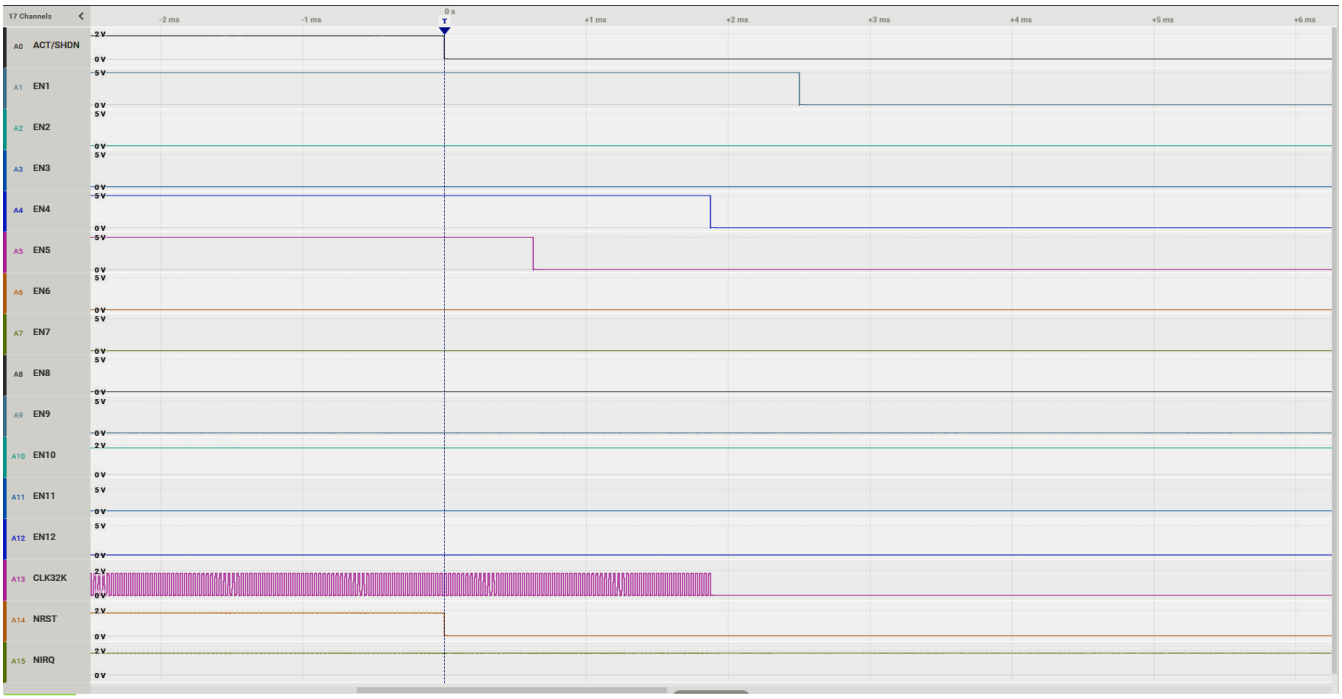


EVB TEST RESULTS *(continued)*

V_{DD} = 5V, V_{PU} = 1.8V, V_{BAT} = 5V, T_A = 25°C, unless otherwise noted.

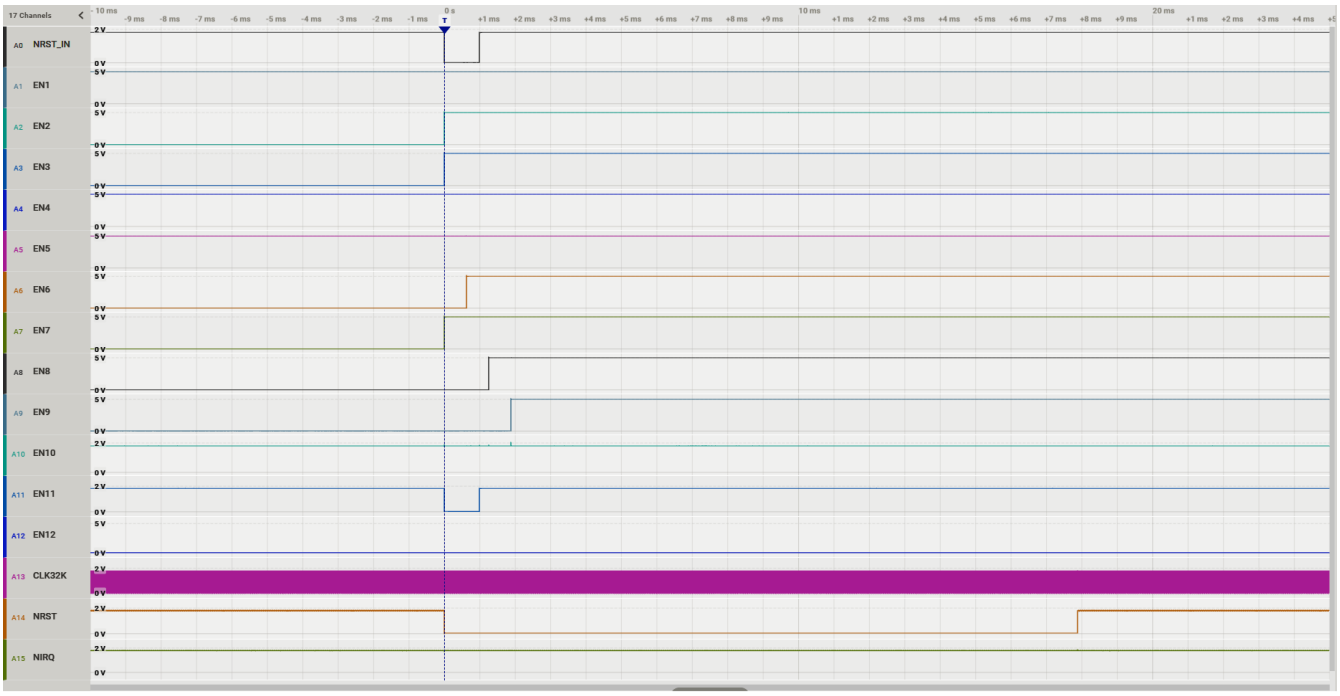
Sequence 6: Power-Down from SLEEP to SHDN1 by ACT/SHDN Controlled

EN10 (NEM_PD) = high, ACT/SLP = low, register 0x28, bit[2] = 0b



Sequence 7: SLEEP Exit Due to NRST_IN Assertion

EN10 (NEM_PD) = high, EN11 configured as NRST_IN (registers 0x20, bit[2] = 1b, 0x21, bit[2] = 1b, 0x3D = 00h, 0x5D = 00h)

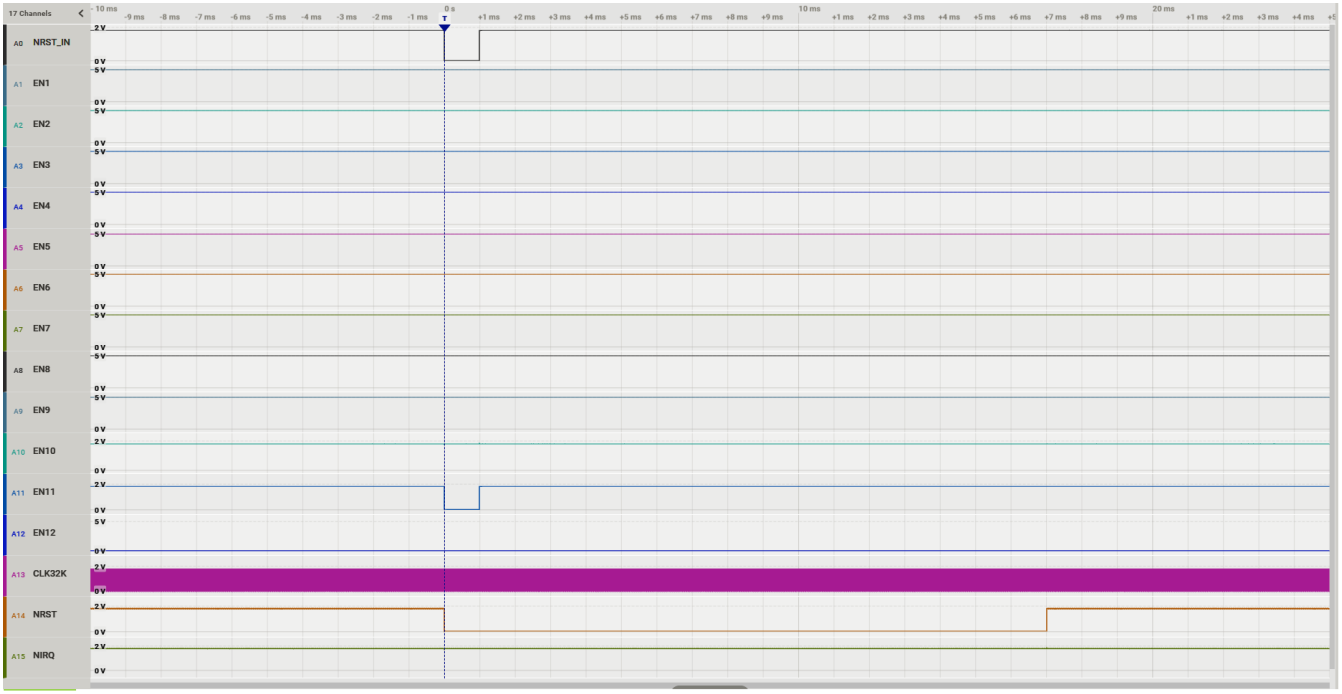


EVB TEST RESULTS *(continued)*

V_{DD} = 5V, V_{PU} = 1.8V, V_{BAT} = 5V, T_A = 25°C, unless otherwise noted.

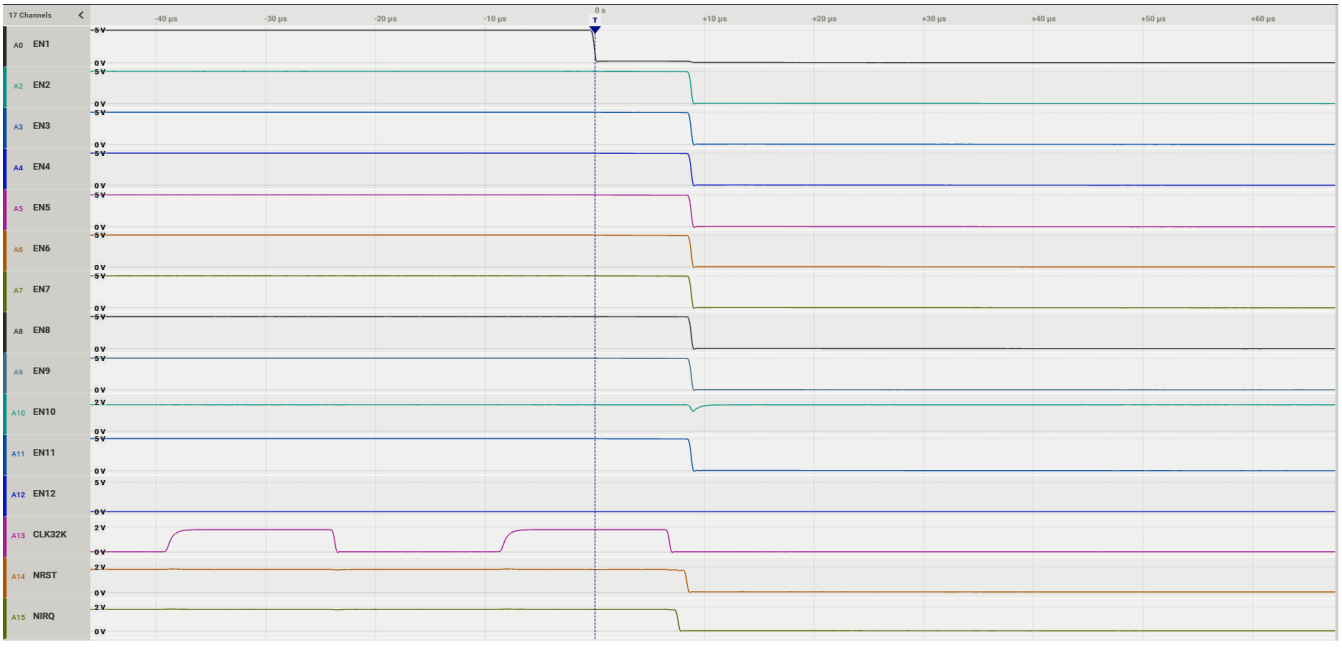
Sequence 8: Reset Due to NRST_IN Assertion

EN10 (NEM_PD) = high, EN11 configured as NRST_IN (registers 0x20, bit[2] = 1b, 0x21, bit[2] = 1b, 0x3D = 00h, 0x5D = 00h)



Sequence 9: FAILSAFE Power-Down from ACTIVE via F_EN

EN10 (NEM_PD) = high, Pull EN1 to GND



PCB LAYOUT (2)

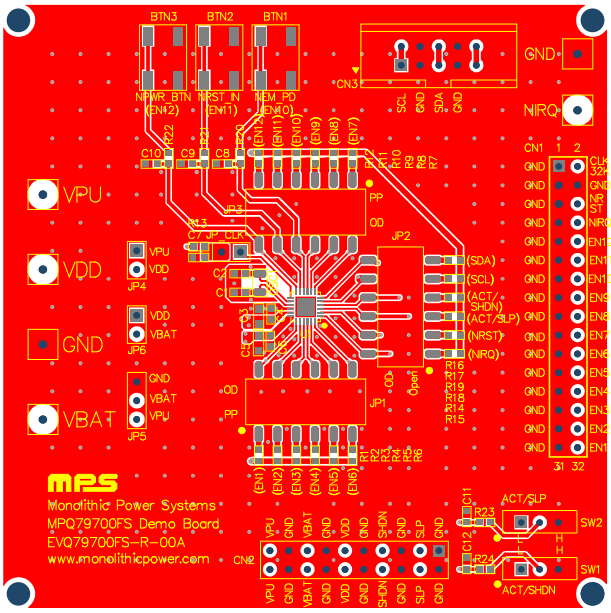


Figure 4: Top Silk and Top Layer

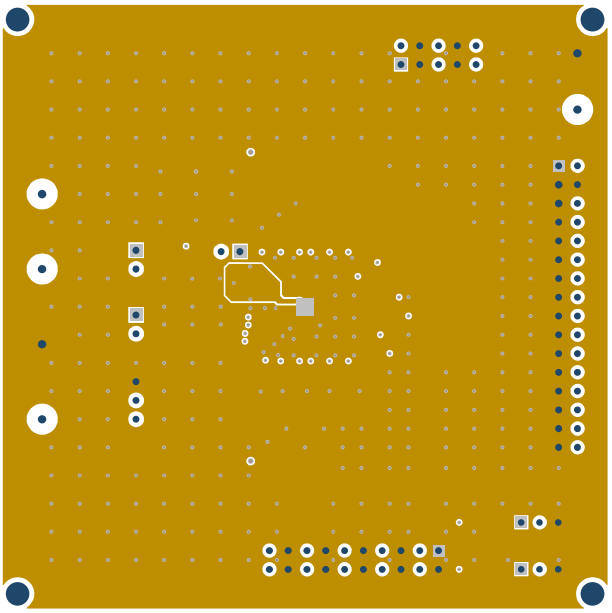


Figure 5: Mid-Layer 1

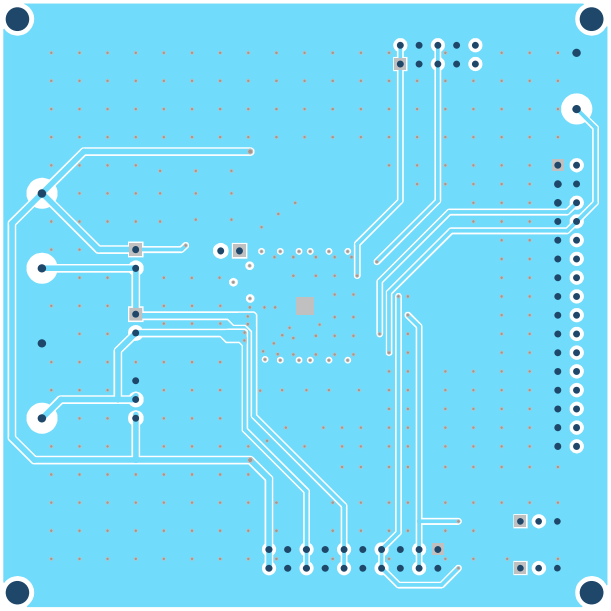


Figure 6: Mid-Layer 2

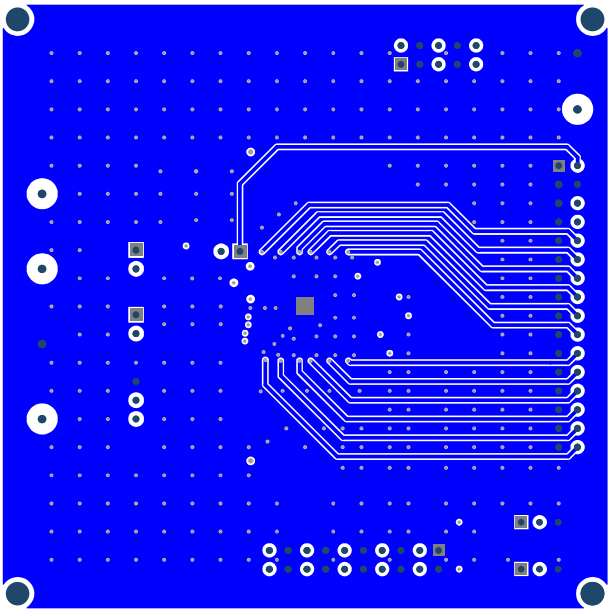


Figure 7: Bottom Layer and Bottom Silk

Note:

2) EVQ79700FS-R-00A, a 4-layer, 2oz copper thickness PCB (8.35cmx8.35cm).

MPQ79700FS-0000 DEFAULT REGISTER VALUES

Register Number	Register Name	Register Value	Register Number	Register Name	Register Value	Register Number	Register Name	Register Value
0x00	DEVICE_ID	09h	0x36	PWR_EN4	24h	0x5D	SLP_EN11	31h
0x01	DEVICE_REV	81h	0x37	PWR_EN5	42h	0x5E	SLP_EN12	00h
0x20	EN_ALT_F	02h	0x38	PWR_EN6	61h	0x5F	SLP_CLK32OE	00h
0x21	AF_IN_OUT	02h	0x39	PWR_EN7	11h	0x70	RTC_T3	00h
0x22	EN_CFG1	0Fh	0x3A	PWR_EN8	24h	0x71	RTC_T2	00h
0x23	EN_CFG2	FFh	0x3B	PWR_EN9	42h	0x72	RTC_T1	00h
0x24	CLK_CFG	C0h	0x3C	PWR_EN10	00h	0x73	RTC_T0	00h
0x25	GP_OUT	00h	0x3D	PWR_EN11	42h	0x74	RTC_A3	FFh
0x26	DEB_IN	00h	0x3E	PWR_EN12	00h	0x75	RTC_A2	FFh
0x27	LP_TTSHLD	00h	0x3F	PWR_CLK32OE	44h	0x76	RTC_A1	FFh
0x28	CTL_1	04h	0x53	SLP_EN1	00h	0x77	RTC_A0	FFh
0x29	CTL_2	C3h	0x54	SLP_EN2	13h	0x80	WDT_CFG	00h
0x2A	TEST_CFG	03h	0x55	SLP_EN3	12h	0x81	WDT_CLOSE	00h
0x2B	IEN_OTHER	00h	0x56	SLP_EN4	00h	0x82	WDT_OPEN	00h
0x30	SEQ_CFG	00h	0x57	SLP_EN5	00h	0x83	WDTKEY	00h
0x31	SEQ_USLOT	02h	0x58	SLP_EN6	21h	0xF0	PROT1	00h
0x32	SEQ_DSLOT	02h	0x59	SLP_EN7	13h	0xF1	PROT2	00h
0x33	PWR_EN1	15h	0x5A	SLP_EN8	32h	0xF9	I2CADDR	3Ch
0x34	PWR_EN2	11h	0x5B	SLP_EN9	41h	0xFA	DEV_CFG	02h
0x35	PWR_EN3	24h	0x5C	SLP_EN10	00h	-	-	-

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	11/10/2022	Initial Release	-