



EVQ6539-V-00A

80V, Three-Phase, BLDC Motor Pre-Driver Evaluation Board, AEC-Q100 Qualified

DESCRIPTION

The EVQ6539-V-00A evaluation board is designed to demonstrate the capabilities of the MPQ6539GVE-AEC1, a three-phase, brushless (BLDC) DC motor pre-driver.

The device is capable to driving 3 half-bridges consisting of 6 N-channel power MOSFETs up to 80V. The MPQ6539GVE-AEC1 uses a bootstrap (BST) capacitor (C_{BST}) to generate a supply voltage for the high-side MOSFET (HS-FET) driver. If the output is held high for an extended period, an internal charge pump maintains the HS-FET.

Internal protections include configurable over-current protection (OCP), adjustable dead-time (DT) control, under-voltage lockout (UVLO), and thermal shutdown.

The driving control signals are generated via an external controller, such as a microcontroller (MCU) or FPGA.

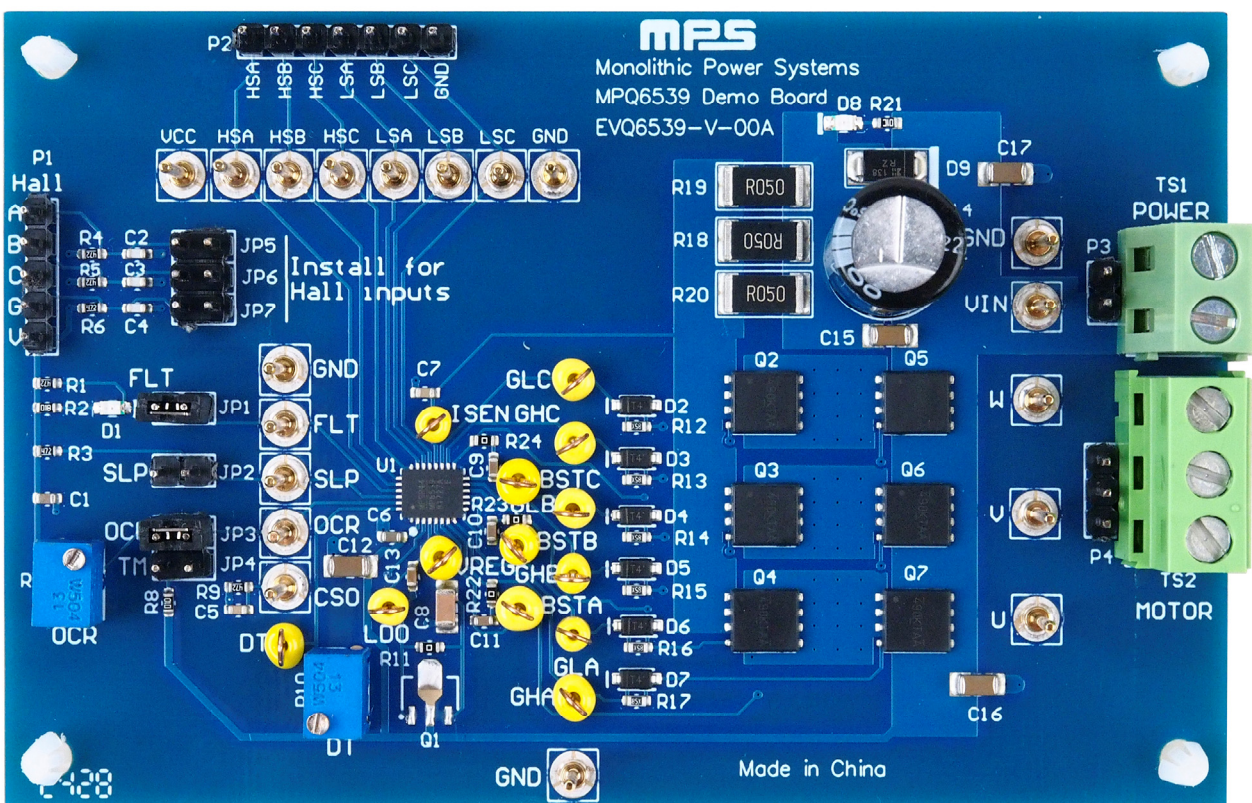
The MPQ6539GVE-AEC1 is available in a QFN-28 (4mmx5mm) package with wettable flanks, and is available in AEC-Q100 Grade 1.

PERFORMANCE SUMMARY

Specifications are at $T_A = 25^{\circ}\text{C}$, unless otherwise noted.

Parameters	Conditions	Value
Input power supply voltage (V_{IN}) range		8V to 80V
Over-current protection (OCP) reference input (OC_REF)		0.125V to 2.4V
Logic power supply voltage (V_{CC})		3.3V or 5V

EVQ6539-V-00A EVALUATION BOARD



LxWxH (11.7cmx6.5cmx2.2cm)

Board Number	MPS IC Number
EVQ6539-V-00A	MPQ6539GVE-AEC1

QUICK START GUIDE

The EVQ6539-V-00A evaluation board is easy to set up and use to evaluate the performance of the MPQ6539GVE-AEC1. For proper measurement set-up, refer to Figure 1 and follow the steps below:

1. Preset the input power supply (V_{IN}) to be between 8V and 80V.
2. Connect the power supply terminals to:
 - a. Positive (+): V_{IN}
 - b. Negative (-): GND
3. Set the logic supply voltage (V_{CC}) to 3.3V or 5V.
4. Connect the logic supply terminals to the following terminals on the P1 connector:
 - a. Positive (+): V
 - b. Negative (-): G
5. To set the over-current protection (OCP) threshold, adjust the OCP reference voltage (V_{REF}) to be between 0.125V and 2.4V via R7.
6. Attach the HSx and LSx driving control signals that are generated via the external controller to the P2 connector.

Table 1 shows the input logic for HSx, LSx, and SHx:

Table 1: Input Logic

LSx	HSx	SHx
Low	Low	Hi-Z
Low	High	V_{IN}
High	Low	GND
High	High	Hi-Z

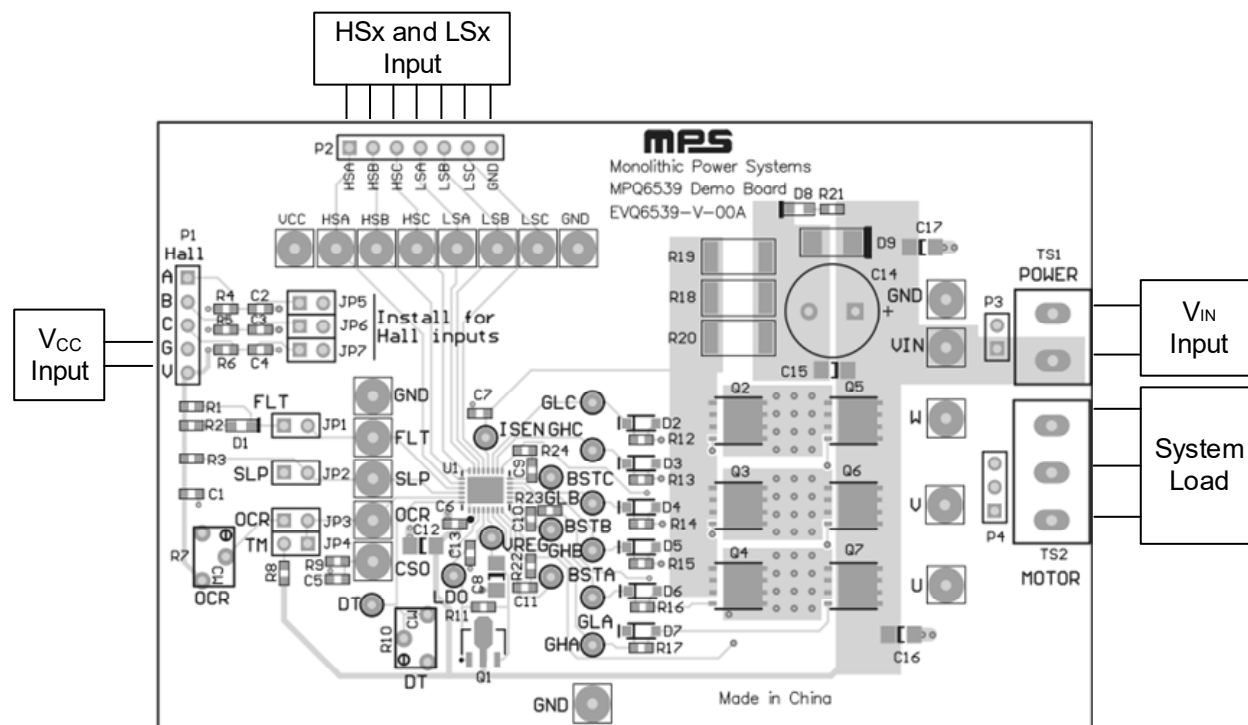


Figure 1: Measurement Equipment Set-Up

EVALUATION BOARD SCHEMATIC

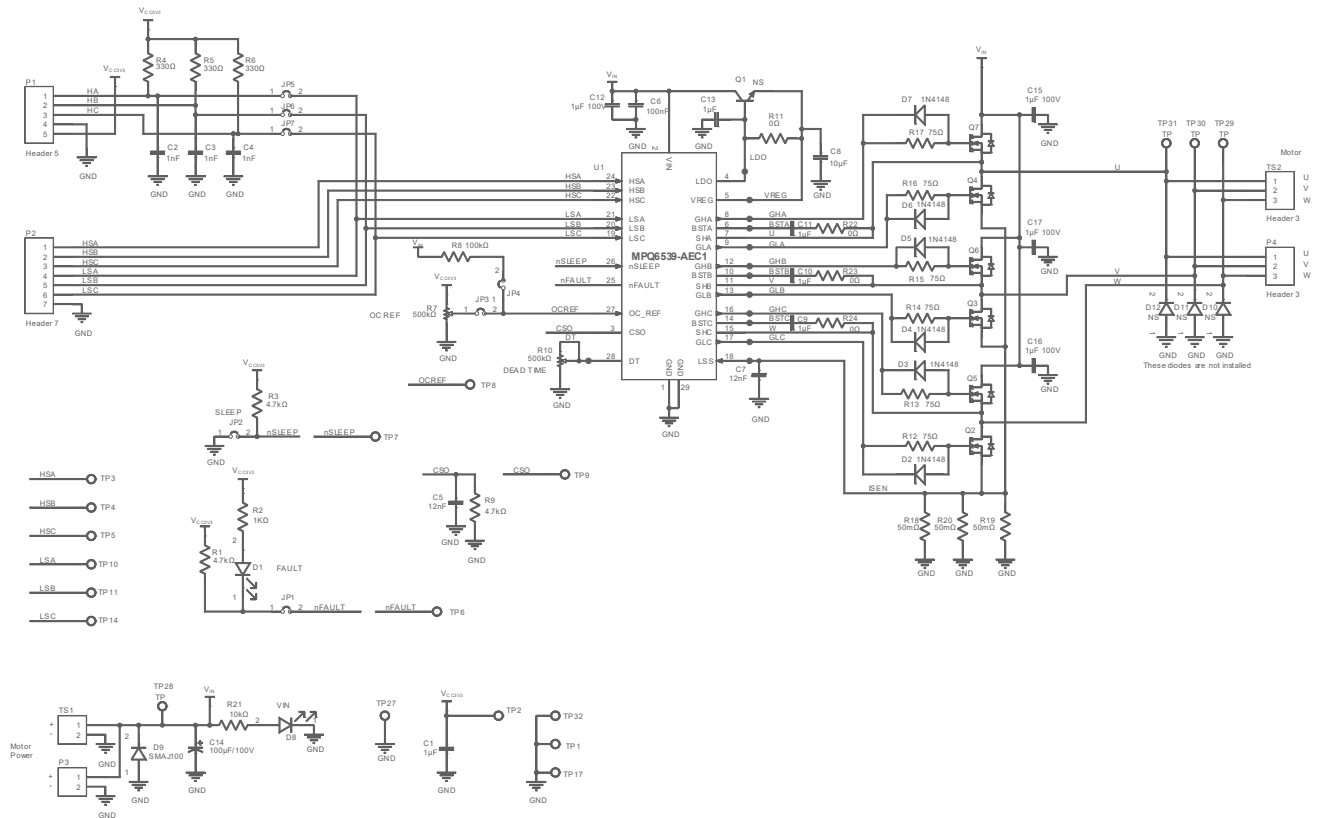


Figure 2: Evaluation Board Schematic

EVQ6539-V-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	C1	1μF	Ceramic capacitor, 6.3V, X5R	0603	Murata	GRM188R60J105KA01D
3	C2, C3, C4	1nF	Ceramic capacitor, 25V, C0G	0603	Murata	GRM1885C1E102JA01D
2	C5, C7	12nF	Ceramic capacitor, 50V, X7R	0603	Murata	GRM188R71H123KA01D
1	C6	100nF	Ceramic capacitor, 100V, X7R	0603	Murata	GRM188R72A104KA35D
1	C8	10μF	Ceramic capacitor, 25V, X7R	1206	Murata	GRM31CR71E106KA12
4	C9, C10, C11, C13	1μF	Ceramic capacitor, 25V, X7R	0603	Murata	GRM188R71E105KA12D
4	C12, C15, C16, C17	1μF	Ceramic capacitor, 100V, X7R	1206	Murata	GRM31CR72A105KA01L
1	C14	100μF	Electrolytic capacitor, 100V	DIP	Panasonic	EEUFR2A101
6	R1, R3, R4, R5, R6, R9	4.7kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-074K7L
1	R2	1kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-071KL
2	R7, R10	500kΩ	Adjustable resistor	DIP	Bourns	3266W-1-504LF
1	R8	100kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-07100KL
4	R11, R22, R23, R24	0Ω	Film resistor, 1%	0603	Yageo	RC0603FR-070RL
6	R12, R13, R14, R15, R16, R17	75Ω	Film resistor, 1%	0603	Yageo	RC0603FR-0775RL
3	R18, R19, R20	50mΩ	Film resistor, 1%	2512	Yageo	RL2512FK-070R05L
1	R21	10kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710KL
2	D1, D8	0.1W	LED green light	0805	Baihong	BL-HGE35A-AV-TRB
6	D2, D3, D4, D5, D6, D7	0.15A	Schottky diode, 75V	SOD-123	Diodes, Inc.	1N4148W
1	D9	2.5A	TVS diode, 100V	SMA	Diodes, Inc.	SMAJ100A
3	D10, D11, D12	NS				
1	Q1	NS				
6	Q2, Q3, Q4, Q5, Q6, Q7	8.3A	N-channel MOSFET, 150V, 48mΩ, Q _G = 58nC	DFN-8L (5mmx6mm)	Analog Power	AM7490N-T1-PF
1	P1	2.54mm	Header, 5-pin	DIP	Any	
1	P2	2.54mm	Header, 7-pin	DIP	Any	
1	P3	2.54mm	Header, 2-pin	DIP	Any	
1	P4	2.54mm	Header, 3-pin	DIP	Any	
1	TS1	5mm	Header, 2-pin	DIP	KEFA	KF128-5.0-02P
1	TS2	5mm	Header, 3-pin	DIP	Würth	691216510003S
7	JP1, JP2, JP3, JP4, JP5, JP6, JP7	2.54mm	Header, 2-pin	DIP	Any	
2	JP1, JP3	2.54m	Short jumper		Any	

EVQ6539-V-00A BILL OF MATERIALS *(continued)*

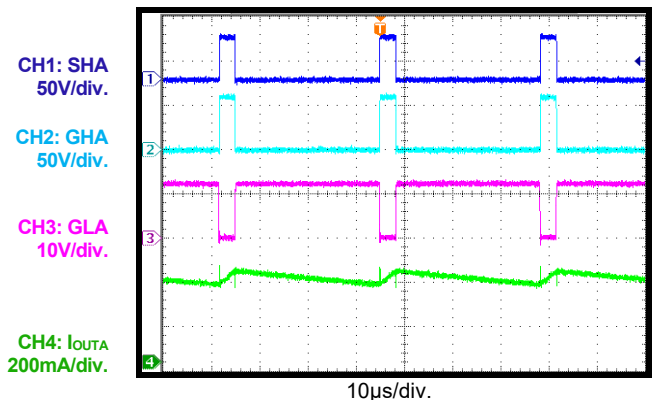
Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer P/N
19	ENA, ENB, ENC, PWMA, PWMB, PWMC, VCC, GND, GND, FLT, SLP, OCR, CSO, GND, VIN, GND, U, V, W	1mm	Male needle	DIP	Any	
13	DT, LDO, VREG, ISEN, BSTA, BSTB, BSTC, GLA, GLB, GLC, GHA, GHB, GHC	1mm	Test points	DIP	Any	
1	U1	MPQ6539- AEC1	80V, three-phase, brushless (BLDC) DC motor pre-driver	QFN-28 (4mmx 5mm)	MPS	MPQ6539GVE-AEC1

EVB TEST RESULTS

$V_{IN} = 48V$, $OC_REF = 0.5V$, $R_{DT} = 1k\Omega$, phase A switching, phase B's low-side (LS) gate driver enabled, $f_{PWMA} = 30kHz$, $T_A = 25^\circ C$, resistor + inductor load = $5\Omega + 1mH$ /phase with a star connection, unless otherwise noted.

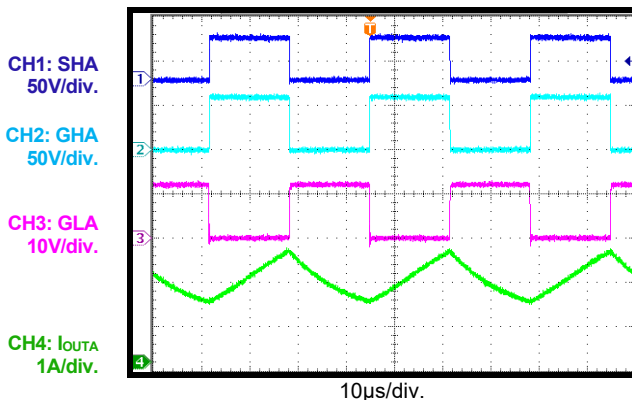
Steady State

Duty cycle = 10%



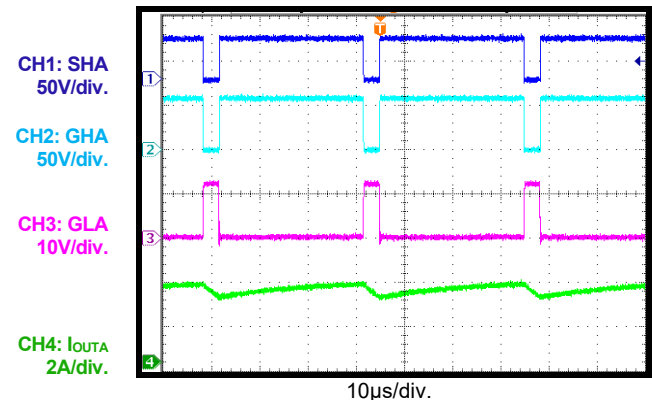
Steady State

Duty cycle = 50%



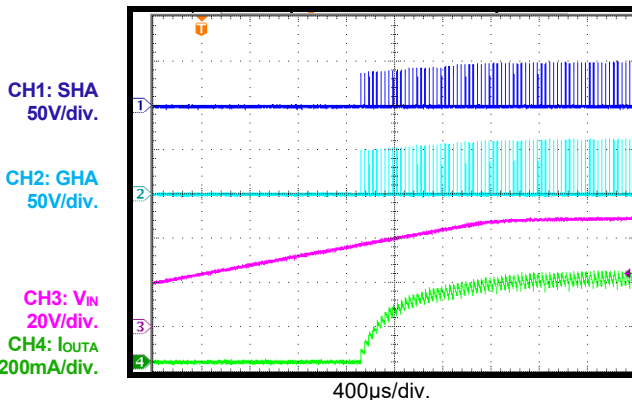
Steady State

Duty cycle = 90%



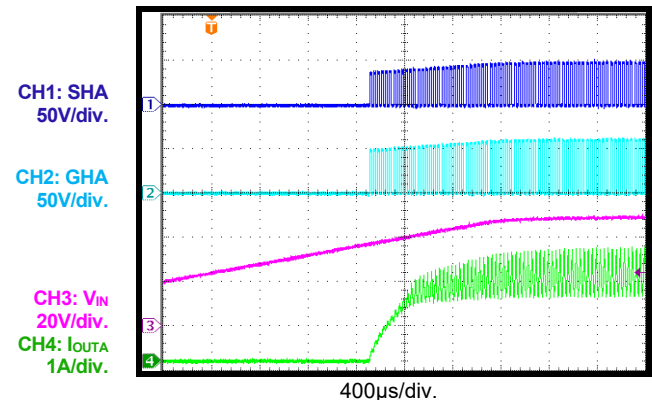
Power Ramping Up

Duty cycle = 10%



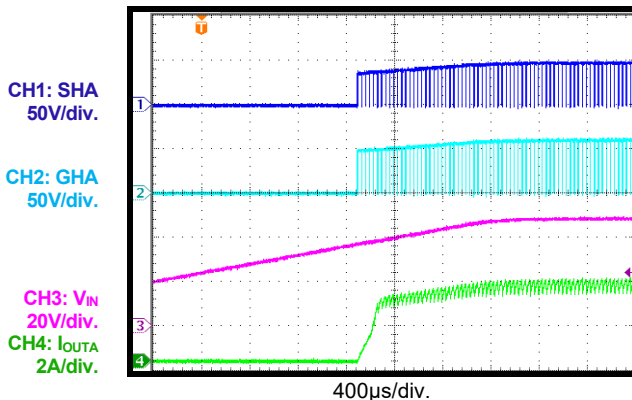
Power Ramping Up

Duty cycle = 50%



Power Ramping Up

Duty cycle = 90%



EVB TEST RESULTS *(continued)*

$V_{IN} = 48V$, $OC_REF = 0.5V$, $R_{DT} = 1k\Omega$, phase A switching, phase B's LS gate driver enabled, $f_{PWMA} = 30kHz$, $T_A = 25^\circ C$, resistor + inductor load = $5\Omega + 1mH$ /phase with a star connection, unless otherwise noted.

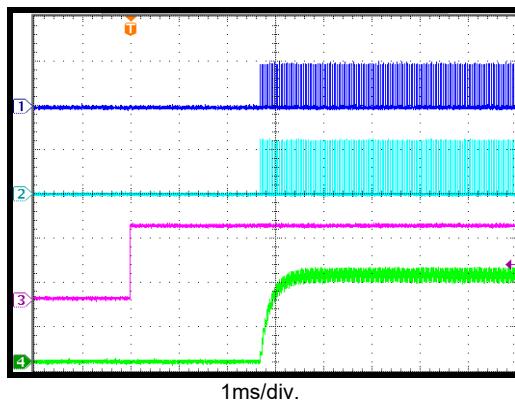
Sleep Recovery

Duty cycle = 10%

CH1: SHA
50V/div.

CH2: GHA
50V/div.

CH3: nSLEEP
2V/div.

CH4: I_{OUTA}
200mA/div.


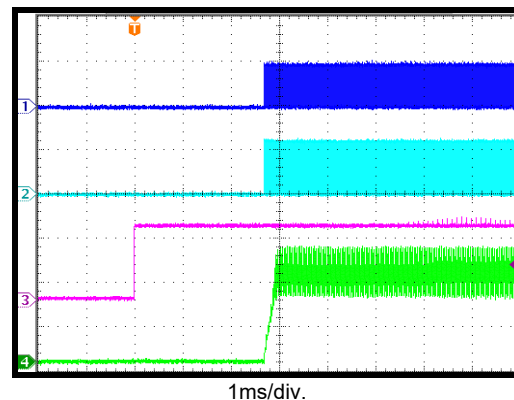
Sleep Recovery

Duty cycle = 50%

CH1: SHA
50V/div.

CH2: GHA
50V/div.

CH3: nSLEEP
2V/div.

CH4: I_{OUTA}
1A/div.


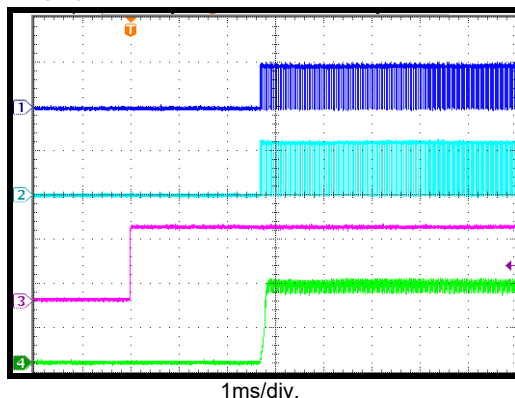
Sleep Recovery

Duty cycle = 90%

CH1: SHA
50V/div.

CH2: GHA
50V/div.

CH3: nSLEEP
2V/div.

CH4: I_{OUTA}
2A/div.


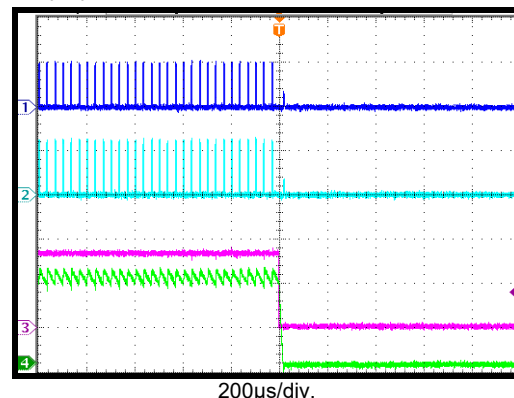
Sleep Entry

Duty cycle = 10%

CH1: SHA
50V/div.

CH2: GHA
50V/div.

CH3: nSLEEP
2V/div.

CH4: I_{OUTA}
200mA/div.


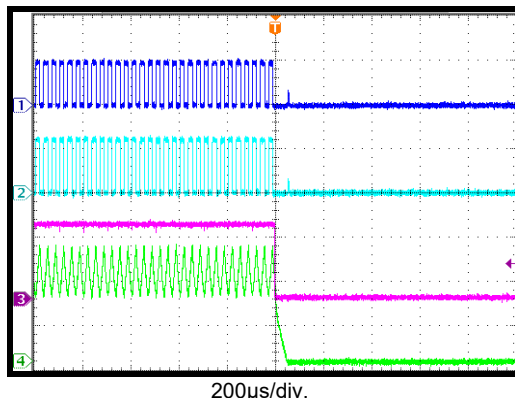
Sleep Entry

Duty cycle = 50%

CH1: SHA
50V/div.

CH2: GHA
50V/div.

CH3: nSLEEP
2V/div.

CH4: I_{OUTA}
1A/div.


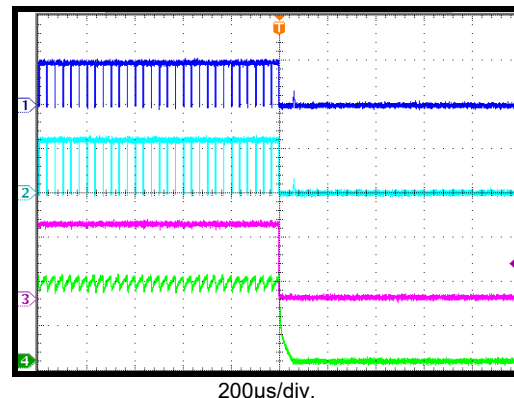
Sleep Entry

Duty cycle = 90%

CH1: SHA
50V/div.

CH2: GHA
50V/div.

CH3: nSLEEP
2V/div.

CH4: I_{OUTA}
2A/div.


PCB LAYOUT

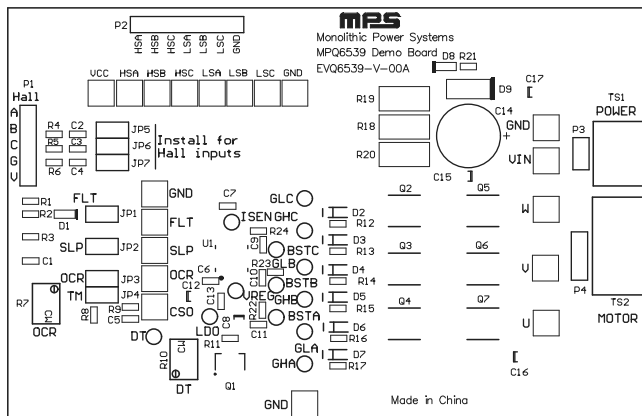


Figure 3: Top Silk

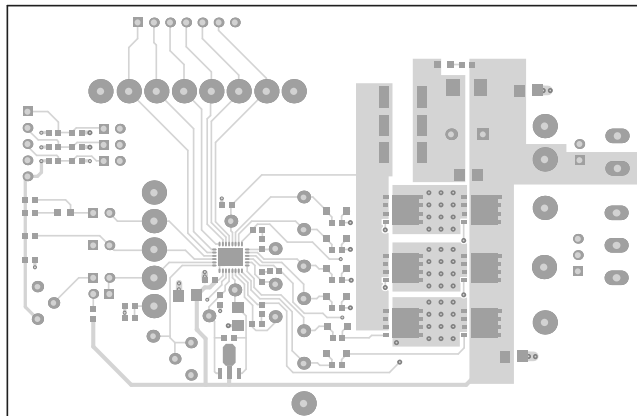


Figure 4: Top Layer

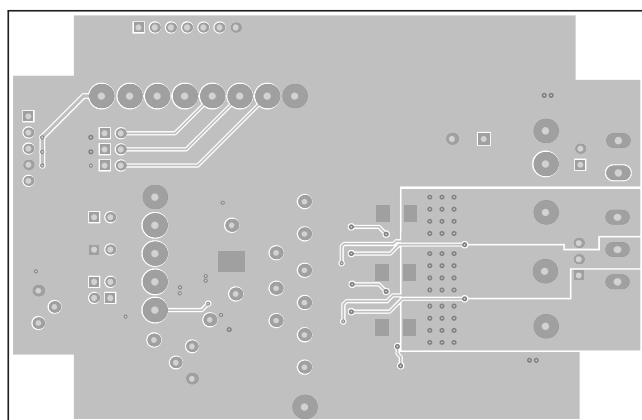


Figure 5: Bottom Layer

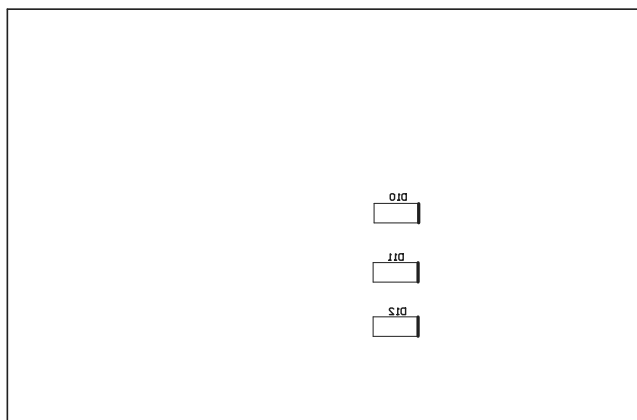


Figure 6: Bottom Silk



REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	11/12/2024	Initial Release	-

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