EVQ4372-V-1001-00A

36V, 22A, Dual-Phase Application, Ultra-Low Quiescent Current, Synchronous, Step-Down Converter Evaluation Board, AEC-Q100 Qualified

DESCRIPTION

The EVQ4372-V-1001-00A evaluation board is designed to demonstrate the capabilities of the MPQ4372-1001, a dual-phase application, synchronous, step-down switching regulator with integrated low on-resistance ($R_{DS(ON)}$) high-side and low-side power MOSFETs (HS-FET and LS-FET, respectively). Part of a highly scalable family of parts, the MPQ4372-1001 provides up to 11A of output current (I_{OUT}) and employs Zero-Delay PWM (ZDP™) control, an MPS-exclusive technology that delivers extremely fast transient response and reduces the need for costly external capacitors. The evaluation board can provide up to 22A of I_{OUT}.

The wide 3.3V to 36V input voltage (V_{IN}) range accommodates a variety of step-down applications in automotive input environments. A 1.8µA shutdown-mode quiescent current (I_Q) allows the device to be used in battery-powered applications.

High power conversion efficiency across a wide load range is achieved by scaling down the switching frequency (f_{SW}) under light-load conditions to reduce switching and gate driver losses.

An open-drain power good (PG) signal indicates whether the output is within 94% to 106% of its nominal voltage. Frequency foldback helps prevent inductor current (I_L) runaway during start-up. Thermal shutdown provides reliable, fault-tolerant operation.

A high duty cycle and low-dropout (LDO) mode provide support for automotive cold-crank conditions.

The EVQ4372-V-1001-00A is a fully assembled and tested evaluation board. The MPQ4372-1001 is available in a QFN-23 (4mmx5mm) package with wettable flanks, and is available in AEC-Q100 Grade 1.

PERFORMANCE SUMMARY

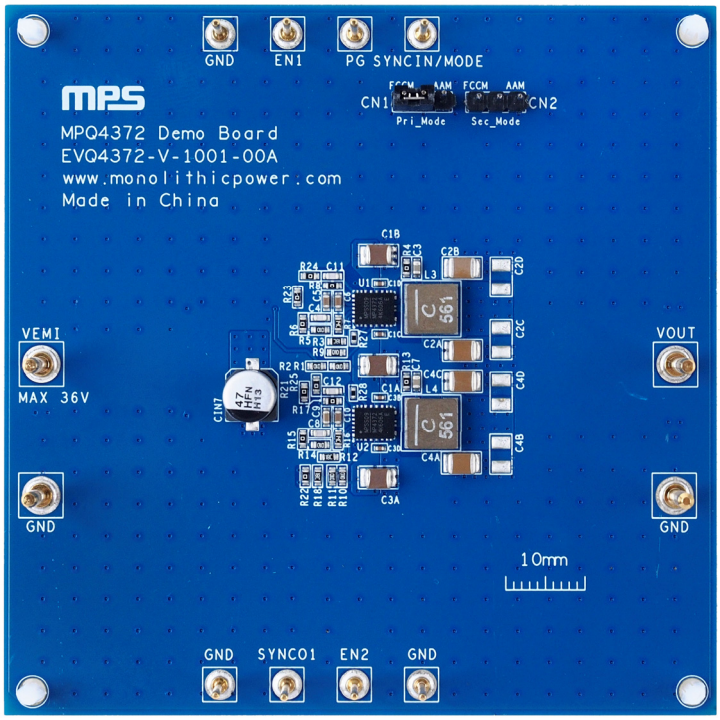
Specifications are at T_A = 25°C, unless otherwise noted.

Parameters	Conditions	Value
Input voltage (V_{IN}) range		3.3V to 36V
Output voltage (V_{OUT})	V_{IN} = 6V to 36V, I_{OUT} = 0A to 22A	V_{OUT} = 5V
Maximum output current (I_{OUT})	V_{IN} = 3.3V to 36V	22A (1)
Typical efficiency	V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 22A	90.29%
Peak efficiency	V_{IN} = 8V, V_{OUT} = 5V, I_{OUT} = 7A	94.5%
Switching frequency (f_{SW})		2.2MHz

Note:

1) Add a heat dissipation device when the board has a high input voltage (V_{IN}) and full load output at room temperature or over-temperature protection (OTP) may be triggered.

EVQ4372-V-1001-00A EVALUATION BOARD



LxWxH (9cmx9cmx1.3cm)

Board Number	MPS IC Number
EVQ4372-V-1001-00A	MPQ4372GVE-1001-AEC1

QUICK START GUIDE

The EVQ4372-V-1001-00A evaluation board is easy to set up and use to evaluate the performance of the MPQ4372-1001 for dual-phase applications. For proper measurement equipment set-up, refer to Figure 2 on page 5 and follow the steps below:

1. Preset the power supply to be between 3.3V and 36V, then turn off the power supply.
2. Set the load current to be between 0A and 22A. Electronic loads represent a negative impedance to the regulator, and setting the current too high may trigger hiccup mode.
3. If longer cables (>0.5m total) are used between the source and the evaluation board, place a damping capacitor at the input terminals, especially when V_{IN} ≥ 24V.
4. Connect the power supply terminals to:
   a. Positive (+): VEMI
   b. Negative (-): GND
5. Connect the load terminals to:
   a. Positive (+): VOUT
   b. Negative (-): GND
6. After making the connections, turn on the power supply. The board should start up automatically.
7. To use the enable (EN) function, apply a digital input to the EN pin. Drive EN above 1V to turn the regulator on; drive EN below 0.85V to turn it off. If the EN function is not used, connect EN directly to VIN.
8. The feedback voltage (V_{FB}) is typically 0.6V for the adjustable-output version. The external resistor divider connected to FB sets the output voltage (V_{OUT}) (see Figure 1). To work in a multi-phase topology, the VOUT/FB pins of the devices must be connected directly or through feedback (FB) resistors.

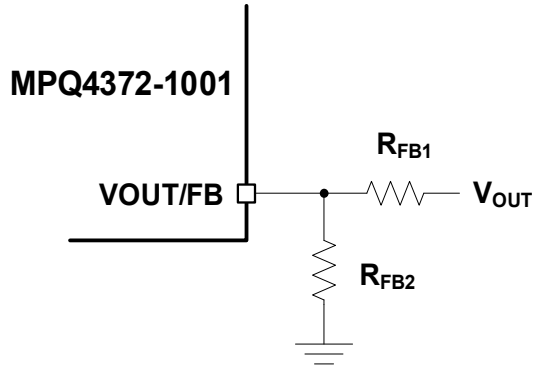


Figure 1: Feedback Divider Network for the Adjustable-Output Version

Table 1 lists the recommended feedback resistances for common output voltages.

Table 1: Feedback Resistor Selection for the Adjustable-Output Version

V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)
1	66.5 (1%)	100 (1%)
3.3	100 (1%)	22.1 (1%)
5	100 (1%)	13.7 (1%)

For primary devices in multi-phase applications, it is recommended for the PG resistance to be 100kΩ. The MPQ4372-1001 has an open-drain PG output to indicate whether the regulator output is within its nominal window. Connect PG to a logic high level power source (e.g. 3.3V) via a pull-up resistor. PG is pulled high if V_{OUT} is within 94% to 106% of its nominal voltage; PG is pulled low if V_{OUT} exceeds 107% or falls below 93% of its nominal voltage. Float the PG pin if it is not used.

For secondary devices in multi-phase applications, the PG pin sets the phase shift via a resistor (R_{PHASE}) connected to ground. Table 2 shows the relationship between the phase shift and R_{PHASE} under high- and low-frequency conditions.

Table 2: Phase Shift vs. R_{PHASE}

Phase Shift	R_{PHASE} = 410kHz	R_{PHASE} = 2.2MHz
90°	33kΩ	4.87kΩ
120°	46.4kΩ	7.32kΩ
180°	73.2kΩ	12.1kΩ
240°	97.6kΩ	16.9kΩ
270°	115kΩ	19.1kΩ
359°	150kΩ	26.1kΩ

9. The MPQ4372-1001's switching frequency (f_{SW}) can be configured via the FREQ pin's resistor (R_{FREQ}). The resistor can be estimated based on the relationship between f_{SW} and R_{FREQ}. Table 3 shows common values for f_{SW} and R_{FREQ}.

Table 3: f_{SW} vs R_{FREQ}

f_{SW} (kHz)	R_{FREQ} (kΩ)
2500	13
2330	14.3
2200	15
2100	15.8
1800	18.7
1520	22.6
1270	27.4
1100	32.4
870	41.2
710	51.1
520	71.5
410	88.7
370	100
210	182

10. Primary and secondary are terms used to describe different IC roles in a multi-phase power converter. The primary IC generates a clock signal that the secondary IC(s) synchronize to, and asserts PG based on the output regulation. The chip detects the SYNCO pin during start-up to configure the primary and secondary ICs. The impedance measurement is done internally by biasing the SYNCO pin and comparing the SYNCO voltage (V_{SYNCO}) to a reference. If V_{SYNCO} is between 5/12 x V_{CC} and 7/12 x V_{CC}, the part acts as a primary device. If V_{SYNCO} exceeds 5/12 x V_{CC} or falls below 7/12 x V_{CC}, the part acts as a secondary device. In applications where the mode is changed during operation, use a ≤4.7kΩ pull-up or pull-down resistor for secondary devices to ensure proper detection.
11. The primary device's SYNCO pin connects to the secondary device's SYNCIN/MODE pins, which are interleaved. If the primary device's SYNCIN/MODE pin is used for mode selection, the secondary device's SYNCO pin can be tied to the primary device's SYNCIN/MODE pin. Pull SYNCIN/MODE low to force the device to operate in advanced asynchronous modulation (AAM) mode; pull it high to force the device to operate in forced continuous conduction mode (FCCM) (see Table 4 on page 5).

If the primary device's SYNCIN/MODE pin is applied with the external clock signal to synchronize the internal oscillator frequency, the secondary device's SYNCO pins can only be pulled high or low, and cannot connect to the primary device's SYNCN/MODE pin.

Table 4: Mode Selection

SYNCIN/MODE Input	Operation
Floating	AAM mode
<0.4V	AAM mode
>1.4V or external clock in	FCCM

Refer to the Application Information section in the MPQ4372-1001 datasheet to calculate the inductance (L) and output capacitance (C_{OUT}).

Figure 2 shows the measurement equipment set-up.

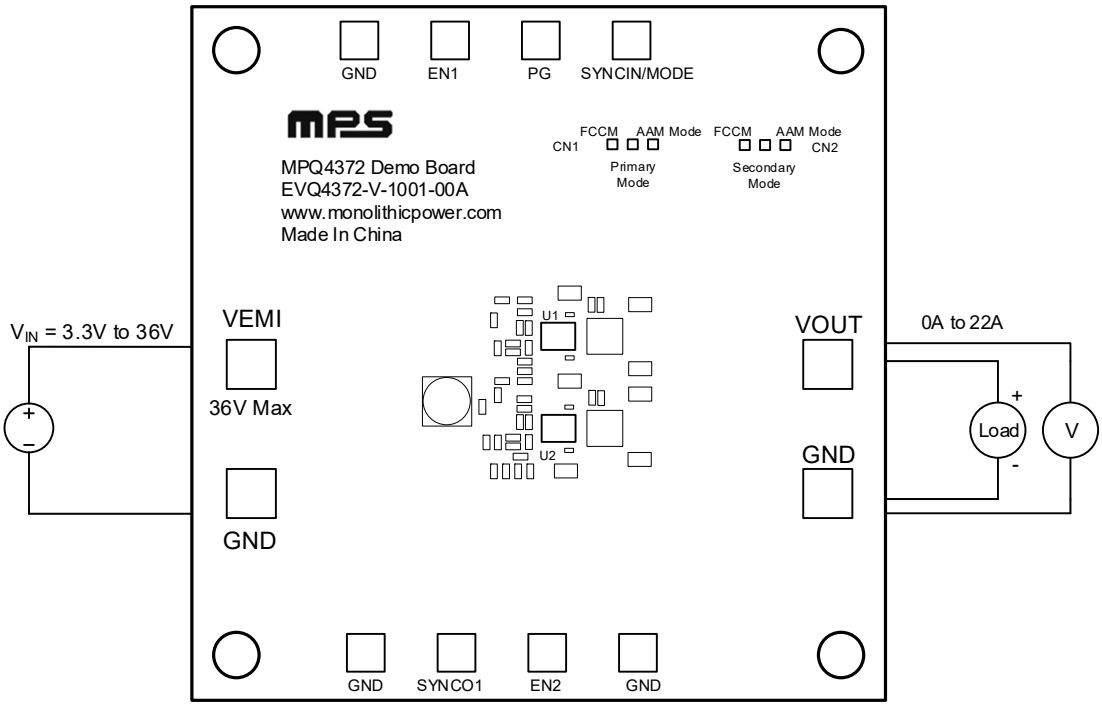


Figure 2: Measurement Equipment Set-Up

EVALUATION BOARD SCHEMATIC

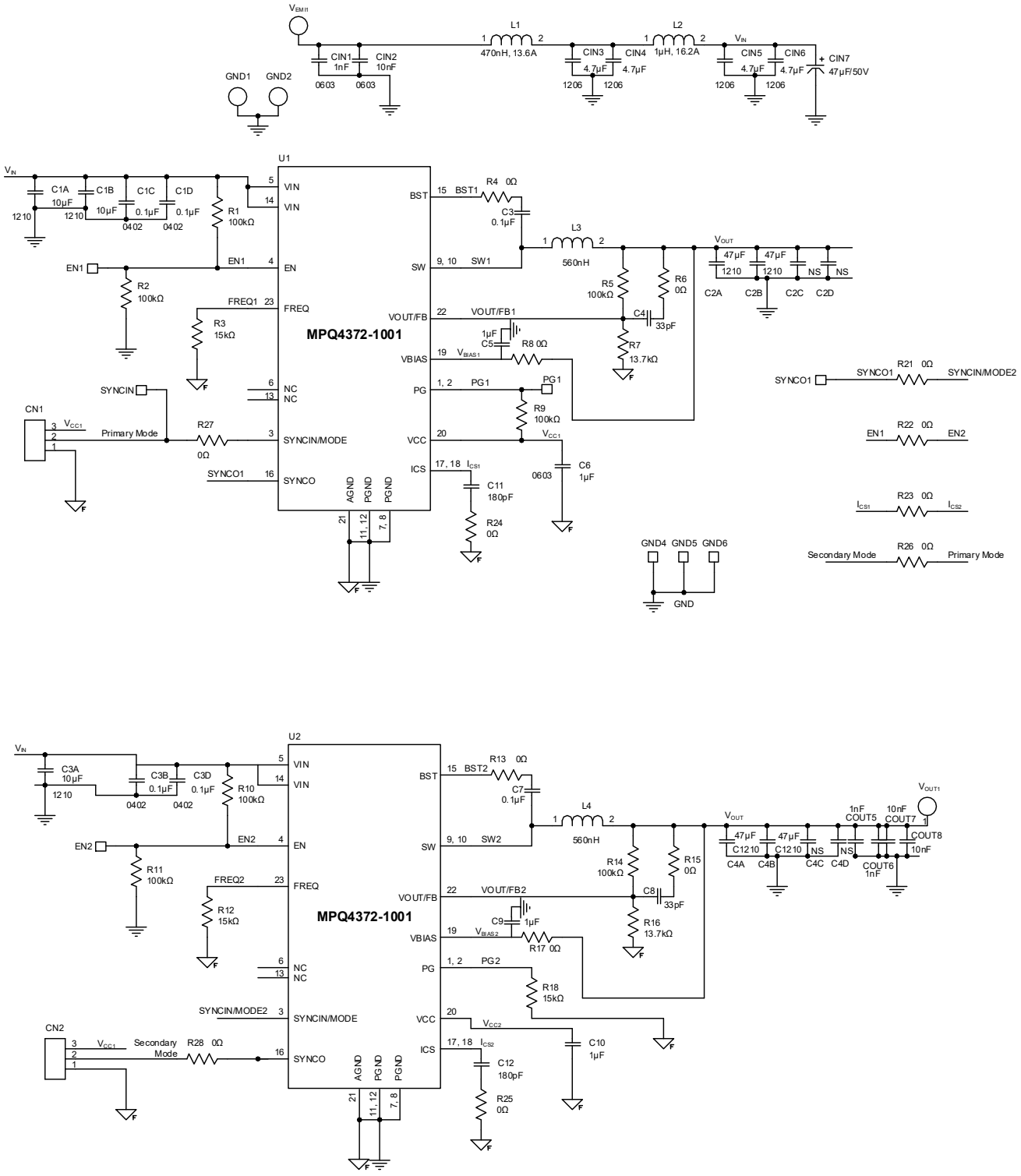
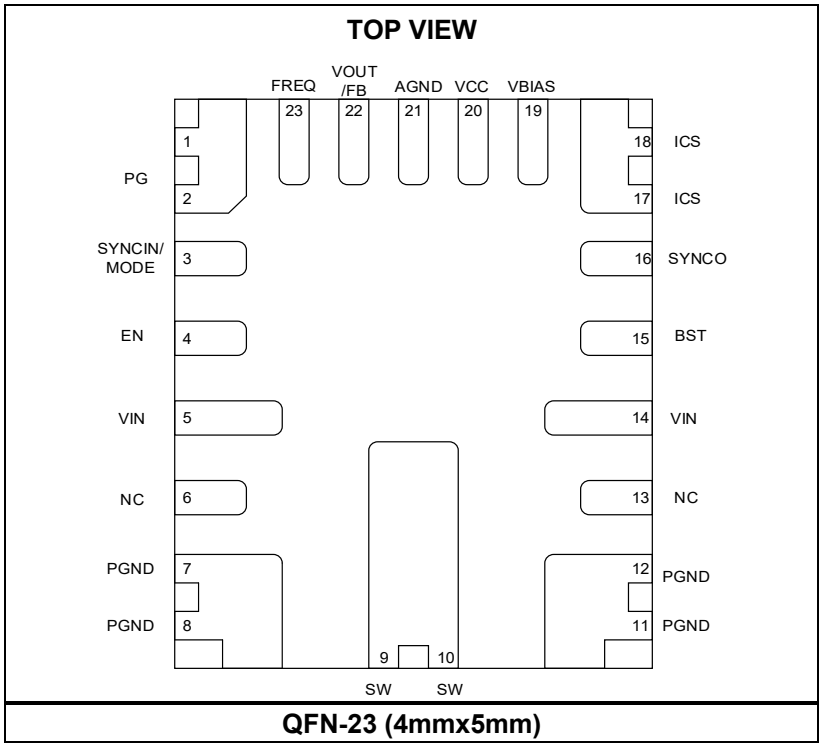


Figure 3: Evaluation Board Schematic

PACKAGE REFERENCE



QFN-23 (4mmx5mm)

EVQ4372-V-1000-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
3	CIN1, COUT5, COUT6	1nF	Ceramic capacitor, 50V, X7R	0603	Murata	GRM216R71H102KA01
3	CIN2, COUT7, COUT8	10nF	Ceramic capacitor, 50V, X7R	0603	Murata	GRM188R71H103KA01D
4	CIN3, CIN4, CIN5, CIN6	4.7μF	Ceramic capacitor, 50V, X7S	1206	Murata	GRM31CC72A475KE11
1	CIN7	47μF	Aluminum capacitor, 50V	SMD	Panasonic	EEEFN1H470XP
3	C1A, C1B, C3A	10μF	Ceramic capacitor, 50V, X7R	1210	Murata	GRM32ER71H106KA12L
4	C1C, C1D, C3B, C3D	0.1μF	Ceramic capacitor, 50V, X7R	0402	Murata	GRM155R71H104KE14D
2	C3, C7	0.1μF	Ceramic capacitor, 50V, X7R	0603	Murata	GCJ188R71H104KA12D
4	C2A, C2B, C4A, C4C	47μF	Ceramic capacitor, 10V, X7R	1210	Murata	LMK325B7476MM-TR
2	C4，C8	33pF	Ceramic capacitor, 50V, C0G	0603	Murata	GRM1885C1H330JA01D
2	C11, C12	180pF	Ceramic capacitor, 50V, C0G	0603	Murata	GRM1885C1H181JA01D
4	C5, C6, C9, C10	1μF	Ceramic capacitor, 16V, X7R	0603	Murata	GRM188R61A475KE15D
4	C2C, C2D, C4C, C4D	NS				
2	L3, L4	560nH	Inductor, 3mΩ, 29A	SMD	Coilcraft	XAL6030-561MEB
7	R1, R2, R5, R9, R10, R11, R14	100KΩ	Film resistor, 1%	0603	Yageo	RC0603FR-07100KL
3	R3, R12, R18	15kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0715KL
14	R4, R8, R6, R13, R15, R17, R21, R22, R23, R24, R25, R26, R27, R28	0Ω	Film resistor, 5%	0603	Yageo	RC0603JR-070RL
2	R7, R16	13.7kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0713K7L
2	CN1, CN2	2.54mm	3-pin	DIP	Any	
4	VEMI GND, VOUT, GND	2mm	Golden pin	DIP	Custom (2)	
10	SYNCIN/MODE, PG, SYNCO1, EN1, EN2, GND	1mm	Golden pin	DIP	Custom (2)	
1	L1	470nH	Inductor, 3.78mΩ, 13.6A	SMD	MPS	MPL-AL5030-R47
1	L2	1μH	Inductor, 4.3mΩ, 16.2A	SMD	MPS	MPL-AL6050-1R0
2	U1, U2	MPQ4372-AEC1	36V, 22A, dual-phase application, sensorless, brushless, step-down DC (BLDC) converter	QFN-23 (4mmx 5mm)	MPS	MPQ4372GVE-1001-AEC1

Note:

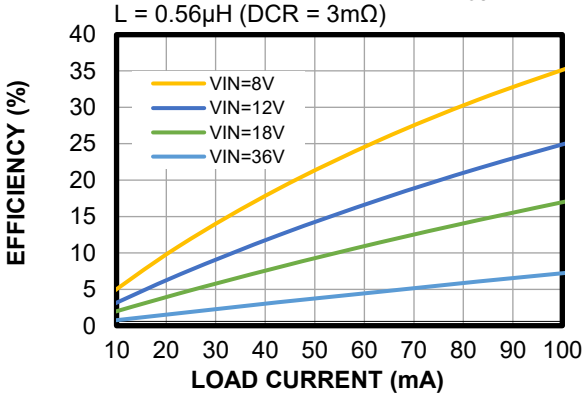
2) MPS custom-produces these pins. Contact an MPS FAE for more information.

EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 12V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ), T_A = 25°C, unless otherwise noted.

Efficiency vs. Load Current

FCCM, V_{OUT} = 5V, f_{SW} = 2.2MHz, dual-phase, V_{BIAS} connected to V_{OUT}, L = 0.56µH (DCR = 3mΩ)



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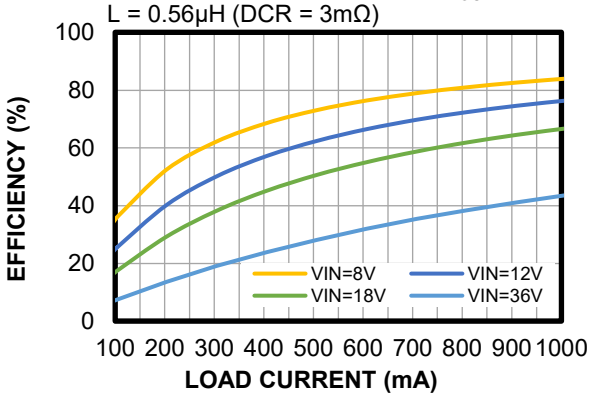
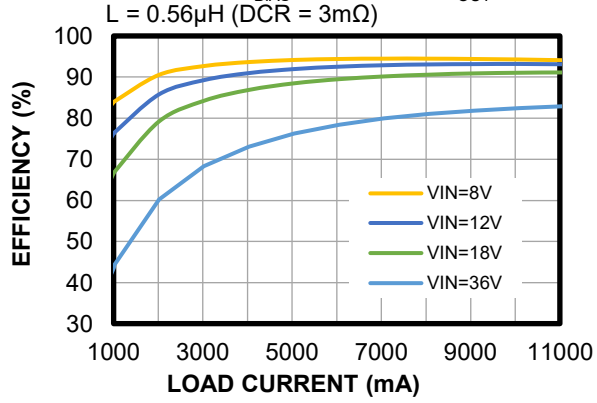


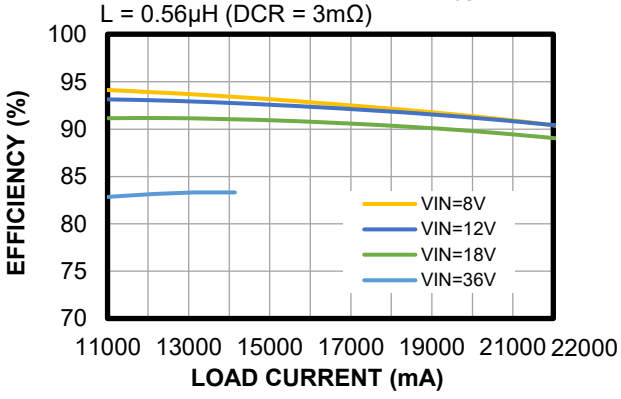
Efficiency vs. Load Current

FCCM, V_{OUT} = 5V, f_{SW} = 2.2MHz, dual-phase, V_{BIAS} connected to V_{OUT}, L = 0.56µH (DCR = 3mΩ)



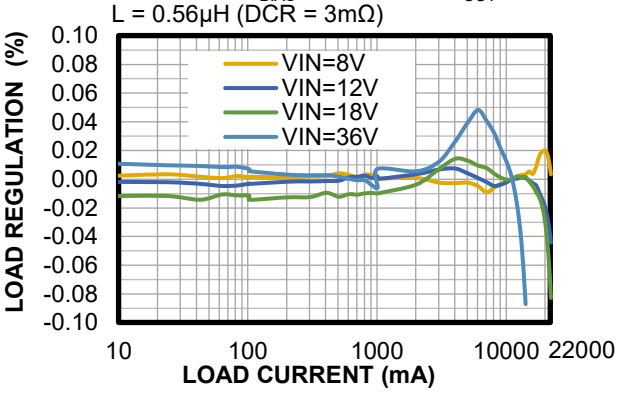
Efficiency vs. Load Current

FCCM, V_{OUT} = 5V, f_{SW} = 2.2MHz, dual-phase, V_{BIAS} connected to V_{OUT}, L = 0.56µH (DCR = 3mΩ)



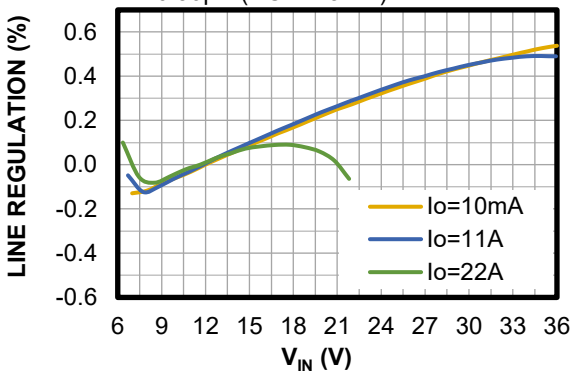
Load Regulation

FCCM, V_{OUT} = 5V, f_{SW} = 2.2MHz, dual-phase, V_{BIAS} connected to V_{OUT}, L = 0.56µH (DCR = 3mΩ)



Line Regulation

FCCM, V_{OUT} = 5V, f_{SW} = 2.2MHz, dual-phase, V_{BIAS} connected to V_{OUT}, L = 0.56µH (DCR = 3mΩ)

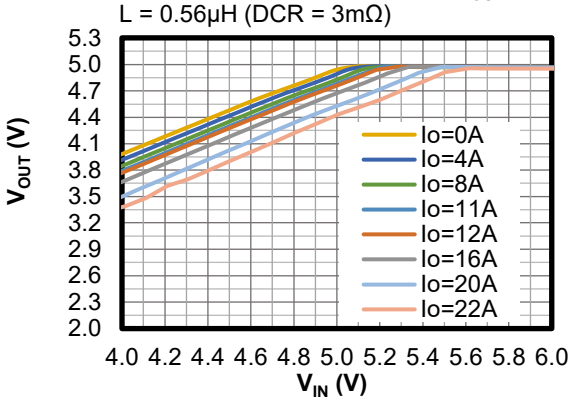


EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 12V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ), T_A = 25°C, unless otherwise noted.

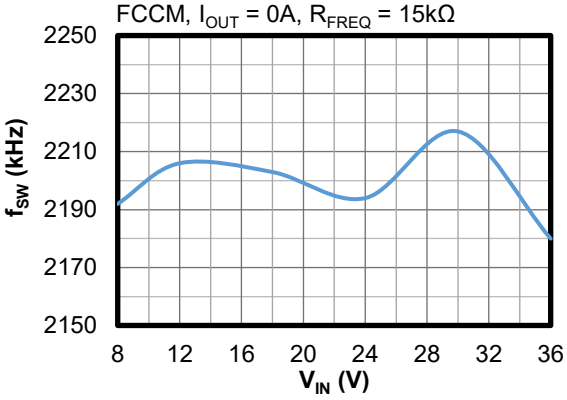
Low-Dropout Mode

FCCM, V_{OUT} = 5V, f_{SW} = 2.2MHz, dual-phase, V_{BIAS} connected to V_{OUT}, L = 0.56µH (DCR = 3mΩ)



Switching Frequency vs. Input Voltage

FCCM, I_{OUT} = 0A, R_{FREQ} = 15kΩ

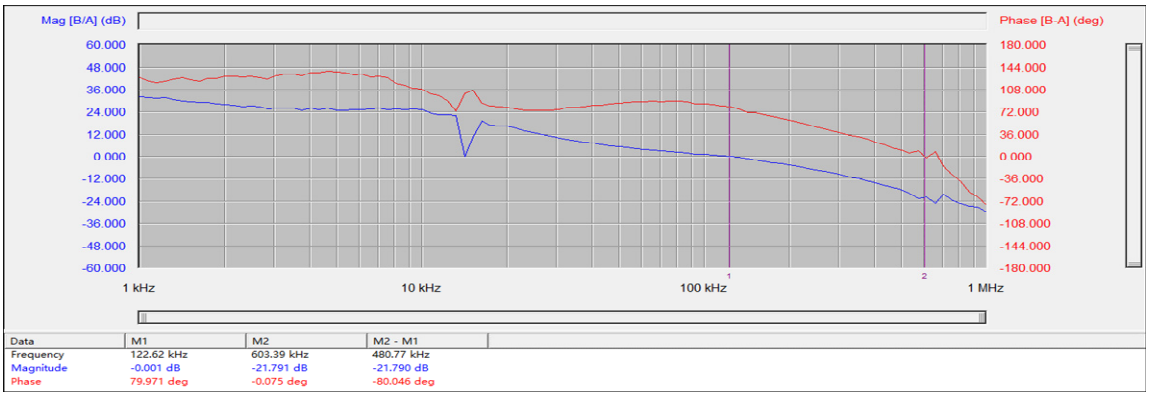


EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 12V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ), T_A = 25°C, unless otherwise noted.

Loop Performance

I_{OUT} = 11A, T_A = 25°C

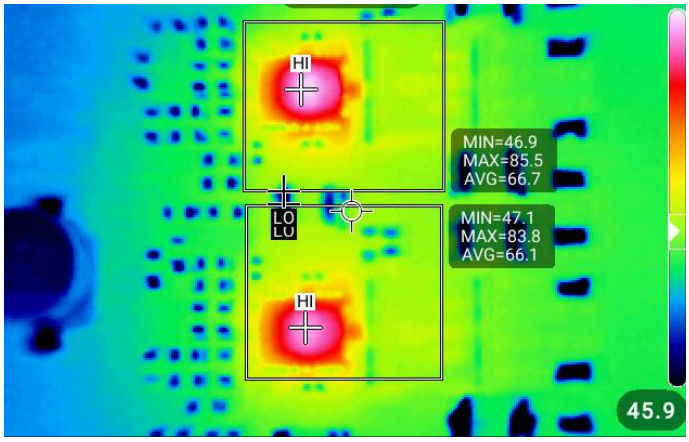


EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 12V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ), T_A = 25°C, unless otherwise noted.

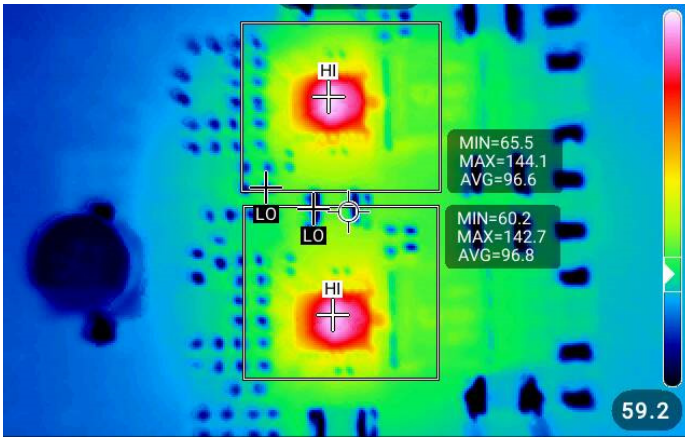
Thermal Performance

V_{OUT} = 5V, I_{OUT} = 11A, no forced airflow, T_{CASE} = 85.5°C



Thermal Performance

V_{OUT} = 5V, I_{OUT} = 18A, no forced airflow, T_{CASE} = 144°C

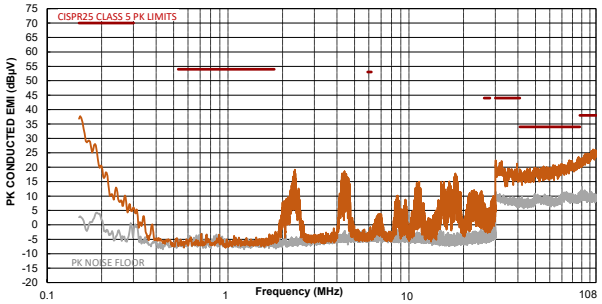


EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 20A, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ), T_A = 25°C, unless otherwise noted.

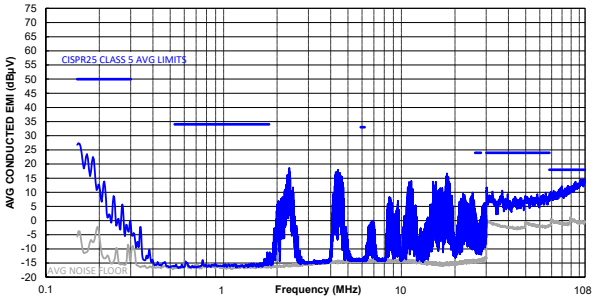
CISPR 25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



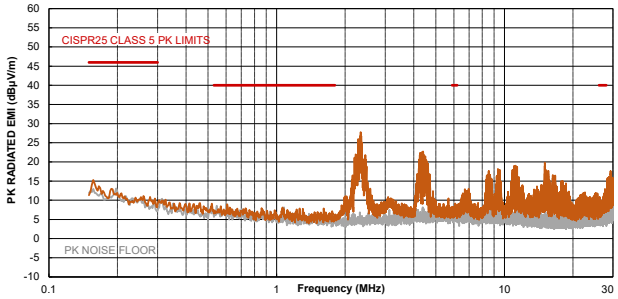
CISPR 25 Class 5 Average Conducted Emissions

150kHz to 108MHz



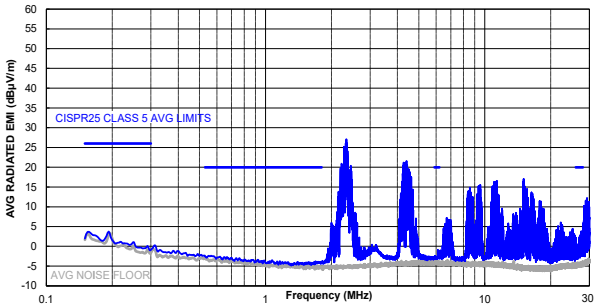
CISPR 25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



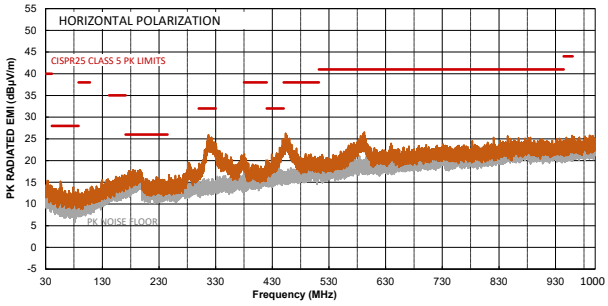
CISPR 25 Class 5 Average Radiated Emissions

150kHz to 30MHz



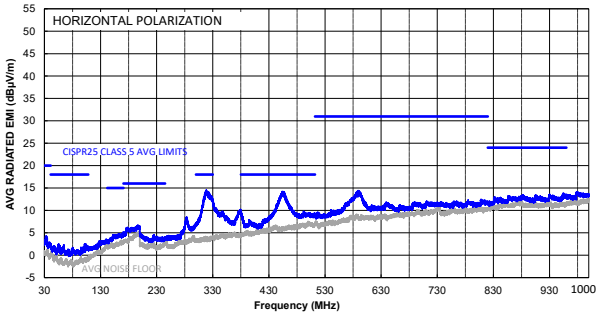
CISPR 25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 1GHz



CISPR 25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 1GHz

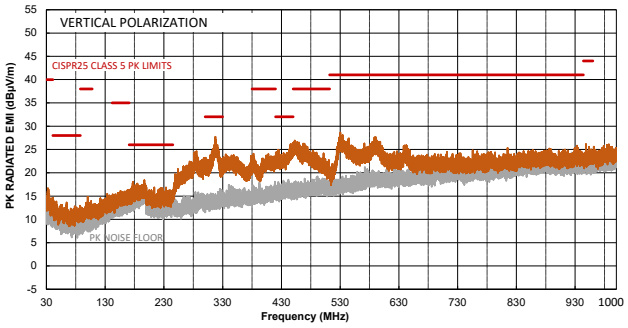


EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 20A, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ), T_A = 25°C, unless otherwise noted.

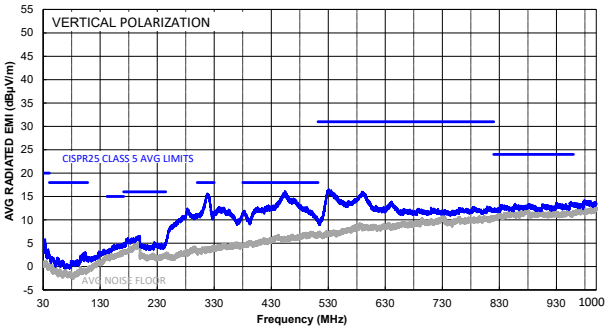
CISPR 25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR 25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz

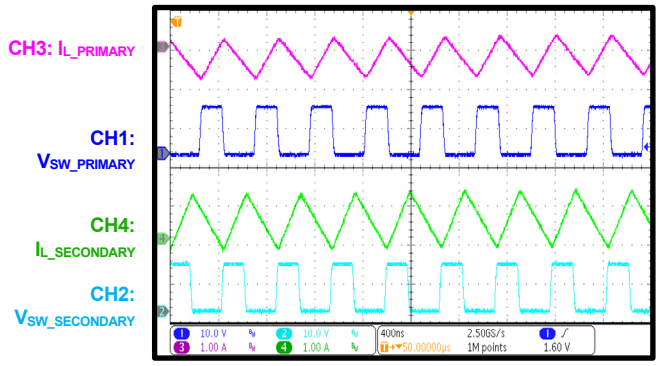


EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 12V, V_{OUT} = 5V, L = 0.56µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

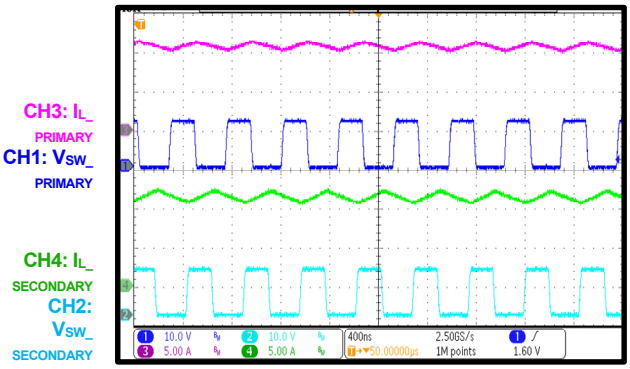
Steady State

I_{OUT} = 0A



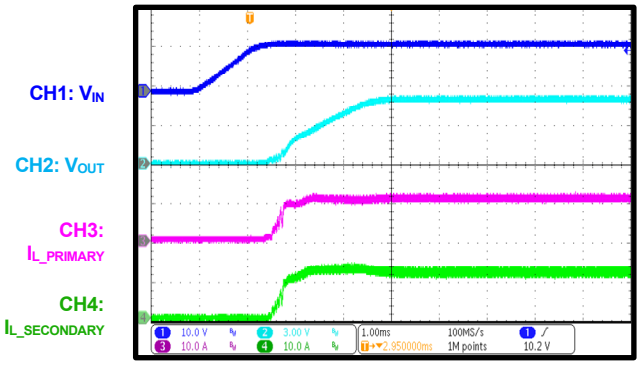
Steady State

I_{OUT} = 22A



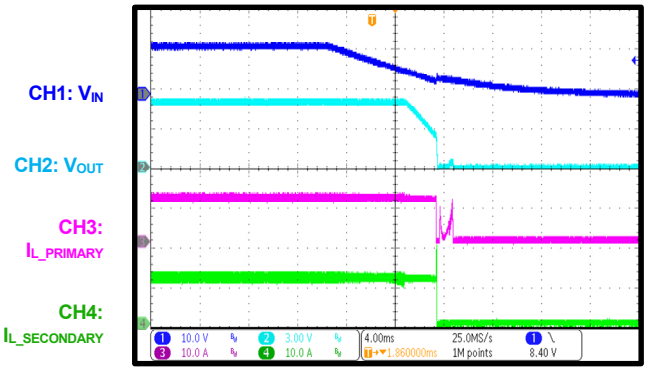
Start-Up through VIN

I_{OUT} = 22A



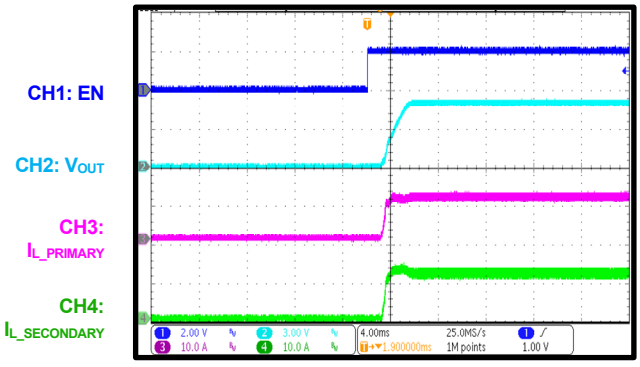
Shutdown through VIN

I_{OUT} = 22A



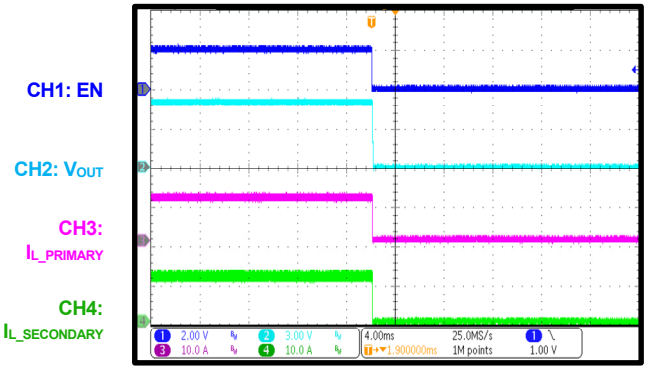
Start-Up through EN

I_{OUT} = 22A



Shutdown through EN

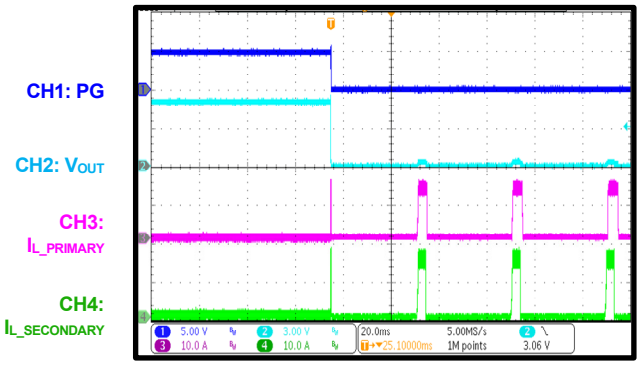
I_{OUT} = 22A



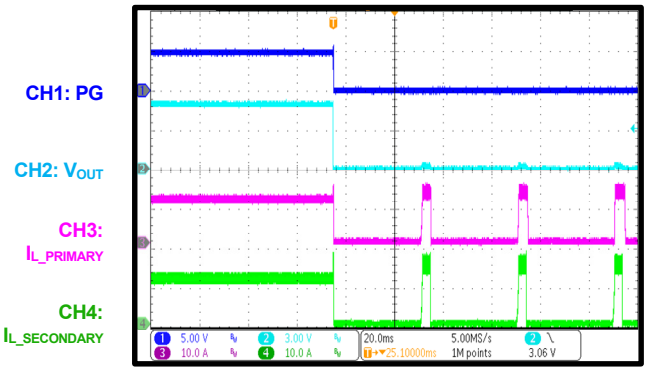
EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 12V, V_{OUT} = 5V, L = 0.56µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

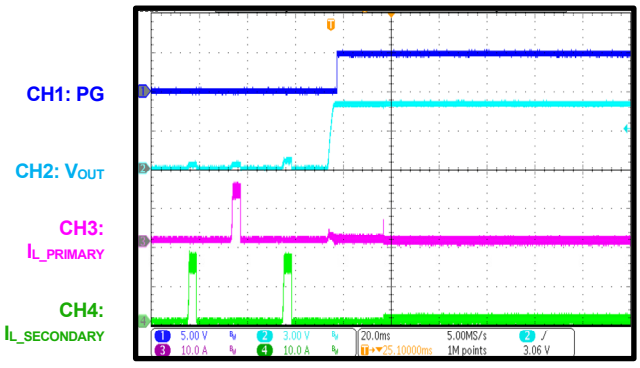
SCP Entry
I_{OUT} = 0A



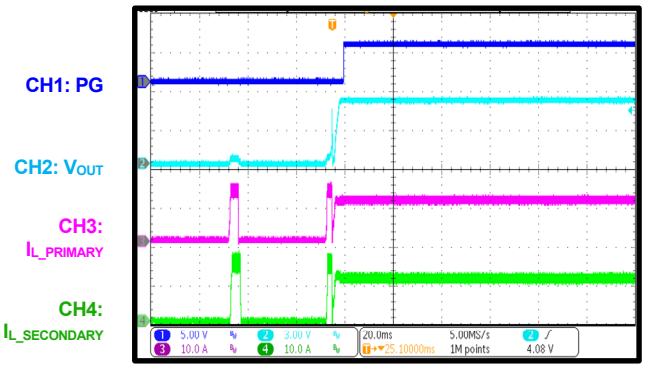
SCP Entry
I_{OUT} = 22A



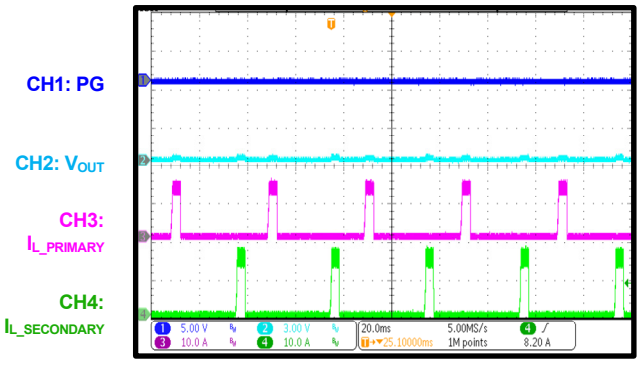
SCP Recovery
I_{OUT} = 0A



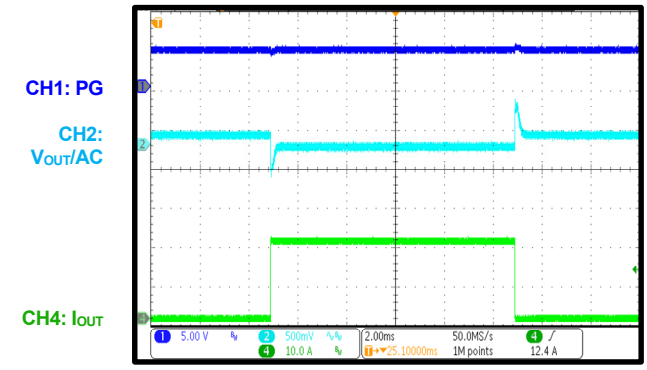
SCP Recovery
I_{OUT} = 22A



SCP Steady State



Load Transient Response
I_{OUT} = 0A to 22A, 1.6A/µs

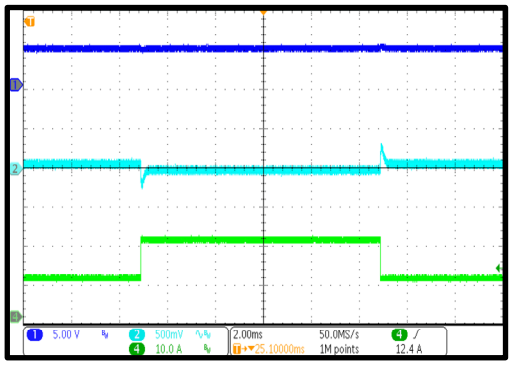


EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 12V, V_{OUT} = 5V, L = 0.56µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

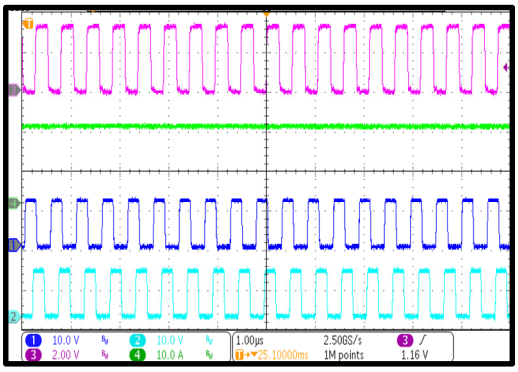
Load Transient Response

I_{OUT} = 11A to 22A, 1.6A/µs



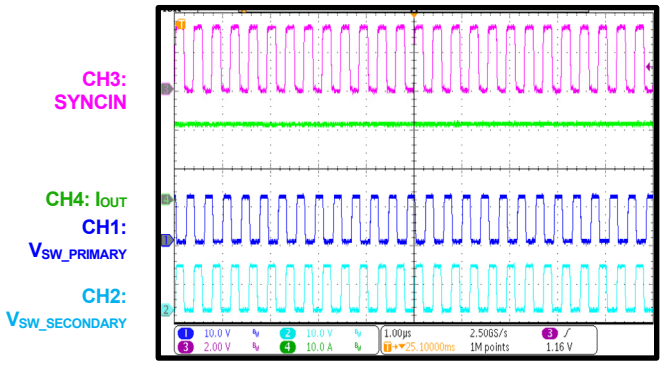
SYNCIN Operation

I_{OUT} = 22A, f_{SYNC} = 1.9MHz



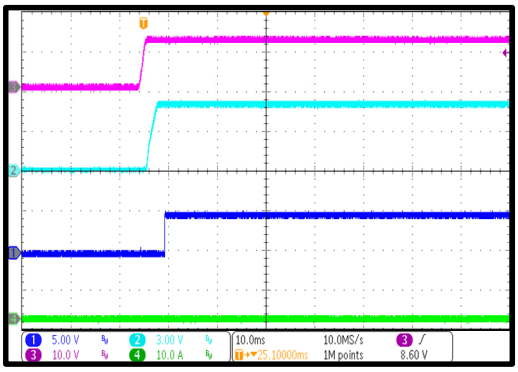
SYNCIN Operation

I_{OUT} = 22A, f_{SYNC} = 2.6MHz



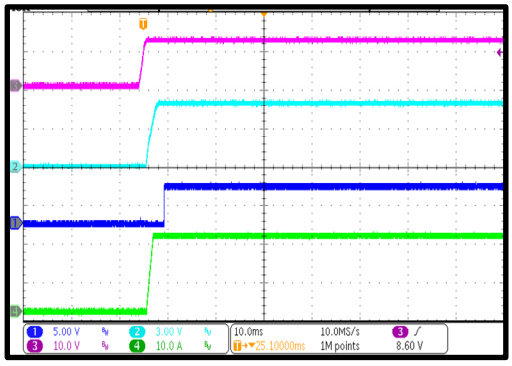
PG in Start-Up through VIN

I_{OUT} = 0A



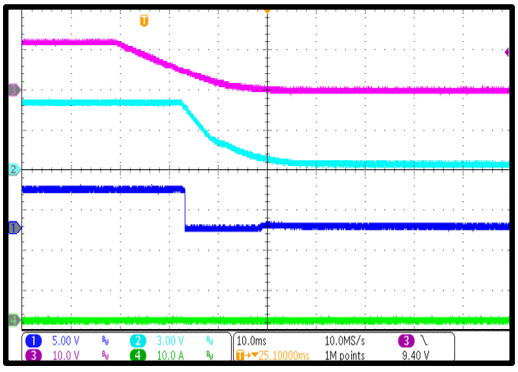
PG in Start-Up through VIN

I_{OUT} = 22A



PG in Shutdown through VIN

I_{OUT} = 0A

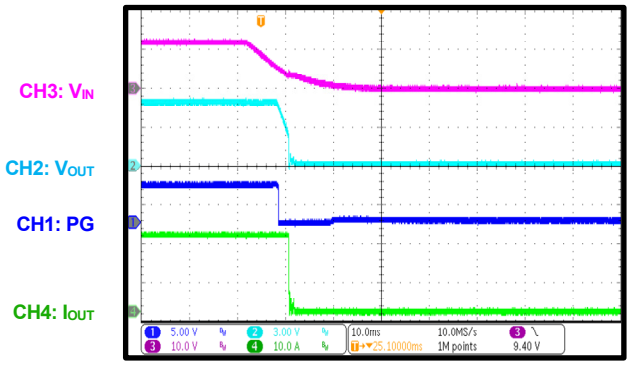


EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 12V, V_{OUT} = 5V, L = 0.56µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

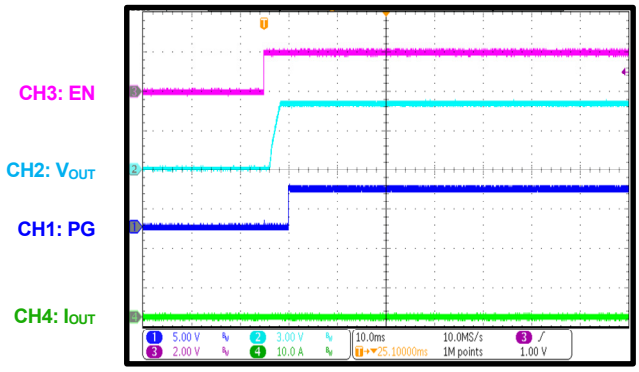
PG in Shutdown through VIN

I_{OUT} = 22A



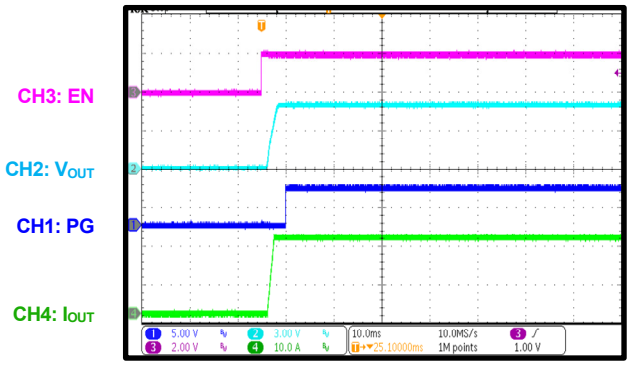
PG in Start-Up through EN

I_{OUT} = 0A



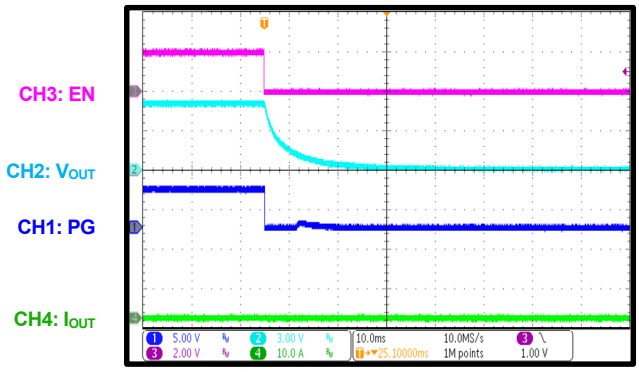
PG in Start-Up through EN

I_{OUT} = 22A



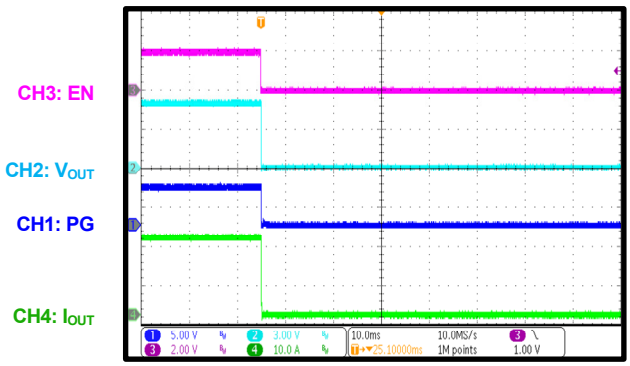
PG in Shutdown through EN

I_{OUT} = 0A



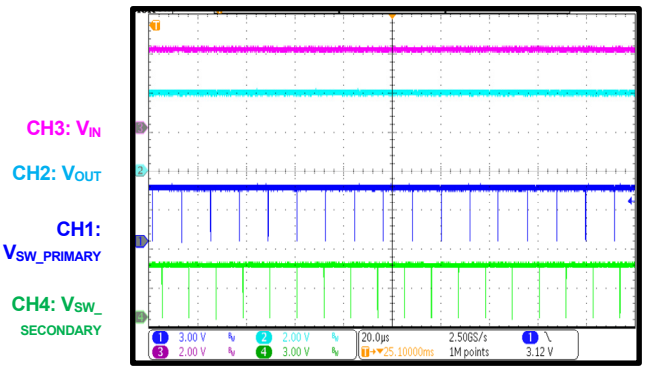
PG in Shutdown through EN

I_{OUT} = 22A



Low-Dropout Mode

V_{IN} = 4V, V_{OUT} set to 5V, I_{OUT} = 0A

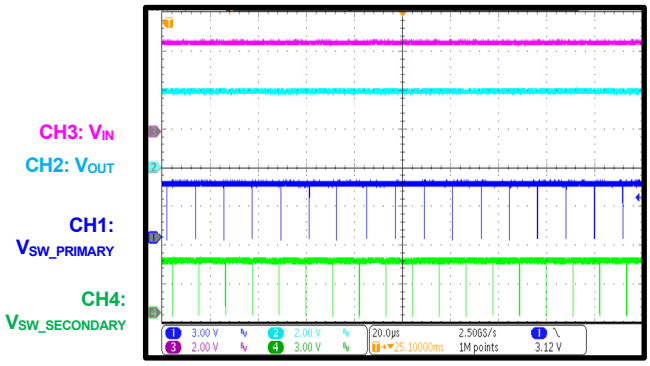


EVB TEST RESULTS *(continued)*

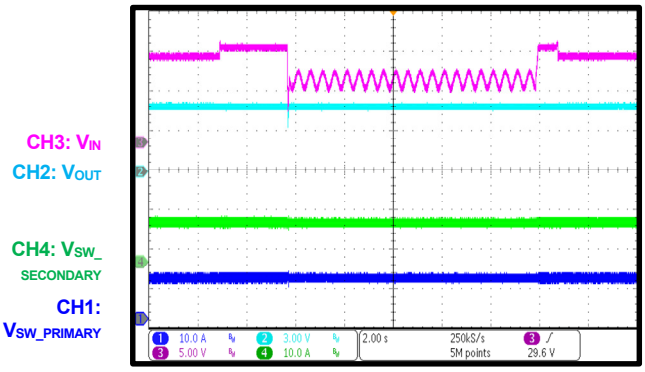
Performance curves and waveforms are tested on the evaluation board. V_{IN} = 12V, V_{OUT} = 5V, L = 0.56µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

Low-Dropout Mode

V_{IN} = 4V, V_{OUT} set to 5V, I_{OUT} = 22A

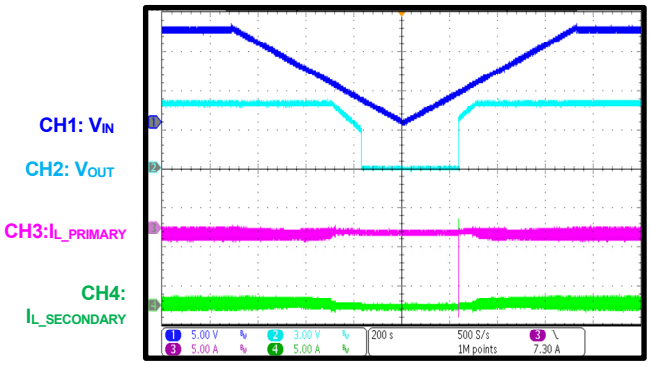


Cold Crank



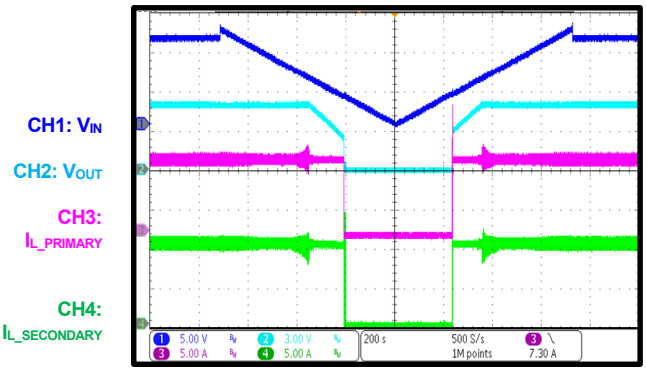
V_{IN} Ramping Down and Up

I_{OUT} = 0A



V_{IN} Ramping Down and Up

I_{OUT} = 22A



PCB LAYOUT (3)

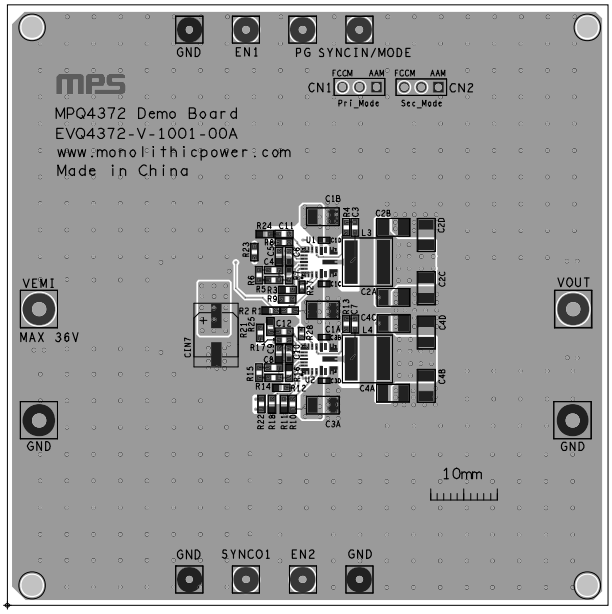


Figure 4: Top Silk and Top Layer

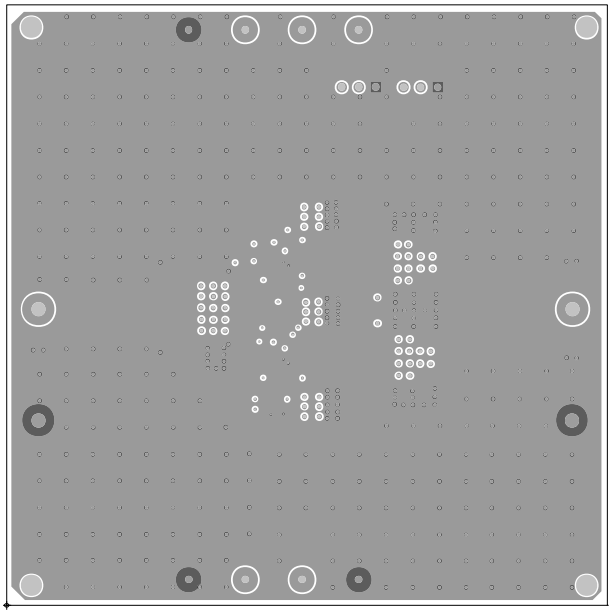


Figure 5: Mid-Layer 1

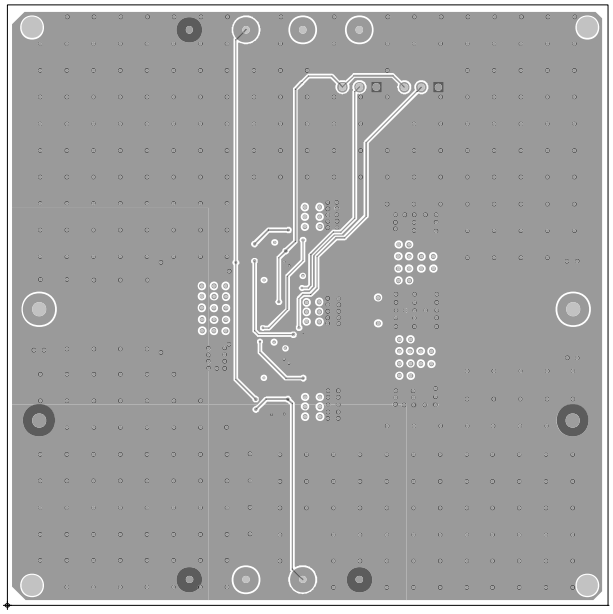


Figure 6: Mid-Layer 2

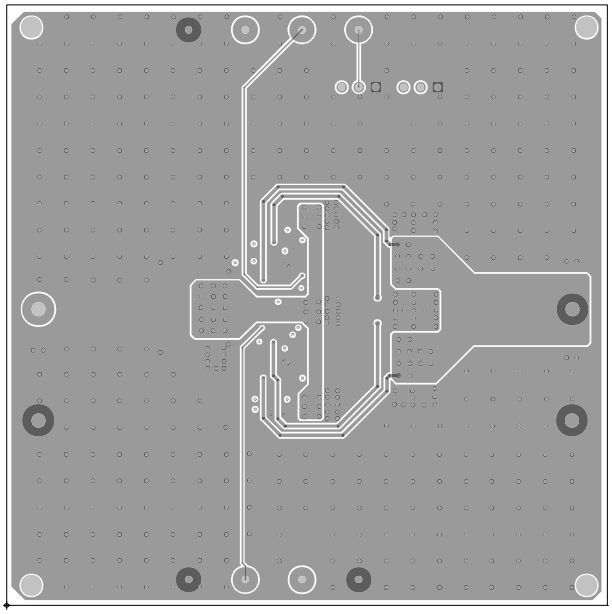


Figure 7: Mid-Layer 3

PCB LAYOUT *(continued)* (3)

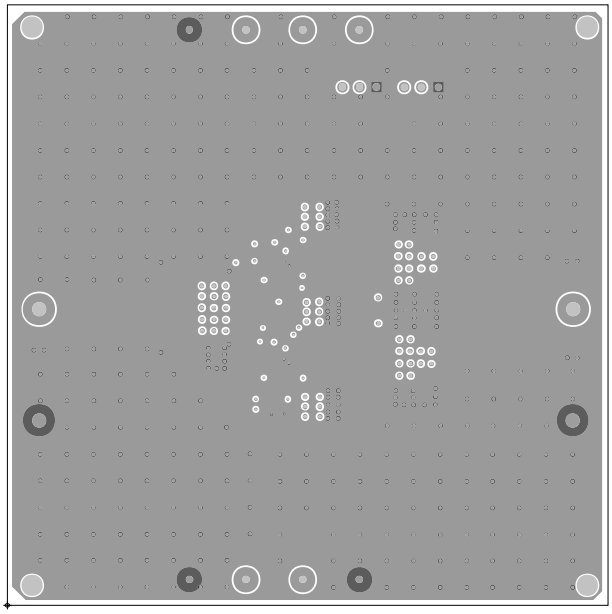


Figure 8: Mid-Layer 4

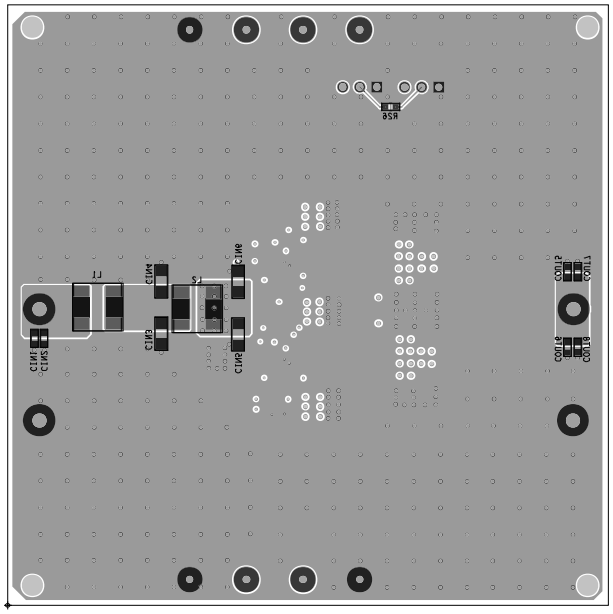


Figure 9: Bottom Layer and Bottom Silk

Note:

3) The copper thickness is 2oz.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	10/29/2024	Initial Release	-