EVQ4263-QVE-00A

36V, 140W Buck-Boost with Integrated Low-Side MOSFETs, Supports High-Side Current Sense and I²C, AEC-Q100 Qualified

DESCRIPTION

The EVQ42463-QVE-00A evaluation board is designed to demonstrate the capabilities of the MPQ4263, a buck-boost converter with two integrated low-side MOSFETs (LS-FETs). The device can deliver up to 140W of peak output power (P_{OUT}) across a certain input voltage (V_{IN}) supply range with excellent efficiency.

The MPQ4263 is well-suited for USB power delivery (PD) applications. It can work well with an external USB PD controller through the I²C interface.

It is recommended to read the MPQ4263 datasheet prior to making any changes to the EVQ4263-QVE-00A.

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C, unless otherwise noted.

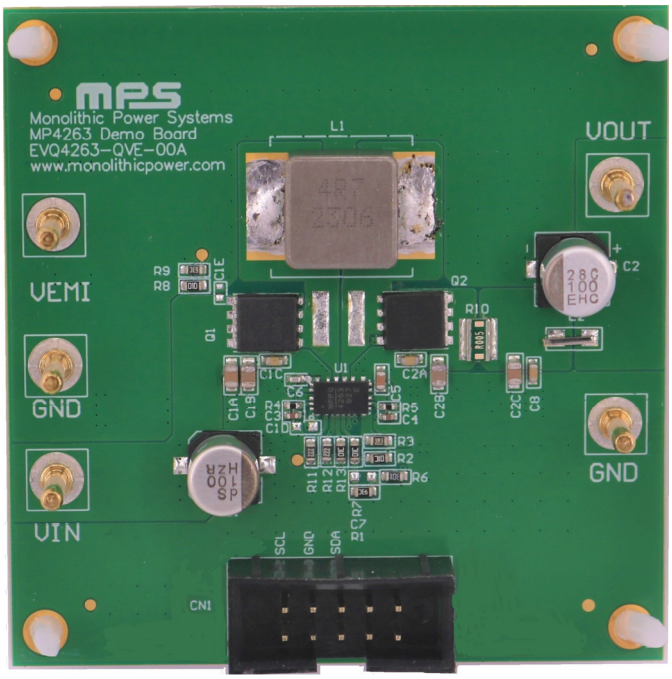
Parameters	Conditions	Value
Input voltage (V_{IN}) range (2)		3.6V to 36V
Output voltage (V_{OUT})	V_{IN} = 3.6V to 36V, I_{OUT} = 0A to 5A	V_{OUT} = 5V
Maximum output current (I_{OUT})		7A (1)
Typical efficiency	V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 5A	94.35%
Peak efficiency	V_{IN} = 12V, V_{OUT} = 15V, I_{OUT} = 2.5A	97.97%
Switching frequency (f_{SW})		420kHz

Notes:

1) The default output current (I_{OUT}) limit is 5.4A, and the resistor (R_{SENS}) must be reduced or shorted to output a 7A current.
2) If V_{IN} > 19V, the device can support 28V/5A, with a 140W output.

MPL Optimized Performance with MPS Inductor MPL-AL5030 Series

EVQ4263-QVE-00A EVALUATION BOARD



LxWxH (60mmx60mmx10mm)

4 Layers, 2oz/1oz/1oz/2oz

Board Number	MPS IC Number
EVQ4263-QVE-00A	MPQ4263GQVE-0000-AEC1

QUICK START GUIDE

1. Preset the power supply (V_{IN}) to 12V, then turn off the power supply.
2. Connect the power supply terminals to:
   a. Positive (+): VIN
   b. Negative (-): GND
3. Connect the electronic load to:
   a. Positive (+): VOUT
   b. Negative (-): GND
4. After making the connections, turn on the power supply.
5. V_{OUT} should start up automatically after start-up.
6. To modify the MPQ4263's register setting, connect the EVQ4263-QVE-00A to the USB-to-I²C communication kit (EVKT-USBI2C-02). Use Virtual Bench Pro 4.0 to read and write to the I²C registers.
7. If the MPQ4263's silicon die temperature exceeds 160°C, over-temperature protection (OTP) is triggered and the entire chip shuts down. Once the temperature drops below 140°C, the chip is enabled again and resumes normal operation.

   Figure 1 shows the measurement equipment set-up.

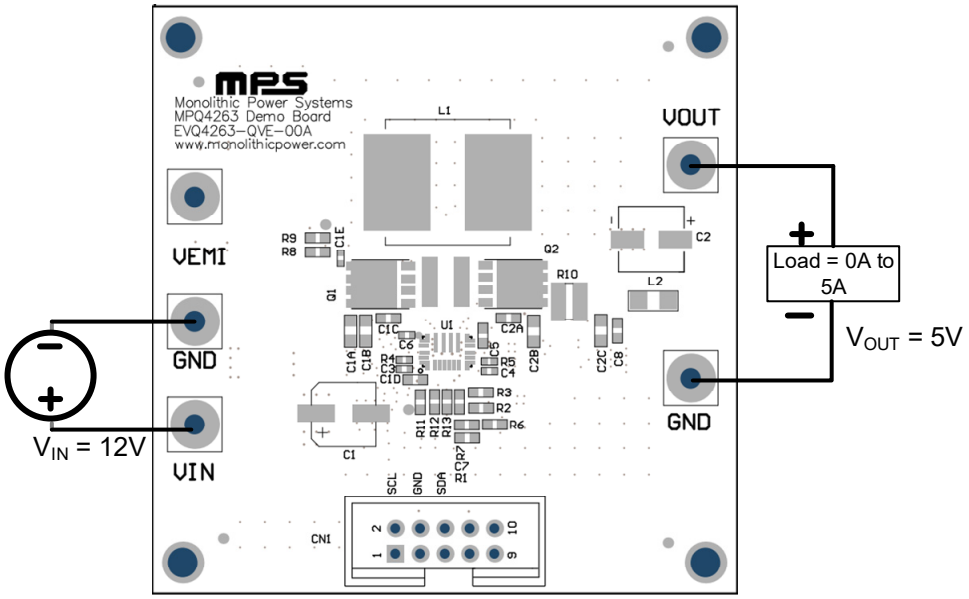


Figure 1: Measurement Equipment Set-Up

MPQ4263GQVE-0000-AEC1 CONFIGURATION TABLE

OTP Items	Description	Value
OPERATION	Sets the device on or off.	1: On
VOUT_COMMAND	Sets the output voltage.	V_{REF} = 0.5V
DITHER_ENABLE	Enables frequency spread spectrum.	0: Disabled
FREQ	Sets the switching frequency.	01: 420kHz
SWA_FET_RON	Sets SWA's on resistance.	01: 10mΩ
OUTPUT_OVP_EN	Enables output over-voltage protection (OVP).	1: Enabled (default)
OUTPUT_DISCHARGE_EN	Enables the output discharge function during the input voltage (V_{IN}), I²C, or EN off period.	1: Enabled (default)
PFM/PWM_MODE	Selects automatic pulse-frequency modulation (PFM) / pulse-width modulation (PWM) mode or forced PWM mode.	1: Forced PWM mode (default)
CONSTANT_ CURRENT_LIMIT	Sets the output current limit.	5.4A
LDC Disable	Sets the output voltage compensation value vs. load current.	0: Enable line drop compensation (default)
Line Drop Compensation	Sets the output voltage compensation value vs. load current.	00: No compensation (default)
SWITCHING_ CURRENT_LIMIT	Sets the SWB valley current limit and SWC peak current limit.	01: SWC peak 12A / SWB valley 9A (default)
RSENS	Selects the R_{SENS} resistor value.	0: 5mΩ
SLEW_RATE_RISE	Sets the V_{OUT} rising slew rate.	01: 0.16mV/μs (default)
SLEW_RATE_FALL	Sets the V_{OUT} falling slew rate.	01: 0.04mV/μs
FREQ_MODE	Sets the frequency for buck-boost mode.	Keep the frequency unchanged in buck-boost mode
CC_DISABLE	Enables the CC function.	0: Enable CC (default)
CC_BLANK_TIMER	Sets the blanking time before entering CC mode.	00: 250μs (default)
VIN OV Threshold	Selects the V_{IN} OV threshold.	0: 38V
V_{IN} UVLO Threshold	Selects the V_{IN} under-voltage lockout (UVLO) threshold.	0: 3.3V
Absolute Output OVP	Selects the absolute OVP threshold.	1: 38.5V
OT Warning Function	Enables the over-temperature (OT) warning function.	1: Disabled
I2C_ADDRESS	Sets the I²C slave address.	67h
VOUT_MSK	Masks ALT pin indication.	1: Mask
IOUT/POUT_MSK		0: No mask
RESERVED_MSK		1: Mask
TEMP_MSK		1: Mask
PG_STATUS#_MSK		1: Mask
PG_ALT_EDGE_MSK		1: Mask
GND_SHORT_ VBATT_MSK		1: Mask
UNKNOWN_MSK		1: Mask

EVALUATION BOARD SCHEMATIC

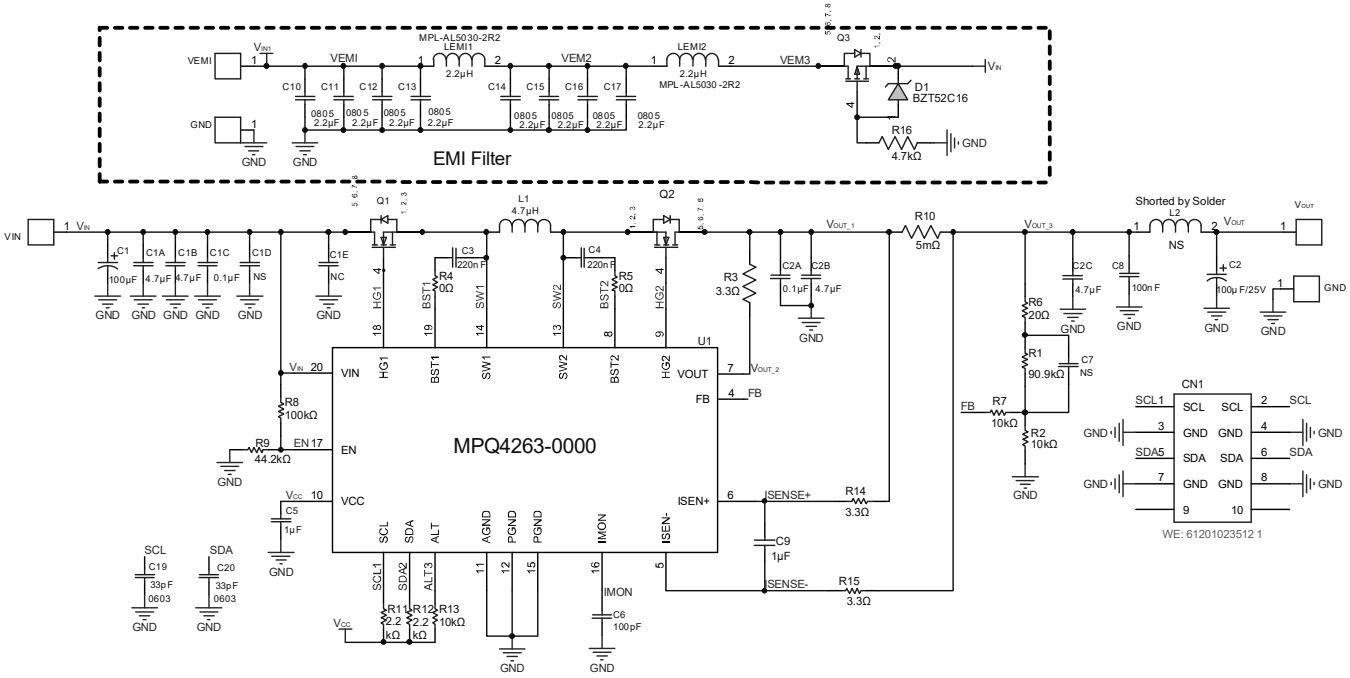


Figure 2: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 3.3V to 21V/5A, Default On)

EVQ4263-QVE-00A BILL OF MATERIALS (3)

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	C1	100µF	100µF/50V	SMD	Nippon Chemi-Con	EMZR500ARA101MF80G
1	C2	100µF	25V, hybrid, 20mΩ	SMD	Nippon Chemi-Con	HHXC250ARA101MF80G
4	C1A, C1B, C2B, C2C	4.7µF	Ceramic capacitor, 50V, X5R	0805	Murata	GRM21BR61H475ME51L
3	C1C, C2A, C8	100nF	Ceramic capacitor, 50V, X7R	0603	Wurth	885012206095
2	C3, C4	220nF	Ceramic capacitor, 16V, X5R	0402	Wurth	885012105017
1	C5	1µF	Ceramic capacitor, 10V, X7R	0603	Wurth	885012206026
1	C6	100pF	Ceramic capacitor, 25V, X7R	0402	Murata	GRM1555C1E101JA01D
1	C9	1µF	Ceramic capacitor, 10V, X5R	0402	Wurth	885012105012
8	C10, C11, C12, C13, C14, C15, C16, C17	2.2µF	Ceramic capacitor, 50V, X7T	0805	Murata	GRM21BD71H225KE01L
2	C19, C20	33pF	Ceramic capacitor, 50V, C0G	0603	Murata	GRM1885C1H330JA01D
0	C1D, C1E, C7	NS				
0	L2	NS	Shorted by solder			
1	L1	4.7µH	Inductor, R_{DC} = 8mΩ, I_{SAT} = 13A	SMD	Superworld	PIAQ1005S4R7MN
1	R1	90.9kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0790K9L
3	R2, R7, R13	10kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710KL
1	R3	3.3Ω	Film resistor, 1%	0603	Yageo	RC0603FR-073R3L
2	R4, R5	0Ω	Film resistor, 1%	0402	Yageo	RC00402FR-070L
1	R6	20Ω	Film resistor, 1%	0603	Yageo	RC0603FR-0720RL
1	R8	100kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-07100KL
1	R9	44.2kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0744K2L
1	R10	5mΩ	1%, long side, 1W, current-sensing resistor	1508	Film Tech	RL3720WT-R005-F
2	R11, R12	2.2kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-072K2L
2	R14, R15	3.3Ω	Film resistor, 1%	0402	Yageo	RC0402FR-073R3L
1	R16	4.7kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-074K7L

EVQ4263-QVE-00A BILL OF MATERIALS *(continued)* (3)

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
2	Q1, Q2	40V	MOSFET, N-channel, 40V, 30A	DFN (5mmx 6mm)	AOS	AONS66406
1	Q3	40V	MOSFET, P-channel, -40V, 50A	DFN-8L (3.3mmx 3.3mm)	Analog Power	AMQS441P
1	D1	16V	Diodes, V_F = 16V, I_F = 5mA, 500mW	SOD-123	Diodes	BZT52C16-7-F
1	CN1	10-pin	10 pins, 2 rows, straight	DIP	Wurth	612010235121
5	VEMI, VIN, VOUT, GND, GND	φ2.0	φ2.0 copper pin	DIP	Any	
1	U1	MPQ4263	Buck-boost with low-side MOSFET	QFN-20 (3mmx 5mm)	MPS	MPQ4263GQVE-0000-AEC1
2	LEMI1, LEMI2	2.2μH	Inductor, R_{DC} = 12.3mΩ, I_{SAT} = 11A	5030	MPS	MPL-AL5030-2R2

Note:

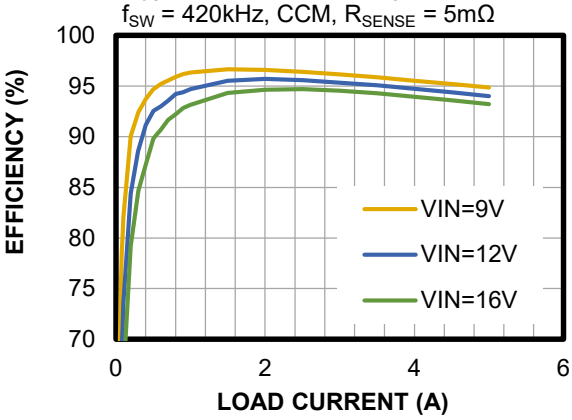
3) The BOM component selection is designed for <25V V_{OUT} applications. For >25V V_{OUT} applications, the BOM selection must change accordingly, such as the e-capacitor voltage rating and the feedback resistors.

EVB TEST RESULTS

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

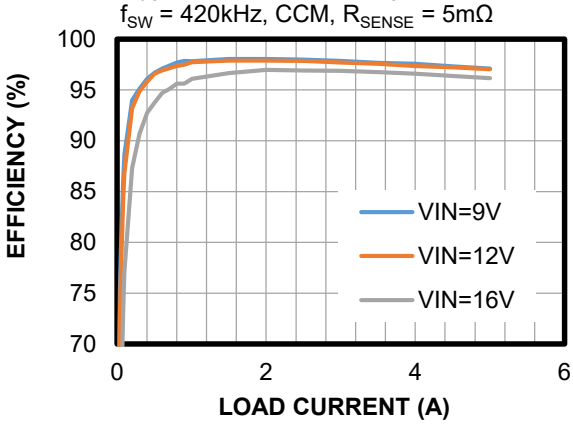
Efficiency vs. Load Current

V_{OUT} = 5V, L = 4.7µH, R_{DC} = 8mΩ, f_{SW} = 420kHz, CCM, R_{SENSE} = 5mΩ



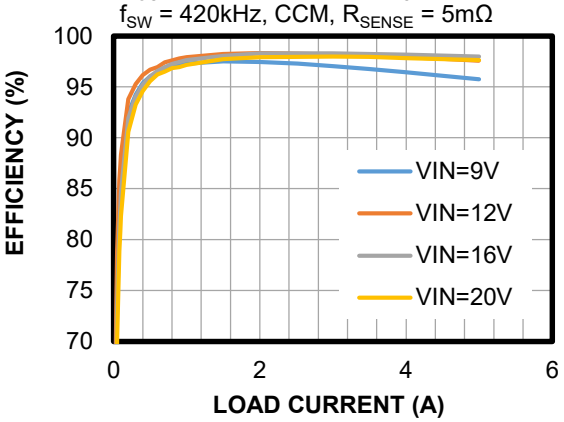
Efficiency vs. Load Current

V_{OUT} = 9V, L = 4.7µH, R_{DC} = 8mΩ, f_{SW} = 420kHz, CCM, R_{SENSE} = 5mΩ



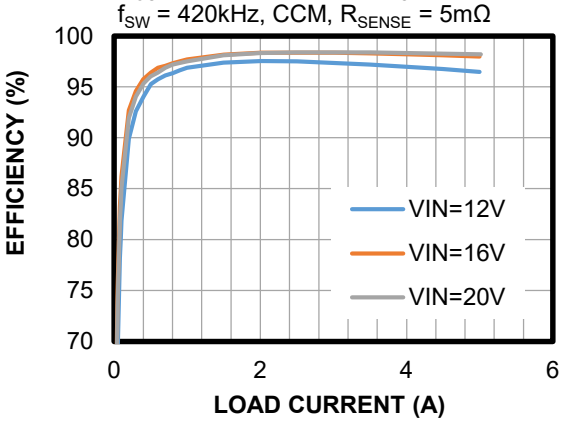
Efficiency vs. Load Current

V_{OUT} = 15V, L = 4.7µH, R_{DC} = 8mΩ, f_{SW} = 420kHz, CCM, R_{SENSE} = 5mΩ



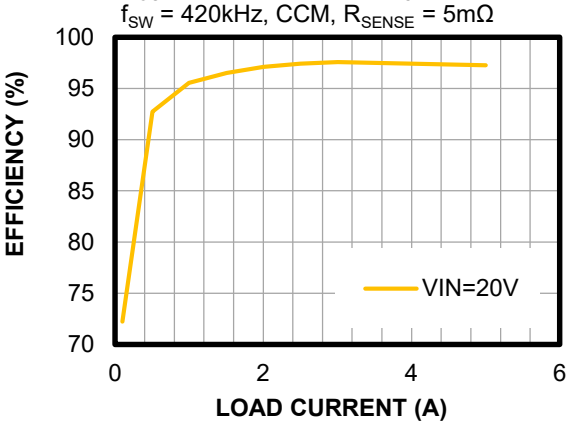
Efficiency vs. Load Current

V_{OUT} = 20V, L = 4.7µH, R_{DC} = 8mΩ, f_{SW} = 420kHz, CCM, R_{SENSE} = 5mΩ



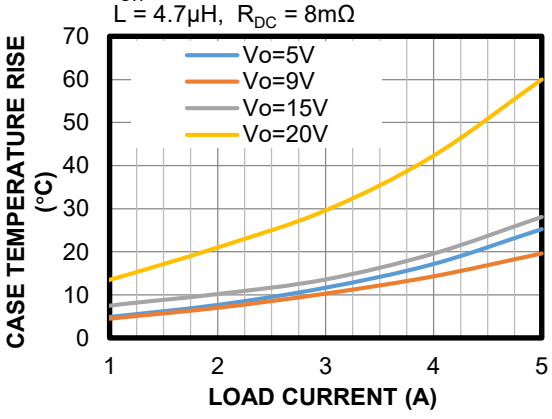
Efficiency vs. Load Current

V_{OUT} = 28V, L = 4.7µH, R_{DC} = 8mΩ, f_{SW} = 420kHz, CCM, R_{SENSE} = 5mΩ



Case Temperature Rise

V_{IN} = 12V, V_{OUT} = 5V/9V/15/20/, f_{SW} = 420kHz, based on 6cmx6cm board, L = 4.7µH, R_{DC} = 8mΩ



PCB LAYOUT

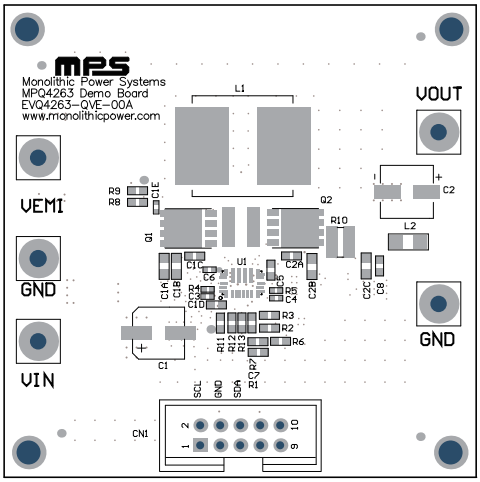


Figure 3: Top Silk

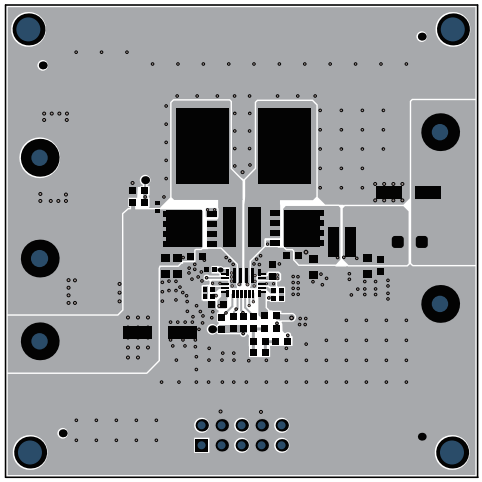


Figure 4: Top Layer

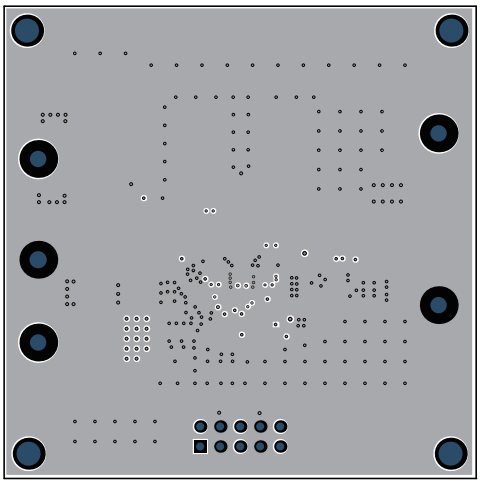


Figure 5: Mid-Layer 1

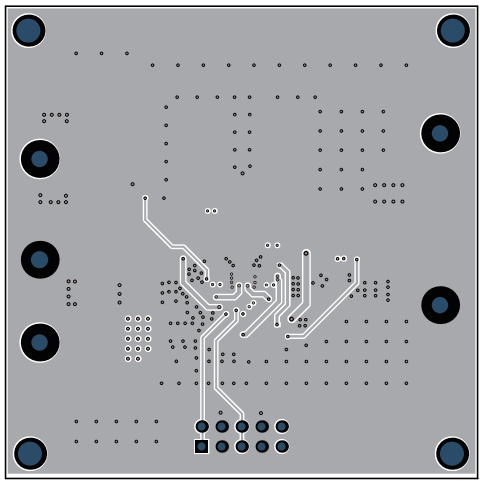


Figure 6: Mid-Layer 2

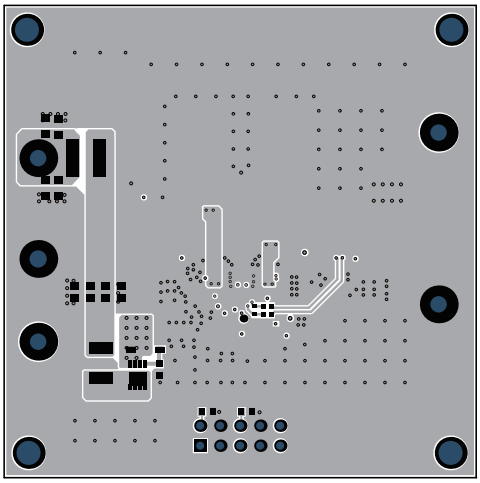


Figure 7: Bottom Layer

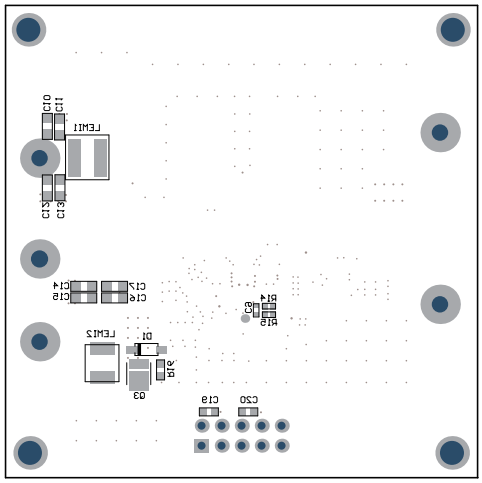


Figure 8: Bottom Silk

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	11/14/2023	Initial Release	-