EVQ18811-10X-Y-00A

Isolated, 5kV$_{RMS}$ Single-Channel Gate Driver Evaluation Board

DESCRIPTION

The EVQ18811-10X-Y-00A is a set of evaluation boards designed to demonstrate the capabilities of the MPQ18811, a single-channel, isolated gate driver solution for driving power switching devices with a short propagation delay and minimal pulse-width distortion. There are three versions: the EVQ18811-10C-Y-00A, the EVQ18811-10E-Y-00A, and the EVQ18811-10F-Y-00A. The EVQ18811-10X-Y-00A applies to all versions throughout the datasheet, unless otherwise noted.

By utilizing MPS's proprietary capacitive-based isolation technology, the SOIC wide-body (WB) package option can provide up to 5kV$_{RMS}$ of withstand voltage (per UL 1577). It can also provide a common-mode transient immunity (CMTI) rating above 150kV/μs between the input side and output driver. With these advanced features, the driver operates at a high efficiency, high power density, and with robustness in a wide variety of automotive power applications.

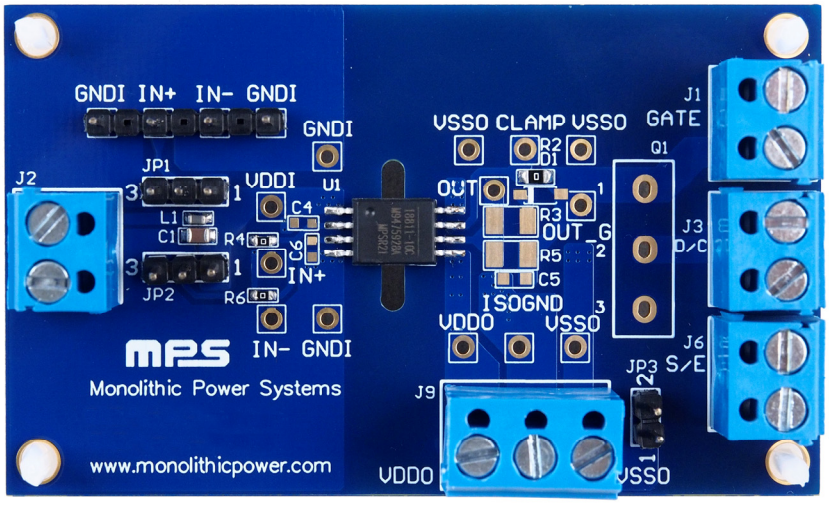
It is recommended to read the MPQ18811 datasheet prior to making any changes to the EVQ18811-10X-Y-00A.

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C, unless otherwise noted.

Parameters	Conditions	Value
VDDI primary supply voltage (V_{DDI} - V_{GNDI})		2.8V to 5.5V
VDDO secondary supply voltage (V_{DDO} - V_{SSO})	-C version, 8V under-voltage lockout (UVLO) threshold	9.2V to 30V
	-E version, 12V UVLO threshold	14.5V to 30V
	-F version, 15V UVLO threshold	17.5V to 30V
Peak driver current (I_{OUT})		6A source, 10A sink

EVALUATION BOARD



LxWxH (7.4cmx4.45cmx1.43cm)

Board Number	MPS IC Number
EVQ18811-10X-Y-00A	MPQ18811-10XGY-AEC1

EVALUATION BOARD BASIC INFORMATION

Evaluation Board Part Number (1)	Output UVLO (V)	Input Logic	Output Configuration	Miller Clamp	IC Package Type
EVQ18811-10C-Y-00A	8	IN+/IN-	OUT	Yes	SOIC-8 WB
EVQ18811-10E-Y-00A	12				
EVQ18811-10F-Y-00A	15				

Notes:

1) These evaluation boards can only be ordered as customized boards though the MPS CSR team. The availability for any required under-voltage lockout (UVLO) revisions will also be through the MPS CSR team.

QUICK START GUIDE

The EVQ18811-10X-Y-00A evaluation board is easy to set up and use to evaluate the performance of the MPQ18811. To get started, follow the steps below:

1. Select the desired jumper setting (see Table 1).

Table 1: Jumper Setting Options

Jumper #	Jumper Name	Jumper Options		Default Setting
JP1	IN+	Option A	Jumper cap not installed. The IN+ pin is controlled via an external signal, and is pulled low by default if left open.	Option A
		Option B	Jumper cap on connection points 2 and 3. Short IN+ to GNDI to set the IN+ pin logic low.	
		Option C	Jumper cap on connection points 2 and 1. Short IN+ to VDDI to set the IN+ pin logic high.	
JP2	IN-	Option A	Jumper cap not installed. The IN- pin is controlled via an external signal, and is pulled high by default if left open.	Option B
		Option B	Jumper cap on connection points 2 and 3. Short IN- to GNDI to set the IN- pin logic low.	
		Option C	Jumper cap on connection points 2 and 1. Short IN- to VDDI to set the IN- pin logic high.	

2. Prepare DC power supply A and DC power supply B, and ensure their outputs are insulated from each other.
3. Preset DC power supply A to 2.8V ≤ (V_{DDI} - V_{GNDI}) ≤ 5.5V. If the chip is controlled by external signals, ensure that V_{DDI} is not below the high level of these signals.
4. Turn off DC power supply A.
5. Preset DC power supply B to 9.2V, 14.5V, or 17.5V ≤ (V_{DDO} - V_{SSO}) ≤ 30V according to the UVLO threshold.
6. Turn off DC power supply B.
7. If needed, connect OUT to an external load.
8. Connect DC power supply A’s output to J2.
9. Connect DC power supply B’s output to J9.
10. After making the connections, turn DC power supply A and DC power supply B on.
11. If needed, enable the external control signals.

EVALUATION BOARD SCHEMATIC

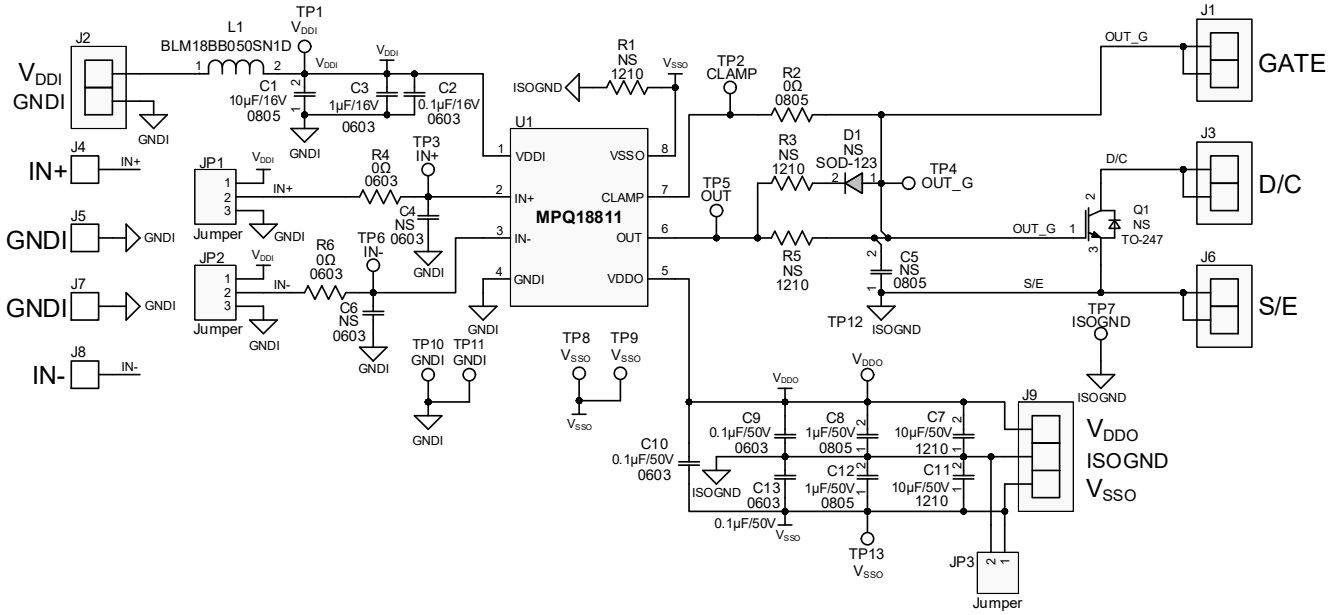


Figure 1: Evaluation Board Schematic

EVQ18811-10X-Y-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	C1	10µF	Ceramic capacitor, 16V, X7R	0805	Murata	GRM21BC71C106KE11L
1	C2	0.1µF	Ceramic capacitor, 16V, X7R	0603	Murata	GRM188R71C104KA01D
2	C7, C11	10µF	Ceramic capacitor, 50V, X7T	1210	Murata	GRM32ER71H106KA12L
2	C8, C12	1µF	Ceramic capacitor, 50V, X7R	0805	Murata	GRM21BR71H105KA12L
3	C9, C10, C13	0.1µF	Ceramic capacitor, 50V, X7R	0603	Murata	GCM188R71H104KA57D
2	C4, C6	NS		0603		
1	C5	NS		0805		
1	D1	NS		SOD-123		
4	J4, J5, J7, J8	2.54mm	Pin header	SIP	Any	
4	J1, J2, J3, J6	5.08mm	Connection terminal block, 2-position	Through-hole	Any	
1	J9	5.08mm	Connection terminal block, 3-position	Through-hole	Any	
3	JP1, JP2, JP3	2.54mm	Pin header with jumper cap	SIP	Any	
1	L1	50mΩ	Ferrite bead, 5Ω at 100MHz, 700mA	0603	Murata	BLM18BB050SN1D
1	Q1	NS		TO-247		
1	R2	0Ω	Thick film chip resistor, 5%	0805	Yageo	RC0805JR-070RL
2	R4, R6	0Ω	Thick film chip resistor, 5%	0603	Yageo	RC0603JR-070RL
3	R1, R3, R5	NS		1210		
13	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13	2.5mm	Test point	Through-hole	Any	
1	U1	MPQ18811	5kVRMS, isolated single-channel gate driver	SOIC-8 WB	MPS	MPQ18811-10XGY-AEC1

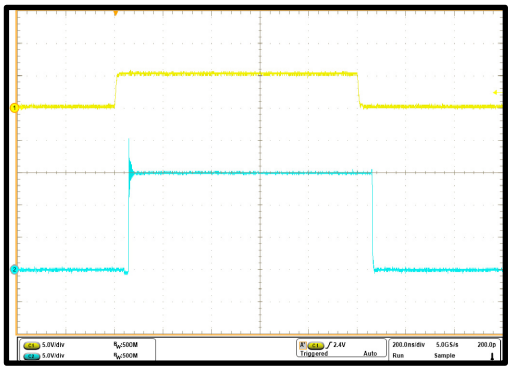
EVB TEST RESULTS

Performance waveforms are tested on the MPQ18811 evaluation board. V_{DDI} - V_{GNDI} = 5V, V_{DDO} - V_{SSO} = 15V, C_{LOAD} = 0pF, T_A = 25°C, all voltages with respect to the corresponding ground(s), unless otherwise noted.

Typical Switching Waveform

CH1: V_{IN+}

CH2: V_{OUT}



PCB LAYOUT

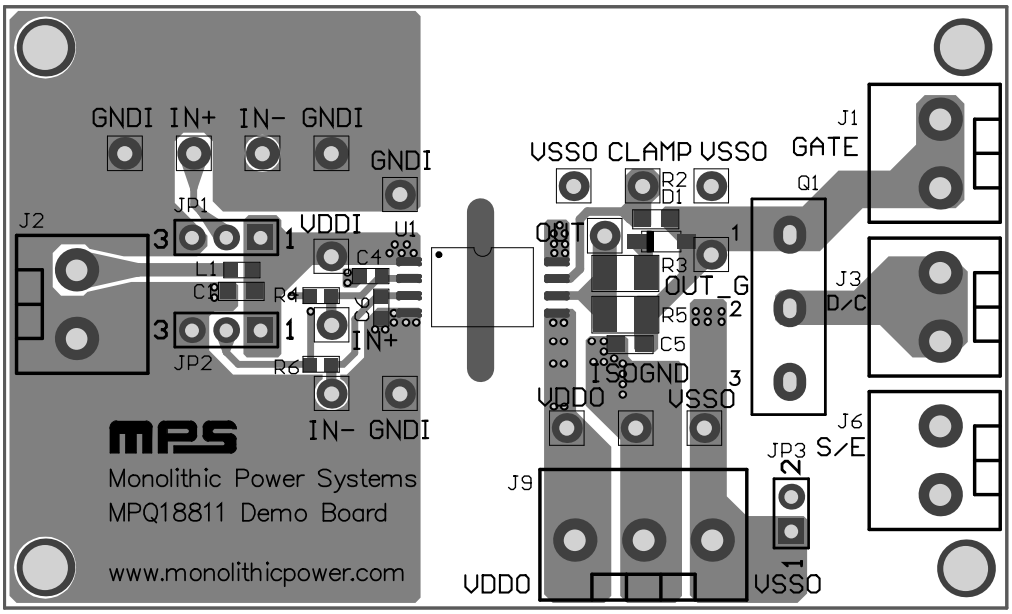


Figure 2: Top Silk and Top Layer

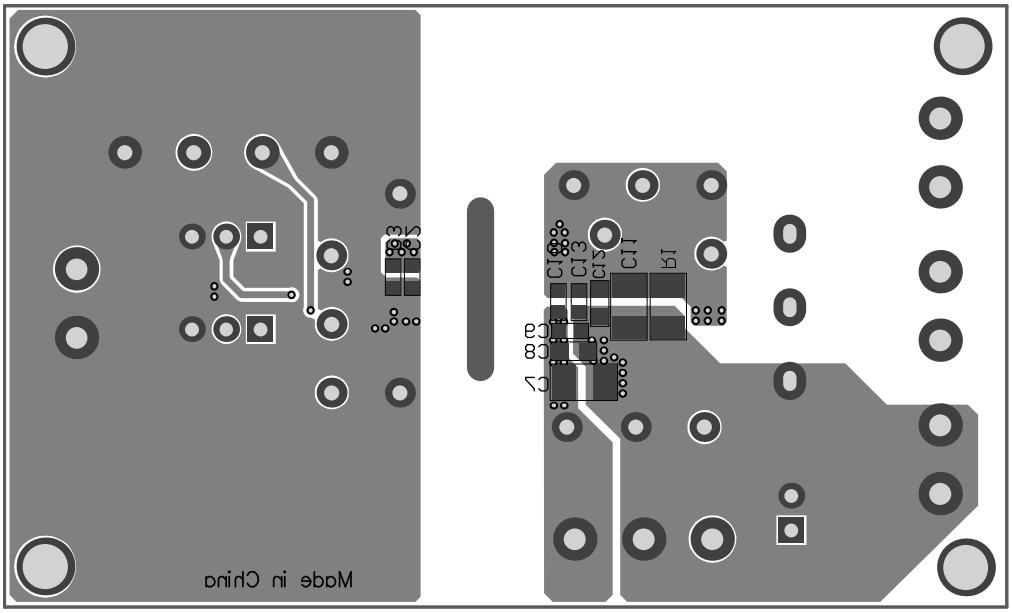


Figure 3: Bottom Layer and Bottom Silk

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	7/3/2024	Initial Release	-