



EVM3812C-PH-01A

5.5V, 1A, Ultra-Small Package

Step-Down Module with CCM Evaluation Board

DESCRIPTION

The EVM3812C-PH-01A evaluation board is designed to demonstrate the capabilities of the MPM3812C, a fully integrated, high-efficiency, synchronous, step-down power module with up to 1A of output current (I_{OUT}).

The MPM3812C adopts internally compensated constant-on-time (COT) control to provide fast

transient response and easy loop stabilization. The switching frequency (f_{SW}) is fixed at 2.4MHz. Refer to the MPM3812C datasheet for more detailed information.

It is recommended to read the datasheet for the MPM3812C prior to making any changes to the EVM3812C-PH-01A.

PERFORMANCE SUMMARY ⁽¹⁾

Specifications are at $T_A = 25^\circ\text{C}$, unless otherwise noted.

Parameters	Conditions	Value
Input voltage (V_{IN}) range		2.3V to 5.5V
Output voltage (V_{OUT})	$V_{IN} = 2.3\text{V to } 5.5\text{V}$, $I_{OUT} = 0\text{A to } 1\text{A}$	1.2V
Maximum output current (I_{OUT})	$V_{IN} = 2.3\text{V to } 5.5\text{V}$, $V_{OUT} = 1.2\text{V}$	1A
Full load efficiency	$V_{IN} = 3.3\text{V}$, $V_{OUT} = 1.2\text{V}$, $I_{OUT} = 1\text{A}$, $f_{SW} = 2.4\text{MHz}$	77.94%
Peak efficiency	$V_{IN} = 3.3\text{V}$, $V_{OUT} = 1.2\text{V}$, $I_{OUT} = 0.5\text{A}$, $f_{SW} = 2.4\text{MHz}$	83.93%
Default switching frequency (f_{SW})		2.4MHz

Note:

- 1) For different input/output voltage specifications with different output capacitors, the application circuit parameters may require changes.

EVALUATION BOARD



(LxWxH) 5cmx5cmx1.5cm

Board Number	MPS IC Number
EVM3812C-PH-01A	MPM3812CGPH

QUICK START GUIDE

The EVM3812C-PH-01A evaluation board is easy to set up to evaluate the performance of the MPM3812C. For proper measurement equipment set-up, refer to Figure 1 and follow the steps below:

1. Preset the power supply (V_{IN}) between 2.3V and 5.5V, then turn off the power supply. ⁽²⁾
2. Connect the power supply terminals to:
 - a. Positive (+): V_{IN}
 - b. Negative (-): GND
3. Set the initial load to 0A.
4. Connect the load terminals to:
 - a. Positive (+): V_O
 - b. Negative (-): GND
5. After making the connections, turn on the power supply. The board should start up automatically.
6. Check for the proper output voltage (V_{OUT}) from the V_O to GND turrets.
7. Once the proper V_{OUT} is established, adjust the load within the operating range, then measure the efficiency, output voltage ripple, and other parameters. ⁽³⁾
8. After completing all tests, adjust the load to 0A, then turn off the input power supply.

Notes:

- 2) Ensure that V_{IN} does not exceed 5.5V.
- 3) When measuring the output voltage ripple or input voltage ripple, do not use the long ground lead on the oscilloscope probe.

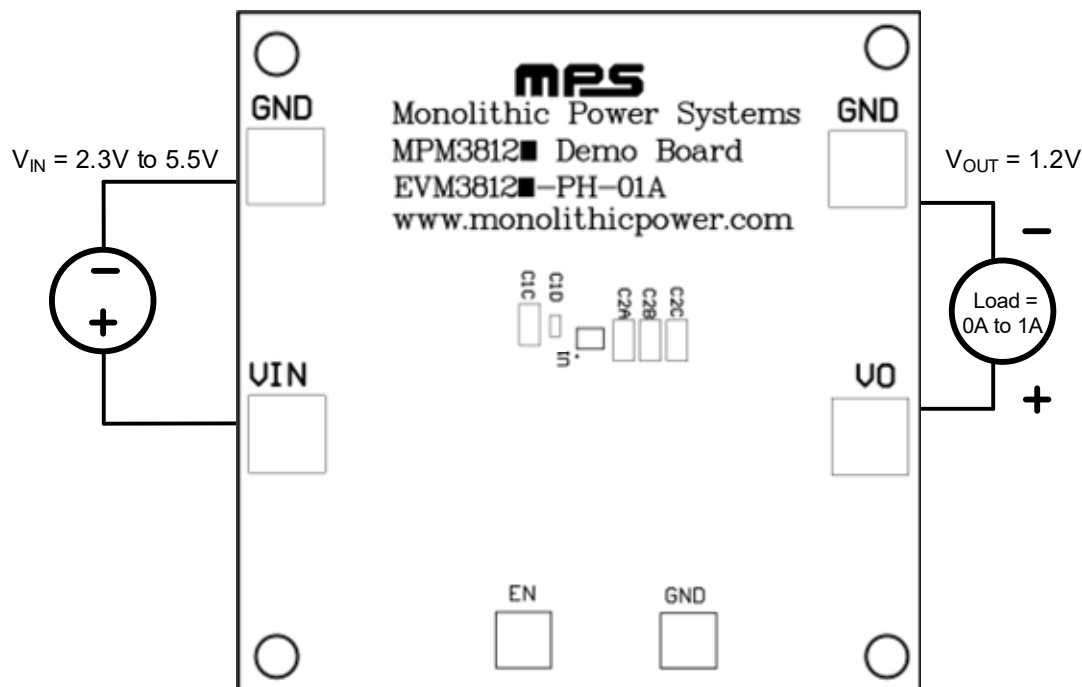


Figure 1: Measurement Equipment Set-Up

EVALUATION BOARD SCHEMATIC

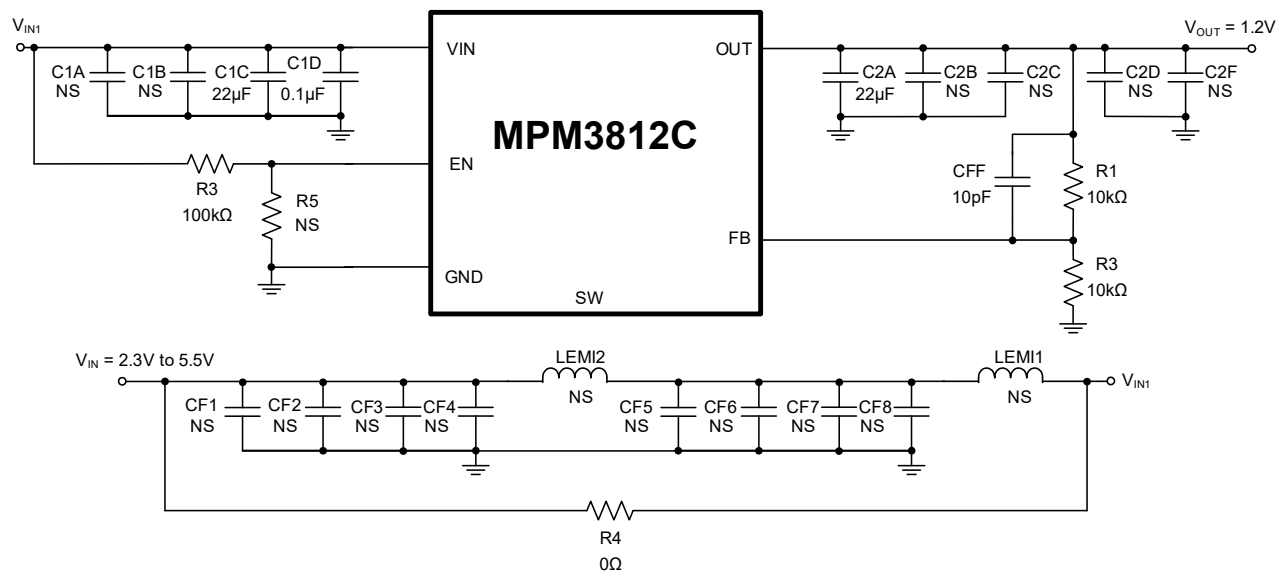


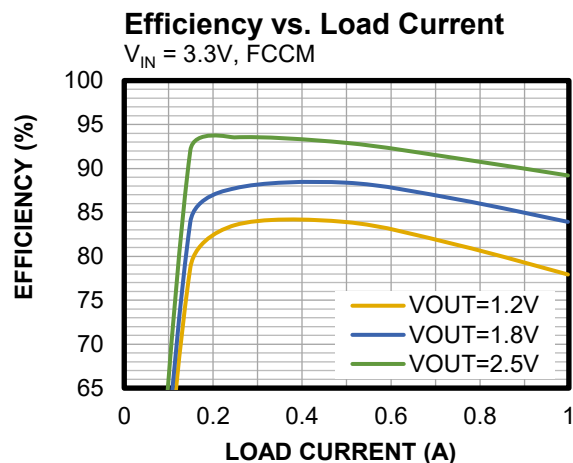
Figure 2: Evaluation Board Schematic

EVM3812C-PH-01A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	C1D	0.1μF	Ceramic capacitor, 10V, X7R	0402	Wurth	885012205018
2	C1C, C2A	22μF	Ceramic capacitor, 10V, X7R	0805	TDK	C2012X7S1A226M
1	CFF	10pF	Ceramic capacitor, 25V, NP0	0402	Wurth	885012005040
2	R1, R2	10kΩ	Film resistor, 1%	0402	Yageo	RC0402FR- 0710KL
1	R3	100kΩ	Film resistor, 1%	0402	Yageo	RC0402FR- 07100KL
1	R4	0Ω	Film resistor, 1%	2512	Yageo	RC2512FK-070RL
1	R5	NS				
0	LEMI1, LEMI2	NS				
0	C1A, C1B, C2B, C2C, C2D, C2F	NS				
0	CF1, CF2, CF3, CF4, CF5, CF6, CF7, CF8	NS				
1	U1	MPM3812C	5.5V, 1A, step-down power module	ECLGA-6 (1.5mmx 2mm)	MPS	MPM3812CGPH

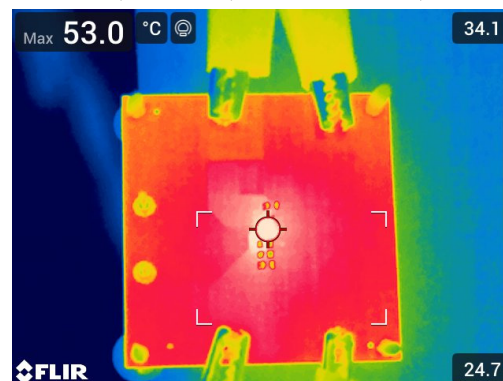
EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board. $V_{IN} = 3.3V$, $V_{OUT} = 1.2V$, $f_{SW} = 2400kHz$, $T_A = 25^{\circ}C$, unless otherwise noted.



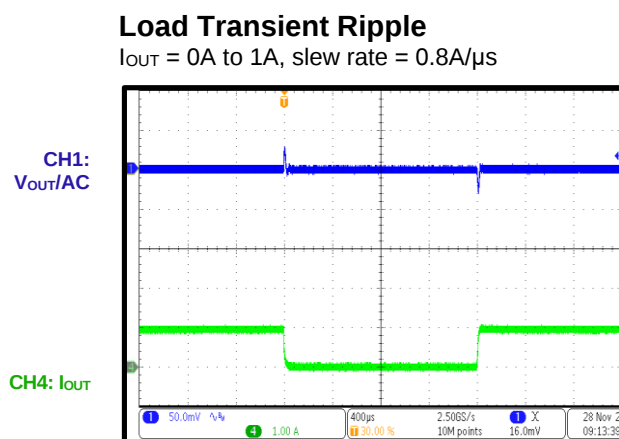
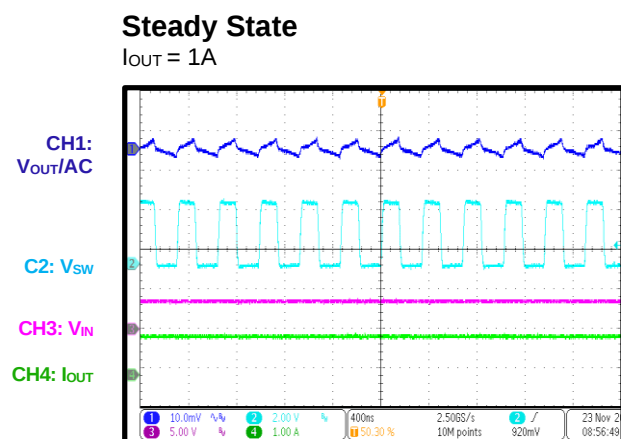
Thermal Performance

$T_A = 28^{\circ}C$, $I_{OUT} = 1A$, no forced airflow, $T_{CASE} = 53^{\circ}C$



EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. $V_{IN} = 3.3V$, $V_{OUT} = 1.2V$, $f_{SW} = 2400kHz$, $T_A = 25^{\circ}C$, unless otherwise noted.



PCB LAYOUT

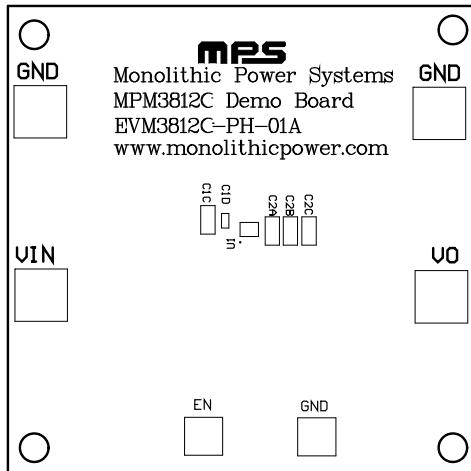


Figure 3: Top Silk

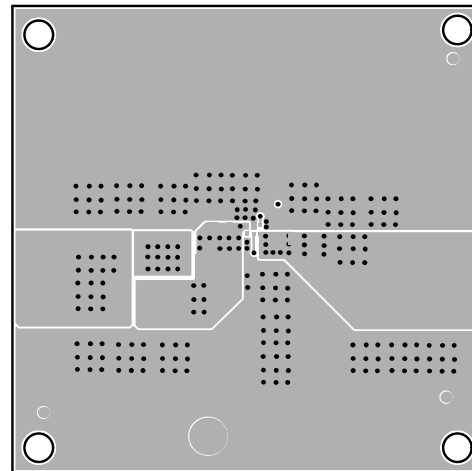


Figure 4: Top Layer

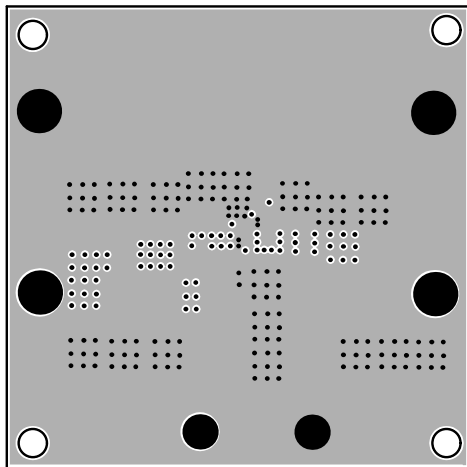


Figure 5: Mid-Layer 1

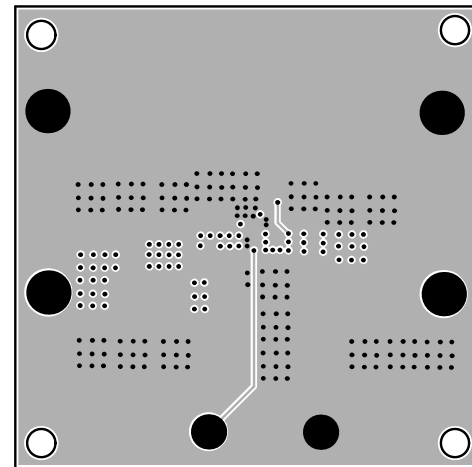


Figure 6: Mid-Layer 2

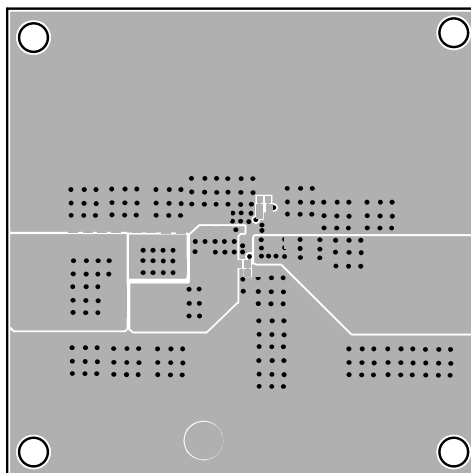


Figure 7: Bottom Layer

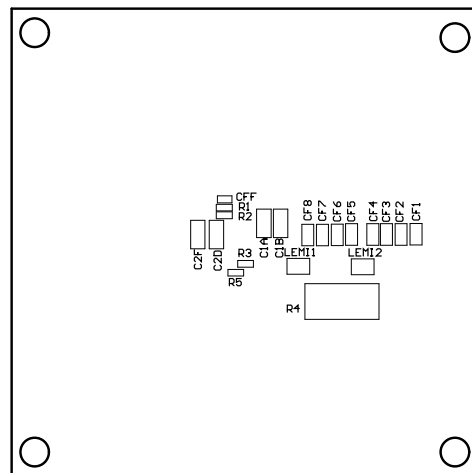


Figure 8: Bottom Silk



REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	6/18/2024	Initial Release	-

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