DESCRIPTION

The EVM3650-QW-00A evaluation board is designed to demonstrate the capabilities of MPS’s MPM3650, a fully integrated, high-frequency, synchronous, rectified, step-down power module with an internal inductor. The MPM3650 offers a very compact solution to achieve 5A of continuous output current over a wide input voltage range with excellent load and line regulation. The MPM3650 offers synchronous mode operation for higher efficiency over the output current load range.

Constant-on-time (COT) control operation provides very fast transient response and easy loop design, as well as very tight output regulation. Full protection features include SCP, OCP, UVP, and thermal shutdown.

ELECTRICAL SPECIFICATIONS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage</td>
<td>(V_{\text{IN}})</td>
<td>2.75 to 17 V</td>
<td></td>
</tr>
<tr>
<td>Output voltage</td>
<td>(V_{\text{OUT}})</td>
<td>1 V</td>
<td></td>
</tr>
<tr>
<td>Output current</td>
<td>(I_{\text{OUT}})</td>
<td>5 A</td>
<td></td>
</tr>
</tbody>
</table>

FEATURES

- Wide 2.75V to 17V Operating Input Range
- 5A Output Current
- High Efficiency with DCM at Light Load
- Output Adjustable from 0.6V
- High-Efficiency Synchronous Mode Operation
- Supports Pre-Biased Start-Up
- Fixed 1200kHz Switching Frequency
- Externally Programmable Soft-Start Time
- EN and Power Good for Power Sequencing
- Over-Current Protection and Hiccup Mode
- Thermal Shutdown
- Available in a QFN-24 (4mmx6mmx1.6mm) Package

APPLICATIONS

- FPGA Power Systems
- Optical Modules
- Telecom
- Networking
- Industries Equipment

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QUICK START GUIDE

1. Preset the power supply to 2.75V ≤ V_{\text{IN}} ≤ 17V.
2. Turn the power supply off.
3. Connect the power supply terminals to:
   a. Positive (+): VIN
   b. Negative (−): GND
4. Connect load (≤5A) to:
   a. Positive (+): VOUT
   b. Negative (−): GND
5. Turn the power supply on after connecting the terminals. The board should start up automatically.

EVALUATION BOARD SCHEMATIC
## EVM3860-QW-00A BILL OF MATERIALS

<table>
<thead>
<tr>
<th>Qty</th>
<th>Ref</th>
<th>Value</th>
<th>Description</th>
<th>Package</th>
<th>Manufacturer</th>
<th>Manufacturer PN</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>C1, C2, C4, C5, C20, C7</td>
<td>22µF</td>
<td>Ceramic capacitor, 25V, X5R</td>
<td>0805</td>
<td>Murata</td>
<td>GRM21BR61E226ME44L</td>
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<tr>
<td>4</td>
<td>C3, C8, C11, C19, C19</td>
<td>0.1µF</td>
<td>Ceramic capacitor, 25V, X5R</td>
<td>0402</td>
<td>Wurth</td>
<td>885012105018</td>
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<tr>
<td>1</td>
<td>C10</td>
<td>1µF</td>
<td>Ceramic capacitor, 25V, X5R</td>
<td>0402</td>
<td>Murata</td>
<td>GRM155R61E105KA12D</td>
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<tr>
<td>1</td>
<td>C9</td>
<td>39pF</td>
<td>Ceramic capacitor, 50V, X5R</td>
<td>0402</td>
<td>Murata</td>
<td>GRM1555C1H390JA01D</td>
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<tr>
<td>1</td>
<td>R1</td>
<td>499kΩ</td>
<td>Film resistor, 1%, 0402, 499kΩ</td>
<td>0402</td>
<td>Yageo</td>
<td>RC0402FR-07499KL</td>
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<tr>
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<td>R4</td>
<td>100kΩ</td>
<td>Film resistor, 1%, 0402, 100kΩ</td>
<td>0402</td>
<td>Yageo</td>
<td>RC0402FR-07100KL</td>
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<tr>
<td>2</td>
<td>R7, R6</td>
<td>0Ω</td>
<td>Film resistor, 1%, 0402, 0R</td>
<td>0402</td>
<td>Yageo</td>
<td>RC0402FR-070RL</td>
</tr>
<tr>
<td>1</td>
<td>R3</td>
<td>20kΩ</td>
<td>Film resistor, 1%, 0402, 20kΩ</td>
<td>0402</td>
<td>Yageo</td>
<td>RC0402FR-0720KL</td>
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<tr>
<td>1</td>
<td>R5</td>
<td>30kΩ</td>
<td>Film resistor, 1%, 0402, 30kΩ</td>
<td>0402</td>
<td>Yageo</td>
<td>RC0402FR-0730KL</td>
</tr>
<tr>
<td>1</td>
<td>EN</td>
<td>3 pins</td>
<td>3-pin, single-row, straight socket header</td>
<td>DIP</td>
<td>Wurth</td>
<td>61300311821</td>
</tr>
<tr>
<td>1</td>
<td>V&lt;sub&gt;O&lt;/sub&gt; Ripple</td>
<td>N/A</td>
<td>SMA mount straight jack, VOUT/AC test component</td>
<td>DIP</td>
<td>Wurth</td>
<td>60312002114503</td>
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<tr>
<td>5</td>
<td>VIN, VEMI, GND x 2, VOUT</td>
<td>φ2.0</td>
<td>φ2.0 copper pin</td>
<td>DIP</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>4</td>
<td>EN, GND, VCC, PG</td>
<td>φ1.0</td>
<td>φ1.0 copper pin</td>
<td>DIP</td>
<td>N/A</td>
<td>N/A</td>
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<tr>
<td>1</td>
<td>U1</td>
<td>N/A</td>
<td>Power module</td>
<td>QFN-24  (4mmx6mm)</td>
<td>MPS</td>
<td>MPM3650</td>
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</tbody>
</table>
EVB TEST RESULTS
Performance curves and waveforms are tested on the evaluation board, \( V_{IN} = 5V \), \( V_{OUT} = 1V \), \( T_A = 25°C \), unless otherwise noted.
EVB TEST RESULTS (continued)
Performance curves and waveforms are tested on the evaluation board, $V_{IN} = 5\, \text{V}$, $V_{OUT} = 1\, \text{V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

**V_{OUT} Ripple**
- $I_{OUT} = 0\, \text{A}$
  - CH1: $V_{OUT}/\text{AC}$
    - 20mV/div.
  - 20ms/div.
- $I_{OUT} = 5\, \text{A}$
  - CH1: $V_{OUT}/\text{AC}$
    - 5mV/div.
  - 400ns/div.

**Load Transient**
- $I_{OUT} = 0\, \text{A}$ to 2.5A
  - CH1: $V_{IN}$
    - 50mV/div.
  - CH4: $I_{OUT}$
    - 0A to 2.5A/div.
  - 100μs/div.
- $I_{OUT} = 2.5\, \text{A}$ to 5A
  - CH1: $V_{OUT}/\text{AC}$
    - 20mV/div.
  - CH4: $I_{OUT}$
    - 5A/div.
  - 100μs/div.

**VIN On**
- $I_{OUT} = 0\, \text{A}$
  - CH1: $V_{OUT}$
    - 1V/div.
  - CH2: $V_{SW}$
    - 5V/div.
  - CH3: $V_{IN}$
    - 5V/div.
  - CH4: $I_{OUT}$
    - 5A/div.
  - 10ms/div.
- $I_{OUT} = 5\, \text{A}$
  - CH1: $V_{OUT}$
    - 1V/div.
  - CH2: $V_{SW}$
    - 5V/div.
  - CH3: $V_{IN}$
    - 5V/div.
  - CH4: $I_{OUT}$
    - 5A/div.
  - 10ms/div.
EVM TEST RESULTS (continued)

Performance curves and waveforms are tested on the evaluation board, $V_{IN} = 5V$, $V_{OUT} = 1V$, $T_A = 25^\circ C$, unless otherwise noted.

**VIN Off**

$I_{OUT} = 0A$

**VIN Off**

$I_{OUT} = 5A$

**EN On**

$I_{OUT} = 0A$

**EN On**

$I_{OUT} = 5A$

**EN Off**

$I_{OUT} = 0A$

**EN Off**

$I_{OUT} = 5A$
EVB TEST RESULTS (continued)

Performance curves and waveforms are tested on the evaluation board, $V_{IN} = 5\text{V}$, $V_{OUT} = 1\text{V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

**SCP Steady State**

- **CH1**: $V_{OUT}$ 1V/div.
- **CH2**: $V_{SW}$ 5V/div.
- **CH3**: $V_{IN}$ 5V/div.
- **CH4**: $I_{OUT}$ 10A/div.

20ms/div.

**SCP Entry and Recovery**

- **CH1**: $V_{OUT}$ 1V/div.
- **CH4**: $I_{OUT}$ 2A/div.

200ms/div.

**PCB LAYOUT**

- **Figure 1**: Top Silk Layer
- **Figure 2**: Top Layer
- **Figure 3**: Mid-Layer 1
- **Figure 4**: Mid-Layer 2
Figure 5: Bottom Layer

Figure 6: Bottom Silk Layer
Revision History

<table>
<thead>
<tr>
<th>Revision #</th>
<th>Revision Date</th>
<th>Description</th>
<th>Pages Updated</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>7/8/2020</td>
<td>Initial Release</td>
<td>-</td>
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