EVL5516-R-00A

16V, 6A, Power-Outage Power Management IC for SSD Applications Evaluation Board

DESCRIPTION

The EVL5516-R-00A is an evaluation board designed to demonstrate the capabilities of the MP5516, a monolithic power management IC (PMIC) that is ideal for power management and conditioning in enterprise solid-state drive (SSD) applications.

The MP5516 consists of an input current limit switch (e-fuse) and a bidirectional buck-boost converter. The e-fuse features low on resistance, current limiting, and reverse-current blocking. The buck-boost converter manages energy storage and energy release.

The e-fuse's configurable current limit prevents inrush current during start-up. Reverse-current blocking prevents backup energy from flowing to the failing input voltage (V_{IN}) port, which allows the backup energy to be utilized during a power outage. Backup energy is stored in the storage capacitors. The configurable charge current controls the rate at which the storage voltage ($V_{STORAGE}$) ramps up. Constant-on-time control (COT) minimizes the voltage dip during the transition from boost charge mode to buck release mode.

The IC also provides a digital I^2C interface and internal analog-to-digital converter (ADC). The I^2C can set the input current limit and perform capacitor health tests. The ADC monitors V_{IN}, the input current (I_{IN}), and the input power (P_{IN}).

The MP5516 requires a minimal number of readily available, standard external components, and is available in a QFN-25 (4mmx4mm) package.

ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Value	Units
Input voltage	V_{IN}	12	V
Storage voltage	$V_{STORAGE}$	28	V
Input power fail threshold	V_{DET}	8.4	V
Backup bus voltage	$V_{BUS_RELEASE}$	8.6	V
Backup bus voltage maximum load	$I_{RELEASE}$	5	A

FEATURES

- **Input Current Limit Switch (E-Fuse):**
  - Wide 2.65V to 16V Input Voltage Range
  - 20mΩ Low $R_{DS(ON)}$ E-Fuse
  - 1.2A to 6A Configurable Input Current Limit
  - 3.3V, 5.0V, and 12V Selectable OVP
  - Reverse-Current Blocking to Prevent Current Leakage
  - Configurable Soft Start (SS)
  - Configurable Start-Up Delay Time (t_{DELAY})
- **36V Charge and Backup Converter:**
  - Up to 36V Configurable Storage Voltage
  - 60mΩ/37mΩ $R_{DS(ON)}$ HS-FET and LS-FET
  - Configurable Boost Inductor Peak Charge Current
  - Auto-Alternating Boost Charge Mode and Buck Release Mode
  - Constant-On-Time (COT) Control for Steady-State Operation in Buck Release Mode with a Configurable Switching Frequency (f_{SW})
  - Short Circuit Protection (SCP)
  - ESR and Storage Capacitance Detection
- **System:**
  - Multiple-Time Programmable (MTP) Memory (Configurable Up to 1000 Times)
  - Digital I^2C for Status Monitoring, Parameter Control, and Operation Control
  - Enable (EN) Control
  - Available in a QFN-25 (4mmx4mm) Package

MPL Optimized Performance with MPS Inductor MPL-AL6050 Series

APPLICATIONS

- Enterprise Solid-State Drives (SSDs)
- Power Backup Solutions

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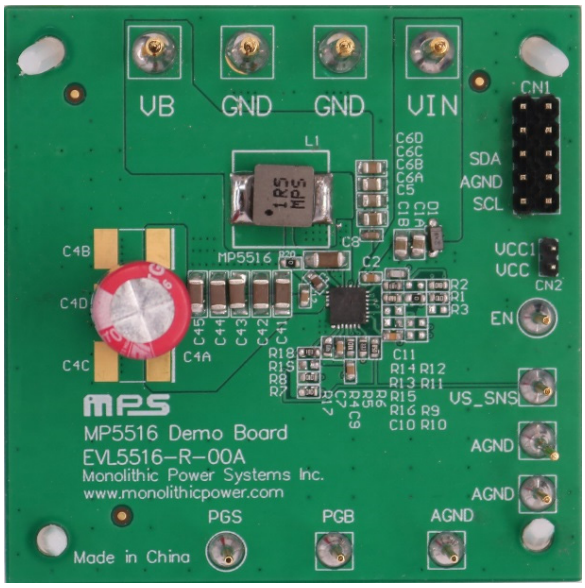
EVL5516-R-00A EVALUATION BOARD

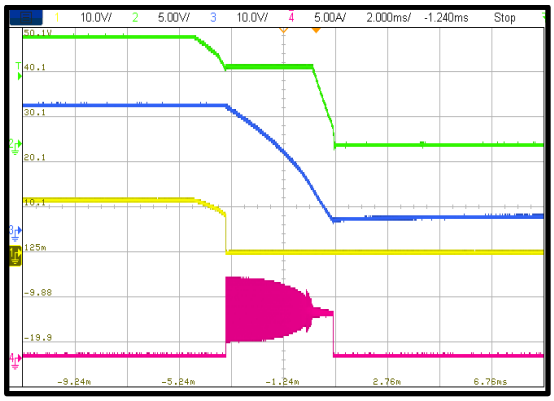


LxW (6.3cmx6.3cm)

Board Number	MPS IC Number	MPS Inductor
EVL5516-R-00A	MP5516GR	MPL-AL6050-1R5

Storage Voltage Release

V_{IN} = 12V, V_{DET} = 8.4V, $V_{BUS_RELEASE}$ = 8.6V, $V_{STORAGE}$ = 28V, L = 1.5µH, f_{SW} = 600kHz, V_{BUS} load = 5A



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QUICK START GUIDE

The board layout accommodates most commonly used components.

1. Connect the load terminals to:
   a. Positive (+): VB
   b. Negative (-): GND
2. Preset the power supply output to 12V, then turn off the power supply.
3. Connect the power supply output terminals to:
   a. Positive (+): VIN
   b. Negative (-): GND
4. Turn on the power supply after making the connections. The MP5516 should charge the storage capacitor ($C_{STORAGE}$) to 28V.
5. Turn off the power supply to observe the power release performance.
6. To use the enable function, apply a digital input to the EN pin. When EN is high, the MP5516 is enabled. When EN goes from high to low, the MP5516 is forced into buck mode until $V_{STORAGE}$ is discharged.
7. Use R15 and R16 to set the I^2C slave address. The ADDR pin can be set to high, low, or floating to change the I^2C address (see Table 1).

Table 1: Selecting the I^2C Address

ADDR Pin	High	Low	Floating
I^2C Address	59h	5Ah	5Bh

8. Use R17 and R19 to set the power failure indication voltage (V_{PFI}), calculated with Equation (1):

$$V_{PFI} = (1 + \frac{R_{19}}{R_{17}}) \times V_{DET_REF} \quad (1)$$

   Where V_{DET_REF} is typically 0.6V.

9. If a power failure occurs, the bus voltage VB regulation ($V_{BUS_RELEASE}$) can be set via R13 and R14, estimated with Equation (2):

$$V_{BUS_RELEASE} = (1 + \frac{R_{14}}{R_{13}}) \times V_{FBB_REF} \quad (2)$$

   Where V_{FBB_REF} is typically 0.6V.

10. Similarly, R5 and R6 can set the storage voltage ($V_{STORAGE}$), calculated with Equation (3):

$$V_{STORAGE} = (1 + \frac{R_6}{R_5}) \times V_{FBS_REF} \quad (3)$$

    Where V_{FBS_REF} is typically 1.2V.

11. If the user must modify the MP5516 register settings, connect the MP5516 to the EVKT-USBI2C-02 kit, and use the MP5516 GUI to read and write the I^2C registers.

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EVALUATION BOARD SCHEMATIC

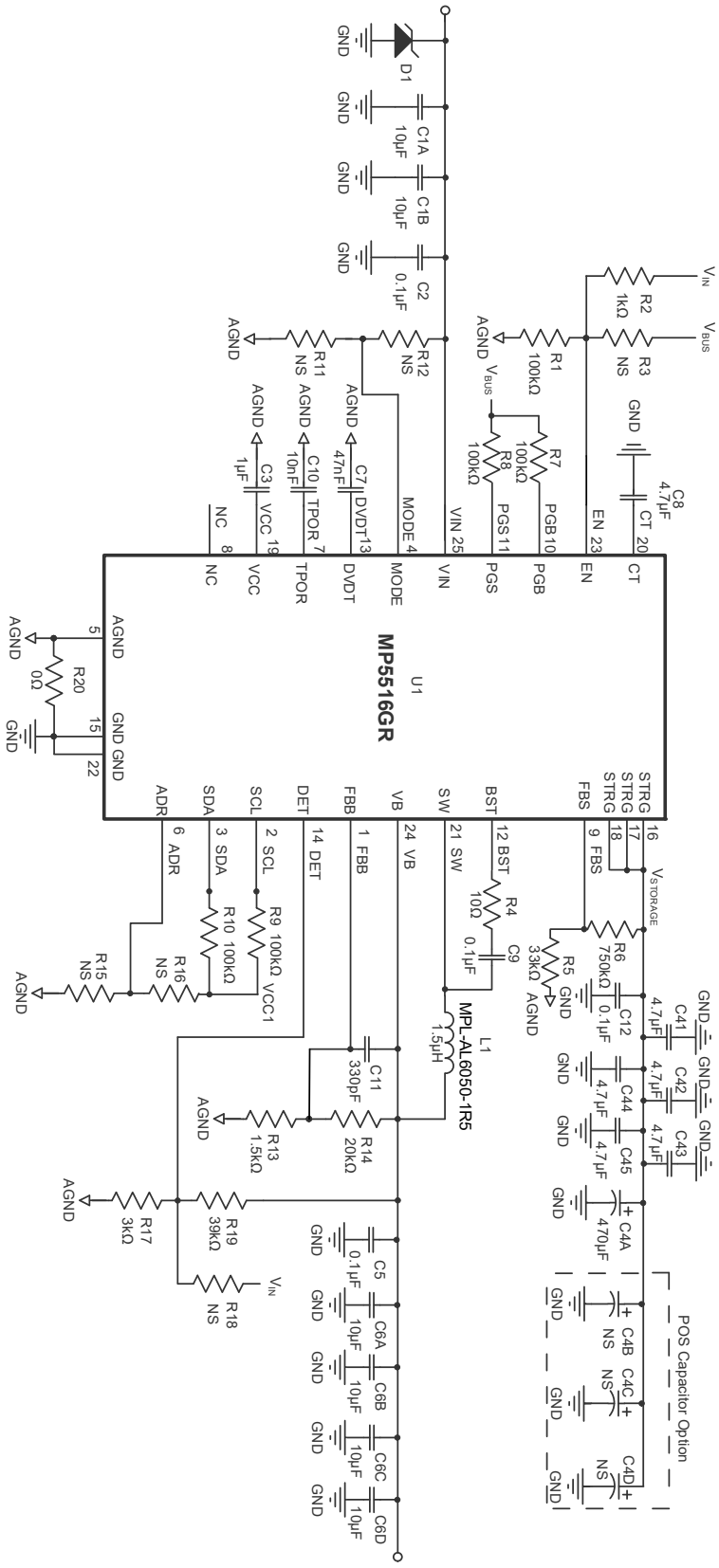

Figure 1: Evaluation Board Schematic

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EVL5516-R-00A BILL OF MATERIALS (1)

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	L1	1.5μH	Inductor, RDC = 6mΩ, I_{SAT} = 18A	6050	MPS	MPL-AL6050-1R5
1	C10	10nF	Ceramic capacitor, 16V, X7R	0603	Wurth	885012206040
1	C11	330pF	Ceramic capacitor, 50V, X7R	0603	Wurth	885012206080
2	C1A, C1B	10μF	Ceramic capacitor, 25V, X5R	0805	TDK	C2012X5R1E106K
4	C2, C5, C9, C12	100nF	Ceramic capacitor, 50V, X7R	0603	Wurth	885012206095
1	C3	1μF	Ceramic capacitor, 16V, X7R	0603	Wurth	885012206052
6	C8, C41, C42, C43, C44, C45	4.7μF	Ceramic capacitor, 50V, X7R	1206	Wurth	885012208094
1	C4A	470μF	Capacitor, 50V	DIP	Wurth	860020675022
4	C6A, C6B, C6C, C6D	10μF	Ceramic capacitor, 50V, X5R	0805	Murata	GRM21BR61H106KE43L
1	C7	47nF	Ceramic capacitor, 25V, X7R	0603	Wurth	885012206069
3	R1, R7, R8	100kΩ	Film resolution, 1%,	0603	Yageo	RC0603FR-07100KL
1	R13	1.5kΩ	Film Res,1%, 0603,1K5	0603	Yageo	RC0603FR-071K5L
1	R14	20kΩ	Film resolution, 1%,	0603	Yageo	RC0603FR-0720KL
1	R17	3kΩ	Film resolution, 1%,	0603	Yageo	RC0603FR-073KL
1	R19	39kΩ	Film resolution, 1%,	0603	Yageo	RC0603FR-0739KL
1	R2	1kΩ	Film resolution, 1%,	0603	Yageo	RC0603FR-071KL
1	R20	0Ω	Film resolution, 1%,	0603	Yageo	RL0603FR-070R016L
1	R4	10Ω	Film resolution, 1%,	0603	Yageo	RC0603FR-0710RL
1	R5	33kΩ	Film resolution, 1%,	0603	Yageo	RC0603FR-0733KL
1	R6	732kΩ	Film resolution, 1%,	0603	Yageo	RC0603FR-07732KL
7	EN, AGND, PGB, PGS, VS_SNS	φ1	1 copper pin	DIP	Custom	
4	VB, VBGND, VIN, VINGND	φ2	2 copper pins	DIP	Custom	
1	CN1	10 pins	10-pin, 2-row, straight header	DIP	Wurth	61301021121
1	CN2	2 pins	2-pin, 2-row, straight header	DIP	Wurth	61300211121
1	D1	21.5V	TVS diode, 21.5V, 9.3A, 200W	SOD123	MCC	SMF13A-TP
1	D1	21.5V	TVS diode, 21.5V, 9.3A, 200W	SOD123	MCC	SMF13A-TP
1	U1	MP5516	Power loss protection PMIC	QFN-25 (4mmx 4mm)	MPS	MP5516GR
8	R3, R9, R10, R11, R12, R15, R16, R18	NS				
3	C4B, C4C, C4D	NS				

Note:

1) Only applicable to the evaluation board with a 12V input voltage.

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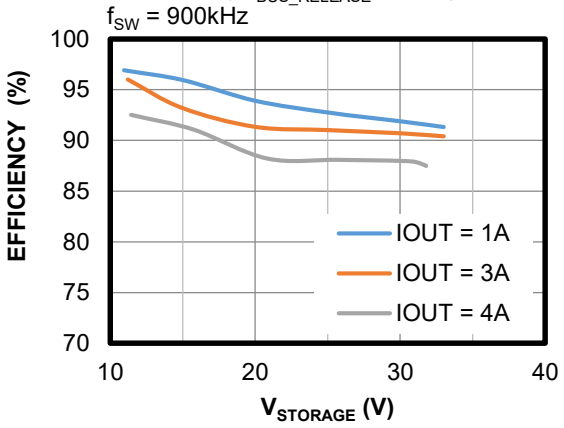
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board. V_{IN} = 12V, $V_{STORAGE}$ = 28V, V_{DET} = 8.4V, $V_{BUS_RELEASE}$ = 8.6V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

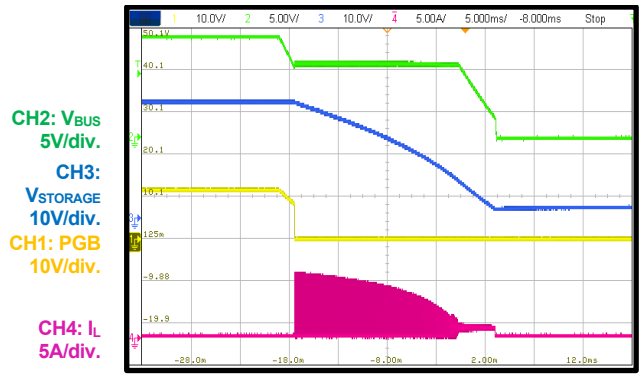
Efficiency vs. $V_{STORAGE}$

Buck mode, $V_{BUS_RELEASE}$ = 8.6V, f_{SW} = 900kHz



$V_{STORAGE}$ Release

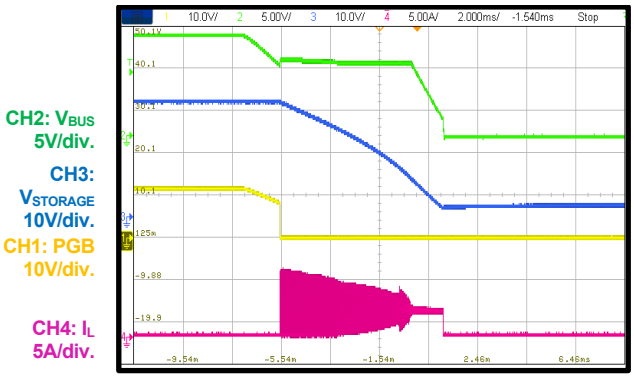
V_{BUS} load = 1A



5ms/div.

$V_{STORAGE}$ Release

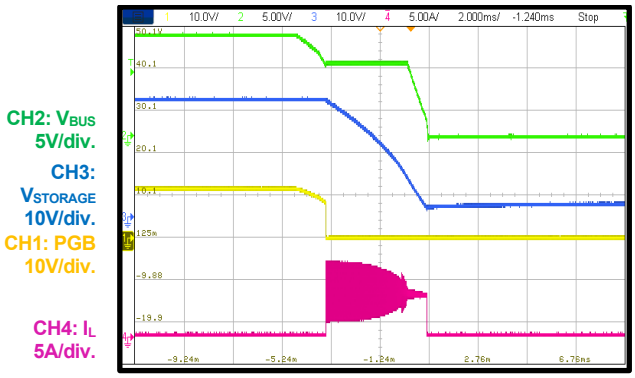
V_{BUS} load = 3A



2ms/div.

$V_{STORAGE}$ Release

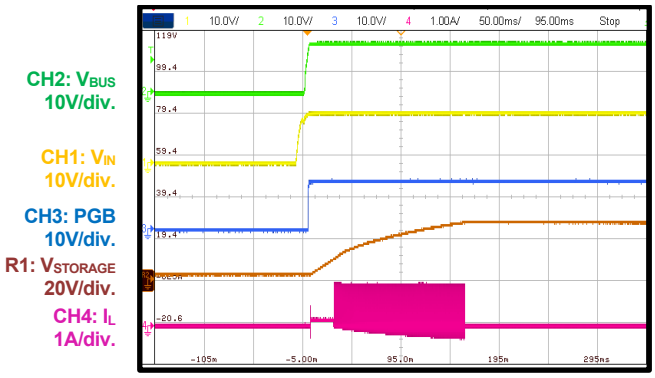
V_{BUS} load = 5A



2ms/div.

Start-Up through VIN

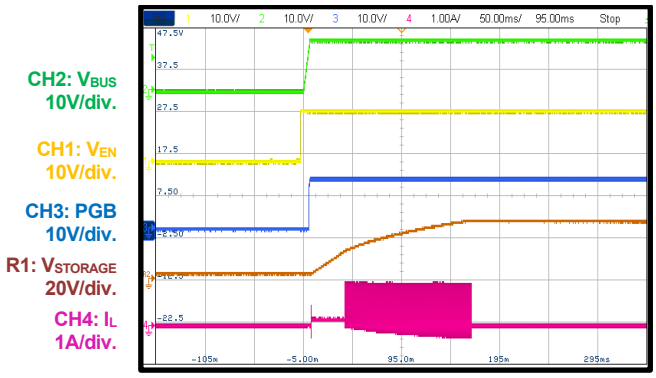
V_{BUS} load = 5A



50ms/div.

Start-Up through EN

V_{BUS} load = 5A



50ms/div.

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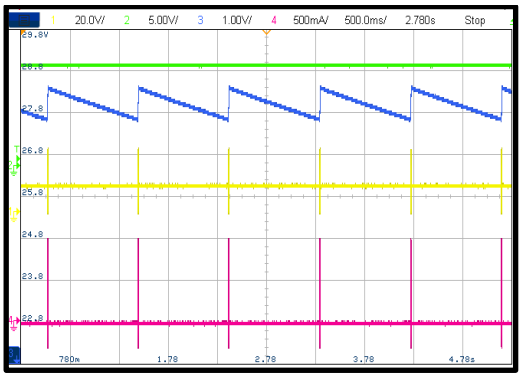
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V_{IN} = 12V, $V_{STORAGE}$ = 28V, V_{DET} = 8.4V, $V_{BUS_RELEASE}$ = 8.6V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

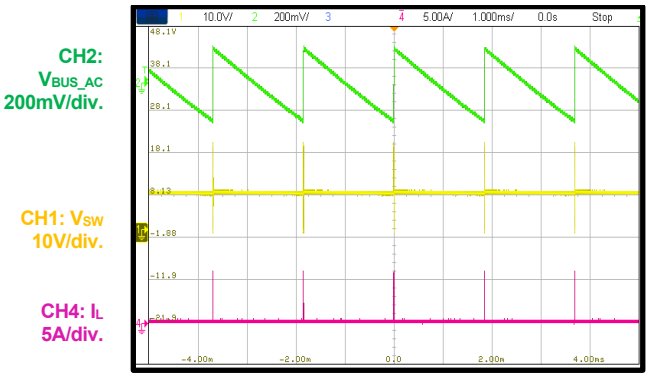
Boost Steady State

I_{CHARGE} = 001



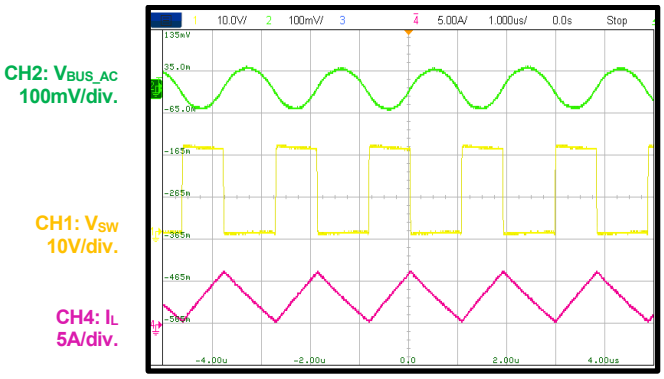
Buck Steady State

$V_{STORAGE}$ = 20V, V_{BUS} load = 0A, f_{SW} = 600kHz, 50µF ceramic capacitor on VB



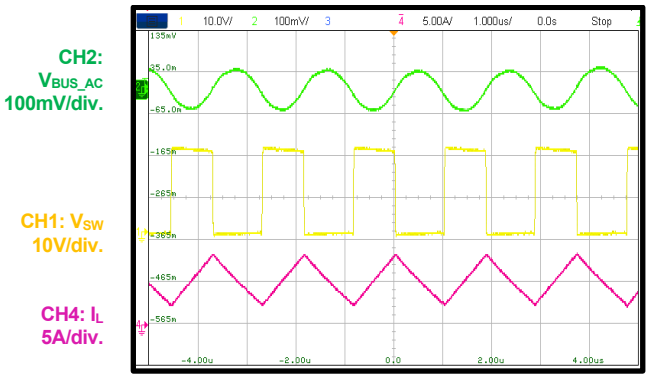
Buck Steady State

$V_{STORAGE}$ = 20V, V_{BUS} load = 3A, f_{SW} = 600kHz, 50µF ceramic capacitor on VB



Buck Steady State

$V_{STORAGE}$ = 20V, V_{BUS} load = 5A, f_{SW} = 600kHz, 50µF ceramic capacitor on VB



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FUNCTIONAL MTP TRIM BITS DESCRIPTION AND DEFAULT VALUES (MTP VERSION: MP5516GR-0000)

Bit #	Name	Description	Default
3	ILIM_EFUSE	E-fuse current limit. 000: 1.2A 001: 2A 010: 2.5A 011: 3A 100: 3.5A 101: 4A 110: 4.5A 111: 6A (default)	111
1	EN	Enables the e-fuse. 0: Disabled 1: Enabled (default)	1
2	IDIS_CAP_TEST	Discharge current during capacitor health detection. 00: 2mA 01: 5mA 10: 10mA 11: 20mA (default)	11
3	ICHRG	Peak inductor current during boost charge mode. Test condition: V_{IN} = 5V, L = 2.2µH. 000 = 0.60A 001 = 0.85A (default) 010 = 1.10A 011 = 1.35A 100 = 1.60A 101 = 1.85A 110 = 2.10A 111 = 2.35A	001
1	ENCH	Enables boost charge mode. 0: Disabled 1: Enabled (default)	1
8	VSTRG1	Capacitor test starting voltage. If the capacitor test is enabled, then the 500Hz timer starts counting once the storage voltage ($V_{STORAGE}$) drops to the VSTRG1 value. 00001010: 1.5V (minimum) 01000110: 10.5V (default) 11110000: 36V (maximum) … 0.15V/step	01000110
8	VSTRG2	Capacitor test completion voltage. If the capacitor test is enabled, then the 500Hz timer stops counting once $V_{STORAGE}$ drops to the VSTRG2 value. The recorded VSTRG2 register value may vary once the counter stops counting. 00001010: 1.5V (minimum) 00101111: 7.05V (default) 11110000: 36V (maximum) … 0.15V/step	00101111

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FUNCTIONAL MTP TRIM BITS DESCRIPTION AND DEFAULT VALUES (MTP VERSION: MP5516GR-0000) *(continued)*

Bit #	Name	Description	Default
1	PGS_MODE	Storage voltage power good indication. 0: PGS goes low once V_{FBS} drops below 1.08V (default) 1: PGS goes low once V_{FBS} drops below 1.08V or the storage capacitor ($C_{STORAGE}$) is detected	0
1	CAP_EN	Enables capacitor health detection. 0: Disabled (default) 1: Enabled	0
2	FSW	PLP converter switching frequency (f_{SW}). 00: 300kHz 01: 600kHz (default) 10: 900kHz 11: 1.2MHz	01
1	ADC_EN	Enables the ADC input voltage and input current. 0: Disabled 1: Enabled (default)	1
1	CLBK_EN	Enables buck release mode once the e-fuse's current limit is triggered. A password is required to activate this function. To activate this function, write the following one after another to register 0xF0: 0x56, 0xE3, 0x5A, and 0xAC. Then read register 0xF0. If register 0xF0 is 0x13, then CLBK_EN can be enabled or disabled. 0: If the input current limit is triggered and V_{FBB} drops to V_{FBB_REF}, then buck release mode remains disabled (default) 1: If the input current limit is triggered and V_{FBB} drops to V_{FBB_REF}, then buck release mode is enabled	0
4	CAP_OPEN_TH	The bits determines a time interval. If the storage voltage discharge time is shorter than this interval, the storage capacitor is considered as open. 0000: 0ms (minimum) 1111: 12ms (maximum) (default) … 0.8ms/step	1111

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PCB LAYOUT

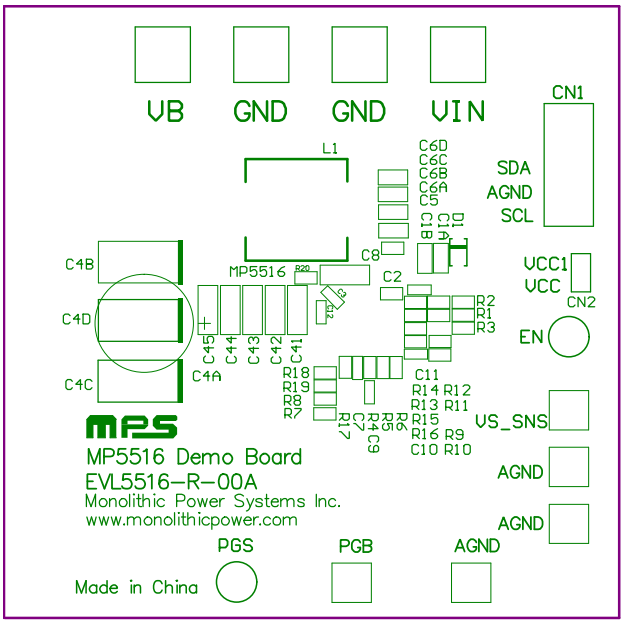

Figure 2: Top Silk

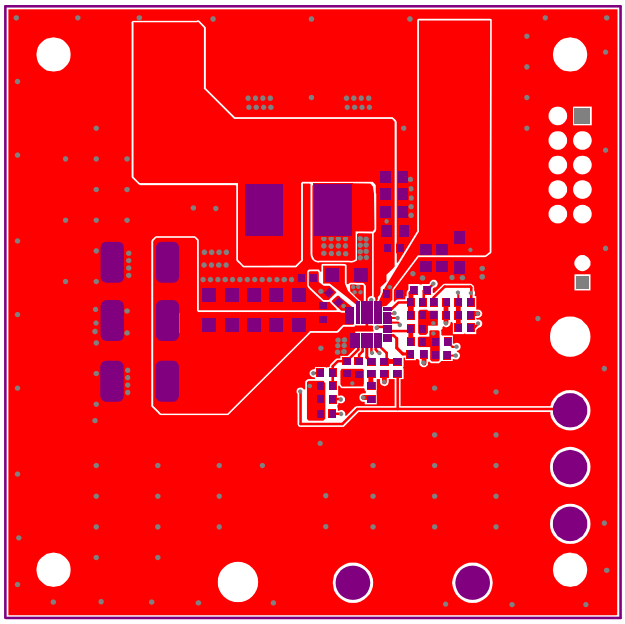

Figure 3: Top Layer

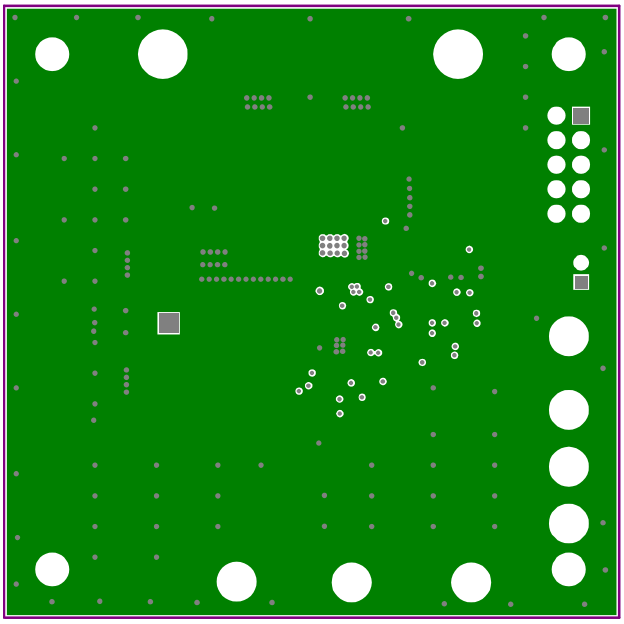

Figure 4: Mid-Layer 1

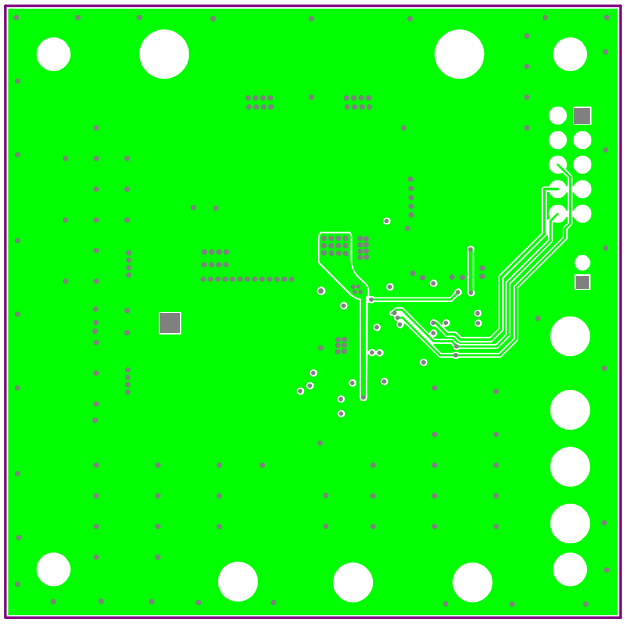

Figure 5: Mid-Layer 2

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PCB LAYOUT *(continued)*

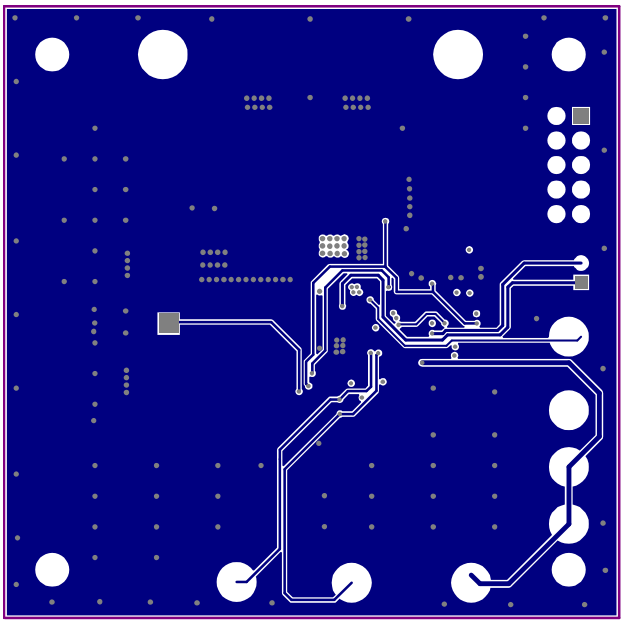

Figure 6: Mid-Layer 3

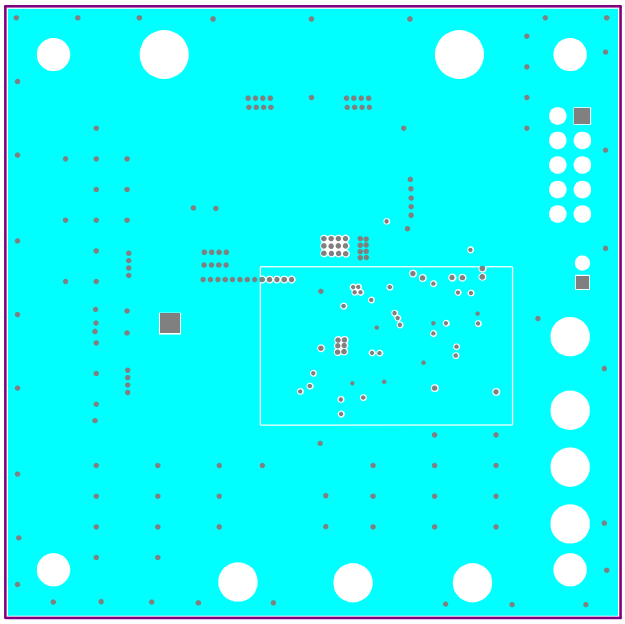

Figure 7: Mid-Layer 4

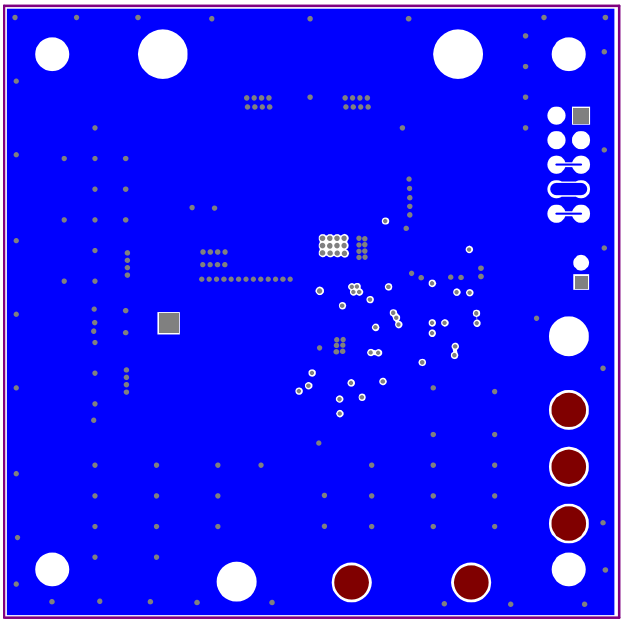

Figure 8: Bottom Layer

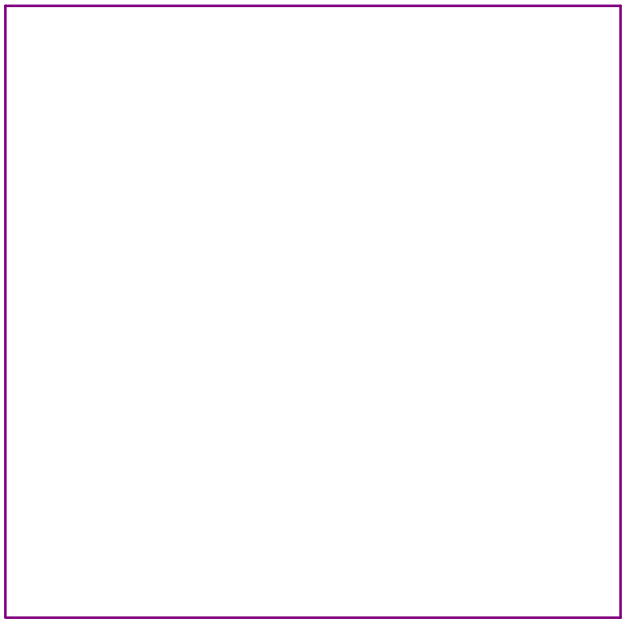

Figure 9: Bottom Silk

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	07/22/2021	Initial Release	-
1.1	9/9/2022	Updated the locations of R11 and R12 in Figure 1	4

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