



EVL28167-N-Q-00A

2.8V to 22V, 3A, 4-Switch, Integrated Buck-Boost Converter with PG Indication Evaluation Board

DESCRIPTION

The EVL28167-N-Q-00A is an evaluation board designed to demonstrate the capabilities of the MP28167-N, a high-efficiency, synchronous buck-boost converter with four integrated power switches and an I²C interface. The device can regulate output voltages across a wide 2.8V to 22V input voltage (V_{IN}) supply range.

The MP28167-N's integrated output voltage (V_{OUT}) scaling and configurable output current (I_{OUT}) limiting functions are ideal for USB power delivery (PD) applications.

In buck mode, the MP28167-N uses constant on-time (COT) control. In boost mode, it uses

constant-off-time control. This provides fast load transient response and a smooth buck-boost mode transient. The MP28167-N features automatic pulse-frequency modulation (PFM) and pulse-width modulation (PWM) modes, forced PWM mode, as well as configurable constant current (CC) limiting and soft start (SS). These features provide flexible design options for different applications.

The MP28167-N requires a minimal number of readily available, standard external components, and is available in a QFN-16 (3mmx3mm) package.

PERFORMANCE SUMMARY ⁽¹⁾

Specifications are at $T_A = 25^{\circ}\text{C}$, unless otherwise noted.

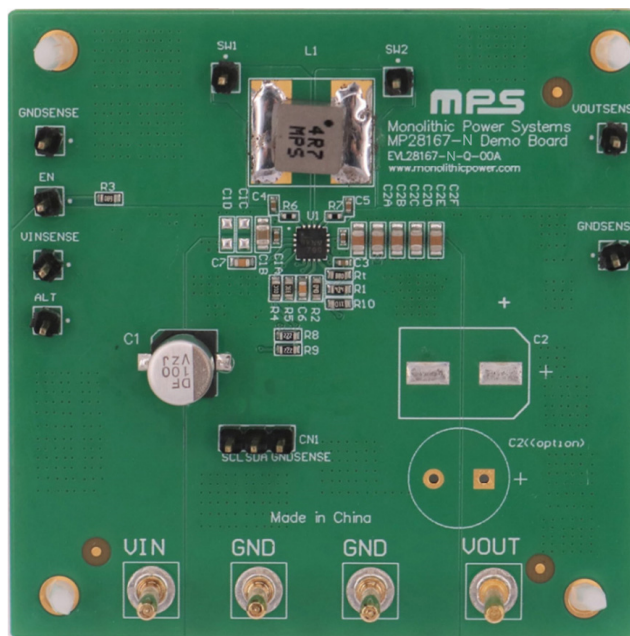
Parameters	Conditions	Value
Operating input voltage (V_{IN})		2.8V to 22V
Switching frequency (f_{SW})	Configured by register 04h, bits[3:2]	500kHz, 750kHz, 1MHz, or 1.25MHz
Output voltage (V_{OUT})	Determined by R1, R2, R_T , and register 00h, bits[2:0] + register 01h, bits[7:0] ⁽¹⁾	1V to 20.47V
Output current (I_{OUT})		3A continuous current or 4A input current

Note:

1) Refer to the MP28167-N datasheet for more details.

 Optimized Performance with MPS Inductor MPL5030 Series

EVL28167-N-Q-00A EVALUATION BOARD



LxW (6.35cmx6.35cm)

Board Number	MPS IC Number
EVL28167-N-Q-00A	MP28167GQ-N

QUICK START GUIDE

1. Connect the load terminals to:
 - a. Positive (+): VOUT
 - b. Negative (-): GND
2. Preset the power supply output to 12V, then turn off the power supply.
3. Connect the power supply output terminals to:
 - a. Positive (+): VIN
 - b. Negative (-): GND
4. After making the connections, turn on the power supply. The board should automatically start up with its default settings. The related parameters can be changed via the I²C. ⁽²⁾

Note:

- 2) Refer to the MP28167-N datasheet for more details.

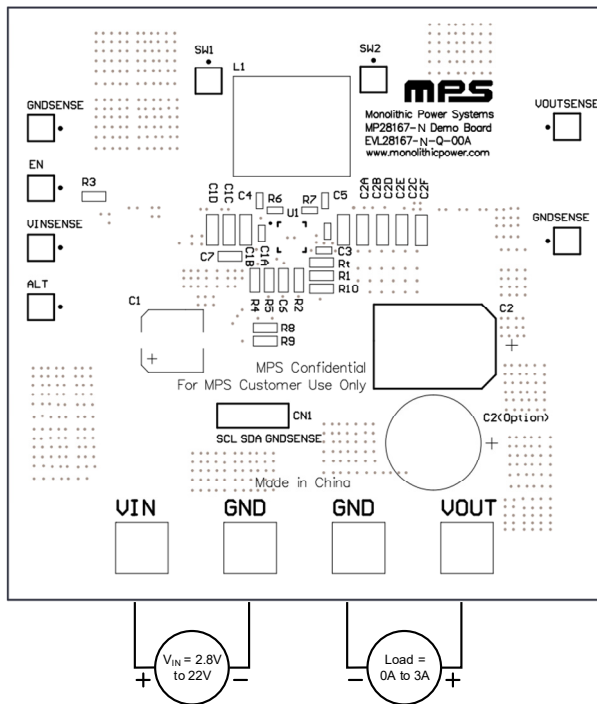


Figure 1: Measurement Equipment Set-Up

EVALUATION BOARD SCHEMATIC

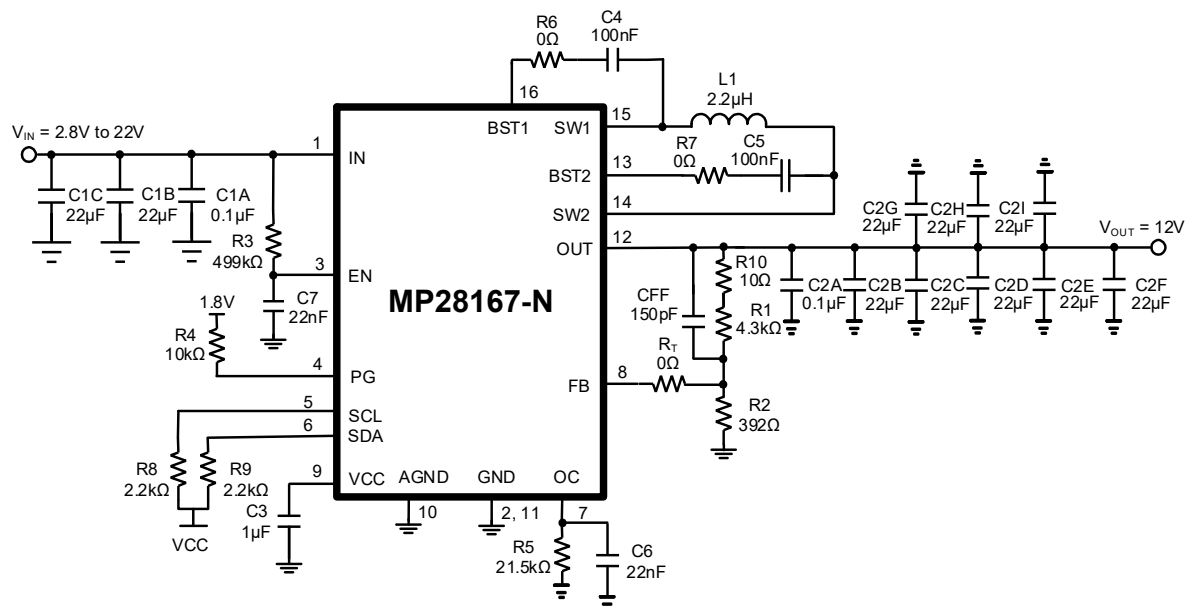


Figure 2: Evaluation Board Schematic

EV28167-N-Q-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
10	C2A, C1B, C2B, C1C, C2C, C2D, C2E, C2F, C2G, C2H	22 μ F	Ceramic capacitor, 25V, X5R	0805	TDK	C2012X5R1E226M
1	C3	1 μ F	Ceramic capacitor, 16V, X6S	0402	Murata	GRM155C81C105KE11D
4	C1A, C2A, C4, C5	100nF	Ceramic capacitor, 50V, X7R	0402	Samsung	CL05B104KB5NNNC
2	C6, C7	22nF	Ceramic capacitor, 50V, X5R	0603	Murata	GRM188R71H223KA01D
1	CFF	150pF	Ceramic capacitor, 50V, X5R	0603	Murata	GRM1885C1H151JA01D
1	R3	499k Ω	Film resistor, 1%	0603	Yageo	RC0603FR-07499KL
1	R5	21.5k Ω	Film resistor, 1%	0603	Yageo	RC0603FR-0721K5RL
1	R4	10k Ω	Film resistor, 1%	0603	Yageo	RC0603FR-0710KL
1	R1	4.3k Ω	Film resistor, 1%	603	Yageo	RC0603FR-07430KL
2	R8, R9	2.2k Ω	Film resistor, 1%	0603	Yageo	RC0603FR-072K2L
1	R2	392 Ω	Film resistor, 1%	0603	Yageo	RC0603FR-07107KL
1	R10	10 Ω	Film resistor, 1%	0603	Yageo	RC0603FR-0710RL
2	R6, R7	0 Ω	Film resistor, 1%	0402	Yageo	RC0402FR-070RL
1	R _T	0 Ω	Film resistor, 1%	0603	Yageo	RC0603FR-07806KL
1	CN1	2.54mm	Test pin, 1x3-pin	DIP	Würth	61300311121
1	L1' ⁽³⁾	2.2 μ H	Inductor, R _{DC} = 12m Ω , I _{SAT} = 14A	SMD	Würth	74437349022
1	L1	2.2 μ H	Inductor, R _{DC} = 12.3m Ω , I _{SAT} = 11A	SMD	MPS	MPL-AL5030-2R2
1	U1	MP28167-N	22V, 3A, 4-switch, integrated buck-boost converter with PG indication	QFN-16 (3mmx 3mm)	MPS	MP28167GQ-N

Note:

3) L1' indicates the backup inductor for L1. L1 is recommended for most applications.

EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board. $V_{IN} = 12V$, $V_{OUT} = 12V$, $L = 2.2\mu H$, $f_{SW} = 1MHz$, $T_A = 25^\circ C$, unless otherwise noted.

Start-Up through EN via I²C Command

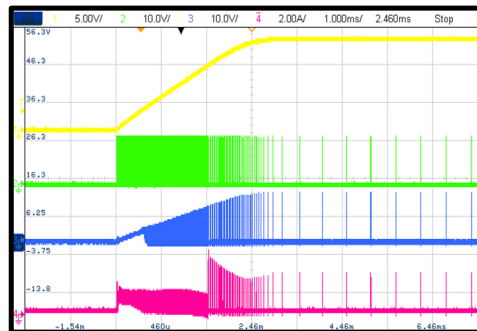
Load = 0A

CH1: V_{OUT}

CH2: SW1

CH3: SW2

CH4: I_L



Start-Up through EN via I²C Command

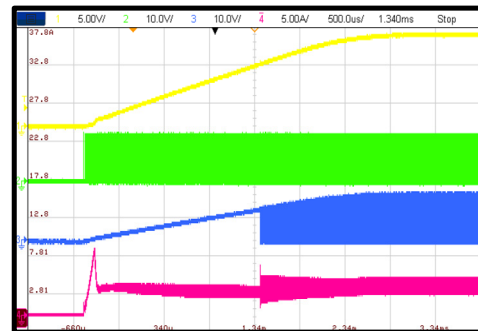
Load = 3A

CH1: V_{OUT}

CH2: SW1

CH3: SW2

CH4: I_L



Shutdown through EN via I²C Command

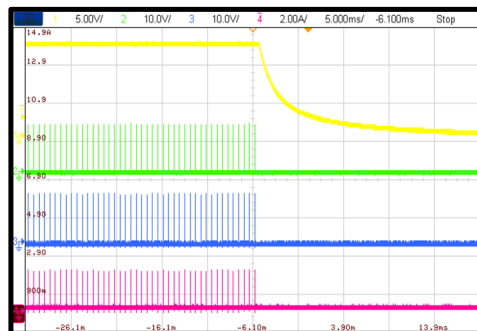
Load = 0A

CH1: V_{OUT}

CH2: SW1

CH3: SW2

CH4: I_L



Shutdown through EN via I²C Command

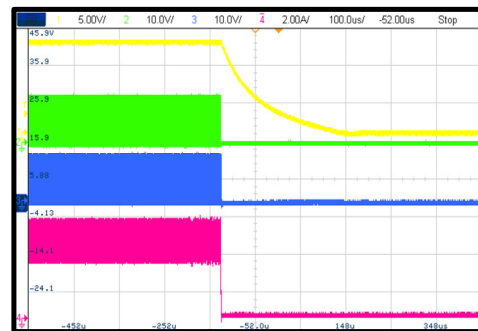
Load = 3A

CH1: V_{OUT}

CH2: SW1

CH3: SW2

CH4: I_L



Start-Up through EN

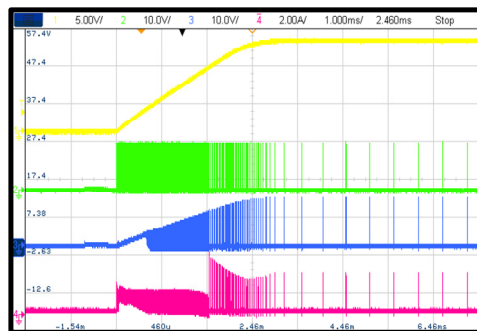
Load = 0A

CH1: V_{OUT}

CH2: SW1

CH3: SW2

CH4: I_L



Start-Up through EN

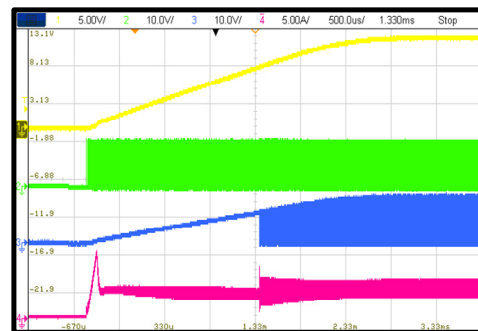
Load = 3A

CH1: V_{OUT}

CH2: SW1

CH3: SW2

CH4: I_L



EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. $V_{IN} = 12V$, $V_{OUT} = 12V$, $L = 2.2\mu H$, $f_{SW} = 1MHz$, $T_A = 25^\circ C$, unless otherwise noted.

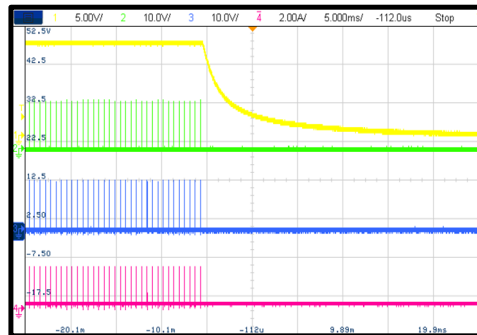
Shutdown through EN

Load = 0A

CH1: V_{OUT}
CH2: SW1

CH3: SW2

CH4: I_L



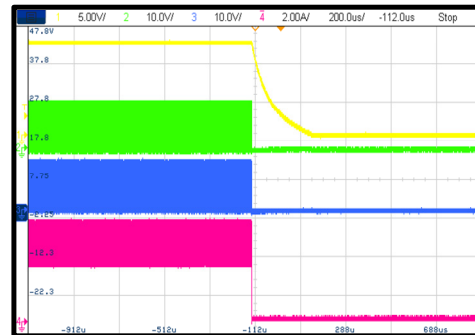
Shutdown through EN

Load = 3A

CH1: V_{OUT}
CH2: SW1

CH3: SW2

CH4: I_L



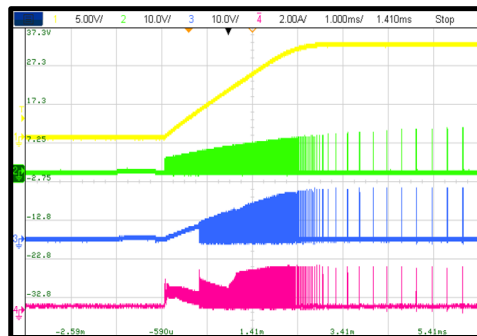
Start-Up through VIN

Load = 0A

CH1: V_{OUT}
CH2: SW1

CH3: SW2

CH4: I_L



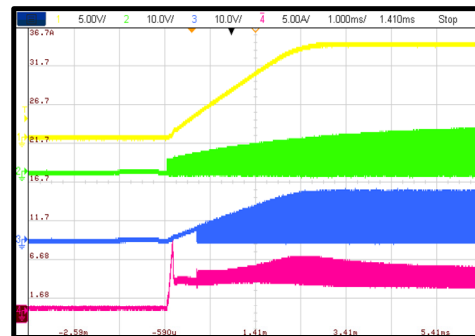
Start-Up through VIN

Load = 3A

CH1: V_{OUT}
CH2: SW1

CH3: SW2

CH4: I_L



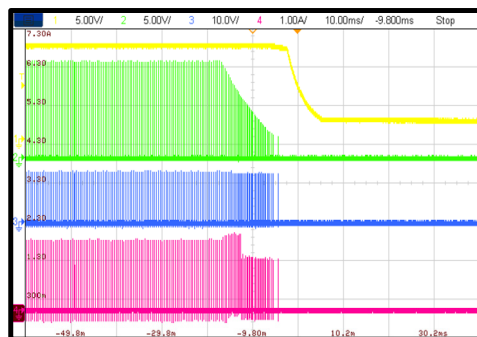
Shutdown through VIN

Load = 0A

CH1: V_{OUT}
CH2: SW1

CH3: SW2

CH4: I_L



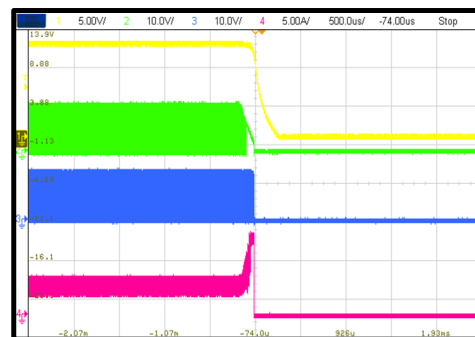
Shutdown through VIN

Load = 3A

CH1: V_{OUT}
CH2: SW1

CH3: SW2

CH4: I_L



EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. $V_{IN} = 12V$, $V_{OUT} = 12V$, $L = 2.2\mu H$, $f_{SW} = 1MHz$, $T_A = 25^\circ C$, unless otherwise noted.

Steady State (Automatic PFM/PWM Mode)

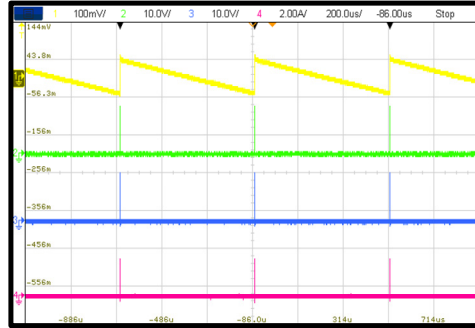
$V_{OUT} = 12V$, load = 0A, $f_{SW} = 1MHz$

CH1: V_{OUT}

CH2: SW1

CH3: SW2

CH4: I_L



Steady State (Automatic PFM/PWM Mode)

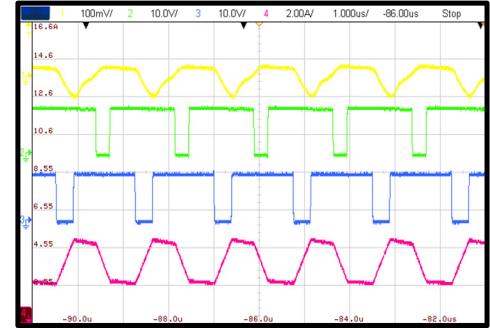
$V_{OUT} = 12V$, load = 3A, $f_{SW} = 1MHz$

CH1: V_{OUT}

CH2: SW1

CH3: SW2

CH4: I_L



Steady State (Automatic PFM/PWM Mode)

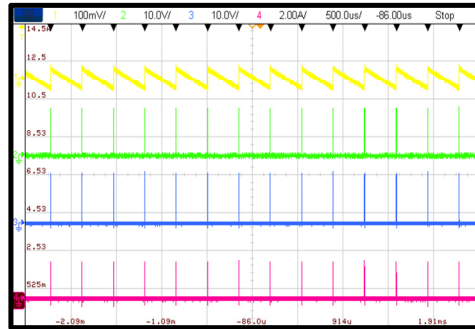
$V_{OUT} = 12V$, load = 0A, $f_{SW} = 1.25MHz$

CH1: V_{OUT}

CH2: SW1

CH3: SW2

CH4: I_L



Steady State (Automatic PFM/PWM Mode)

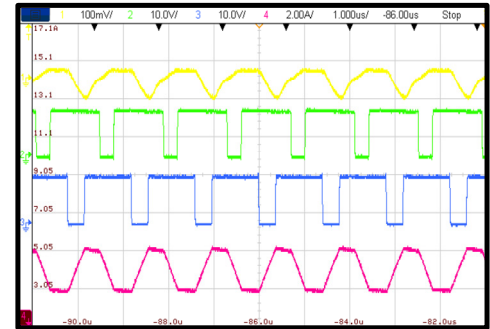
$V_{OUT} = 12V$, load = 3A, $f_{SW} = 1.25MHz$

CH1: V_{OUT}

CH2: SW1

CH3: SW2

CH4: I_L



I^2C VID

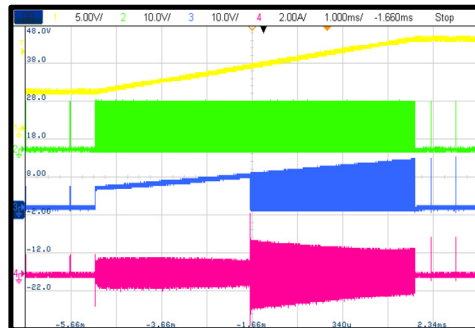
$V_{OUT} = 5V$ to $12V$, $I_{OUT} = 0A$, $R_1 = 4.3k\Omega$, $R_2 = 392k\Omega$

CH1: V_{OUT}

CH2: SW1

CH3: SW2

CH4: I_L



I^2C VID

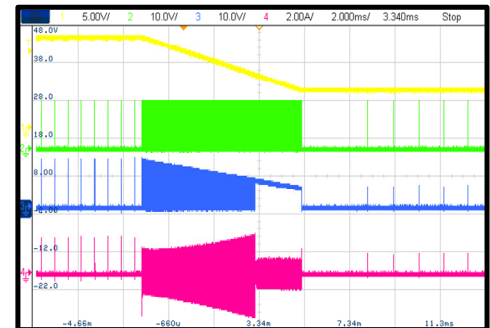
$V_{OUT} = 12V$ to $5V$, $I_{OUT} = 3A$, $R_1 = 4.3k\Omega$, $R_2 = 392k\Omega$

CH1: V_{OUT}

CH2: SW1

CH3: SW2

CH4: I_L

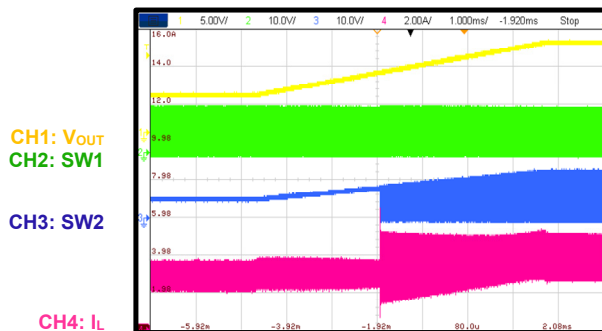


EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. $V_{IN} = 12V$, $V_{OUT} = 12V$, $L = 2.2\mu H$, $f_{SW} = 1MHz$, $T_A = 25^\circ C$, unless otherwise noted.

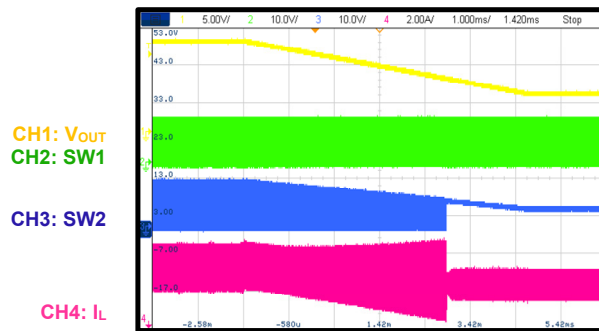
I^2C VID

$V_{OUT} = 5V$ to $12V$, $I_{OUT} = 0A$, $R_1 = 4.3k\Omega$,
 $R_2 = 392k\Omega$



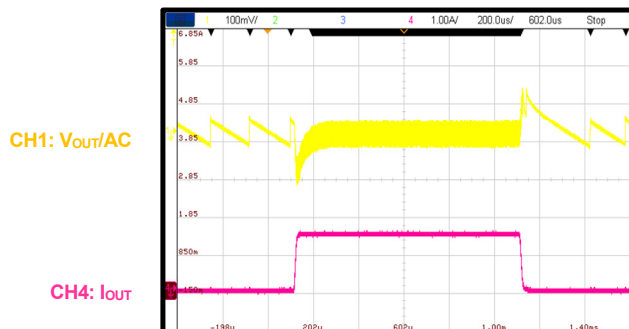
I^2C VID

$V_{OUT} = 12V$ to $5V$, $I_{OUT} = 3A$, $R_1 = 4.3k\Omega$,
 $R_2 = 392k\Omega$



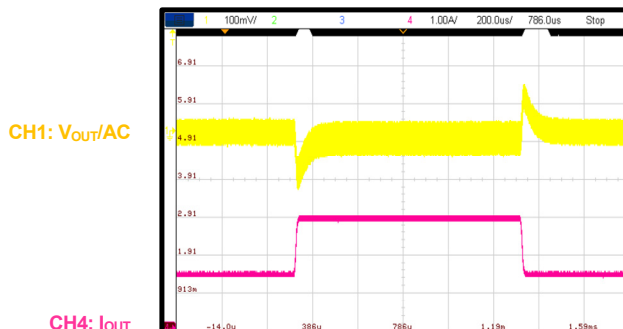
Load Transient

$V_{IN} = 12V$, $V_{OUT} = 12V$, no line drop
compensation, $0A$ to $1.5A$, $150mA/\mu s$

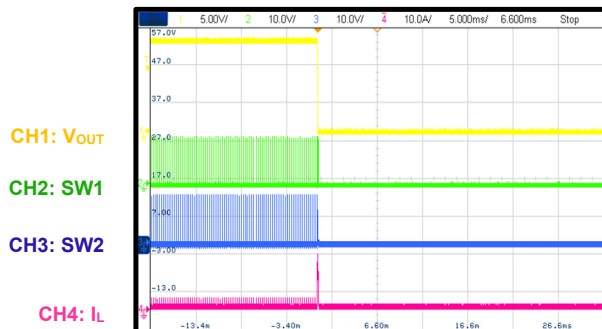


Load Transient

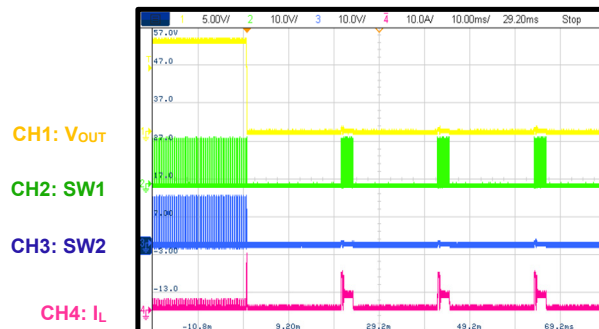
$V_{IN} = 12V$, $V_{OUT} = 12V$, no line drop
compensation, $1.5A$ to $3A$, $150mA/\mu s$



SCP Entry in Latch-Off Mode



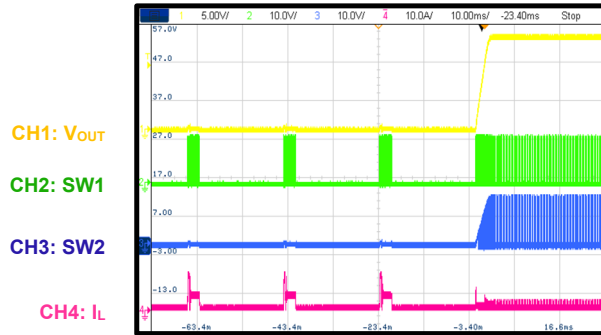
SCP Entry in Hiccup Mode



EVB TEST RESULTS *(continued)*

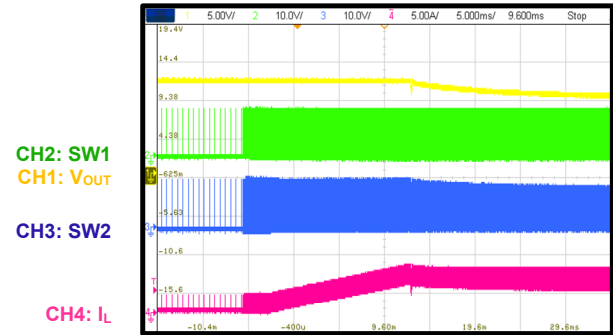
Performance curves and waveforms are tested on the evaluation board. $V_{IN} = 12V$, $V_{OUT} = 12V$, $L = 2.2\mu H$, $f_{SW} = 1MHz$, $T_A = 25^\circ C$, unless otherwise noted.

SCP Recovery in Hiccup Mode

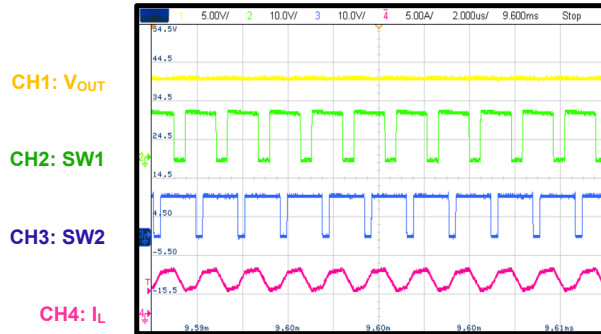


CC Limit Entry

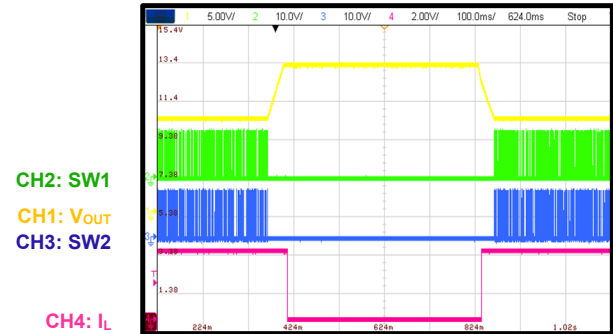
Tested in constant voltage (CV) mode on an electronic load



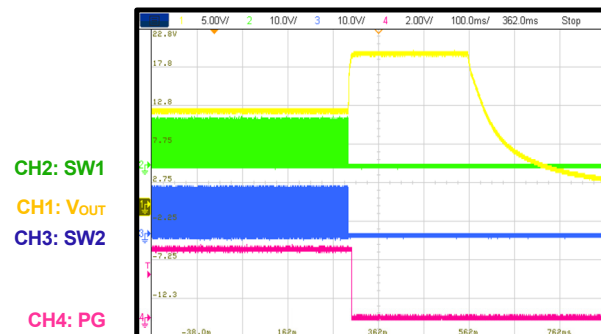
CC Limit Steady State



V_{OUT} OVP in Hiccup Mode



V_{OUT} OVP in Latch-Off Mode



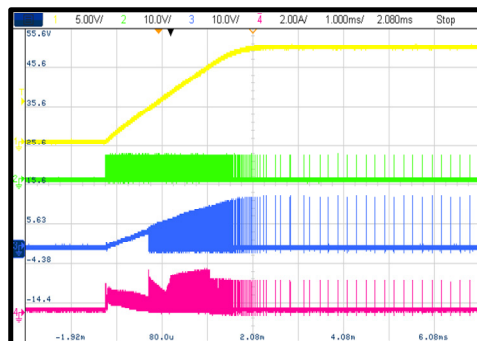
EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. $V_{IN} = 6V$, $V_{OUT} = 12V$, $L = 2.2\mu H$, $f_{SW} = 1MHz$, $T_A = 25^\circ C$, unless otherwise noted.

Start-Up through EN via I²C Command

Load = 0A

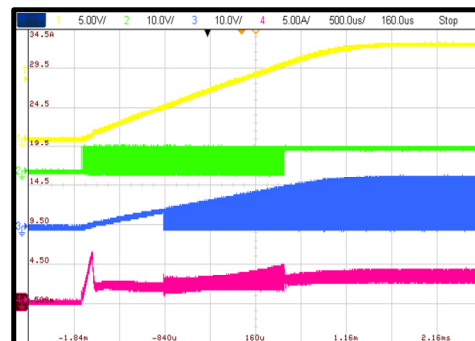
CH1: V_{OUT}
CH2: SW1
CH3: SW2
CH4: I_L



Start-Up through EN via I²C Command

Load = 1.4A

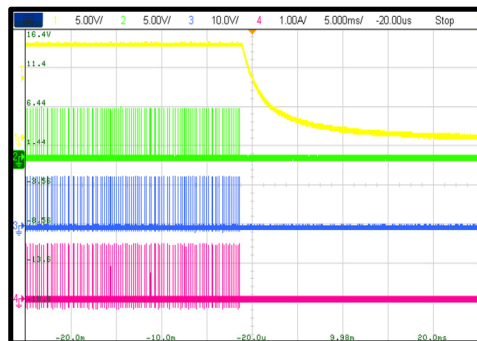
CH1: V_{OUT}
CH2: SW1
CH3: SW2
CH4: I_L



Shutdown through EN via I²C Command

Load = 0A

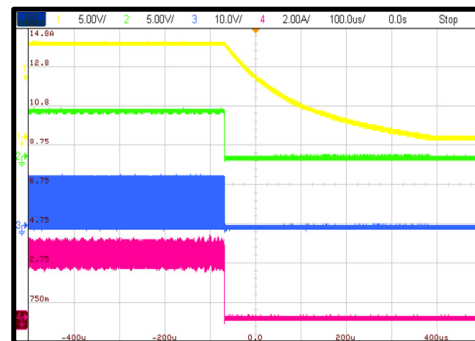
CH1: V_{OUT}
CH2: SW1
CH3: SW2
CH4: I_L



Shutdown through EN via I²C Command

Load = 1.4A

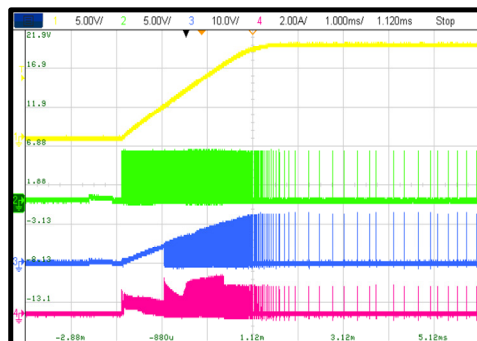
CH1: V_{OUT}
CH2: SW1
CH3: SW2
CH4: I_L



Start-Up through EN

Load = 0A

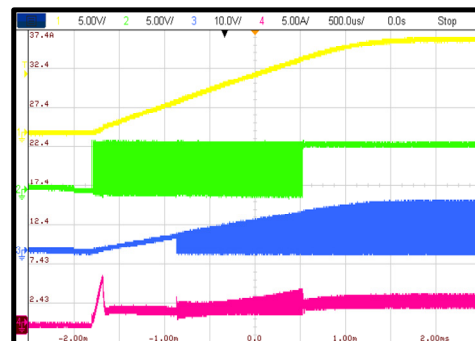
CH1: V_{OUT}
CH2: SW1
CH3: SW2
CH4: I_L



Start-Up through EN

Load = 1.4A

CH1: V_{OUT}
CH2: SW1
CH3: SW2
CH4: I_L



EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. $V_{IN} = 6V$, $V_{OUT} = 12V$, $L = 2.2\mu H$, $f_{SW} = 1MHz$, $T_A = 25^\circ C$, unless otherwise noted.

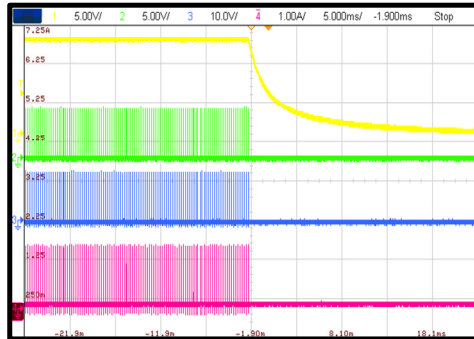
Shutdown through EN

Load = 0A

CH1: V_{OUT}
CH2: SW1

CH3: SW2

CH4: I_L



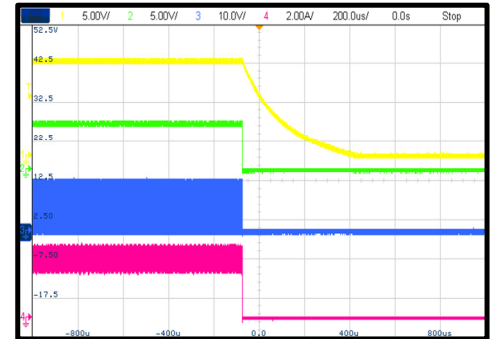
Shutdown through EN

Load = 1.4A

CH1: V_{OUT}
CH2: SW1

CH3: SW2

CH4: I_L



Start-Up through VIN

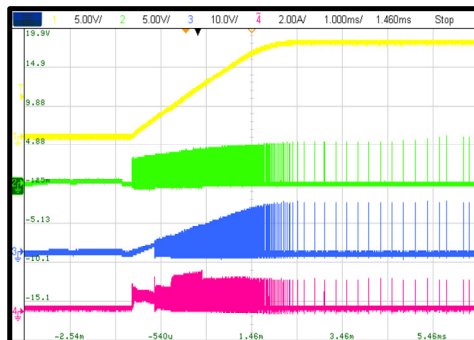
Load = 0A

CH1: V_{OUT}

CH2: SW1

CH3: SW2

CH4: I_L



Start-Up through VIN

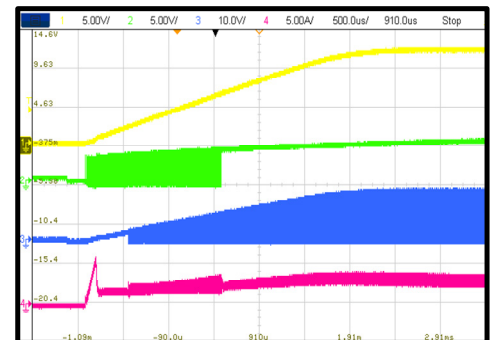
Load = 1.4A

CH1: V_{OUT}

CH2: SW1

CH3: SW2

CH4: I_L



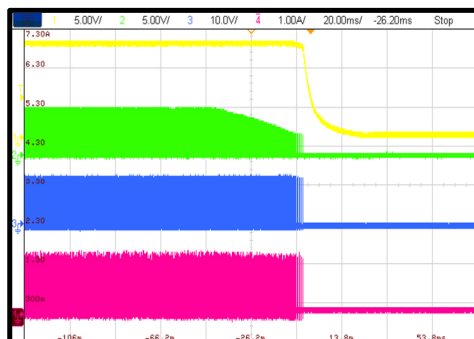
Shutdown through VIN

Load = 0A

CH1: V_{OUT}
CH2: SW1

CH3: SW2

CH4: I_L



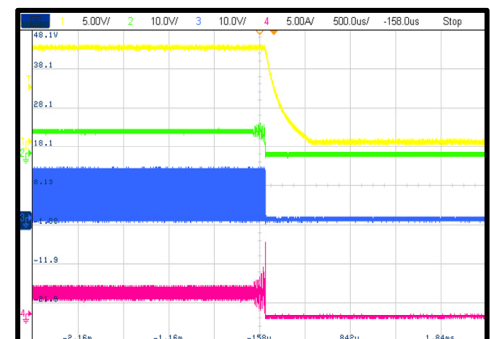
Shutdown through VIN

Load = 1.4A

CH1: V_{OUT}
CH2: SW1

CH3: SW2

CH4: I_L



EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. $V_{IN} = 6V$, $V_{OUT} = 12V$, $L = 2.2\mu H$, $f_{SW} = 1MHz$, $T_A = 25^\circ C$, unless otherwise noted.

Steady State (Automatic PFM/PWM Mode)

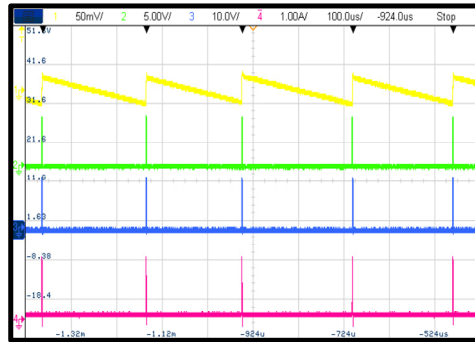
$V_{OUT} = 12V$, load = 0A, $f_{SW} = 1MHz$

CH1: V_{OUT}

CH2: SW1

CH3: SW2

CH4: IL



Steady State (Automatic PFM/PWM Mode)

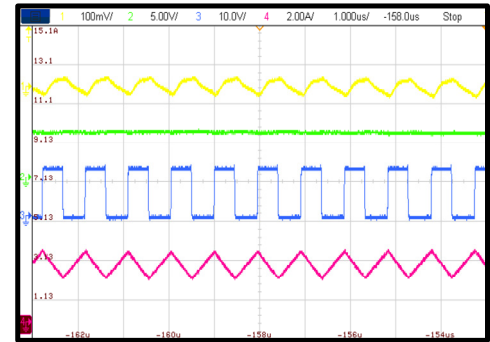
$V_{OUT} = 12V$, load = 1.4A, $f_{SW} = 1MHz$

CH1: V_{OUT}

CH2: SW1

CH3: SW2

CH4: IL



Steady State (Automatic PFM/PWM Mode)

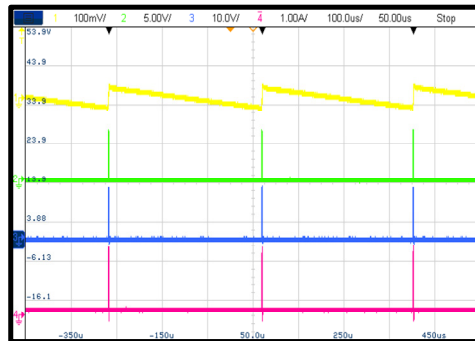
$V_{OUT} = 12V$, load = 0A, $f_{SW} = 1.25MHz$

CH1: V_{OUT}/AC

CH2: SW1

CH3: SW2

CH4: IL



Steady State (Automatic PFM/PWM Mode)

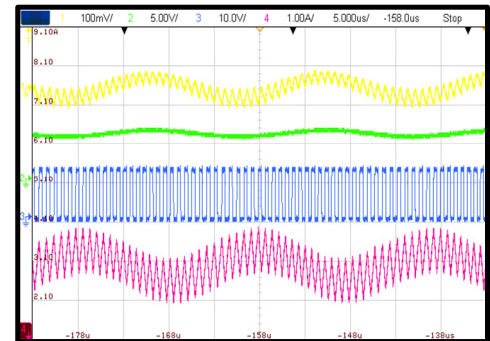
$V_{OUT} = 12V$, load = 1.4A, $f_{SW} = 1.25MHz$

CH1: V_{OUT}/AC

CH2: SW1

CH3: SW2

CH4: IL



I²C VID

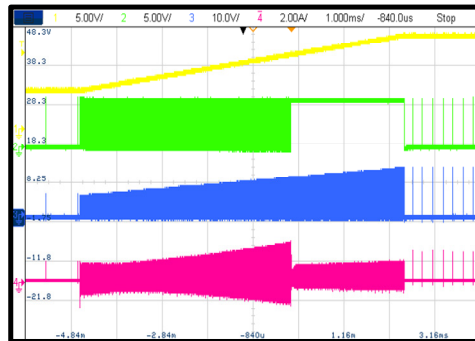
$V_{OUT} = 5V$ to $12V$, $I_{OUT} = 0A$, $R_1 = 4.3k\Omega$, $R_2 = 392k\Omega$

CH1: V_{OUT}

CH2: SW1

CH3: SW2

CH4: IL



I²C VID

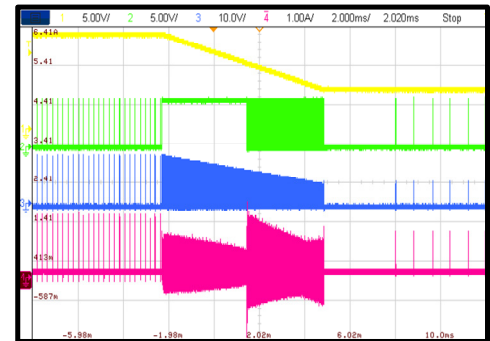
$V_{OUT} = 12V$ to $5V$, $I_{OUT} = 0A$, $R_1 = 4.3k\Omega$, $R_2 = 392k\Omega$

CH1: V_{OUT}

CH2: SW1

CH3: SW2

CH4: IL



EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. $V_{IN} = 6V$, $V_{OUT} = 12V$, $L = 2.2\mu H$, $f_{SW} = 1MHz$, $T_A = 25^\circ C$, unless otherwise noted.

I²C VID

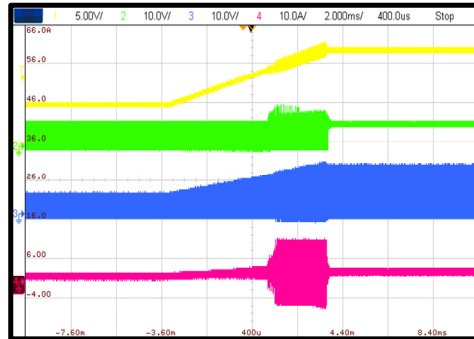
$V_{OUT} = 5V$ to $12V$, $I_{OUT} = 1.2A$, $R_1 = 4.3k\Omega$,
 $R_2 = 392k\Omega$

CH1: V_{OUT}

CH2: SW1

CH3: SW2

CH4: I_L



I²C VID

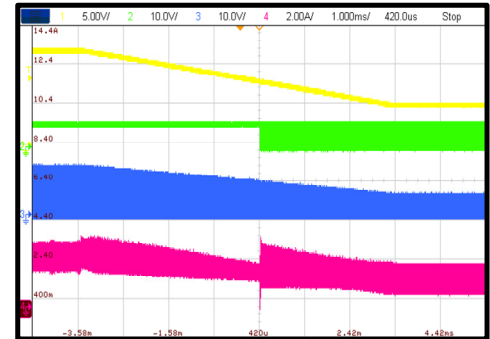
$V_{OUT} = 12V$ to $5V$, $I_{OUT} = 1.2A$, $R_1 = 4.3k\Omega$,
 $R_2 = 392k\Omega$

CH1: V_{OUT}

CH2: SW1

CH3: SW2

CH4: I_L

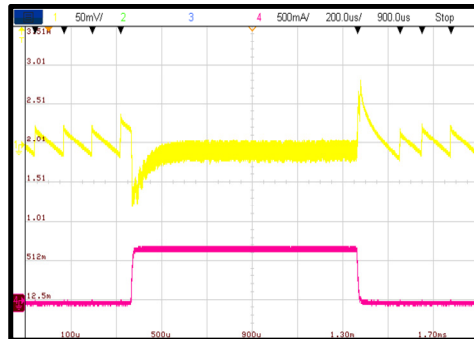


Load Transient

$V_{IN} = 12V$, $V_{OUT} = 12V$, no line drop
compensation, 0A to 0.7A, 150mA/ μs

CH1: V_{OUT}/AC

CH4: I_{OUT}

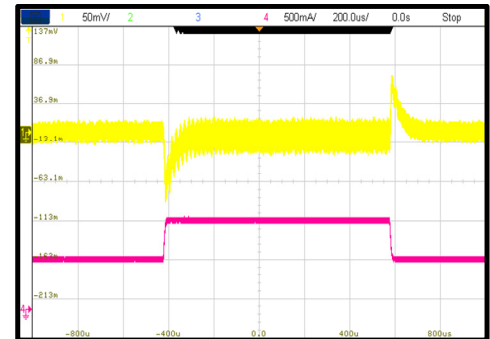


Load Transient

$V_{IN} = 12V$, $V_{OUT} = 12V$, no line drop
compensation, 0.7A to 1.4A, 150mA/ μs

CH1: V_{OUT}/AC

CH4: I_{OUT}



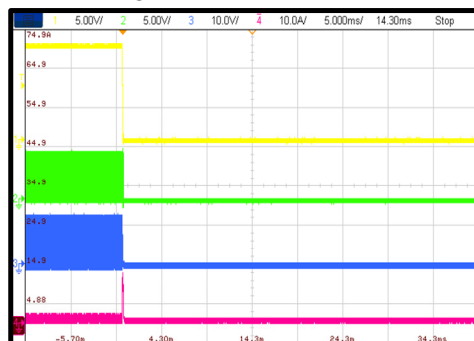
SCP Entry in Latch-Off Mode

CH1: V_{OUT}

CH2: SW1

CH3: SW2

CH4: I_L



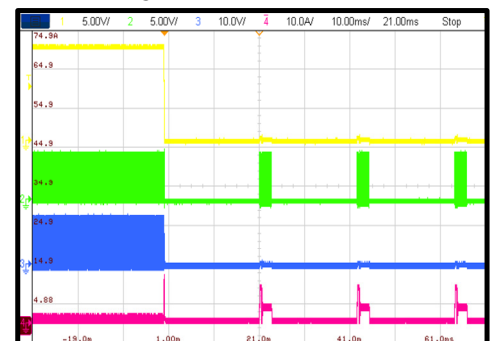
SCP Entry in Hiccup Mode

CH1: V_{OUT}

CH2: SW1

CH3: SW2

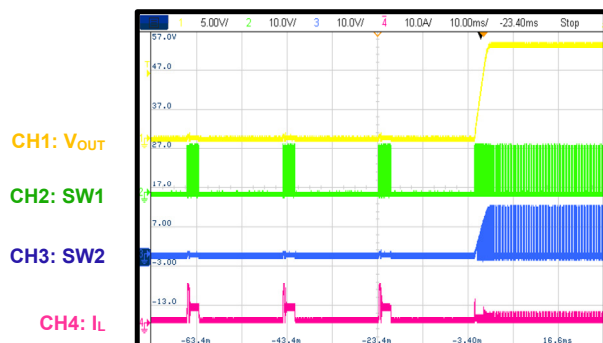
CH4: I_L



EVB TEST RESULTS *(continued)*

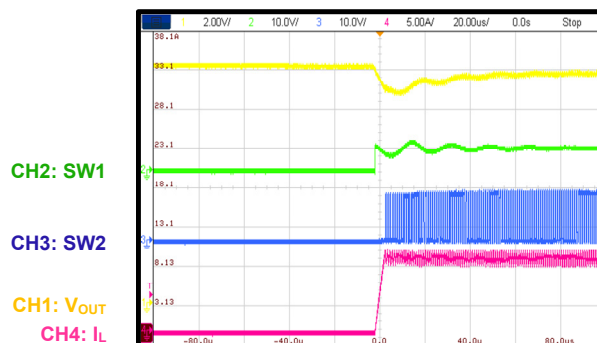
Performance curves and waveforms are tested on the evaluation board. $V_{IN} = 6V$, $V_{OUT} = 12V$, $L = 2.2\mu H$, $f_{SW} = 1MHz$, $T_A = 25^\circ C$, unless otherwise noted.

SCP Recovery in Hiccup Mode

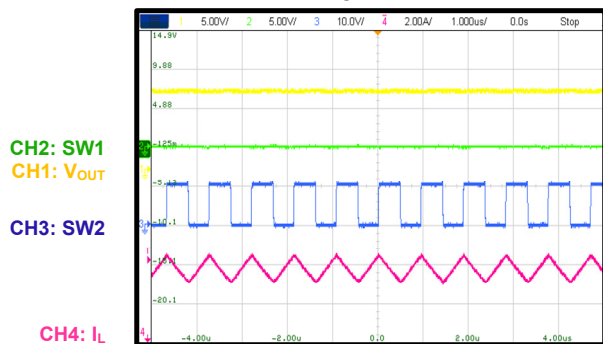


CC Limit Entry

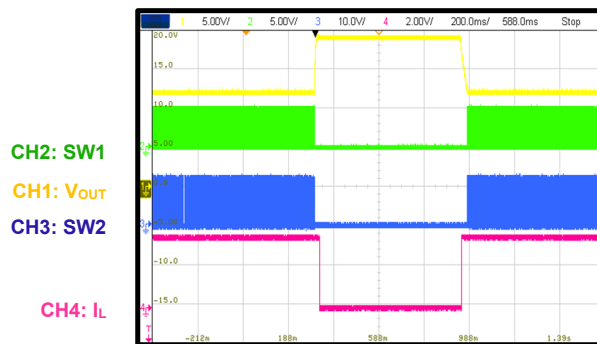
Tested in constant resistance (CR) mode on an electronic load



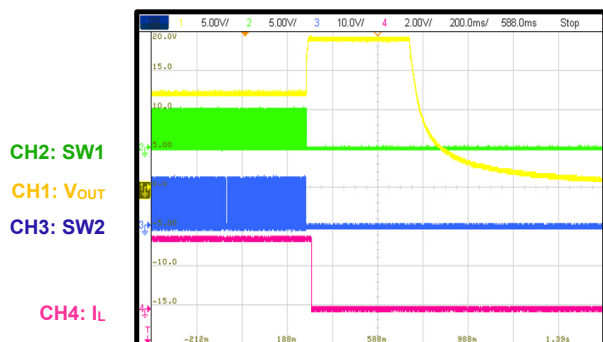
CC Limit Steady State



V_{OUT} OVP in Hiccup Mode



V_{OUT} OVP in Latch-Off Mode



PCB LAYOUT

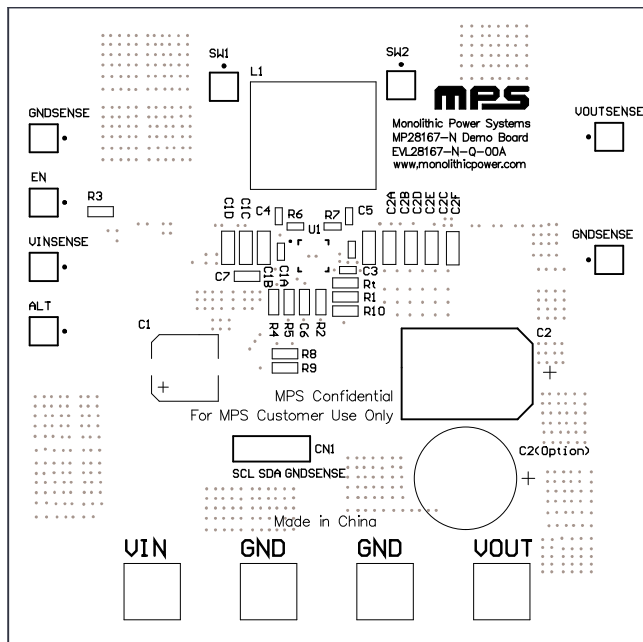


Figure 3: Top Silk

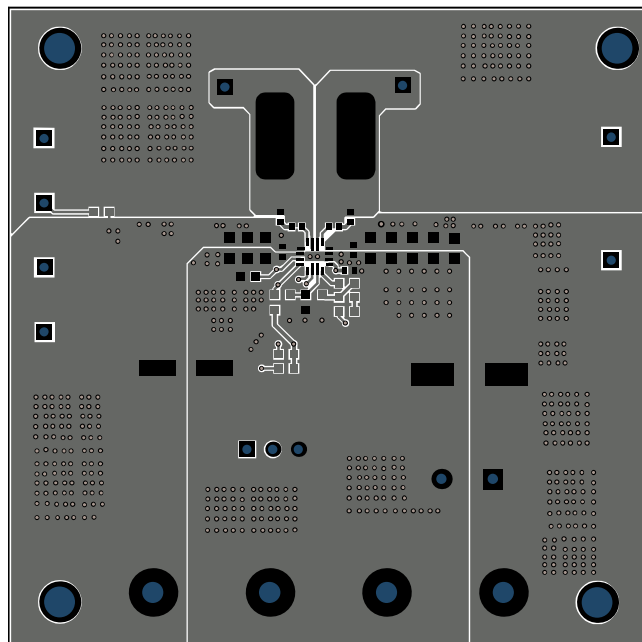


Figure 4: Top Layer

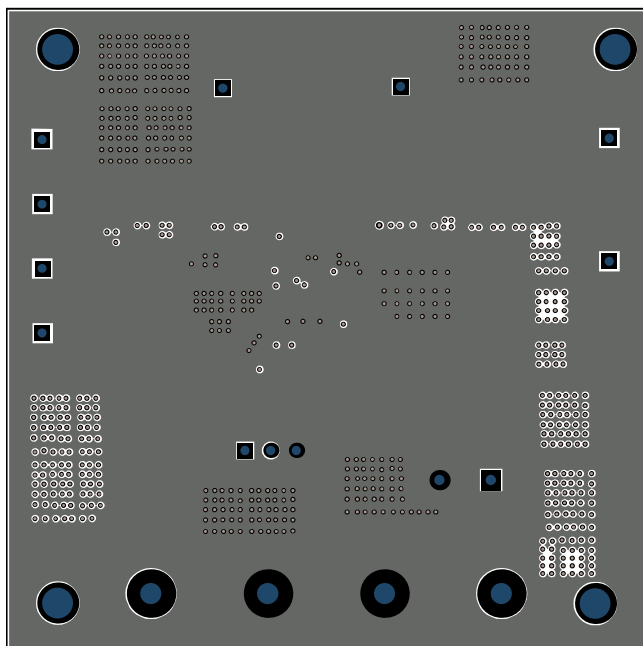


Figure 5: Mid-Layer 1

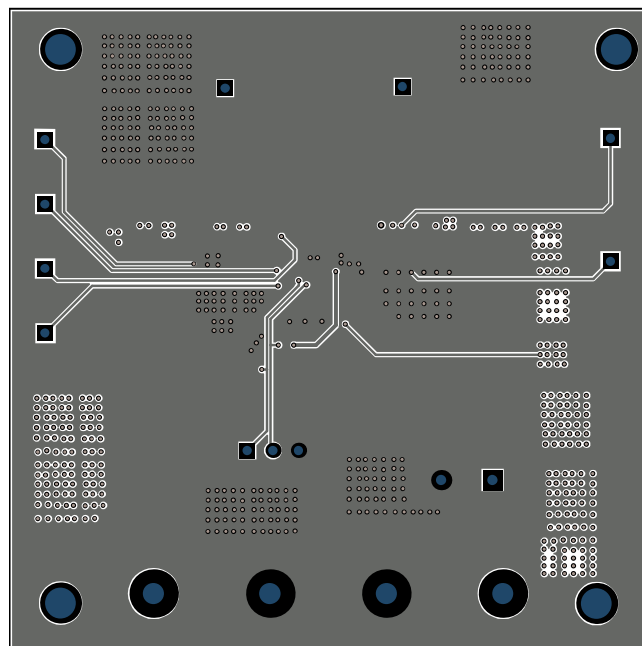


Figure 6: Mid-Layer 2

PCB LAYOUT *(continued)*

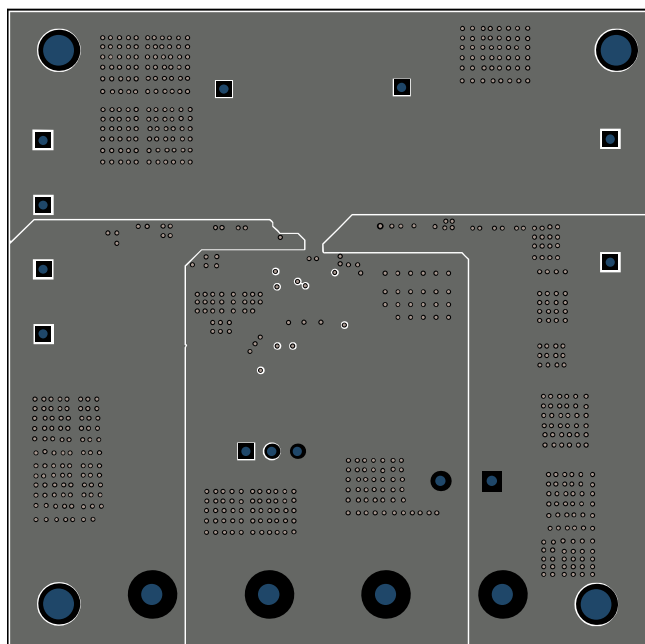


Figure 7: Bottom Layer



REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	5/8/2023	Initial Release	-

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