EVL2772-C-00A

2A, Switching Charger for 1-Cell Battery with NVDC, I²C, OTG, and Load Switch Evaluation Board

DESCRIPTION

The EVL2772-C-00A is an evaluation board designed to demonstrate the capabilities of the MP2772, a buck charger that can simultaneously charge a 1-cell battery and power the system's load. The MP2772 integrates a battery charger, boost converter, and two embedded load switches into a single device.

MP2772 only requires one inductor to charge the battery or boost the battery voltage to power the device. To extend the battery's shelf life, the MP2772 achieves a low quiescent current (I_Q) down to 5μA in shipping mode and provides a low I_Q for boost operation under light loads. The integrated analog-to-digital converter (ADC) monitors battery charging parameters and load parameters during boost operation.

The MP2772 provides various safety features for battery charging and system operations, including a charge safety timer, battery/junction temperature monitoring, as well as over-voltage (OV), and over-current (OC) protections. The device asserts an interrupt (INT) signal to the microcontroller (MCU) host after encountering a fault condition.

The MP2772's I²C interface flexibly configures the charging and boosting parameters, such as the input voltage limit, input current limit, charging current, charge-full voltage, boost output voltage, and current limit.

The MP2772 also provides battery MOSFET disable control to enter shipping mode and a system pin reset function via the /DISC pin.

The EVL2772-C-00A supports 5V input sources, including standard USB host ports and wall adapters. The EVL2772-C-00A supports boost output operation by supplying 4V to 6V (100mV/step) with a maximum 1.5A load in OTG mode.

The default function of this board is preset for charger mode, and the charge full voltage is preset to 4.2V.

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C, unless otherwise noted.

Parameters	Conditions	Value
Input voltage (V_{IN}) range		4V to 6.5V
Battery voltage (V_{BATT})	V_{IN} = 5V, I_{BATT} = 20mA to 2A	4.2V
Maximum charge current (I_{CC_MAX})	V_{IN} = 5V, V_{BATT} = 3.8V	2A
Typical charge efficiency	V_{IN} = 5V, V_{BATT} = 3.8V, I_{BATT} = 1.5A	92.6%
Peak charge efficiency	V_{IN} = 5V, V_{BATT} = 4.2V, I_{BATT} = 0.5A	96%
Fast charge current	V_{IN} = 5V, V_{BATT} = 3.8V	2A
LDSW current limit Setting	V_{IN} or V_{BOOST} = 5V, QR or QL are enabled	600mA
Switching frequency (f_{SW})		1.5MHz

MPL Optimized Performance with MPS Inductor MPL-AY3020 Series

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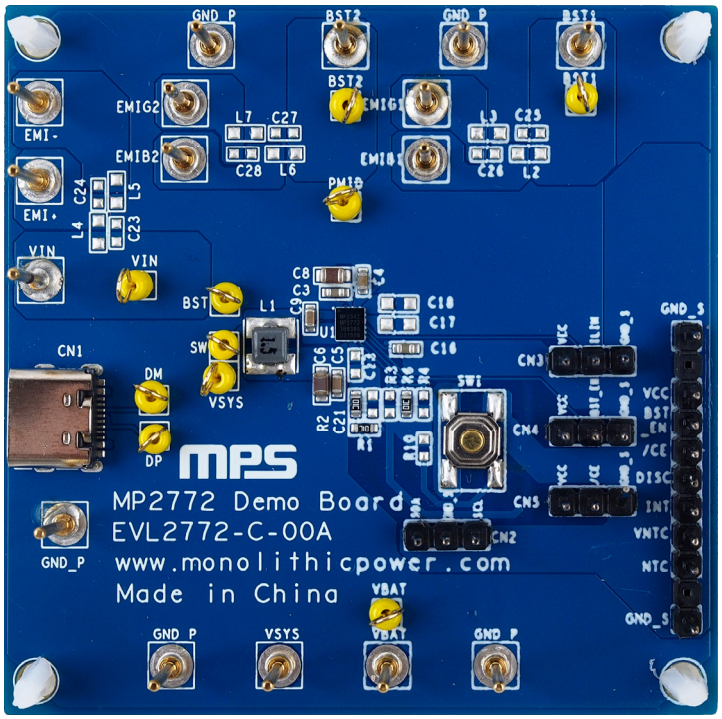
EVALUATION BOARD



LxWxH (6.35cmx6.35cmx1.3cm)

Board Number	MPS IC Number
EVL2772-C-00A	MP2772GC-0000

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QUICK START GUIDE

This EVL2772-C-00A is designed for MP2772 when the MP2772 is used as a buck charger to charge a 1-cell battery and power the system load simultaneously. The MP2772 is a 30-pin, highly integrated, switching battery charger that provides a complete solution for wearable and portable devices. The device includes an 8-bit analog-to-digital converter (ADC) for battery and system monitoring, smart power-path management, narrow-voltage DC (NVDC) charging, a push-button controller, integrated load switches with individual enable functions, and an autonomous battery charging profile.

The EVL2772-C-00A's layout accommodates most commonly used capacitors. The default function of this board is preset for charger mode, and the charge-full voltage is preset to 4.2V for single-cell Li-ion batteries. The EVL2772-C-00A can be used even when the jumpers on the board are not connected. Only CN2 should be connected to the I²C connector.

Evaluation Platform Preparation

1. Use a USB cable and a computer with at least one available USB port. The MP2772 evaluation software must be properly installed.
2. Prepare the USB-to-I²C communication interface (EVKT-USBI2C-02).

Figure 1: USB-to-I²C Communication Interface

3. To access the software, double-click on the "MP2772 Evaluation Kit" .exe file to run the MP2772 evaluation software. The software is supported on Windows XP, Windows 7, and later operating systems. The MP2772 evaluation kit .exe file can be downloaded from the MPS website.
4. Configure the test set-up for the MP2772 (see Figure 2).

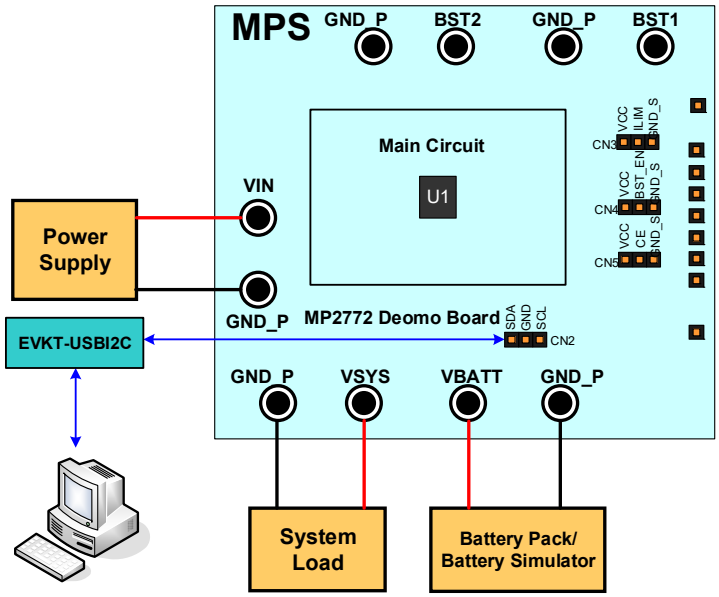

Figure 2: Test Set-Up for the MP2772

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5. Attach the battery terminals to:
   a. Positive (+): VBATT
   b. Negative (-): GND_P
6. If using a battery simulator, preset the battery voltage to 3.8V with a charge/discharge current limit of 5A, then turn off the battery simulator. Connect the battery simulator output to the VBATT and GND_P pins, respectively. Keep the battery simulator turned off before starting the test.
7. In charge mode, set the input power source to 5V (DC) with an output current limit at 5A, then turn off the input power source. Attach the input voltage and the input ground to the VIN and GND_P pins, respectively.
8. In USB on-the-go (OTG) mode, attach the load terminals to:
   a. Positive (+): VIN
   b. Negative (-): GND_P

Table 1 shows how to connect the jumpers.

Table 1: Jumper Connections (1)

Jack	Description	Factory Connection	Setting
CN3	IN_CTL: Pull up to VCC through R5, or connect to GND_S. This is the input current limit configuration pin. A high logic sets the limit to 2.5A; a low logic sets the limit to 0.5A. When the ILIM pin is floating, it is pulled low internally. This pin control can be disabled via ILIM_PIN_EN = 0.	Open	I_{IN_LIM} = 0.5A
CN4	BST_CTL: This is the boost function's external control pin. A high logic enables the boost function; a low logic disables the function. When the BST_EN pin is floating, it is pulled low internally. This pin control can be disabled via PIN_CTRL_EN = 0.	Open	Boost disabled
CN5	CE_CTL: This is the charging function's external control pin. A high logic disables the charge function; a low logic enables it. When the /CE pin is floating, it is pulled low internally. This pin control can be disabled via PIN_CTRL_EN = 0.	Open	Charge enabled

Note:

1) The three jumper connections are set to open by default. When using the board to start the test, set the register bits ILIM_PIN_EN and PIN_CTRL_EN to 0 (disabled); then certain control settings are handled by the register.

9. Launch the MP2772 evaluation software.

   Turn on the battery simulator; the main window of the software should be visible (see Figure 3). If the connection is successful, the lower-left corner should display "Device connected" with a green light; otherwise, the lower-left corner should display "Device disconnected" with a red light.

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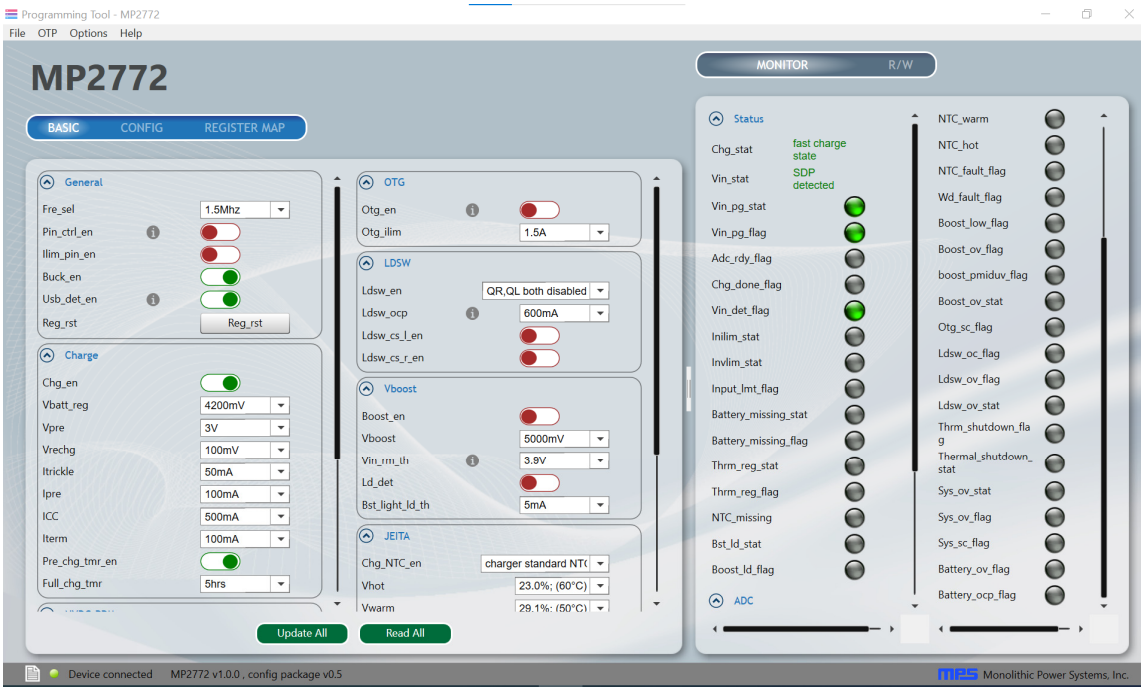

Figure 3: MP2772 Evaluation Software

10. Turn on the input power source and float the loads on the load switches and VSYS. The MP2772 works in charge mode by default.

Modifying Parameters via the GUI

1. Set PIN_CTRL_EN and ILIM_PIN_EN to 0 (disabled) so that the charge control and input current limit are determined by the registers; otherwise they are determined by CN3 ,CN4, and CN5
2. The part should work to charge the battery with the default setting.

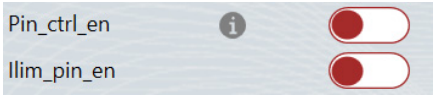

Figure 4: PIN_CTRL_EN and ILIM_PIN_EN

3. Set the basic general charge controls (see Figure 5).

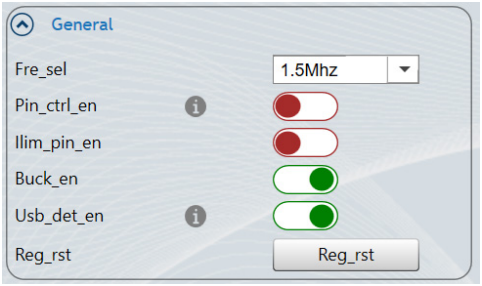

Figure 5: MP2772 Charge General Setting

The basic controls include selecting the operation frequency and other on/off controls. Refer to the MP2772's datasheet for detailed register map information.

Keep the default settings but set PIN_CTRL_EN and ILIM_PIN_EN to 0.

4. Set the charging parameters (see Figure 6).

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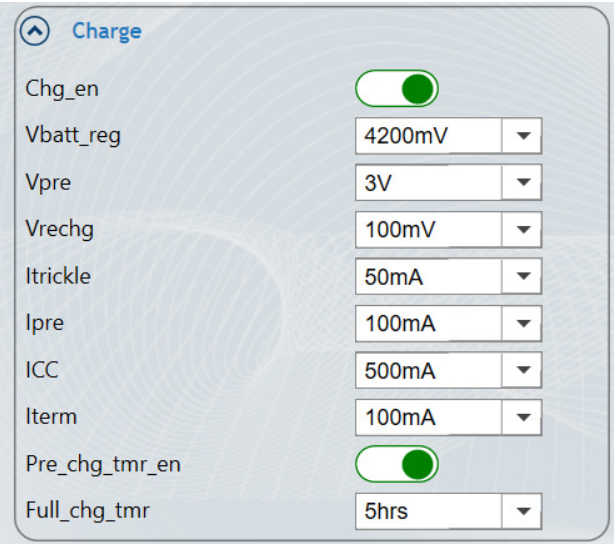

Figure 6: MP2772 Charging Setting Parameters

a. Chg_en: Controls whether charging is enabled. It does not enable/disable the battery's discharging function.

b. Vbatt_reg: The default value is 4.2V. The battery regulation voltage (V_{BATT_REG}) can be set between 3.6V and 4.6V, with 10mV/step.

c. Vpre: This value sets the V_{BATT} threshold at which charge mode changes from pre-charge to constant-current (CC) charge. The threshold can be set to 2.4V, 2.6V, 2.8V, or 3V. The default value is 3V.

d. Itrickle: The trickle current ($I_{TRICKLE}$) ranges between 10mA and 70mA, with 10mA/step.

e. Ipre: The pre-charge current (I_{PRE}) ranges between 10mA and 160mA, with 10mA/step.

f. Iterm: The termination current (I_{TERM}) ranges between 10mA and 160mA, with 10mA/step.

g. Pre_chg_tmr_en: This bit enables the timer during the pre-charge period. The pre-charge timer is set to 2hr internally.

h. Full_chg_tmr: This setting provides the timer setting during CC and constant-voltage (CV) charging. The options are 5hr, 10hr, and 15hr. This setting can also disable the timer.

5. Set the NVDC parameters (see Figure 7).

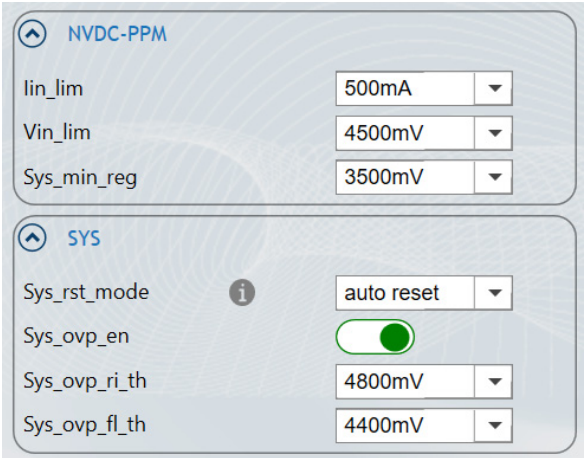

Figure 7: MP2772 NVDC Setting Parameters

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a. Iin_lim: The default value is 500mA, but the input current limit (I_{IN_LIM}) can range between 100mA and 3200mA, with 100mA/step. The default I_{IN_LIM} is set according to the BC1.2 detection result. Change the ILIM_RECONFIG bit to 1 to set I_{IN_LIM} using this setting.

b. Vin_lim: The default value is 4500mV, but the input voltage limit (V_{IN_LIM}) can range between 3900mV and 5400mA, with 100mV/step. This setting set the minimum input voltage limit.

c. Sys_min_reg: This selection is for the NVDC charger. When V_{BATT} is below the SYS_MIN_REG threshold, then the system voltage (V_{SYS}) is set to the VSYS_MIN_REG + VTRACK. The setting ranges between 3200mV and 4250mA, with 150mV/step.

d. Sys_rst_mode: Controls the system's auto-reset mode, which refers to the application when a user wants to reset the system. There are two modes, described as below.

The first mode is an automatic reset. If this setting is selected, the system turns off for a time period when the /DISC pin pulls low for a certain time. If there is no V_{IN}, the battery FET stays off during this period; if V_{IN} is present, both the DC/DC converter and the battery FET are off.

The second mode is a manual reset. When manual reset mode is selected, the battery FET turns off, and it does not turn on automatically. Manual reset mode is valid only when there is no input power.

e. Sys_ovp_en: Enables the system's over-voltage protection (OVP) function.

f. Sys_ovp_ri_th: Sets the OVP rising threshold.

g. Sys_ovp_fl_th: Sets the OVP falling threshold.

6. Set the charge termination parameters on the "CONFIG" page (see Figure 8).

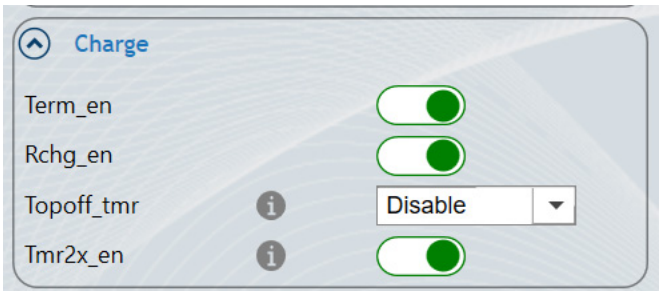

Figure 8: MP2772 Charge Termination Control

a. Term_en: Enables charge termination.

b. Rchg_en: Enables the auto-recharge function.

c. Topoff_timer: Enables the top off timer setting. It is disabled by default.

d. Tmr2x_en: Selects whether the general timer is extended to 2 times during a DPM status (IIN_LIM state or VIN_LIM state).

7. Set the charge NTC JEITA parameters (see Figure 9 on page 8).

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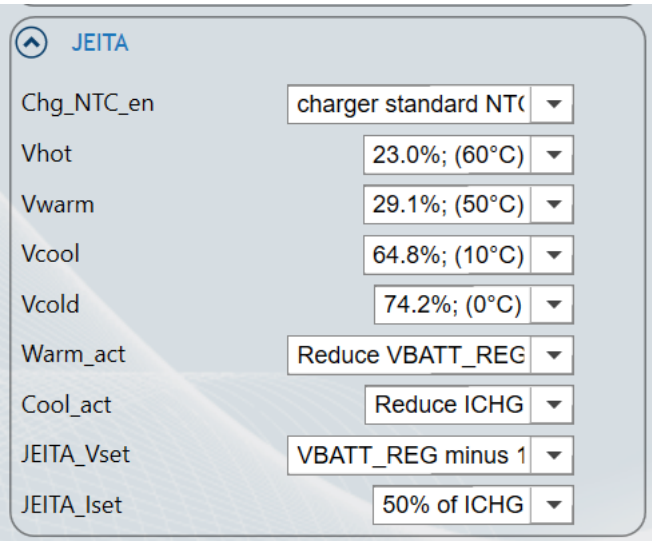

Figure 9: MP2772 Charge NTC JEITA Setting

a. Chg_NTC_en: Selects the NTC protection as either standard NTC protection (only hot and cold thresholds) or JEITA protection. If NTC JEITA monitoring is selected, all the thresholds can be configured (V_{HOT}, V_{WARM}, V_{COOL}, and V_{COLD}), and the action during warm and cool conditions can also be configured.

8. Set the boost mode parameters (see Figure 10). The MP2772 can work in boost mode to supply power to the IN pin or LDSW output from the battery.

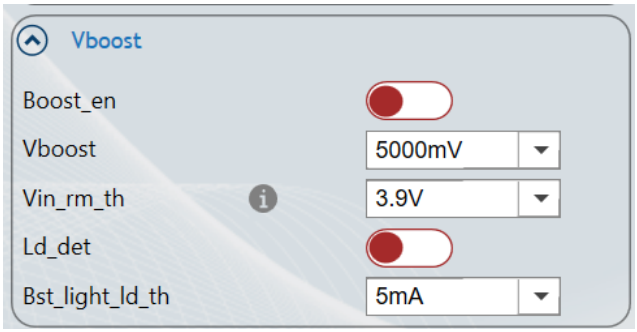

Figure 10: MP2772 Boost Mode Setting

a. Boost_en: Enables the boost function.

b. Vboost: Sets the boost output voltage. This ranges between 4000mV and 6000mV, with 100mV/step.

c. Vin_rm_th: Sets the V_{IN} falling threshold to enter auto-boost mode when V_{IN} is removed. If BOOST_EN is enabled and V_{IN} drops below this threshold, the auto-boost function begins.

d. Ld_det: Enables the boost's no-load detection function.

e. Bst_light_ld_th: Sets boost mode's light-load threshold. If this threshold is reached, an INT is sent and the related status bit (BST_LD_STAT) is set to 1 to indicate that the boost load is below this threshold.

9. When BOOST_EN is enabled, OTG mode can be enabled (see Figure 11).

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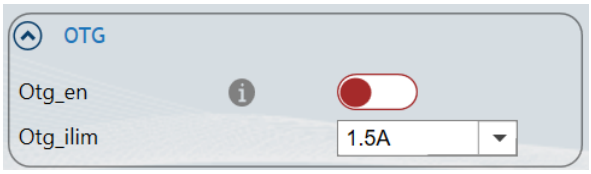

Figure 11: MP2772 OTG Mode Setting

a. Otg_en: Enables OTG mode, which means the boost output from the IN pin powers the OTG load.

b. Otg_ilim: Sets the OTG current limit. This can be set to 500mA, 900mA, 1.2A, or 1.5A. The default value is 1.5A.

10. Set the battery thresholds on the “CONFIG” page (see Figure 12).

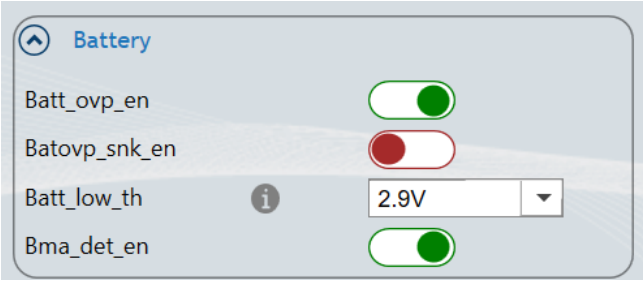

Figure 12: MP2772 Battery Threshold Setting and Control

a. Batt_ovp_en: Enables battery OVP.

b. Batt_ovp_snk_en: Enables the sink load on the battery pin if battery OVP occurs.

c. Batt_low_th: Sets a threshold to limit the minimum V_{BATT} in boost mode. This threshold can be set to 2.7V or 2.9V, and this limit can also be disabled via this bit.

d. Bma_det_en: Enables missing battery detection. This is enabled by default.

11. Set the parameters related to the LDSW (see Figure 13).

The MP2772 provides two paths for the load switch output: BST1 and BST2. The user can set either BST1 and BST2 to control whether the LDSW is on. Otherwise, both BST1 and BST2 can be used in buck mode or boost mode to control whether the LDSW is on. In buck mode, the input passes the power to LDSW through a block FET, and the LDSW switches. In boost mode, the LDSW is powered from the PMID (boost output). OTG mode and LDSW mode cannot be powered at the same time in boost mode. The two LDSW outputs can work individually or they can be shorted together to one output port. The default current limit of the load switch is 600mA for each rail. In buck mode, there are 4 options for the LDSW OCP threshold; in boost mode; only 600mA is recommended.

For LDSW short-circuit protetion (SCP) and over-current protection (OCP), the device enters hiccup or latch-off mode after the event is detected 8 times. LDSW_CS_EN must be enabled.

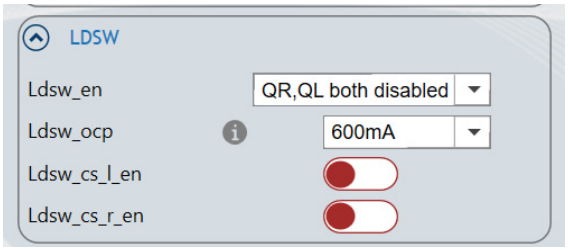

Figure 13: MP2772 LDSW Setting and control

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a. Ldsw_en: On/off control bit for QR and QL.

b. Ldsw_ocp: Sets the LDSW load current limit.

c. Ldsw_cs_l_en: Enables the QL current-sense function.

d. Ldsw_cs_r_en: Enables the QR current-sense function.

12. Set the parameters for shipping mode. Figure 14 shows the battery FET (BATTFET) registers.

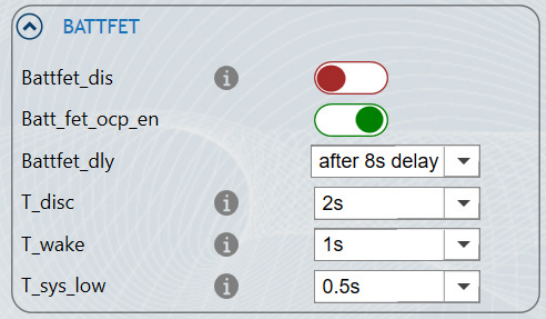

Figure 14: MP2772 BATTFET Control

a. Battfet_dis: Directly controls whether the BATTFET is on/off. This bit is only valid when there is no input.

b. Batt_fet_ocp_en: Enables the battery discharge OCP function.

c. Battfet_dly: Sets the BATTFET turn-off delay to 2s, 4s, 8s, or no delay. When there is no input, to turn off the BATTFET (enter shipping mode) via the I^2C, the BATTFET_DIS bit is set and the BATTFET turns off after the delay time set by this bit.

d. T_disc: In addition to I^2C control, the MP2772's /DISC pin can also turn off the BATTFET. Pull the /DISC pin from high to low when first setting the time via this register. The options include 1s, 2s, 4s, and 8s.

e. T_wake: When the MP2772 is in shipping mode, there are only two methods to exit shipping mode. The first method is to remove V_{IN}, and the second method is to pull the /DISC pin from high to low for the time set by this register. This time can be set to 500ms,1s, 2s, or 4s.

f. T_sys_low: When the SYS is set to auto-reset mode and the /DISC pin is pulled low to turn off the BATTFET, the BATTFET automatically turns on (at the earliest) after the time period set by this register. The time can be set to 0.5s, 1s, 2s, or 4s.

13. Set the watchdog timer parameters (see Figure 15). The watchdog timer is disabled by default. To enable the watchdog timer, set the watchdog timer to auto-reset before the timer runs out; otherwise, the registers reset to their default values.

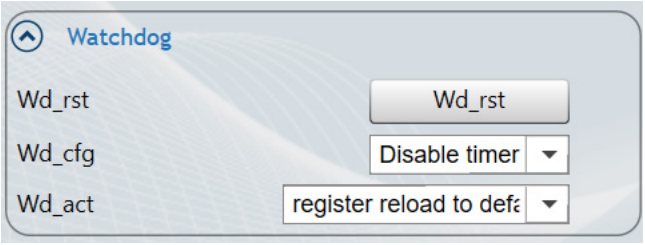

Figure 15: MP2772 Watchdog Timer Setting

a. Wd_rst: Clears the watchdog timer to 0.

b. Wd_cfg: Sets the watchodog timer period. This period can be set to 40s, 80s, 160s, or disabled.

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c. Wd_act: Sets the IC's actions when the watchodog timer times out. The default setting is to reload the register's default values, but it can also be set such that the SYS pin cycles its power when the timer runs out.

14. The MP2772 provides one-shot ADC conversion for certain parameters (see Figure 16).

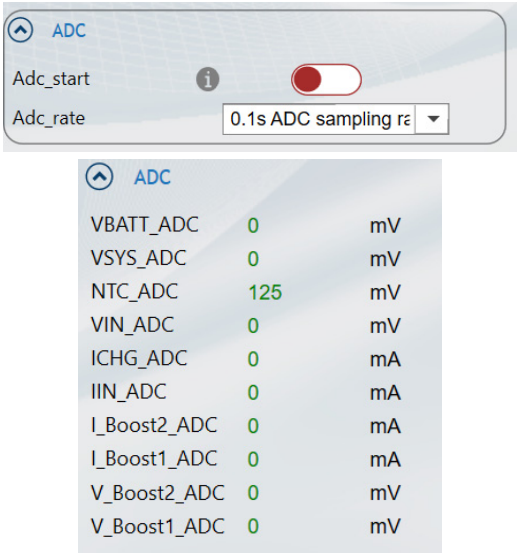

Figure 16: MP2772 ADC Coversion Parameter

When ADC_START is set to 1, the IC starts the ADC conversion for one time. Read the ADC registers for the result(s).

15. Set the INT and flag bits (see Figure 17). The MP2772 provides INT and flag bits to show the MP2772's state.

The INT function can be masked by the following registers. If the INT function is required, unmask the INT function.

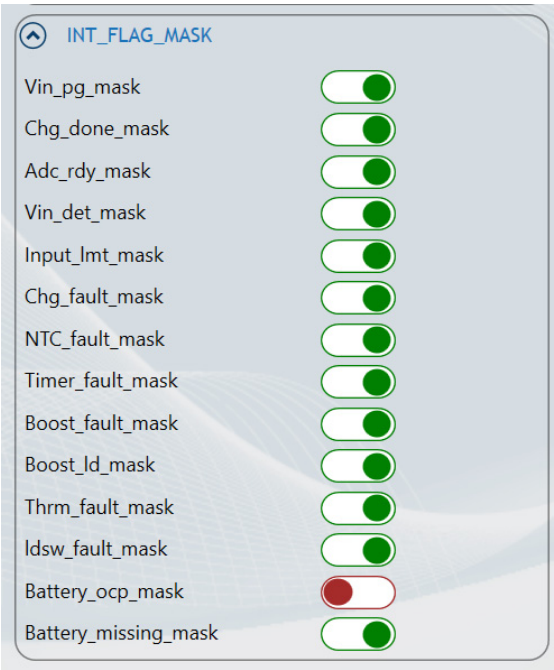

Figure 17: INT Masks

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Before INT asserts, clear the faults flags from register 10h to register 12h, and ensure that they are unmasked. Figure 18 shows the potential fault statuses and flags.

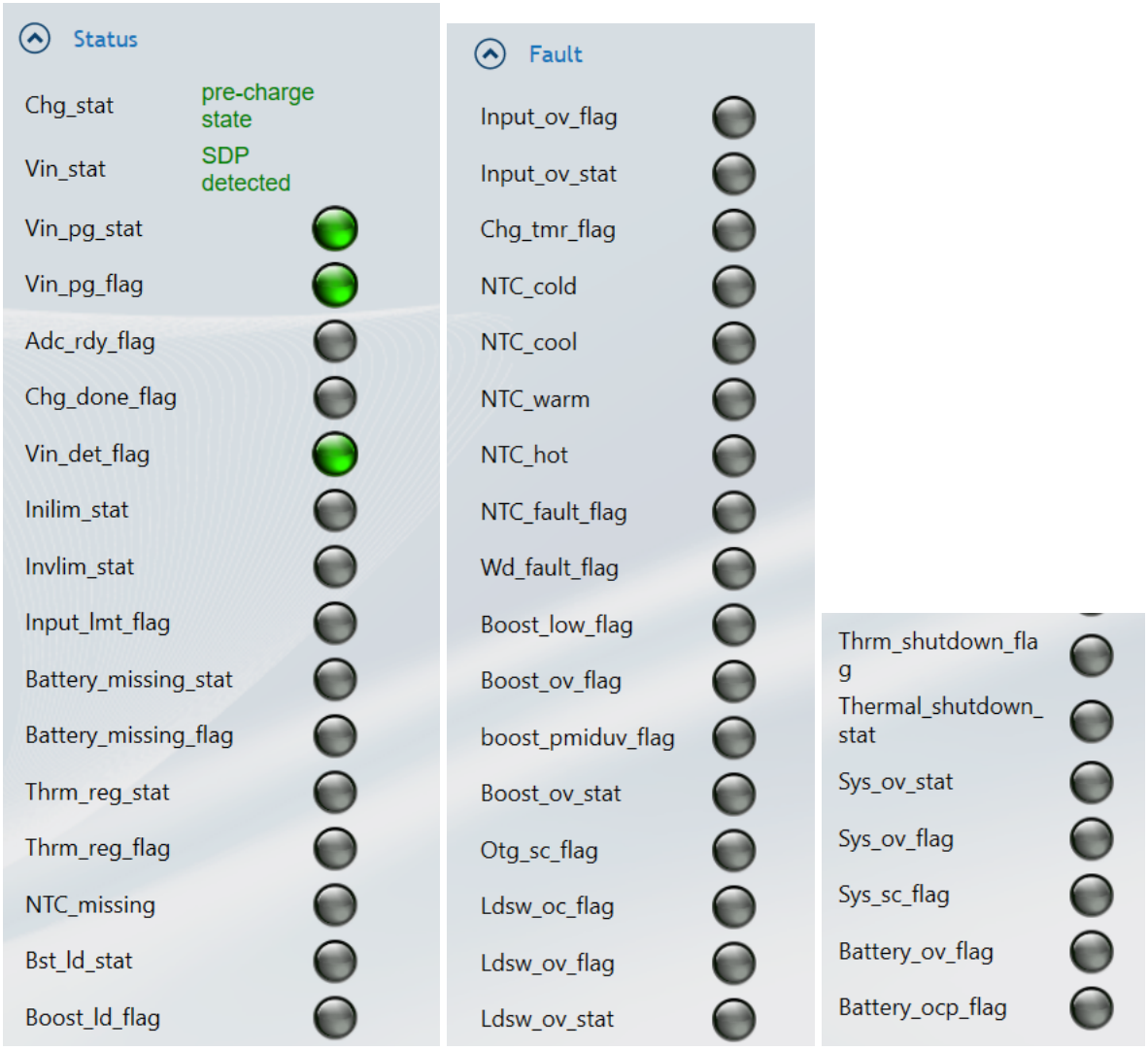

Figure 18: MP2772 Status and Fault Flag Bits

The flag bits must be written to 1 to be cleared; otherwise, they always show up. After the flag bit is read, it is recommended to write 1 to the bit so that it is cleared.

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EVALUATION BOARD SCHEMATIC

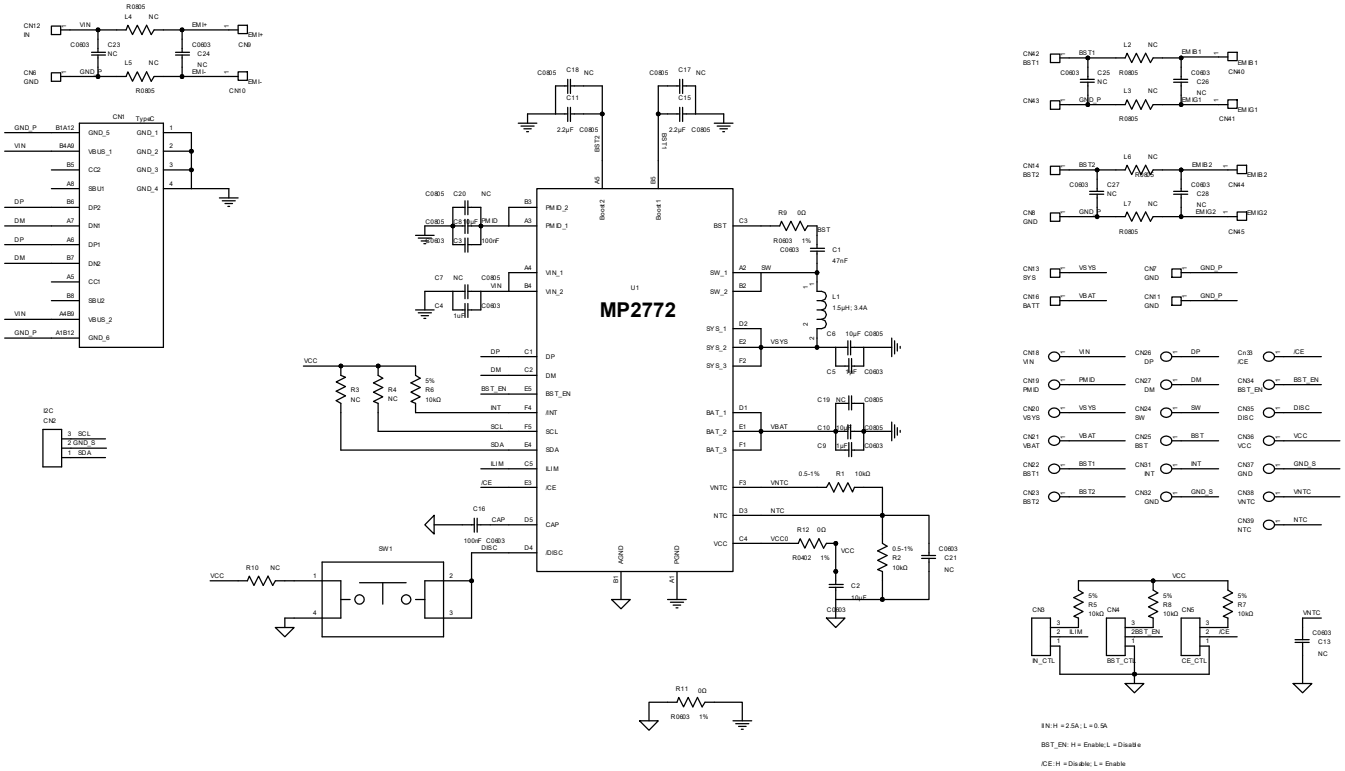

Figure 19: Evaluation Board Schematic

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EVL2772-C-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	C1	47nF	Capacitor, 25V, X7R	0603	HHEC	C0603X473K025T
1	C2	10μF	Capacitor, 10V, X7R	0603	Murata	GRM188Z71A106KA73D
2	C3, C16	100nF	Capacitor, 50V, X7R	0603	Murata	GRM188R71H104KA93D
1	C4	1μF	Capacitor, 50V , X5R	0603	Murata	GRM188R61H105KAAL
2	C5, C9	1μF	Capacitor, 16V, X7R	0603	Murata	GRM188R71C105KA12D
1	C6	10μF	Capacitor, 25V, X5R	0805	Murata	GRJ21BR61E106KE01L
3	C7, C19, C20	NC	Capacitor, 35V, X7R	0805	NC	NC
2	C8, C10	10μF	Capacitor, 35V, X5R	0805	Murata	GRM21BR6YA106KE43L
2	C11, C15	2.2μF	Capacitor, 25V, X7R	0805	Murata	GCM21BR71E225KA73L
8	C13, C21, C23, C24, C25, C26, C27, C28	NC				
2	C17,C18	NC				
6	L2, L3, L4, L5, L6, L7	NC				
2	R1, R2	10kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710KL
3	R3, R4, R10	NC	Film resistor, 5%	0603		
4	R5, R6, R7, R8	10kΩ	Film resistor, 5%	0603	Yageo	RC0603JR-0710K
2	R9, R11	0Ω	Film resistor, 1%	0603	Yageo	RC0603FR-070RL
1	R12	0Ω	Film resistor, 1%	0402	Yageo	RC0402FR-070RL
1	CN1	8.6mmx 2.5mmx 6.8mm	Connector, USB Type-C	DIP	Any	
4	CN2, CN3, CN4, CN5	2.54mm	Connector, 1x3, 180°C, 2.54mm, jumper	DIP	Any	
16	CN6, CN7, CN8, CN9, CN10, CN11, CN12, CN13, CN14, CN16, CN40, CN41, CN42, CN43, CN44, CN45	1.0mm	Connector	DIP	Any	
10	CN18, CN19, CN20, CN21, CN22, CN23, CN24 ,CN25, CN26, CN27,	2.54mm	Connector; test point; yellow	DIP	Any	

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EVL2772-C-00A BILL OF MATERIALS *(continued)*

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
9	CN31, CN32, CN33, CN34, CN35, CN36, CN37, CN38, CN39	2.54mm	Connector	DIP	Any	
1	SW1	4mmx10mm	Push-switching button	Any	Any	
1	U1	MP2772	Switching charger	WLCSP-30	MPS	MP2772GC
1	L1	1.5μH	Inductor, 35mΩ, 3.4A	SMD	MPS	MPL-AY3020-1R5

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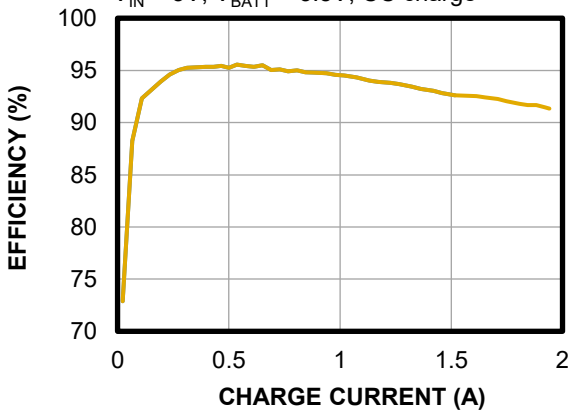
EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 5V, V_{BATT} = 3.8V, T_A = 25°C, unless otherwise noted.

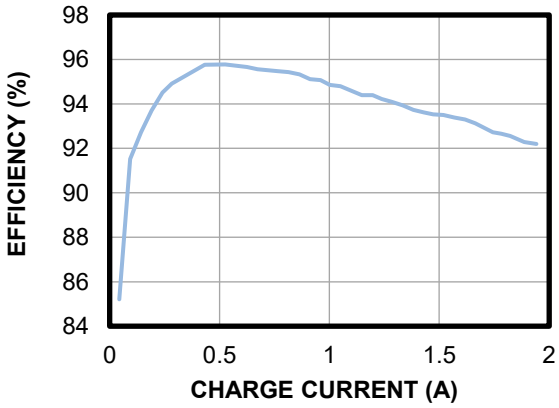
Efficiency vs. Charge Current

V_{IN} = 5V, V_{BATT} = 3.8V, CC charge



Efficiency vs. Charge Current

V_{IN} = 5V, V_{BATT} = 4.2V, CV charge

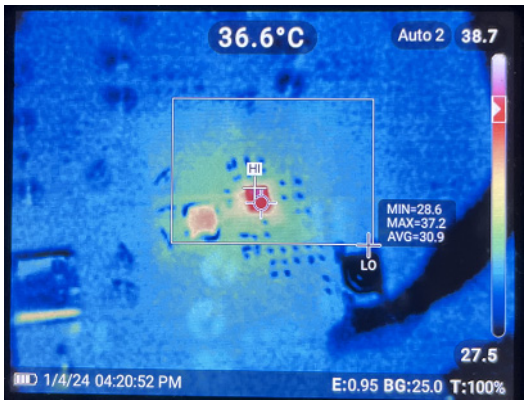


Thermal Performance

Charge mode, V_{IN} = 5V, V_{BATT} = 3.8V, I_{BATT} = 2A, no forced airflow, T_{CASE} = 44.9°C

Thermal Performance

Boost mode; V_{BST} = 5V, V_{BATT} = 3.8V, I_{BST} = 1A (short two LDSW outputs together), no forced airflow, T_{CASE} = 38.7°C



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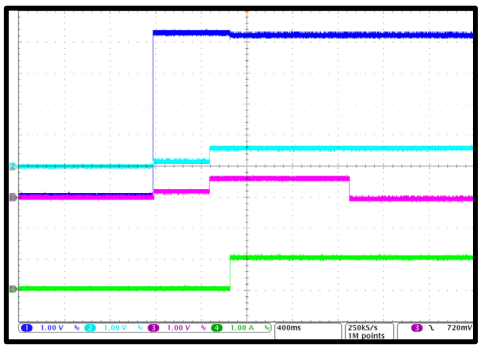
EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 5V, V_{BATT} = full range, I^2C-controlled, I_{CC} = 0.5 to 2A, I_{IN_LIM} = 0.5A, V_{IN_MIN} = 4.5V, L = 1.5µH (DCR = 35mΩ), T_A = 25°C, unless otherwise noted.

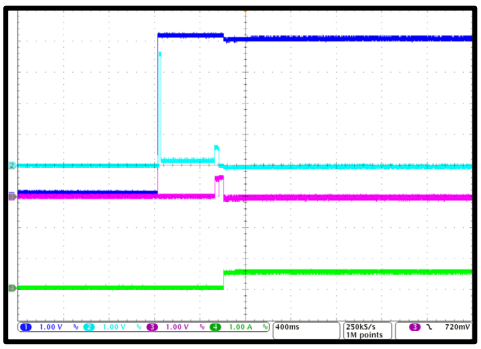
Adapter Plugged In

I_{CC} = 1A, V_{BATT} = 3.8V, DCP adapter inserted



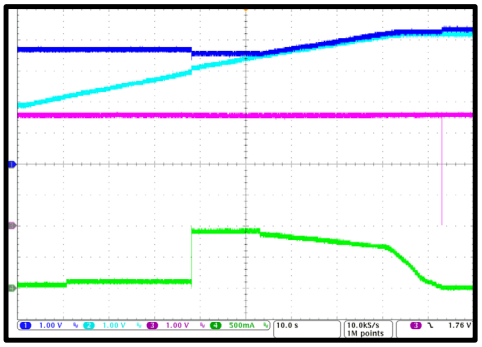
Adapter Plugged In

I_{CC} = 1A, V_{BATT} = 3.8V, SDP USB inserted



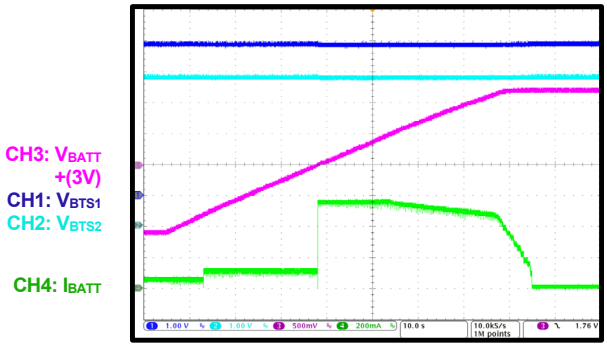
Battery Charge Profile

I_{IN_LIM} = 1.5A, I_{CC} = 1A, QR and QL are off



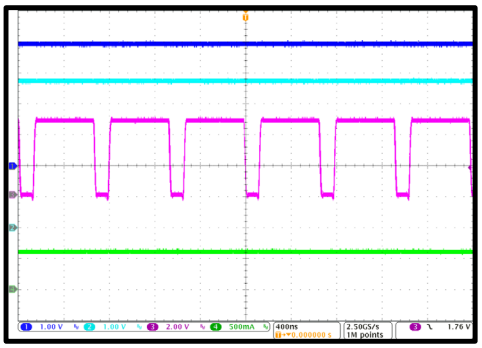
Battery Charge Profile

I_{IN_LIM} = 1.5A, I_{CC} = 1A, I_{BST1} = I_{BST2} = 0.5A



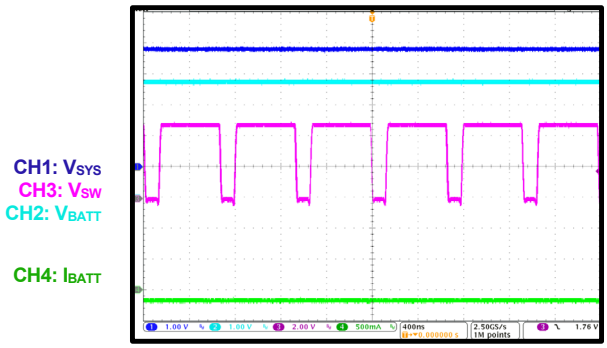
Charge Steady State

V_{BATT} = 3.8V, I_{IN_LIM} = 1.5A, I_{CC} = 1A, I_{BST1} + I_{BST2} = 1A



Charge Steady State

V_{BATT} = 3.8V, I_{IN_LIM} = 1.5A, I_{CC} = 1A, I_{SYS} = 2A



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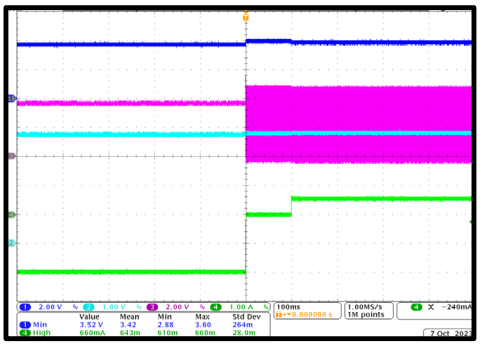
EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 5V, V_{BATT} = full range, I^2C-controlled, I_{CC} = 0.5 to 2A, I_{IN_LIM} = 0.5A, V_{IN_MIN} = 4.5V, L = 1.5µH (DCR = 35mΩ), T_A = 25°C, unless otherwise noted.

Buck On

V_{BATT} = 3.8V, I_{IN_LIM} = 3.2A, I_{CC} = 0.5A, I_{SYS} = 2A

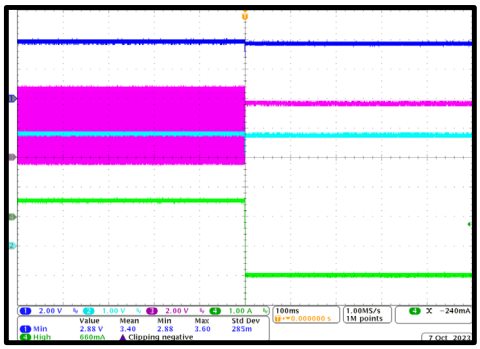
CH1: V_{SYS}
CH3: V_{SW}
CH4: I_{BATT}
CH2: V_{BATT}



Buck Off

V_{BATT} = 3.8V, IIN_LIM = 3.2A, I_{CC} = 0.5A, I_{SYS} = 2A

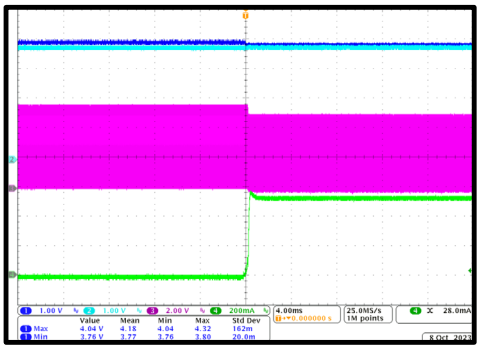
CH1: V_{SYS}
CH3: V_{SW}
CH4: I_{BATT}
CH2: V_{BATT}



Charge On

V_{BATT} = 3.8V, I_{IN_LIM} = 3.2A, I_{CC} = 0.5A, I_{SYS} = 0A

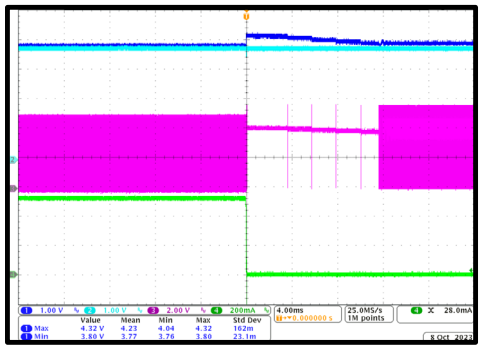
CH1: V_{SYS}
CH2: V_{BATT}
CH3: V_{SW}
CH4: I_{BATT}



Charge Off

V_{BATT} = 3.8V, I_{IN_LIM} = 3.2A, I_{CC} = 0.5A, I_{SYS} = 0A

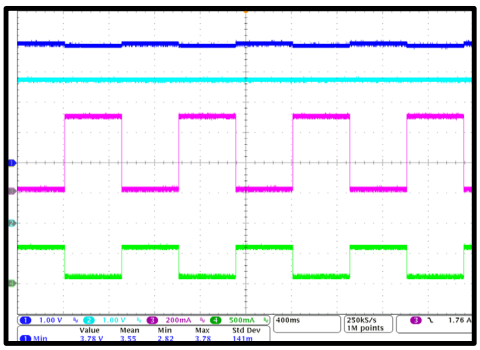
CH1: V_{SYS}
CH2: V_{BATT}
CH3: V_{SW}
CH4: I_{BATT}



SYS Load Transient Response

V_{BATT} = 3.8V, I_{IN_LIM} = 1.5A, I_{CC} = 1A, I_{SYS} = 0A to 0.5A; I_{BST1} + I_{BST2} = 1A

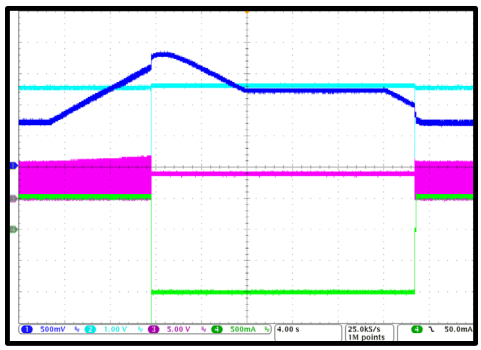
CH1: V_{SYS}
CH3: I_{SYS}
CH2: V_{BST}
CH4: I_{BATT}



V_{IN} OVP

V_{BATT} = 3.8V, I_{IN_LIM} = 3.2A, I_{CC} = 0.5A, I_{SYS} = 1A

CH1: V_{IN}
CH2: INT
CH3: V_{SW}
CH4: I_{BATT}



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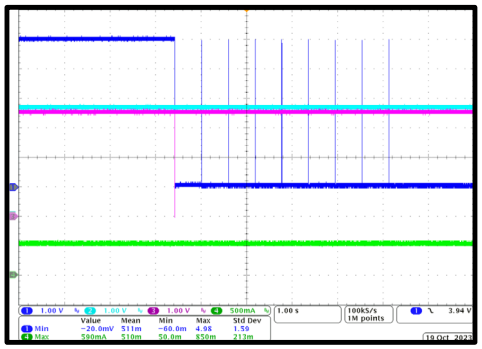
EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 5V, V_{BATT} = full range, I^2C-controlled, I_{CC} = 0.5 to 2A, I_{IN_LIM} = 0.5A, V_{IN_MIN} = 4.5V, L = 1.5µH (DCR = 35mΩ), T_A = 25°C, unless otherwise noted.

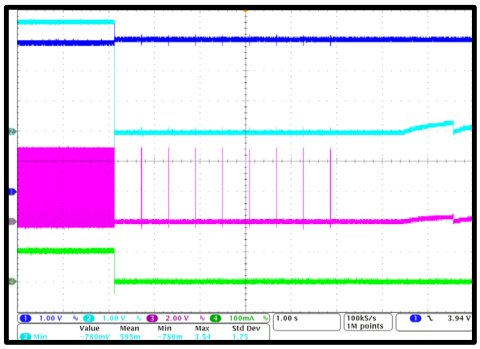
LDSW Over-Current

V_{BATT} = 3.3V, I_{IN_LIM} = 1.5A, I_{CC} = 1A, I_{SYS} = 0A, LDSW_OCP = 600mA, I_{BST1} = 0.9A



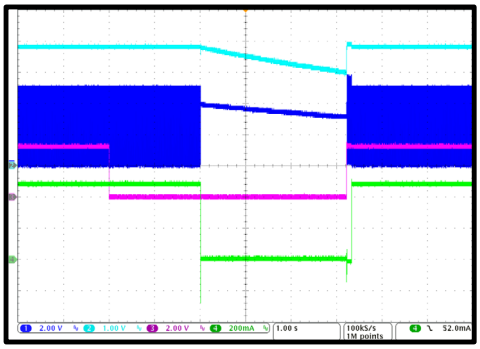
SYS Short Protection

V_{BATT} = 2.5V, I_{IN_LIM} = 3.2A, I_{PRE} = 100mA, I_{SYS} = 2A



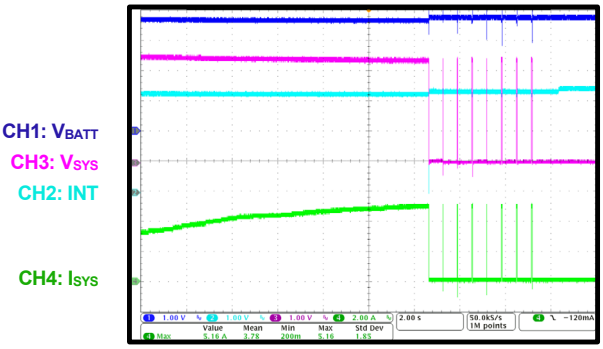
SYS Auto-Reset Mode

V_{BATT} = 3.8V; I_{IN_LIM} = 1.5A, I_{CC} = 0.5A, I_{SYS} = 0A, T_SYS_LOW = 0.5s



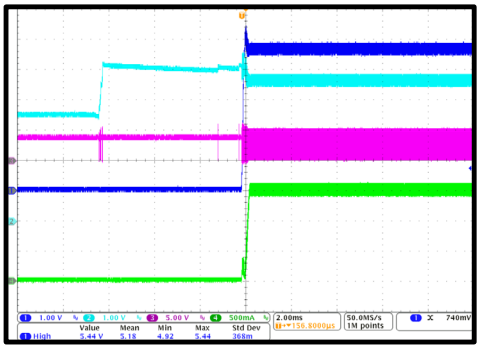
Idle State- Battery Discharging OCP

V_{BATT} = 3.7V



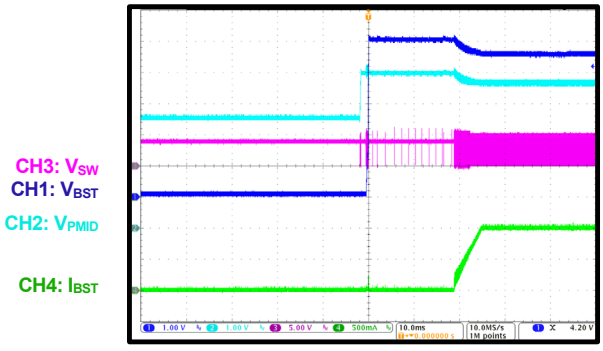
Boost and OTG Mode On

V_{BATT} = 3.8V, V_{BOOST} = 5V, I_{OTG_LIM} = 1.5A, I_{OTG} = 1.5A



Boost and LDSW On

V_{BATT} = 3.8V, V_{BOOST} = 5V, I_{BST1} + I_{BST2} = 1A



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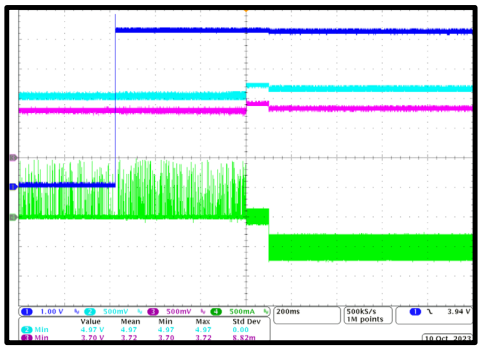
EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 5V, V_{BATT} = full range, I^2C-controlled, I_{CC} = 0.5 to 2A, I_{IN_LIM} = 0.5A, V_{IN_MIN} = 4.5V, L = 1.5µH (DCR = 35mΩ), T_A = 25°C, unless otherwise noted.

Boost to Buck Transient

V_{BATT} = 3.8V, V_{BOOST} = 5V, V_{IN} = 5V,
insert VIN during boost operation

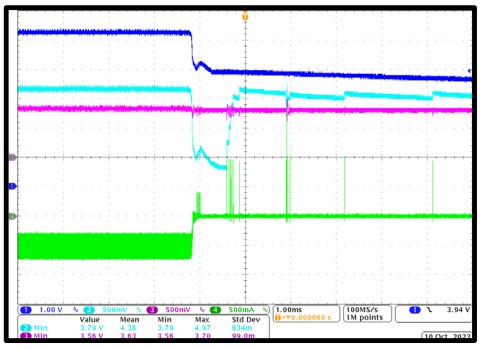
CH2: V_{PMID} + 3V
CH3: V_{SYS} + 3V
CH1: V_{IN}
CH4: I_L



Buck to Boost Transient

V_{BATT} = 3.8V, V_{BOOST} = 5V, V_{IN} = 5V,
enable boost function before removing VIN

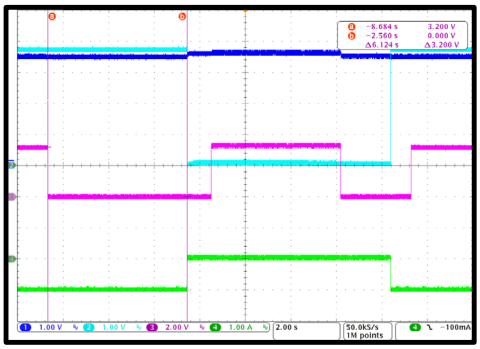
CH2: V_{PMID} + 3V
CH3: V_{SYS} + 3V
CH1: V_{IN}
CH4: I_L



Enter/Exit Shipping Mode by /DISC

V_{BATT} = 3.8V, T_DISC = 2s,
BATTFET_DLY = 4s, T_WAKE = 2s

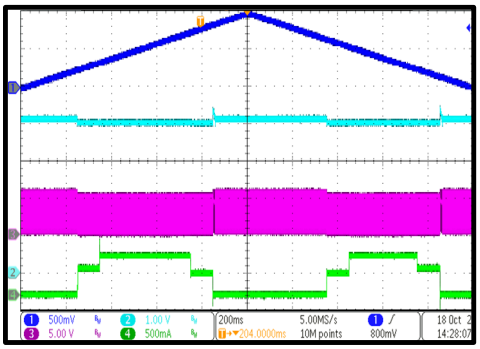
CH1: V_{CC}
CH2: V_{SYS}
CH3: /DISC
CH4: I_{BATT}



NTC JEITA Protection

V_{BATT} = 3.95V, I_{CC} = 0.5A,
JEITA_ISET = 50%, JEITA_VSET = -250mV

CH1: VNTC
CH3: V_{SW}
CH2: V_{SYS}
CH4: I_{BATT}



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PCB LAYOUT

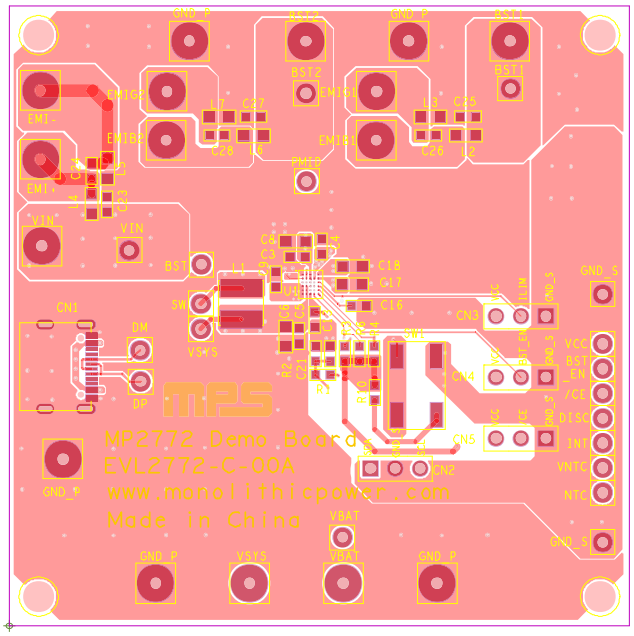

Figure 20: Top Silk and Top Layer

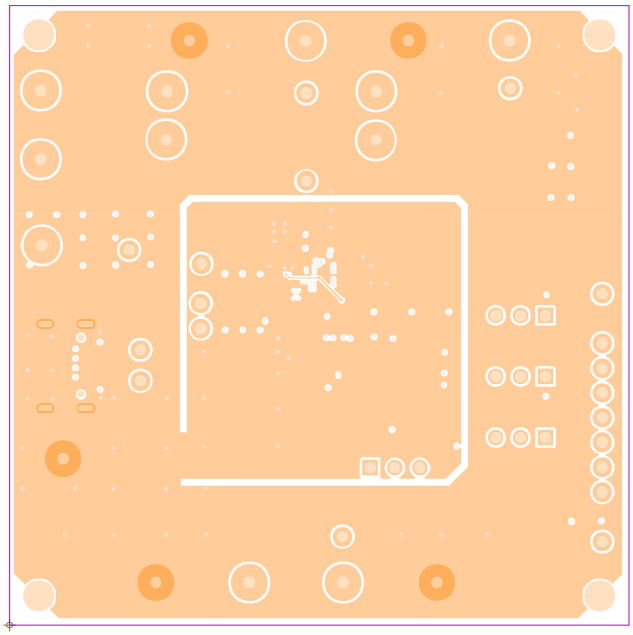

Figure 21: Mid-Layer 1

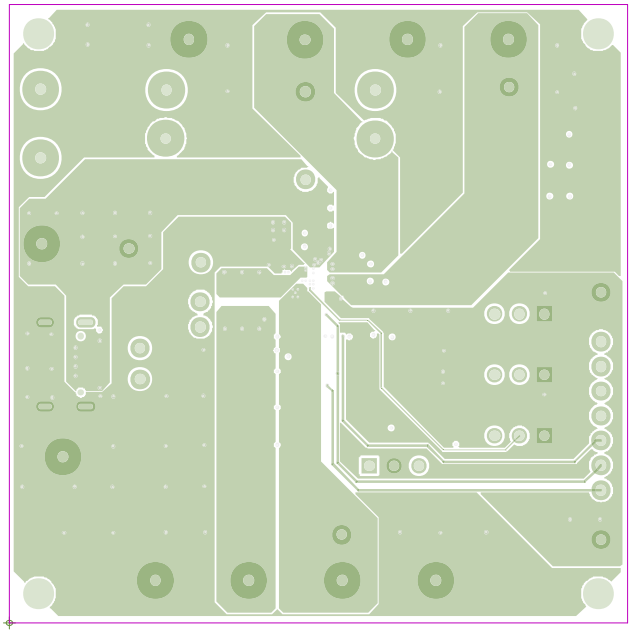

Figure 22: Mid-Layer 2

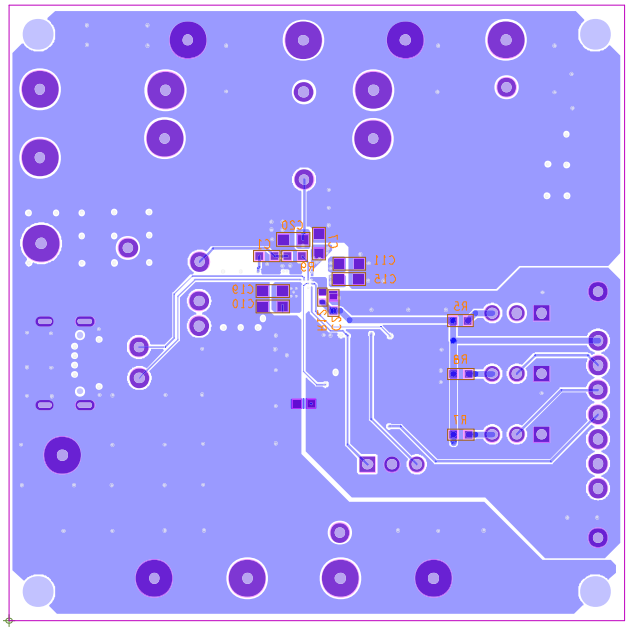

Figure 23: Bottom Layer

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	10/1/2024	Initial Release	-

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