



EV8040-N-00A

Full-Bridge or Single-Ended Audio Amplifier Evaluation Board

DESCRIPTION

The EV8040-N-00A is an evaluation board designed to demonstrate the capabilities of MPS's MP8040. It can be configured as a stereo single-ended amplifier or a full-bridge mono amplifier.

The MP8040 is a general purpose, high-frequency, half-bridge power driver. It integrates both top and bottom N-channel MOSFET power switches. It interfaces with standard logic signals, and is available in small, 8-lead SOIC package.

ELECTRICAL SPECIFICATION

| Parameter | Symbol | Value | Units |
|----------------------|----------------|-----------|-------|
| Input supply voltage | V_{IN} | 7.5 to 24 | V |
| Peak output current | $I_{PEAK-MAX}$ | 9 | A |
| RMS output current | $I_{RMS-MAX}$ | 4.25 | A |

FEATURES

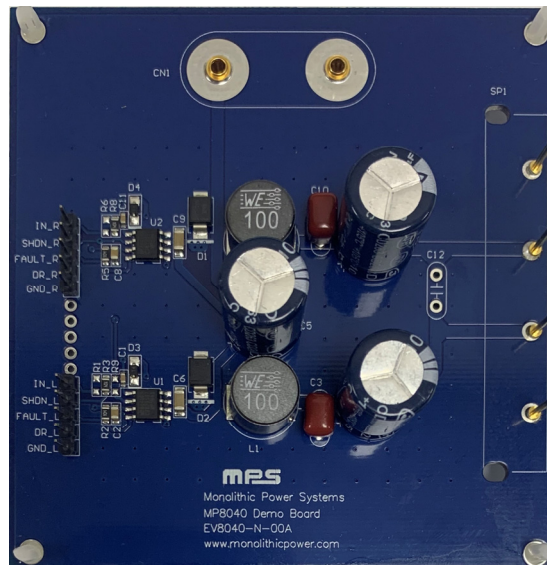
- Up to 1.2MHz Switching Frequency
- Protected Integrated Power 0.1Ω Switches
 - Designed Switch Dead time of 30ns
 - All Switches Current Limited
 - Internal Under-Voltage Protection (UVP)
 - Internal Thermal Protection
- 2.5μA Standby Mode
- Fault Indicator Output

APPLICATIONS

- Full or Half-Bridge DC/DC Switching Regulators
- Class-D Audio Drivers
- Motor Drivers

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EV8040-N-00A EVALUATION BOARD



(LxWxH) 8.89cmx9.14cmx3cm

| Board Number | MPS IC Number |
|--------------|---------------|
| EV8040-N-00A | MP8040DN |

QUICK START GUIDE

1. The EV8040-N-00A can be configured as a stereo single-ended audio amplifier.
2. To configure the board as a full-bridge circuit, short R4, R7, and R9. Then remove C4 and C7. Lastly, use a 0.47 μ F capacitor for C12.
3. Connect the audio inputs to the IN pins (see Figure 1).
4. Connect speakers to pins 1, 2, 3, and 4 for single-ended configuration (see Figure 1). Use pins 2 and 3 to form a bridged circuit.
5. Connect the power supply to the VIN terminals (see Figure 1).
6. SHDN enables/disables the MP8040. Drive SHDN low to turn the MP8040 on; drive SHDN high to turn the device off. If SHDN is not used, connect it to GND.
7. A low output at FLT indicates that the MP8040 has detected a fault, and the device shuts down as a result.
8. The DR pin is an optional, 5V fixed-voltage output capable of driving a 1mA load for external circuitry.

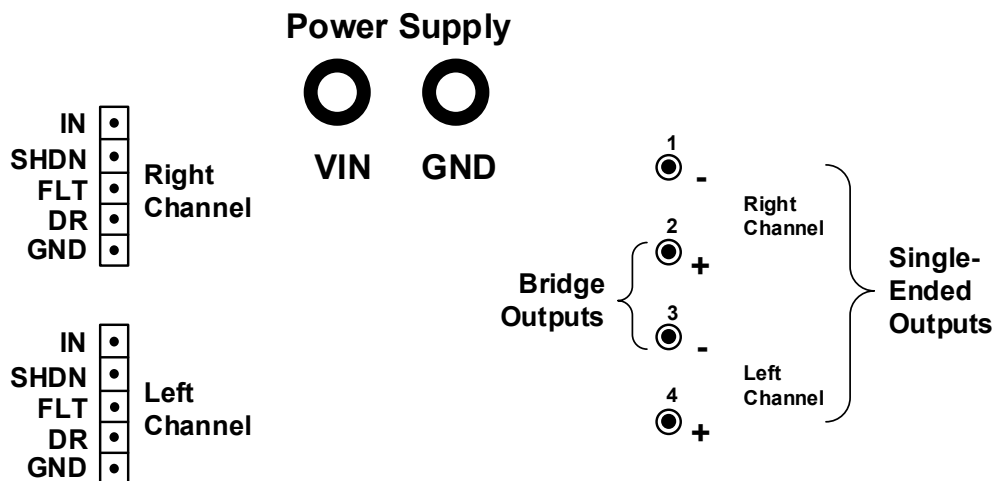
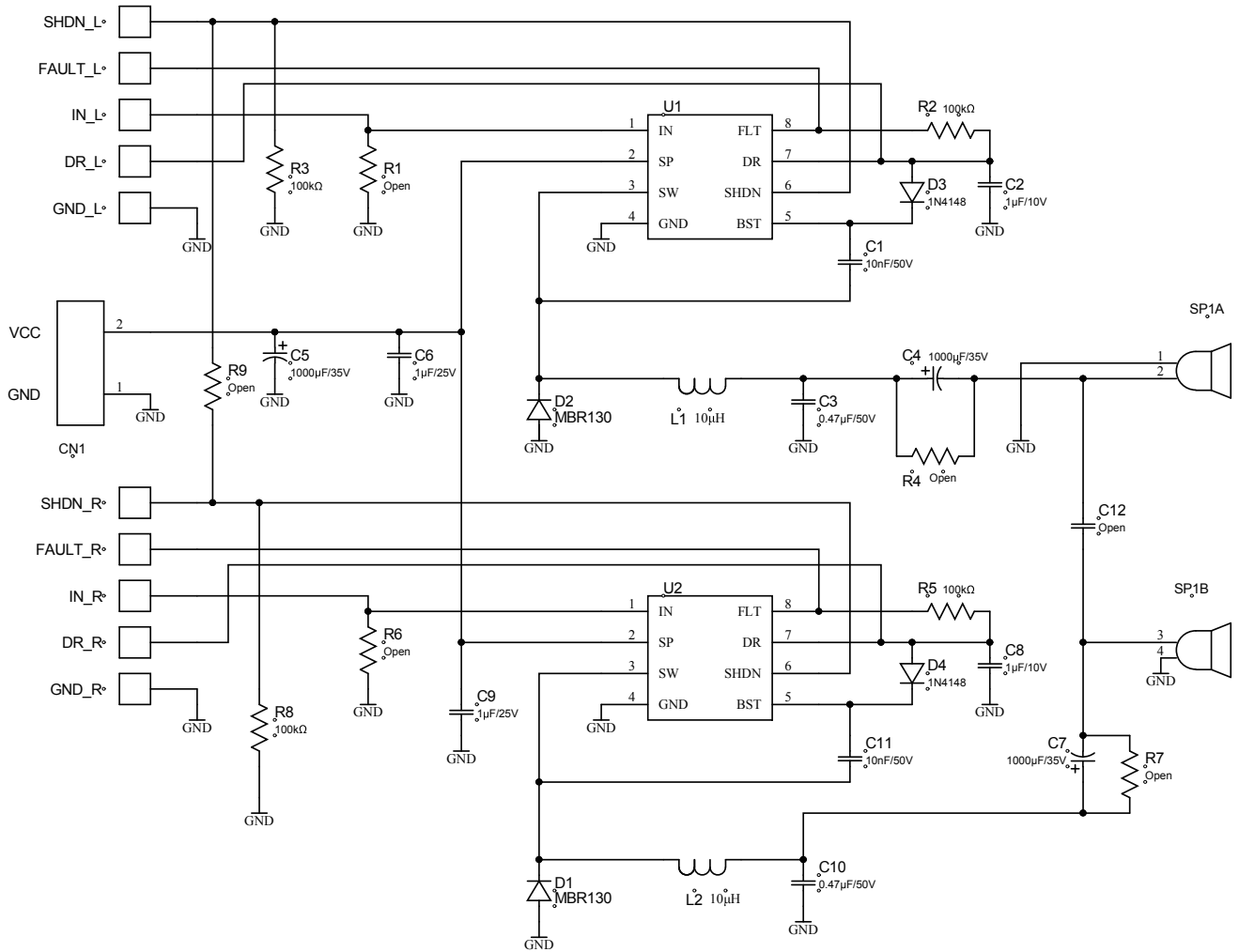


Figure 1: Top-Side Evaluation Board Diagram

EVALUATION BOARD SCHEMATIC


EV8040-N-00A BILL OF MATERIALS

| Qty | Ref | Value | Description | Package | Manufacturer | Manufacturer P/N |
|-----|---|-----------------|----------------------------------|-----------|-------------------|---------------------|
| 2 | U1, U2 | 24V, 4.25A | PWM power driver | SOIC-8N | MPS | MP8040DN |
| 3 | C4, C5, C7 | 1000 μ F | Electrolytic capacitor, 35V, DIP | 12.5 x 20 | Jiang Hai | CD263-35V1000 |
| 3 | C3, C10 | 0.47 μ F | Film capacitor, 50V | 5.08 | Panasonic | ECQV1H474JL |
| 2 | C1, C11 | 10nF | Ceramic capacitor, 50V, NPO/X7R | 0603 | murata | GRM188R71H103KA01D |
| 2 | C2, C8 | 1 μ F | Ceramic capacitor, 10V, X7R | 0805 | murata | GRM21BR71A105KA01L |
| 2 | C6, C9 | 1 μ F | Ceramic capacitor, 25V, X7R | 1206 | murata | GRM31MR71E105KA01 |
| 2 | L1, L2 | 10 μ H | 10 μ H, 5A, inductor | DIP | wurth | 7447471100 |
| 4 | R2, R3, R5, R8 | 100k Ω | 5% resistor | 0805 | Yageo | RC0805JR-07100KL |
| 2 | D1, D2 | 1A, 30V | 1A, 30V, Schottky rectifier | SMB | On Semiconductor | MBRS130T3G |
| 2 | D3, D4 | 300mA, 100V | 300mA, 100V, rectifier | SOD123 | Diodes Inc. | 1N4148WS |
| 10 | IN_L, SHDN_L, FAULT_L, DR_L, GND_L, IN_R, SHDN_R, FAULT_R, DR_R, GND_R | 2.54mm | 2.54mm Connector | DIP | Electrical Market | 61304011121 |
| 4 | SP1 | Φ = 1mm | 1mm connector | DIP | Electrical Market | Φ = 1mm Needle |
| 2 | CN1 | Φ = 2mm | 2mm connector | DIP | Electrical Market | Φ = 2mm Needle |

PCB LAYOUT

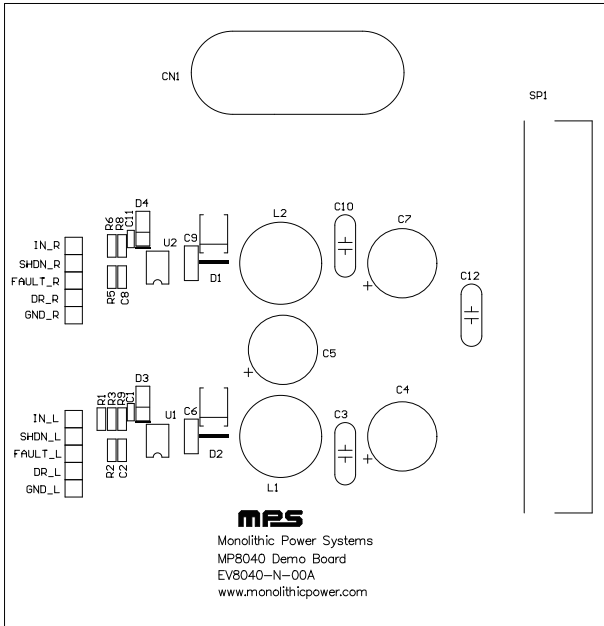


Figure 2: Top Silk Layer

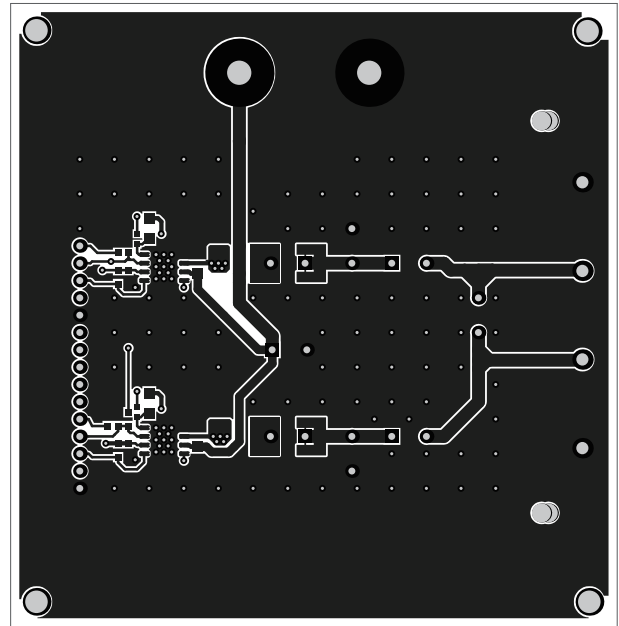


Figure 3: Top Layer

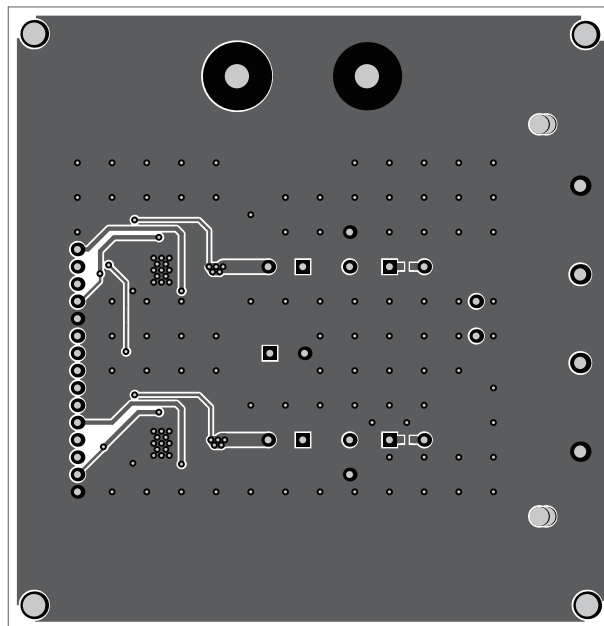


Figure 4: Bottom Layer

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