EV2790-0000/0002-FP-00A

7-Cell to 10-Cell, High-Accuracy I²C/SPI Monitoring and Protection IC with Coulomb Counting Evaluation Board

END OF LIFE, REFER TO EV2790-0000-FP-00B

DESCRIPTION

The EV2790-0000/0002-FP-00A is an evaluation board designed to demonstrate the capabilities of the MP2790, a complete analog front-end (AFE) monitoring and protection IC. The MP2790 supports 7-cell to 10-cell series battery packs with outstanding measurement accuracy and a complete set of protection features.

The MP2790 measures each cell's voltage, while also synchronously the measuring charge and discharge currents via an external current-sense resistor. The MP2790 includes high-side MOSFET (HS-FET) drivers for charge and discharge control. It also measures die temperature and cell temperature via 4 negative temperature coefficient (NTC) thermistor inputs. The MP2790 contains internal passive balancing MOSFETs capable of driving up to 58mA, and is also capable of driving external balancing transistors for higher currents.

The discharge (DSCHG) MOSFET driver includes configurable soft start (SS), which provides controlled start-up and eliminates the need for an external pre-charge circuit. The MOSFET drivers also incorporate over-current protection (OCP), short-circuit protection (SCP), battery under-voltage protection (UVP), battery over-voltage protection (OVP), and high/low-temperature protection. All of these protections have configurable thresholds.

The EV2790-0000/0002-FP-00A combines the MP2790 with power MOSFETs and a current-sense resistor to support up to 70A of charge and discharge current. The evaluation board also includes placeholders to add external transistors for higher balancing current, if needed.

The EV2790-0000/0002-FP-00A can be evaluated by connecting to an 18V to 55V battery pack (or simulated battery pack). The evaluation board requires a computer with an available USB port and the MPS evaluation software installed. An MPS USB-to-I²C/SPI communication interface allows the PC to interface with the MP2790 communication port: The EV2790-0000-FP-00A includes the MP2790DFP-0000 and supports I²C communication. The EV2790-0002-FP-00A includes the MP2790DFP-0002 and supports SPI communication.

The MP2790 is available in a TQFP-48 (7mmx7mm) package.

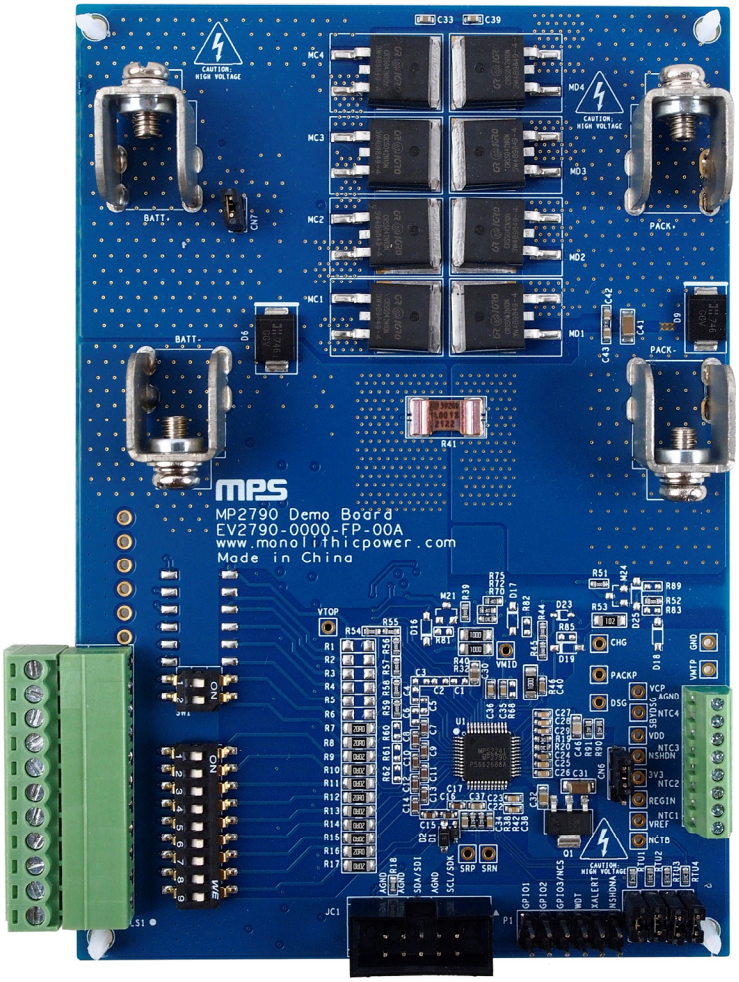
PERFORMANCE SUMMARY

Specifications are at T_A = -40°C to +85°C, unless otherwise noted.

Parameters	Conditions	Value
Battery pack voltage range		18V to 55V
Cell voltage range		0V to 5V
Continuous charge current		0A to 70A
Continuous discharge current		0A to 70A
Internal balancing current	V_{BATT} = 4V, T_A = 25°C	58mA
Supported cells in series		7 to 10

END OF LIFE, REFER TO EV2790-0000-FP-00B

EVALUATION BOARD



LxWxH (14cmx9.6cmx1.5cm)

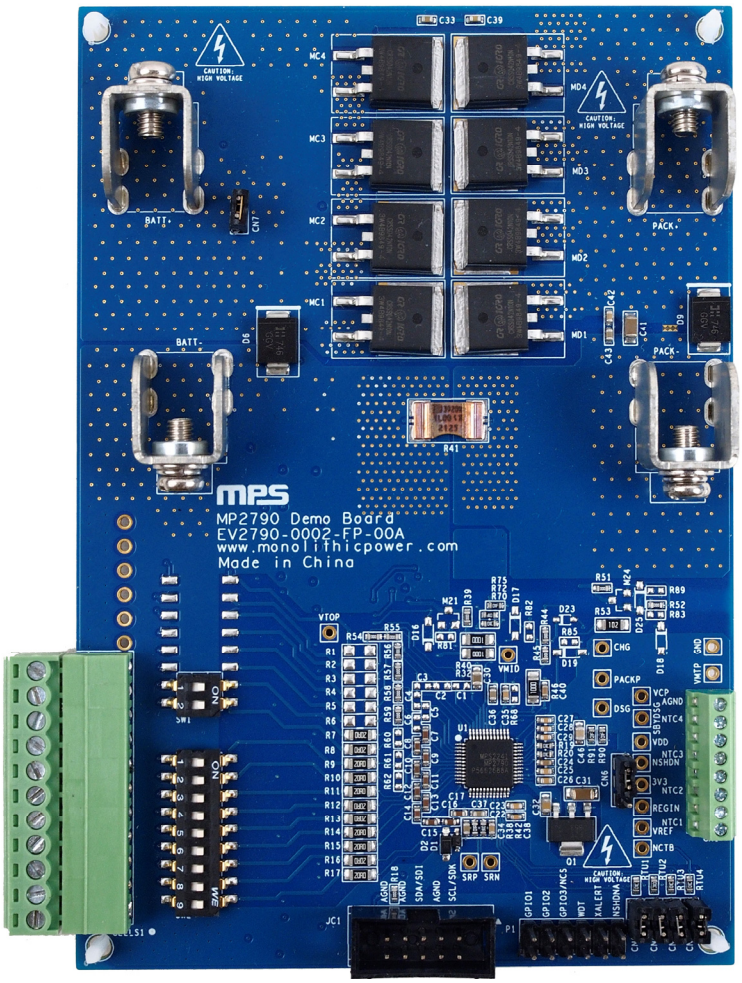
Board Number	MPS IC Number
EV2790-0000-FP-00A	MP2790DFP-0000 (1)

Note:

1) "0000" is the register setting option that supports I²C communication. For custom options, contact an MPS FAE to obtain a "xxxx" value.

END OF LIFE, REFER TO EV2790-0000-FP-00B

EVALUATION BOARD



LxWxH (14cmx9.6cmx1.5cm)

Board Number	MPS IC Number
EV2790-0002-FP-00A	MP2790DFP-0002 (2)

Note:

2) "0002" is the register setting option that supports SPI communication. For custom options, contact an MPS FAE to obtain a "xxxx" value.

QUICK START GUIDE

The EV2790-0000/0002-FP-00A is designed to evaluate the MP2790, and can be configured to support 7-cell to 10-cell series connections. The evaluation board incorporates the MP2790, power MOSFETs, current-sense resistor, and other components. The EV2790-0000/0002-FP-00A includes placeholders to add external MOSFETs and balancing resistors to support >58mA of balancing current, if needed. The board includes protections with configurable thresholds for the following conditions: over-current (OC), short-circuit (SC), under-voltage (UV), over-voltage (OV), unbalanced cell, and high/low temperature.

Evaluation Board Set-Up:

1. To use the evaluation board, the following is required:
   a. Computer with at least one USB port
   b. USB cable
   c. USB-to-I²C communication interface (EVKT-USBI2C-02, see Figure 1) or USB-to-SPI communication interface (EVKT-USBSPI-00, see Figure 2)
   d. The MP2790 Programming graphic user interface (GUI) (3)

Note:

3) The GUI software can be downloaded from the MPS website.

Figure 1: USB-to-I²C Communication Interface

Figure 2: USB-to-SPI Communication Interface

2. To install the software, click on the programming tool file “MP2790.exe”, then open the software. The software is supported by Windows 7, or later.

To set up the board using a cell simulator shunt (i.e. without a real battery pack) (see Figure 3 and Figure 4 on page 5), follow the steps below:

   a. Short CN7, and turn the SW1 and SW2 channels on.
   b. Apply a DC power supply between BATT+ and BATT-.

c. Adjust the power supply to about 37.5V/1A.

d. If evaluating the MP2790DFP-0000, connect the USB-to-I²C communication interface to JC1 (carefully consider where SCL and SDA are positioned). If evaluating the MP2790DFP-0002, connect the USB-to-SPI communication interface to JC1 (carefully consider where NCS, SCK, SDO, and SDI are positioned).

Figure 3 shows the test set-up for the MP2790DFP-0000 using a cell simulator shunt.

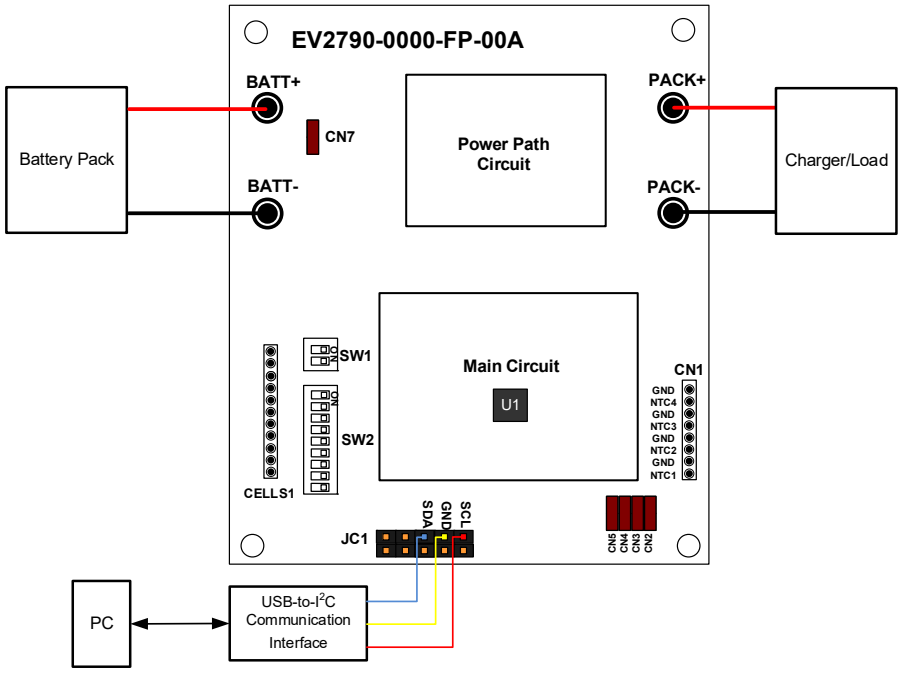


Figure 3: Test Set-Up for the MP2790DFP-0000 Using a Cell Simulator Shunt

Figure 4 shows the test set-up for the MP2790DFP-0002 using a cell simulator shunt.

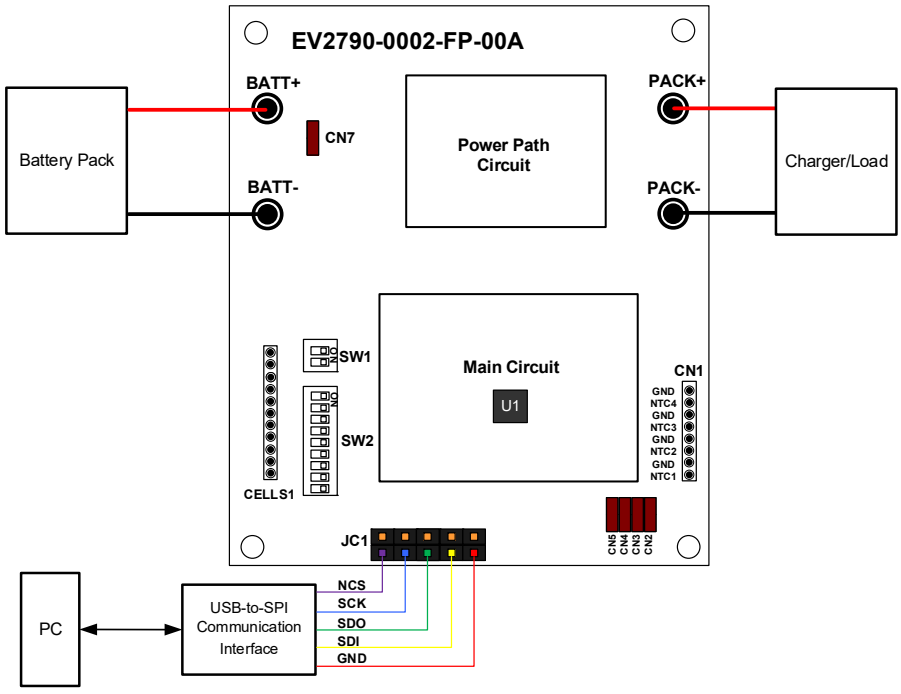


Figure 4: Test Set-Up for the MP2790DFP-0002 Using a Cell Simulator Shunt

3. The evaluation board has 10 cells in series by default. To evaluate the MP2790 at a lower series number using a cell simulator shunt, short the unused cell channels. Figure 5 shows an 8-cell series connection using a cell simulator shunt.

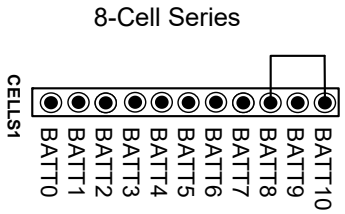


Figure 5: 8-Cell Series Connection

The DC power supply voltage between BATT+ and BATT- should be reduced, depending on the number of cells in series.

The open-wire detection and cell-balancing functions cannot be tested using a cell simulator shunt. A real battery pack must be used to evaluate these functions.

To set up the board using a battery pack (see Figure 7 on page 7, and Figure 8 on page 8), follow the steps below:

4. Remove the CN7 jumper, and turn the SW1 and SW2 channels off.
5. If the application has less than 10 cells in series, short all unused cell channels to the practical maximum cell channel using 0Ω resistors. For example, if using an 8-cell series battery pack, add 0Ω resistors to R60 and R61. If the application has 10 cells in series, skip this step.
6. Connect the cell terminals (CELLS1) to each cell sensing point. If there are <10 cells in the battery pack, float the connectors of the higher channels.
7. Connect the battery terminals to:
   a. Positive (+): BATT+
   b. Negative (-): BATT-
8. The EV2790-0000/0002-FP-00A has a bypass P-channel MOSFET. In safe mode, turn the P-channel MOSFET on using GPIO2 to power PACK with low power consumption. When the PACK voltage (V_{PACK}) is below (V_{TOP} - 2V), the P-channel MOSFET current capacity is about 25mA. When V_{PACK} > (V_{TOP} - 2V), the P-channel MOSFET can bypass about a 1A current. If this function is not used, set the GPIO2 output low. It is also recommended to use GPIOHV1 to control the bypass P-channel MOSFET.
9. Remove CN2, CN3, CN4, and CN5. Connect the temperature sensors to support up to four negative temperature coefficient (NTC) thermistors.
10. Connect the charger terminals to:
    a. Positive (+): PACK+
    b. Negative (-): PACK-
11. If evaluating the MP2790DFP-0000, connect SDA, SCL, and GND to the USB-to-I²C communication interface. If evaluating the MP2790DFP-0002, connect NCS, SCK, SDO, and SDI for the USB-to-SPI communication interface. Carefully consider where SCL and SDA are positioned.
12. Connect the USB cable to the PC, turn on the computer, and launch the MP2790 GUI evaluation software (Figure 6 on page 7).

If the evaluation board is connected properly, “MP2790 Demo board: Connected” will be shown in the bottom left corner of the GUI’s main window. If the evaluation board is not connected properly, “MP2790 Demo board: Disconnected!” will be shown.

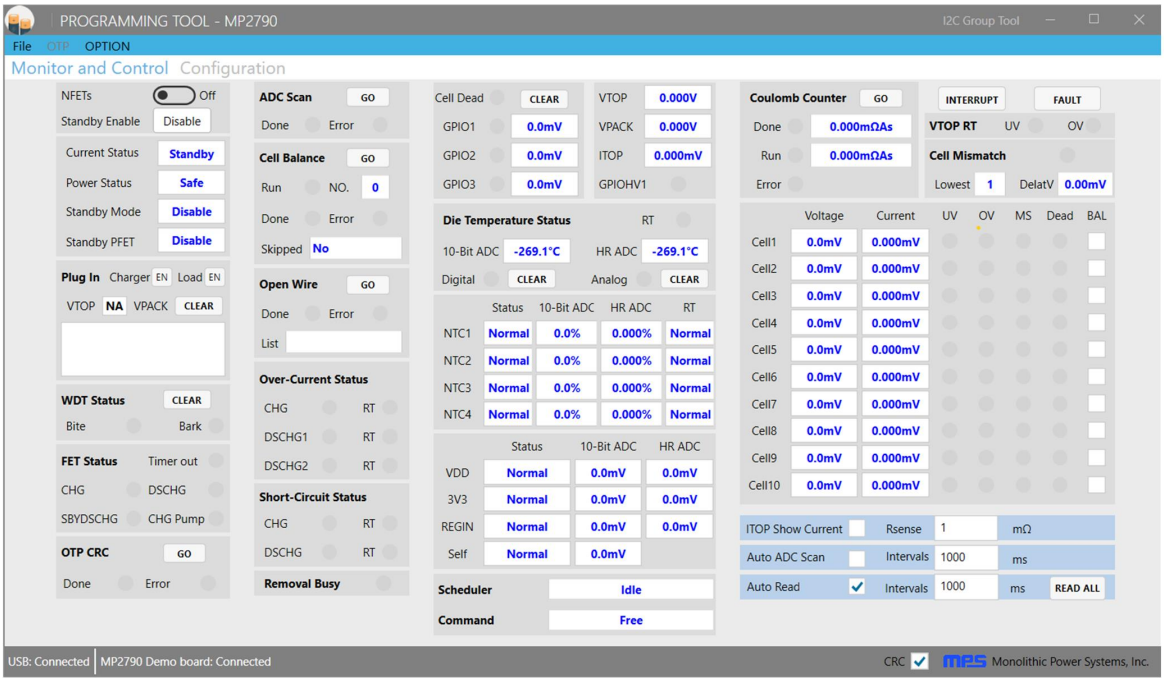


Figure 6: MP2790 Programming GUI

Figure 7 shows the test set-up for the MP2790DFP-0000 using a battery pack.

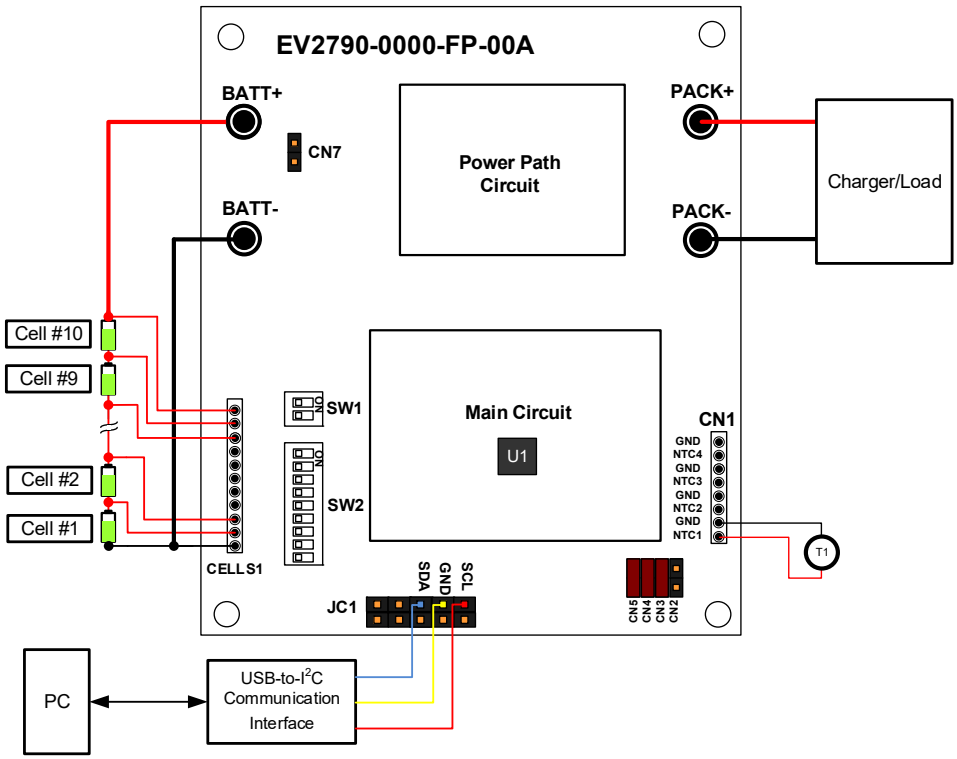


Figure 7: Test Set-Up for the MP2790DFP-0000 with a Battery Pack

Figure 8 shows the test set-up for the MP2790DFP-0002 using a battery pack.

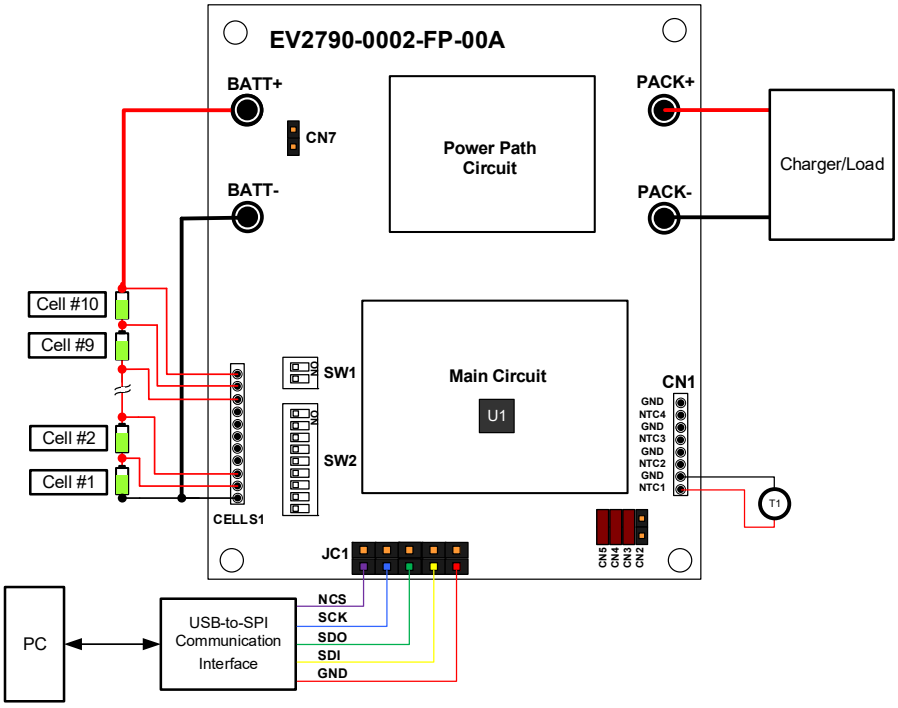


Figure 8: Test Set-Up for the MP2790DFP-0002 with a Battery Pack

PROCEDURE

1. Ensure that all the connections are successful (e.g. between the USB-to-I²C/SPI communication interface and the EV2790-0000/0002-FP-00A).
2. Click the “Configuration” tab to view the configurations (see Figure 9). The software should automatically read all the configurations. Items with a lock symbol can be configured as read-only.

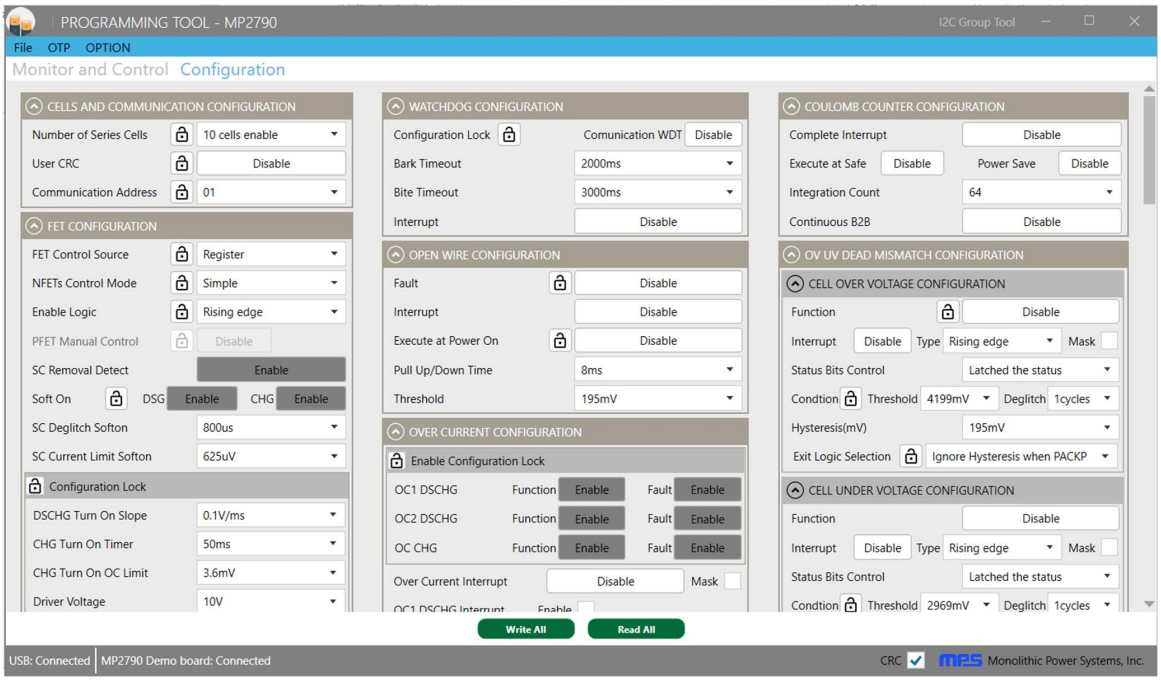


Figure 9: MP2790 Configurations

3. Configure the protection thresholds, enable all relevant functions, and enable the fault protections.
4. Click the “Write All” button to write the configurations to the register.
5. Click the “Monitor and Control” tabs to switch the view.
6. Turn on the N-channel MOSFETs.
7. Click the “Read All” button. The MOSFET status should be displayed in green for CHG, DSCHG, and CHG Pump. The power status should be set to active automatically.
8. Click the “Go” button for the analog-to-digital converter (ADC) scan. The ADC result should be updated in the corresponding register.
9. Click the “Read All” button. The updated values should be displayed in the GUI. If the “Auto Read” checkbox is selected, it is not required to click the “Read All” button.
10. Figure 10 shows how to configure the cell and communication parameters.

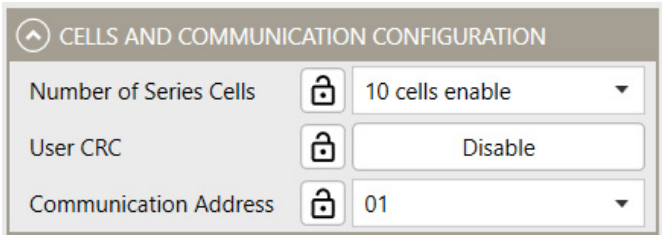


Figure 10: Cell and Communication Configuration

a. Number of Series Cells: The number of cells in series can be set between 7 and 10.

b. User CRC: To enable cyclic redundancy check (CRC), select the “CRC” box at the bottom right of the GUI window. Otherwise, the value cannot be written to the register.

c. Communication Address: The default slave address is 01h, and the configurable communication address range is between 00h and 7Fh. After configuring this value, the new address should be used for the next communication. For devices with different “-xxxx” suffixes, the default address may be different. The GUI scans the address automatically. This function can be disabled by not selecting the “Monitor chip connection” box under the “Option” tab.

11. Figure 11 shows how to configure the MOSFET parameters.

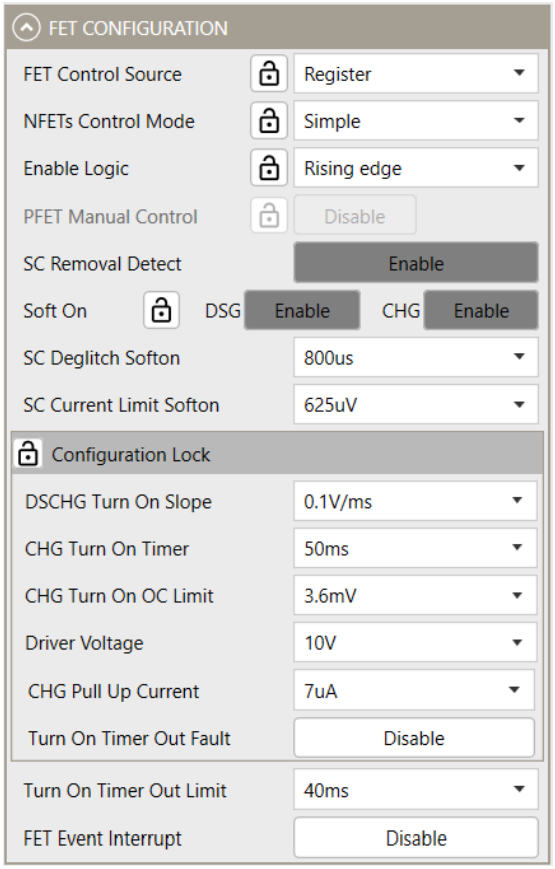


Figure 11: MOSFET Configuration

a. FET Control Source: The MOSFET control source can be set to GIPO control or register control.

b. NFETs Control Mode: The N-channel MOSFETs control mode can be set to simple or direct mode. In direct mode with GPIO control, GPIO1 controls the discharge (DSCHG) MOSFET, and GPIO2 controls the charge (CHG) MOSFET.

c. Enable Logic: The enable logic can be set to rising edge active or level active.

d. SC Removal Detect: Enables the SC detection sequence that occurs before the DSCHG MOSFET turns on.

e. SC Deglitch Soft on and SC Current Limit Soft on: When enabled, the DSCHG MOSFET is protected from inrush current while charging a large capacitive load. These two settings protect the DSCHG MOSFET while it ramps up during soft start (SS).

f. DSCHG Turn-On Slope: The DSCHG turn-on slope can be set between 0.1V/ms and 1.6V/ms.

g. CHG Turn-On OC Limit: The OC threshold during SS can be set to 3.6mV or 4.8mV.

h. Driver Voltage: The gate-to-source voltage (V_{GS}) for the CHG and DSCHG MOSFETs can be set between 7V and 12V.

i. CHG Pull-Up Current: The CHG pin's output current (I_{OUT}) during the CHG soft-start time (t_{SS}) can be set between 3μA and 10μA to control the CHG MOSFET driver voltage's rising slope.

12. Figure 12 shows how to configure the power status parameters.

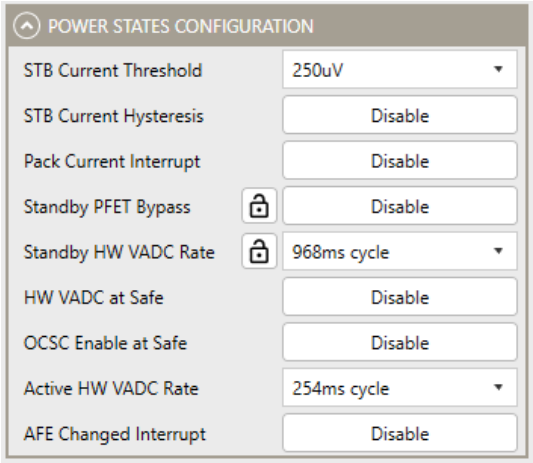


Figure 12: Power Status Configuration

a. HW VADC at Safe: If protections are required in safe mode, enable this function to ensure that the voltage can be monitored for protections.

b. Standby HW VADC Rate: The standby HW voltage ADC (VACD) rate can be used with voltage protection monitoring to refresh the ADC result while in safe or standby mode. This rate can be configured to refresh the voltage protection reading every 254ms, 492ms, or 968ms.

c. Active HW VADC Rate: The active HW VACD rate can be used with voltage protection monitoring to refresh the ADC result while in active mode. This rate can be configured to refresh the voltage protection reading every 135ms or 254ms.

13. Figure 13 shows how to configure the plug-in detection parameters.

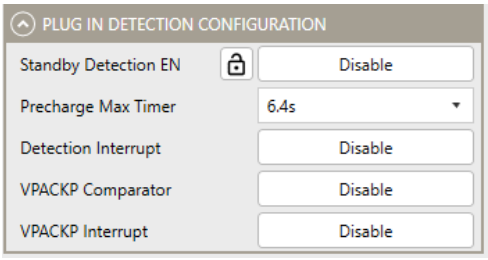


Figure 13: Plug-In Detection Configuration

a. Pre-Charge Max Timer: The PACKP pre-charge expiration timer can be set between 0.2s to 24s.

b. VPACKP Comparator: Enables the V_{PACK} vs. V_{TOP} comparator. When disabled, the comparator can still be enabled internally for other functions, such as plug-in detection.

14. Figure 14 shows how to configure the GPIOx pin parameters.

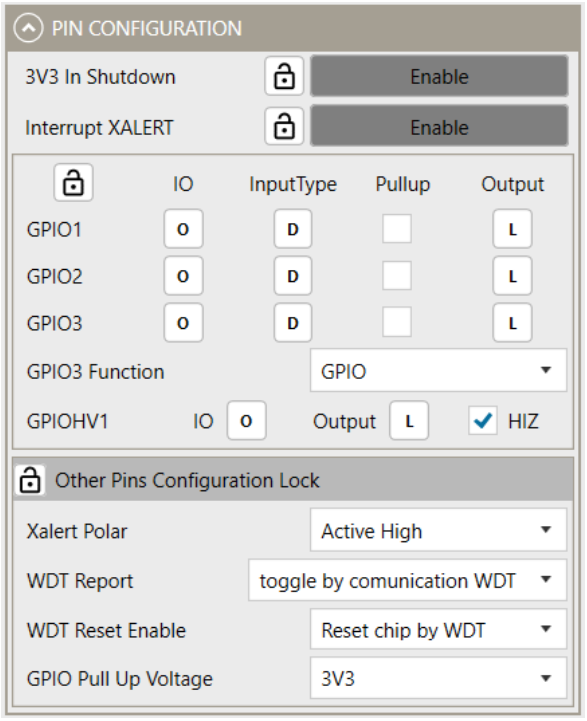


Figure 14: GPIOx Pin Configuration

a. IO: The GPIOx pins can be set to act as inputs or outputs. If they are set to inputs, they cannot be left floating and must be connected to a high or low level. Otherwise, GPIOx can consume excess power. GPIO2 can control the bypass P-channel MOSFET. Pull GPIO2 high to turn the P-channel MOSFET on; pull GPIO2 low to turn it off.

b. Input Type: Defines whether the input type for GPIO1~3 is a digital input or a buffered ADC input.

c. Pull-Up: Enables GPIOx's pull-up capability. When enabled, a 20kΩ pull-up resistance is applied.

d. Output: GPIOx's target output level can be set to high or low. This configuration bit is only effective when the corresponding GPIOx pin is set as a digital output.

e. GPIO3 Function (I²C version only): GPIO3 can be configured as a GPIO or fault indicator. This configuration is only valid when GPIO3 is set as an output.

f. GPIOHV1: GPIOHV1's target level can be set to high or low. This configuration bit is only effective when GPIOHV1 is used as a digital output and GPIOHV1_HZ = 0. If "HIZ" is selected, then GPIOHV1 is in Hi-Z mode. In this mode, the GPIOHV1 pin status ignores GPIOHV1_O, and the bypass P-channel MOSFET turns off. If "HIZ" is not selected, then GPIOHV1 is controlled by GPIOHV1_O in output mode, and the bypass P-channel MOSFET turns on when the output is low. It is recommended to use GPIOHV1 to control the bypass P-channel MOSFET.

g. GPIO Pull-Up Voltage: Sets the GPIOx pull-up voltage to 3V3 or REGIN.

15. Figure 15 shows how to configure the ADC scan parameters.

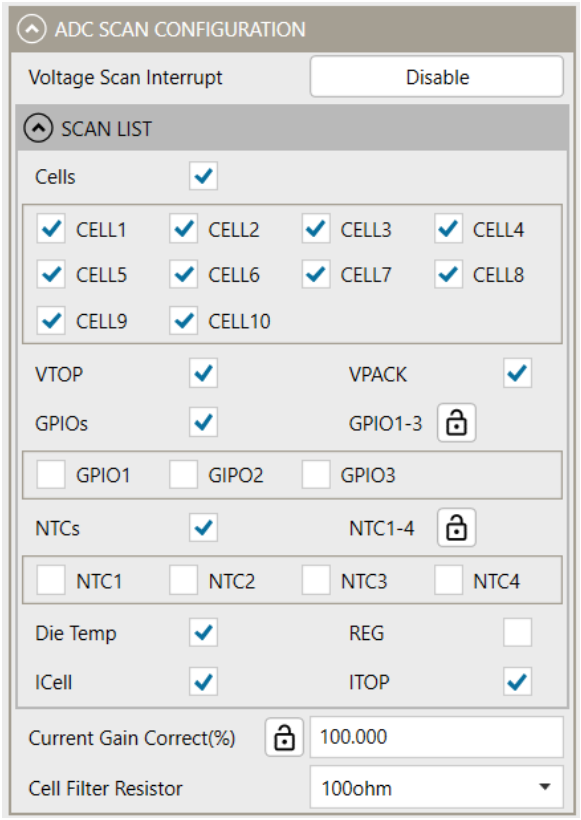


Figure 15: ADC Scan Configuration

a. Select a checkbox to enable the related parameter. If a parameter is enabled, that parameter is read and updated during the high-resolution VADC scan. If disabled, the parameter is excluded from the high-resolution VADC scan.

b. Current Gain Correct (%): Compensates for the current-sense resistor and surface-mounted technology (SMT) variation. The correction is applied to both coulomb counting and synchronous current ADC readings. The correction is not applied to SC and OC detection. The current gain correction can be set between 87.5% and 112.476%.

c. Cell Filter Resistor: The default cell filter resistance is 100Ω, and the ADC cell readings are not compensated. Set the cell filter resistance to 1kΩ when a 1kΩ filtering resistor is used (e.g. for external current balancing). This compensates for the ADC cell readings, and removes the drop caused by the input current during ADC conversion.

16. Figure 16 shows how to configure the watchdog timer parameters.

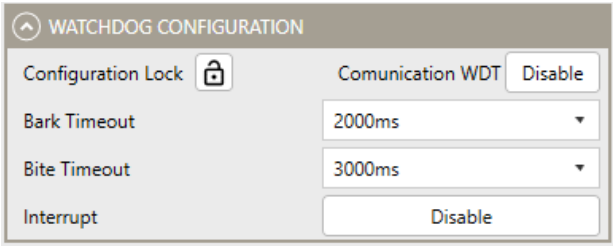


Figure 16: Watchdog Timer Configuration

a. Bark Timeout: The delay between the last watchdog reset and the bark can be set between 25ms and 3200ms.

b. Bite Timeout: The delay between the bark and the bite can be set between 25ms and 3200ms.

17. Figure 17 shows how to configure the open-wire detection parameters.

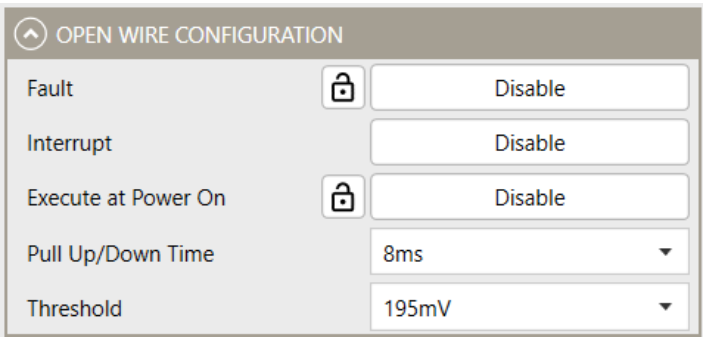


Figure 17: Open-Wire Detection Configuration

a. Execute at Power On: Enables open-wire detection during the start-up sequence (while exiting shutdown mode).

b. Pull-Up/Down Time: The length of each pull-up and pull-down phase can be set between 1ms and 16ms.

c. Threshold: The open-wire detection threshold for the detection sequence can be set between 39mV and 625mV.

18. Figure 18 shows how to configure the coulomb counting parameters.

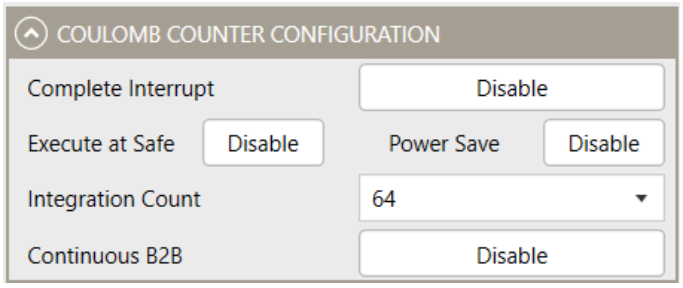


Figure 18: Coulomb Counting Configuration

a. Power Save: If enabled, the coulomb counter operates in power-save mode; if disabled, power-save mode is not used. Power-save mode reduces overall current consumption at the expense of accuracy.

b. Integration Count: The coulomb counter integration length sets the number of time slots, which are each 32ms. The length can be set between 1 (32ms) and 64 (2048ms). This register should only be updated when coulomb counting is not active.

c. Continuous B2B: Enables back-to-back accumulation mode. When enabled, a new coulomb counting conversion starts automatically after the most recent conversion is complete.

19. Figure 19 shows how to configure the OC parameters.

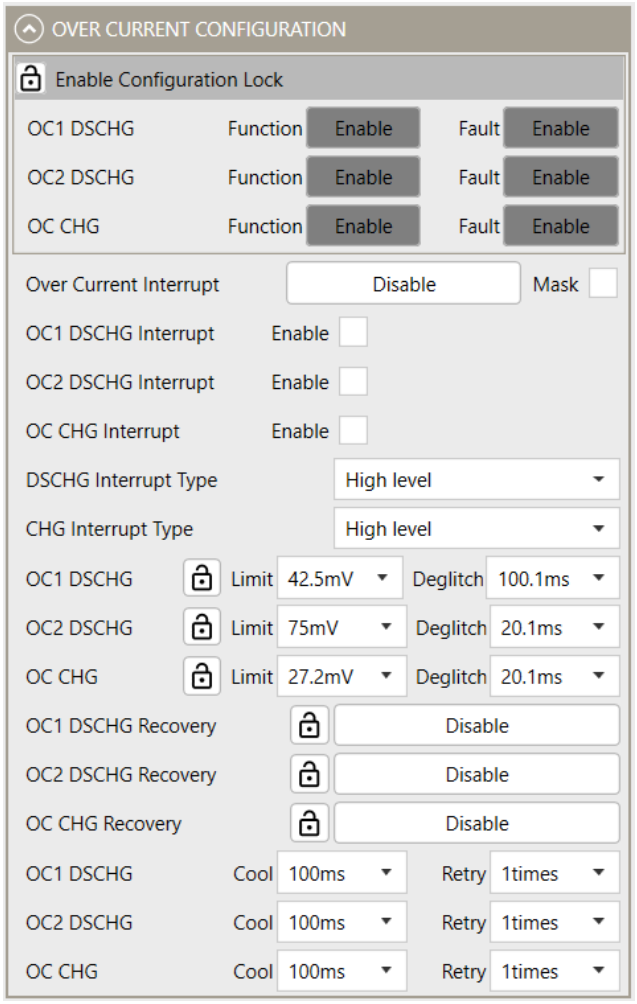


Figure 19: Over-Current Configuration

a. Select the OC interrupt “Mask” checkbox to enable the OC interrupt mask function. When enabled, the OC interrupt flag is cleared and the interrupt pin is pulled low, unless other interrupts are pending. When disabled, an OC condition can trigger the interrupt flag.

b. OC1 and OC2 DSCHG Limit: The OCx DSCHG limit can be set between 2.5mV and 80mV when OCx_DCHG_RNG is configured to 0, and between 7.5mV and 240mV when OCx_DCHG_RNG is configured to 1.

c. OC1 and OC2 DSCHG Deglitch: The OCx DSCHG deglitch time can be set between 0.1ms and 2520.1ms. The response time is about 100μs after the OC condition is detected.

d. OC CHG Limit: The OC CHG limit can be set between 1.6mV and 51.2mV when OC_CHG_RNG is configured to 0, and between 4.8mV and 153.6mV when OC_CHG_RNG is configured to 1.

e. OC CHG Deglitch: The OC CHG deglitch time can be set between 0.1ms and 2520.1ms. The response time is about 100μs after the OC condition is detected.

f. Recovery: The OC conditions can be enabled for automatic recovery, or disabled for manual recovery.

g. Cool: The cool down times can be set to 100ms, 200ms, 500ms, or 1s.

h. Retry: The number of retry attempts can be set to one time, two times, three times, or infinite (keep trying).

20. Figure 20 shows how to configure the SC parameters.

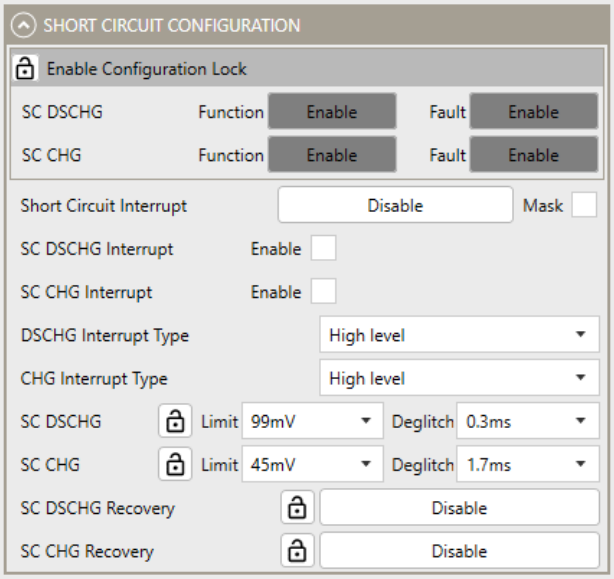


Figure 20: Short Circuit Configuration

a. Select the SC interrupt “Mask” checkbox to enable the SC interrupt mask function. When enabled, the SC interrupt flag is cleared and the interrupt pin is pulled low, unless other interrupts are pending. When disabled, an SC condition can trigger the interrupt flag.

b. Short-Circuit DSCHG Limit: The SC DSCHG limit can be set between 5.5mV and 176mV when SC_DCHG_RNG is configured to 0, and between 16.5mV and 528mV when SC_DCHG_RNG is configured to 1.

c. Short-Circuit DSCHG Deglitch: The SC DSCHG deglitch time can be set between 0.1ms and 25.5ms. The response time is about 100μs after the SC condition is detected.

d. Short-Circuit CHG Limit: The SC CHG limit can be set between 2.5mV and 80mV when SC_CHG_RNG is configured to 0, and between 7.5mV and 240mV when SC_CHG_RNG is configured to 1D.

e. Short-Circuit CHG Deglitch: The SC CHG deglitch time can be set between 0.1ms and 25.5ms. The response time is about 100μs after the SC condition is detected.

f. Recovery: The recovery settings can be set to enable automatic recovery or manual recovery.

21. Figure 21 shows how to configure the SC removal parameters.

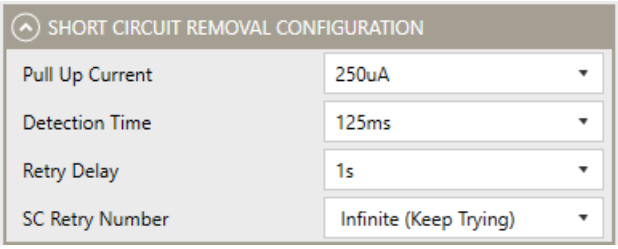


Figure 21: Short-Circuit Removal Configuration

a. Pull-Up Current: The pull-up current during SC removal detection can be set to 250μA, 500μA, or 750μA.

b. Detection Time: The detection time can be set to 125ms, 250ms, 500ms, or 1s.

c. Retry Delay: The retry delay between SC removal detections can be set between 1s and 25s.

d. SC Retry Number: The SC retry number can be set to 1, 2, 4, or to infinite (keep trying).

22. Figure 22 shows how to configure the NTC parameters.

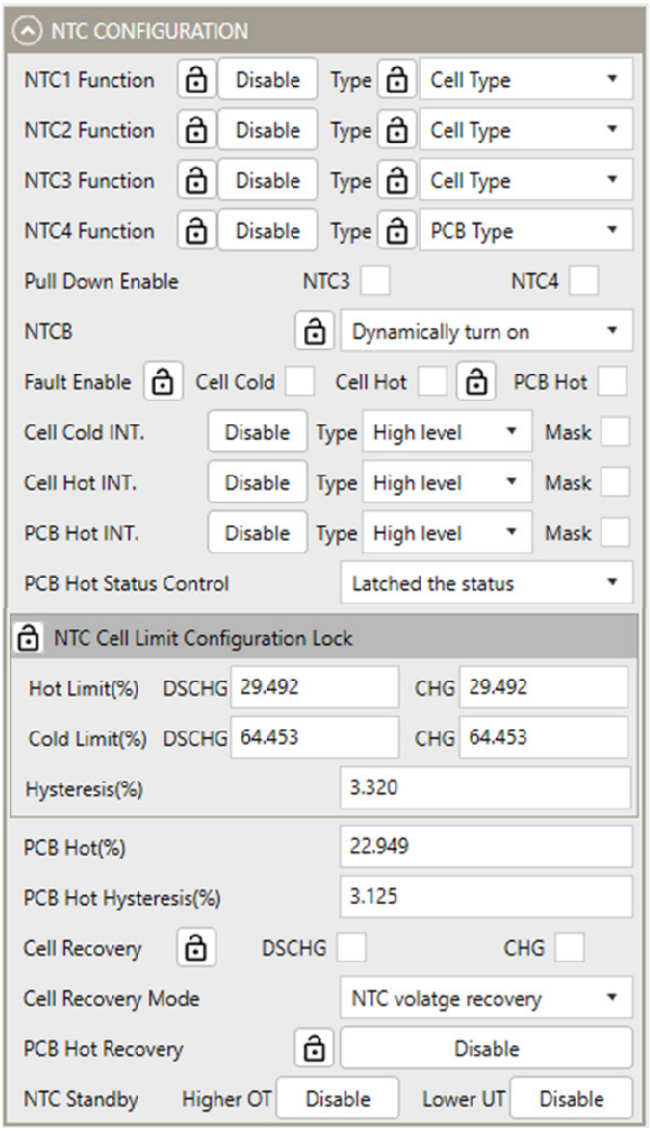


Figure 22: NTC Configuration

a. NTC Type: The NTC can be set to monitor the cells (Cell Type) or the PCB (PCB Type).

b. Pull-Down Enable: Enables NTC3 and NTC4 to be pulled down.

c. NTCB: NTCB is set to turn on dynamically. NTCB is dynamically biased during ADC conversions of the NTC channels. If NTCB is continuously on, current consumption increases.

d. PCB Hot Status Control: The PCB hot status control can be set to show the latched status (which goes to the interrupt controller) or show the real-time status.

e. NTC Cell Limit: The NTC cell limit can be set to be between 0% and 99.9% of NTCB.

f. Hysteresis (%): The hysteresis can be set to be between 0% and 6.055% of NTCB.

g. Cell Recovery Mode: Defines the recovery logic from NTC hot/cold conditions in charge mode. Set the NTC_CHG_REC_MODE bit to 0 for NTC voltage recovery. Set it to 1 for NTC voltage recovery or if the charger is removed.

h. Higher OT: Defines the selection criteria for the NTC hot threshold when the battery pack current is within the standby current range. If disabled, select the hotter threshold; if enabled, select the colder threshold.

i. Lower UT: Defines the selection criteria for the NTC cold threshold when the battery pack current is within the standby current threshold. If disabled, select the colder threshold; if enabled, select the hotter threshold.

23. Figure 23 shows how to configure the die temperature parameters.

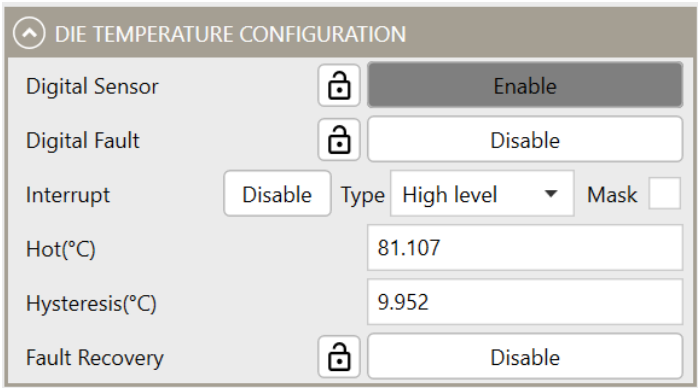


Figure 23: Die Temperature Configuration

a. Hot (°C): The resolution is 0.474°C.

b. Hysteresis (°C): The hysteresis can be set between 0°C and 14.692°C.

24. Figure 24 shows how to configure the cell-balancing parameters.

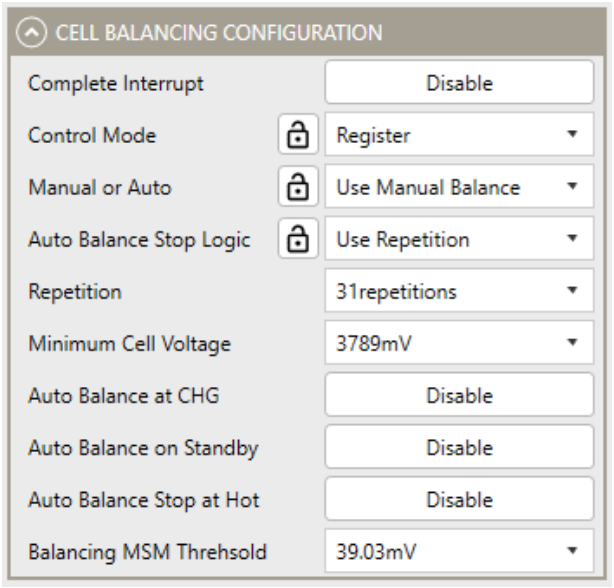


Figure 24: Cell-Balancing Configuration

a. Control Mode: The control mode can be set to register control or GIPO3 control when using automatic balancing.

b. Manual or Auto: The balancing mode can be configured for manual balancing or automatic balancing.

c. Auto-Balance Stop Logic: Only used when automatic balance is enabled. If set to “Use Repetition,” balancing uses repetition to control the number of balance iterations. If set to “Use List,” balancing continues until the balancing list is empty. To stop constant automatic cell-balancing before the balancing list is empty, disable this bit.

d. Repetition: The number of repetitions for each balancing list execution can be set between 0 and 31 repetitions. If 31 repetitions are selected, 32 balancing cycles are executed.

e. Minimum Cell Voltage: The qualifying minimum cell voltage to run automatic balancing can be set between 2500mV and 4961mV. When a cell is below this level, it is excluded from the balancing list. All other qualifying cells are balanced if they meet the criteria.

f. Balancing MSM Threshold: The balancing MSM threshold is used by the automatic balancing algorithm, and can be set between 19.5mV and 87.85mV.

25. Figure 25 shows how to configure the cell OV parameters.

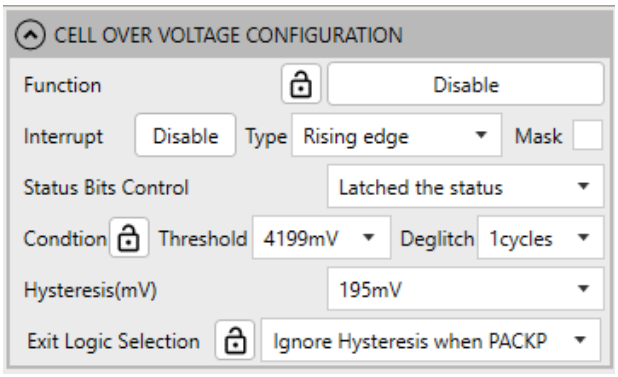


Figure 25: Cell Over-Voltage Configurations

a. Threshold: The cell OV threshold can be set between 0mV and 4980.15mV.

b. Hysteresis (mV): The OV hysteresis can be set between 0mV and 292.5mV.

c. Exit Logic Selection: The exit logic can be set to either “Lower than Cell OV - Hysteresis” or “Ignore Hysteresis when PACKP < VTOP”.

26. Figure 26 shows how to configure the cell UV parameters.

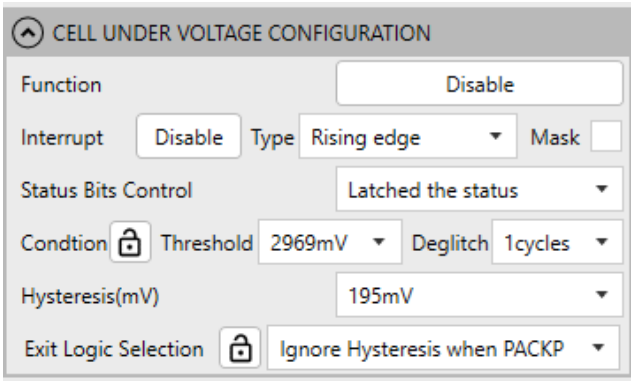


Figure 26: Cell Under-Voltage Configurations

a. Threshold: The cell UV threshold can be set between 0mV and 4980.15mV.

b. Hysteresis (mV): The UV hysteresis ranges can be set between 0mV and 292.5mV.

c. Exit Logic Selection: The exit logic can be set to either “Higher than Cell UV + Hysteresis” or “Ignore Hysteresis when PACKP > VTOP”.

27. Figure 27 shows how to configure the cell mismatch parameters.

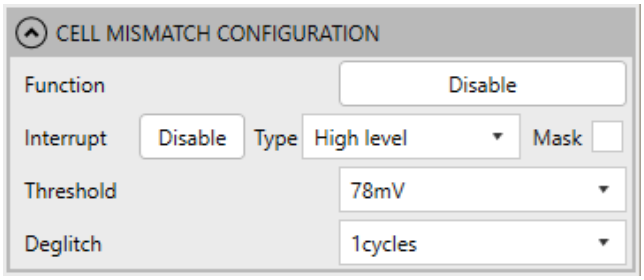


Figure 27: Cell Mismatch Configuration

Threshold: The cell mismatch threshold can be set between 0mV and 1211mV.

28. Figure 28 shows how to configure the cell dead parameters.

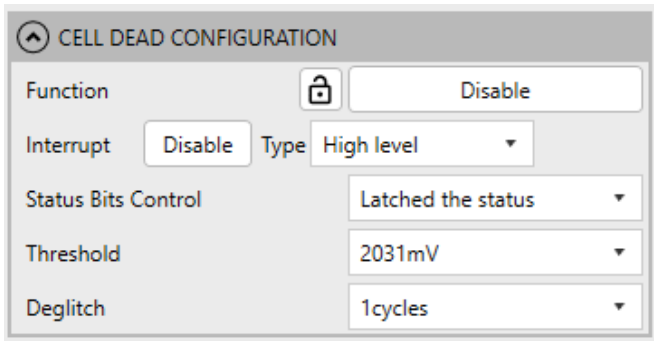


Figure 28: Cell Dead Configuration

Threshold: The cell dead threshold can be set between 0mV and 2480mV.

29. Figure 29 shows how to configure the VTOP UV parameters.

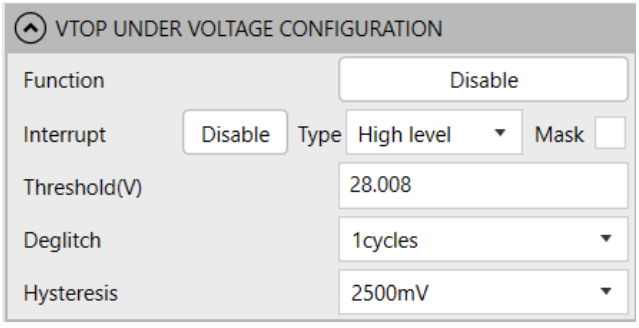


Figure 29: VTOP Under-Voltage Configuration

a. Threshold (V): The VTOP UV threshold can be set between 0V and 79.98V.

b. Hysteresis: The VTOP UV hysteresis can be set between 0mV and 4922mV.

30. Figure 30 shows how to configure the VTOP OV parameters.

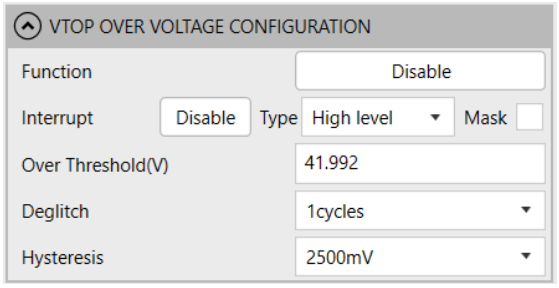


Figure 30: VTOP Over-Voltage Configuration

a. Over Threshold (V): The VTOP OV threshold can be set between 0V and 79.98V.

b. Hysteresis: The VTOP OV hysteresis can be set between 0mV to 4922mV.

31. Figure 31 shows how to configure the REGIN, 3V3, VDD, and ADC self-test checks.

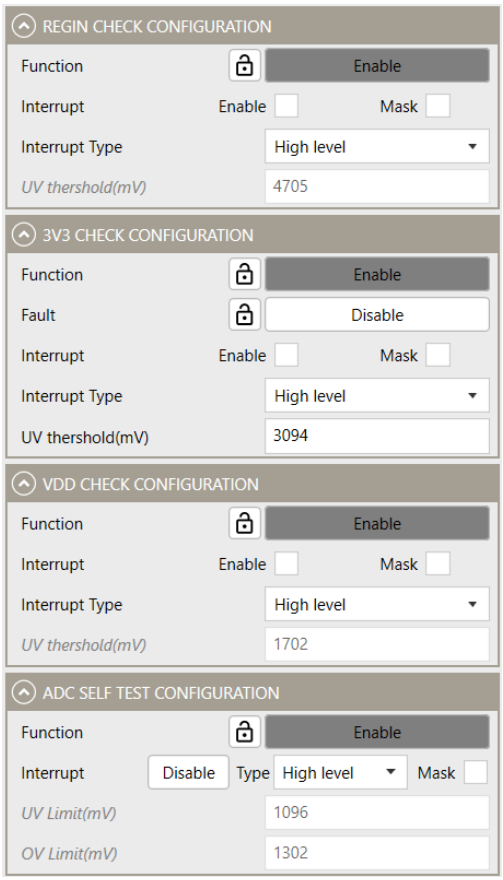


Figure 31: REGIN, 3V3, VDD, ADC Self-Test Check Configuration

32. Figure 32 shows how to configure the one-time programmable (OTP) memory CRC.

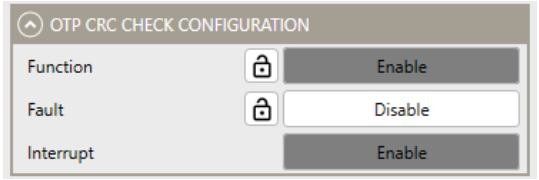


Figure 32: OTP CRC Configuration

33. Figure 33 shows how to configure simple mode MOSFET control.

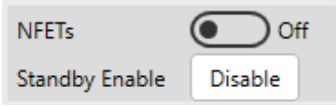


Figure 33: Simple Mode MOSFET Control

34. Figure 34 shows how to configure direct mode MOSFET control. Modify the control mode on the configuration tab, and then the options on the control tab change accordingly.

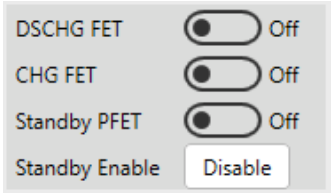


Figure 34: Direct Mode MOSFET Control

35. Figure 35 shows how to configure the status monitor.

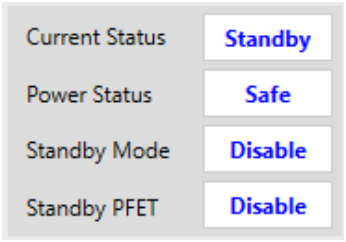


Figure 35: Status Monitor

36. Figure 36 shows how to configure the plug-in detection control and monitor.

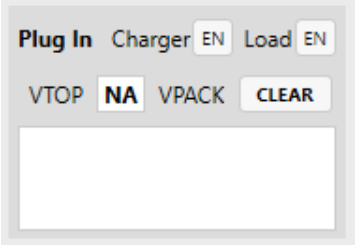


Figure 36: Plug-In Detection Control and Monitor

37. Figure 37 shows the watchdog status monitor.

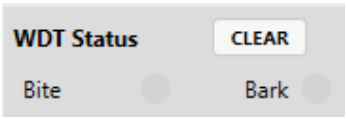


Figure 37: Watchdog Status Monitor

38. Figure 38 shows the MOSFET status monitor.

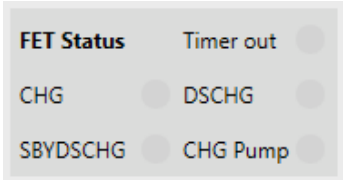


Figure 38: MOSFET Status Monitor

39. Figure 39 shows how to configure the ADC, cell-balancing, and open-wire control and monitor.

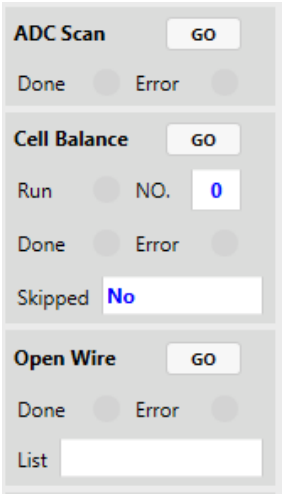


Figure 39: ADC, Cell-Balancing, and Open-Wire Control and Monitor

40. Figure 40 shows the OC and short-circuit status monitor.

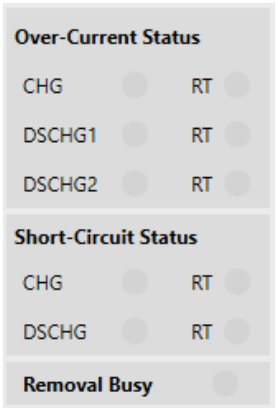


Figure 40: Over-Current and Short-Circuit Status Monitor

41. Figure 41 shows the GPIO and VTOP status monitor.

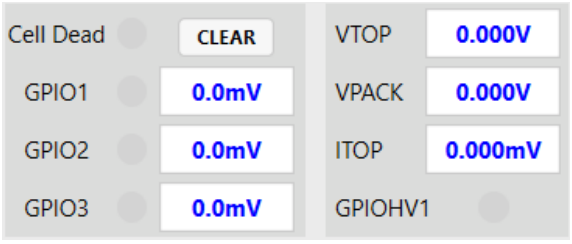


Figure 41: GPIO and VTOP Status Monitor

42. Figure 42 shows the die temperature monitor.

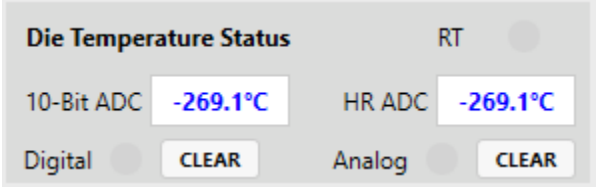


Figure 42: Die Temperature Monitor

43. Figure 43 shows the OTP memory CRC monitor.

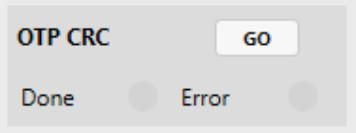


Figure 43: OTP CRC Monitor

44. Figure 44 shows the NTC monitor.

	Status	10-Bit ADC	HR ADC	RT
NTC1	Normal	0.0%	0.000%	Normal
NTC2	Normal	0.0%	0.000%	Normal
NTC3	Normal	0.0%	0.000%	Normal
NTC4	Normal	0.0%	0.000%	Normal

Figure 44: NTC Monitor

Figure 45 shows the NTC functional block.

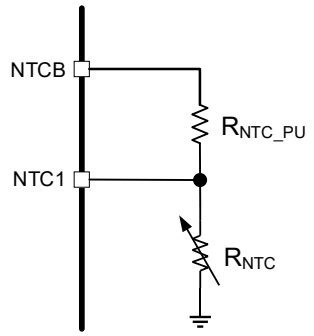


Figure 45: NTC Functional Block

The NTC resistance (R_{NTC}) can be estimated with Equation (1):

$$R_{NTC}=\frac{A\times R_{NTC\_PU}}{32768 - A} \quad (1)$$

Where A is the NTC ADC reading, and R_{NTC_PU} is the NTC pull-up resistor (10kΩ is recommended).

The ambient temperature (T, in Kelvin) can be calculated with Equation (2):

$$T=\frac{1}{\frac{1}{T_0}+\frac{1}{B}\ln\frac{R_{NTC}}{R_0}} \quad (2)$$

Where R_0 is the NTC resistance when the ambient temperature is T_0 (in Kelvin), and B is the thermistor constant (in Kelvin).

For example, if the NTC ADC reading (A) is 9830 (0x2666) for the thermistor NCP18XH103, R_0 is 10kΩ at 25°C (298.15K), and B is 3380K, then R_{NTC} = 4.285kΩ and T = 322K. This means that if the NTC ADC reading is 9830, then the ambient temperature is about 49°C.

45. Figure 46 shows the low-dropout (LDO) monitor.

	Status	10-Bit ADC	HR ADC
VDD	Normal	0.0mV	0.0mV
3V3	Normal	0.0mV	0.0mV
REGIN	Normal	0.0mV	0.0mV
Self	Normal	0.0mV	

Figure 46: LDO Monitor

46. Figure 47 shows the cell ADC monitor.

	Voltage	Current	UV	OV	MS	Dead	BAL
Cell1	0.0mV	0.000mV					
Cell2	0.0mV	0.000mV					
Cell3	0.0mV	0.000mV					
Cell4	0.0mV	0.000mV					
Cell5	0.0mV	0.000mV					
Cell6	0.0mV	0.000mV					
Cell7	0.0mV	0.000mV					
Cell8	0.0mV	0.000mV					
Cell9	0.0mV	0.000mV					
Cell10	0.0mV	0.000mV					

Figure 47: Cell ADC Monitor

EVALUATION BOARD SCHEMATICS

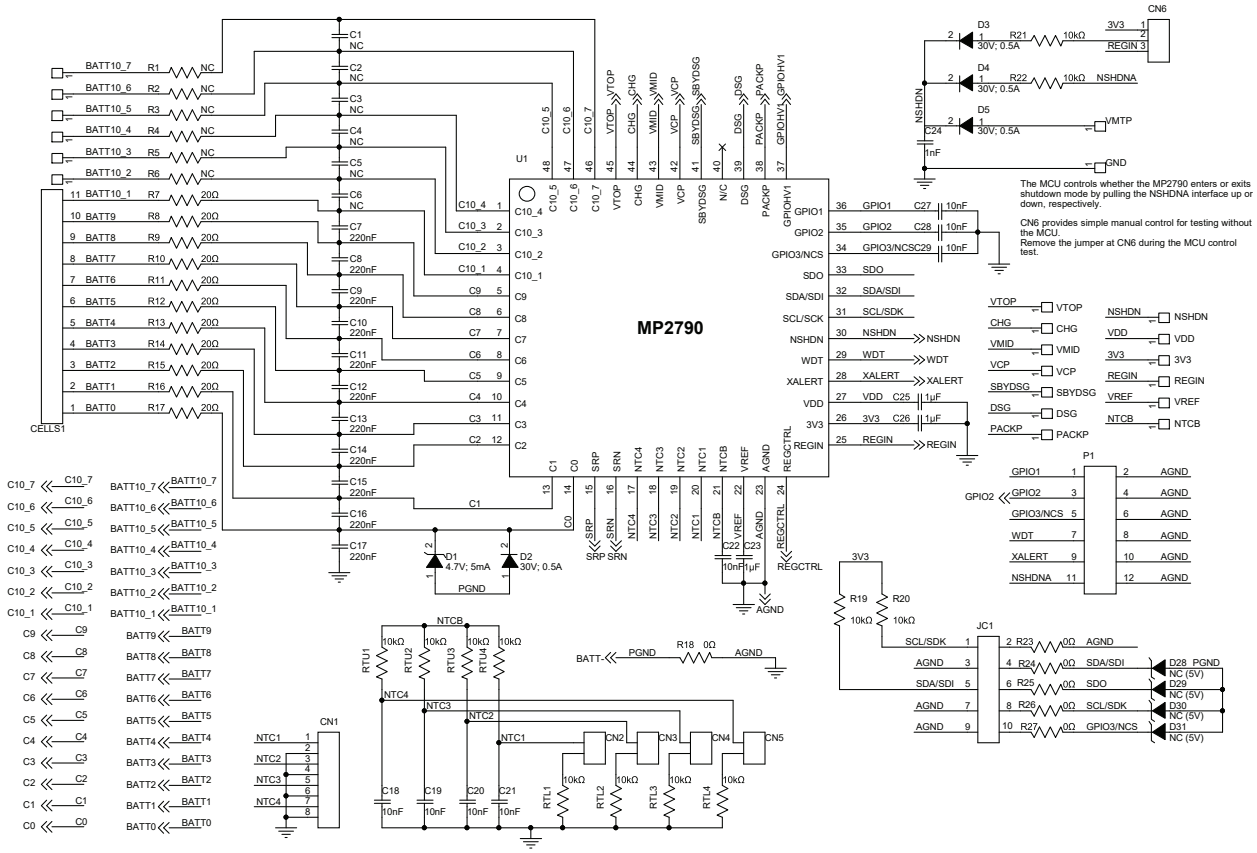


Figure 48: Evaluation Board Schematic (IC and Connector)

EVALUATION BOARD SCHEMATICS *(continued)*

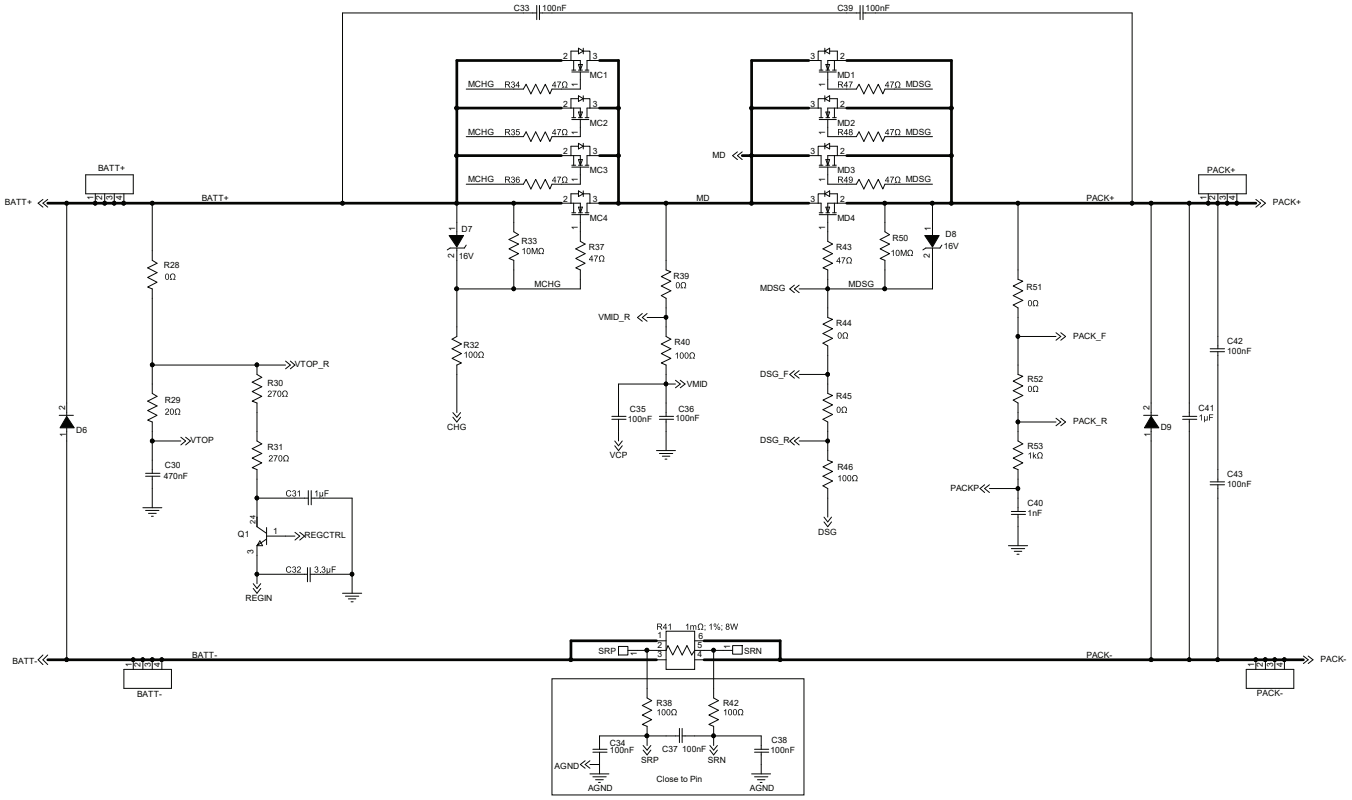


Figure 49: Evaluation Board Schematic (Power Path)

EVALUATION BOARD SCHEMATICS *(continued)*

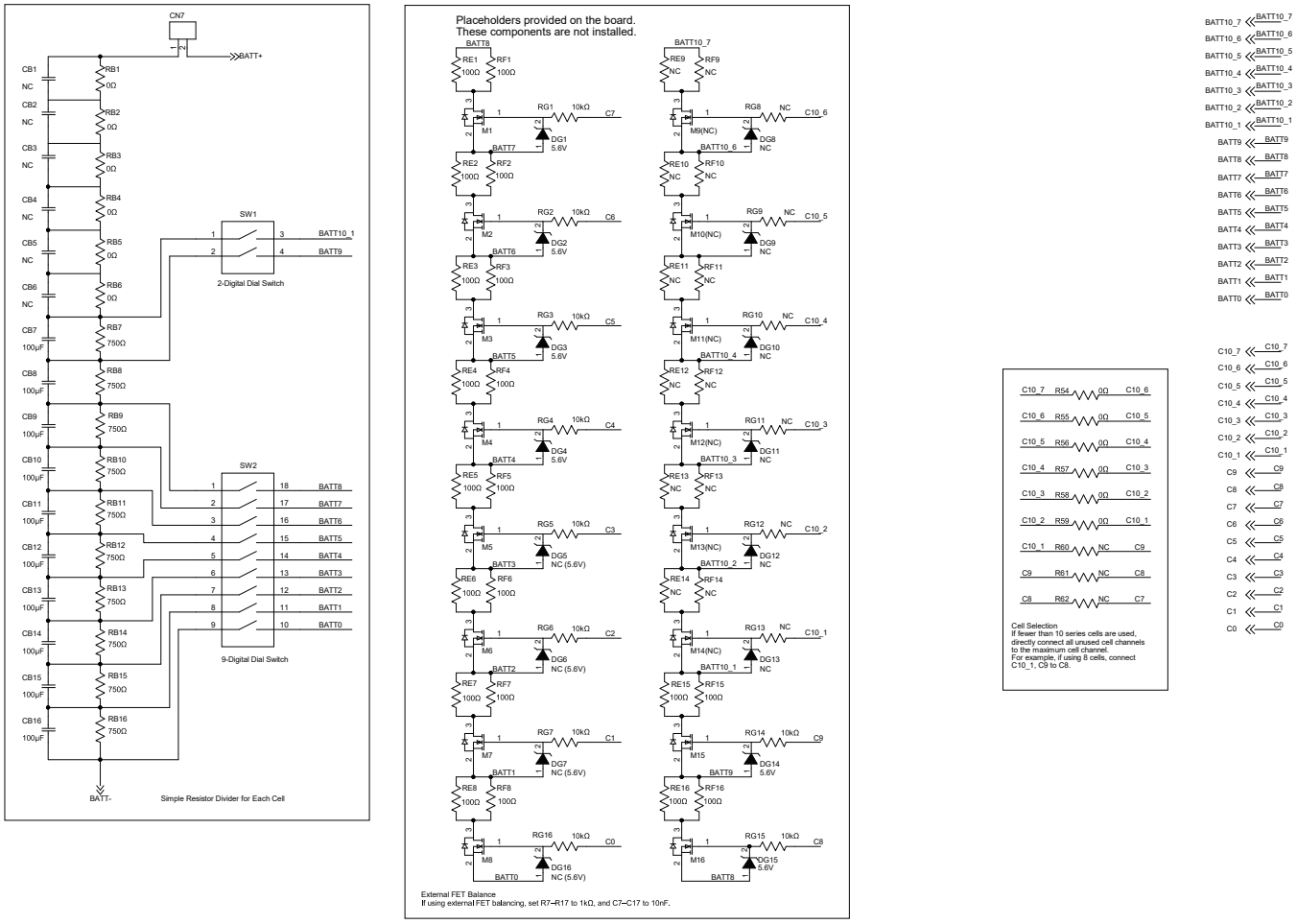


Figure 50: Evaluation Board Schematic (Battery Connection)

EVALUATION BOARD SCHEMATIC *(continued)*

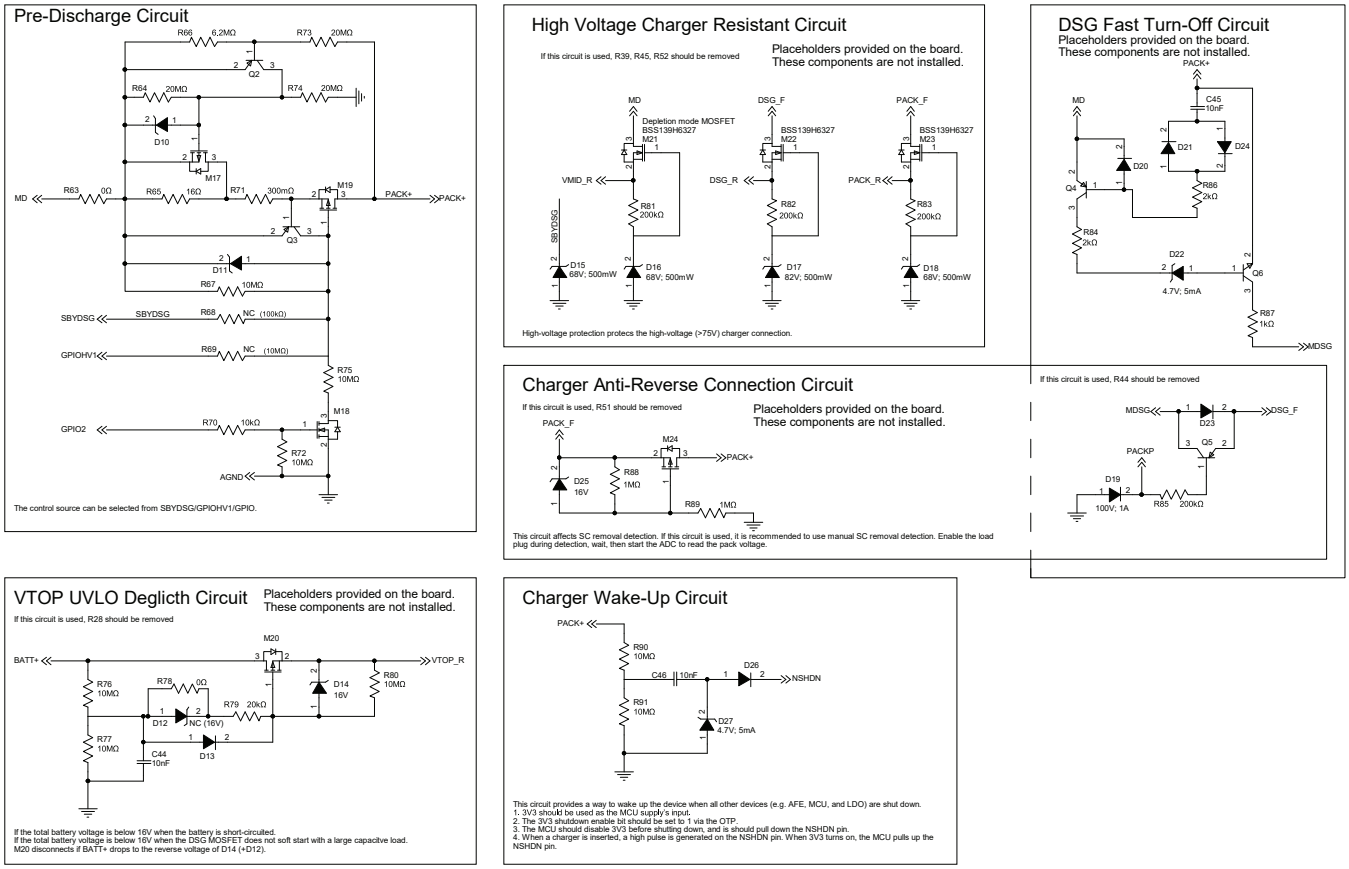


Figure 51: Evaluation Board Schematic (Additional Circuit)

END OF LIFE, REFER TO EV2790-0000-FP-00B

EV2790-0000-FP-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
4	PACK-, PACK+, BATT-, BATT+	12mmx 18mm	Connector	DIP	Zhengyou	ZY_50
10	CB7, CB8, CB9, CB10, CB11, CB12, CB13, CB14, CB15, CB16	100µF	Capacitor, 6.3V, X6T	1206	Murata	GRM31CD80J107ME39L
1	CN1	2.54mm	8-pin connector	DIP	Wurth	691210910008
5	CN2, CN3 ,CN4, CN5, CN7	2.54mm	2-pin connector	DIP	Any	
1	CN6	2.54mm	3-pin connector	DIP	Any	
1	CELLS1	3.5mm	11-pin connector	DIP	Kefa	KF2EDGR-3.5-11P
11	C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17	220nF	Capacitor, 50V, X7R	0603	Murata	GRM188R71H224KAC4D
8	C18, C19, C20, C21, C22, C27, C28, C29	10nF	Capacitor, 25V, X7R	0603	Wurth	885012206065
3	C23, C25, C26	1µF	Capacitor, 16V, X7R	0603	Wurth	885012206052
2	C24, C40	1nF	Capacitor, 100V, X7R	0603	Murata	GRM188R72A102KA01D
1	C30	470nF	Capacitor, 100V, X7R	0805	Murata	GRM21BR72A474KA73L
2	C31, C41	1µF	Capacitor, 100V, X7R	1206	Murata	GRM31CR72A105KA01L
1	C32	3.3µF	Capacitor, 16V, X5R	0805	Murata	GRM21BR61C335KA88
9	C33, C34, C35, C36, C37, C38, C39, C42, C43	100nF	Capacitor, 100V, X7R	0603	Wurth	885012206120
1	C46	10nF	Capacitor, 250V, X7R	0805	Murata	GRM21BR72E103KW03
2	D1, D27	4.7V	Zener diode, 5mA	SOD-323	Diodes, Inc.	BZT52C4V7S
4	D2, D3, D4, D5	30V	Schottky diode, 0.5A	SOD-123	JCET	B0530W
2	D6, D9	60V	TVS diode	DO-214AB	Vishay	SMCJ60A
4	D7, D8, D10, D11	16V	Zener diode, 5mA, 500mW	SOD-123	Diodes, Inc.	BZT52C16-7-F
1	D26	75V	Diode, 300mA	SOD-323	Diodes, Inc.	1N4148WS
1	JC1	2.54mm	2-row, 5-pin connector	DIP	Wurth	61201021621
1	P1	2.54mm	2-row, 6-pin connector	DIP	Any	
8	MD1, MC1, MD2, MC2, MD3, MC3, MD4, MC4	100V	N-channel MOSFET, 3.6mΩ, 90nC,120A,	TO-263	CR Micro	CRSS042N10N
1	M17	-30V	P-channel MOSFET, 172mΩ, 2.5A	SOT-23	Analog Power	AM2329P-T1-PF
1	M18	100V	N-channel MOSFET,6Ω, 170mA	SOT-23	Analog Power	LBSS123LT1G
1	M19	-200V	P-channel MOSFET, 950mΩ, 6A, 15nC	TO-252	Analog Power	AM10P20-690D

EV2790-0000-FP-00A BILL OF MATERIALS *(continued)*

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	Q1	100V	Transistor, NPN, 6A, 3W	SOT-223	Zetex	FZT853TA
2	Q2,Q3	-20V	Transistor, PNP, 1.5A	SOT-23	JCET	SS8550LT1
10	RB7, RB8, RB9, RB10, RB11, RB12, RB13, RB14, RB15, RB16	750Ω	Film resistor, 1%	0603	Yageo	RC0603FR-07750RL
3	R32, R40, R46	100Ω	Film resistor, 1%	1206	Yageo	RC1206FR-07100RL
13	RTU1, RTL1, RTU2, RTL2, RTU3, RTL3, RTU4, RTL4, R19, R20, R21, R22, R70	10kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710KL
11	R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17	20Ω	Film resistor, 1%	1206	Yageo	RC1206FR-0720RL
20	RB1, RB2, RB3, RB4, RB5, RB6, R18, R28, R39, R44, R45, R51, R52, R54, R55, R56, R57, R58, R59, R63	0Ω	Film resistor, 5%	0603	Royalohm	0603WAJ0000T5E
1	R29	20Ω	Film resistor, 5%	1206	Yageo	RC1206JR-0720RL
2	R30, R31	270Ω	Film resistor, 5%	2512	Yageo	RC2512JK-07270RL
7	R33, R50, R67, R72, R75, R90, R91	10MΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710ML
8	R34, R35, R36, R37, R43, R47, R48, R49	47Ω	Film resistor, 1%	0603	Yageo	RC1206FR-0747RL
2	R38, R42	100Ω	Film resistor, 1%	0603	Yageo	RC0603FR-07100RL
1	R41	1mΩ	Current-sense resistor, 1%	3920	Bourns	CSS2H-3920R-1L00F
1	R53	1kΩ	Film resistor, 5%	1206	Yageo	RC1206JR-071KL
3	R64, R73, R74	20MΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0720ML
1	R65	16Ω	Film resistor, 1%	0603	Yageo	RC0603FR-0716RL
1	R66	6.2MΩ	Film resistor, 1%	0603	Yageo	RC0603FR-076M2L
1	R71	300mΩ	Film resistor, 1%	2512	Yageo	RL2512FK-070R3L

EV2790-0000-FP-00A BILL OF MATERIALS *(continued)*

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	SW1	2.54mm	2-pin switch	SMD	Wurth	418121270802
1	SW2	2.54mm	9-pin switch	SMD	Wurth	418121270809
1	U1	MP2790	7-cell to 10-cell, high-accuracy battery monitoring and protection IC	TQFP-48 (7mmx 7mm)	MPS	MP2790DFP-0000

EV2790-0002-FP-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
4	PACK-, PACK+, BATT-, BATT+	12mmx 18mm	Connector	DIP	Zhengyou	ZY_50
10	CB7, CB8, CB9, CB10, CB11, CB12, CB13, CB14, CB15, CB16	100µF	Capacitor, 6.3V, X6T	1206	Murata	GRM31CD80J107ME39L
1	CN1	2.54mm	8-pin connector	DIP	Wurth	691210910008
5	CN2, CN3 ,CN4, CN5, CN7	2.54mm	2-pin connector	DIP	Any	
1	CN6	2.54mm	3-pin connector	DIP	Any	
1	CELLS1	3.5mm	11-pin connector	DIP	Kefa	KF2EDGR-3.5-11P
11	C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17	220nF	Capacitor, 50V, X7R	0603	Murata	GRM188R71H224KAC4D
8	C18, C19, C20, C21, C22, C27, C28, C29	10nF	Capacitor, 25V, X7R	0603	Wurth	885012206065
3	C23, C25, C26	1µF	Capacitor, 16V, X7R	0603	Wurth	885012206052
2	C24, C40	1nF	Capacitor, 100V, X7R	0603	Murata	GRM188R72A102KA01D
1	C30	470nF	Capacitor, 100V, X7R	0805	Murata	GRM21BR72A474KA73L
2	C31, C41	1µF	Capacitor, 100V, X7R	1206	Murata	GRM31CR72A105KA01L
1	C32	3.3µF	Capacitor, 16V, X5R	0805	Murata	GRM21BR61C335KA88
9	C33, C34, C35, C36, C37, C38, C39, C42, C43	100nF	Capacitor, 100V, X7R	0603	Wurth	885012206120
1	C46	10nF	Capacitor, 250V, X7R	0805	Murata	GRM21BR72E103KW03
2	D1, D27	4.7V	Zener diode, 5mA	SOD-323	Diodes, Inc.	BZT52C4V7S
4	D2, D3, D4, D5	30V	Schottky diode, 0.5A	SOD-123	JCET	B0530W
2	D6, D9	60V	TVS diode	DO-214AB	Vishay	SMCJ60A
4	D7, D8, D10, D11	16V	Zener diode, 5mA, 500mW	SOD-123	Diodes, Inc.	BZT52C16-7-F
1	D26	75V	Diode, 300mA	SOD-323	Diodes, Inc.	1N4148WS
1	JC1	2.54mm	2-row, 5-pin connector	DIP	Wurth	61201021621
1	P1	2.54mm	2-row, 6-pin connector	DIP	Any	
8	MD1, MC1, MD2, MC2, MD3, MC3, MD4, MC4	100V	N-channel MOSFET, 3.6mΩ, 90nC,120A,	TO-263	CR Micro	CRSS042N10N
1	M17	-30V	P-channel MOSFET, 172mΩ, 2.5A	SOT-23	Analog Power	AM2329P-T1-PF
1	M18	100V	N-Channel MOSFET,6Ω, 170mA	SOT-23	Analog Power	LBSS123LT1G
1	M19	-200V	P-channel MOSFET, 950mΩ, 6A, 15nC	TO-252	Analog Power	AM10P20-690D

EV2790-0002-FP-00A BILL OF MATERIALS *(continued)*

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	Q1	100V	Transistor, NPN, 6A, 3W	SOT-223	Zetex	FZT853TA
2	Q2,Q3	-20V	Transistor, PNP, 1.5A	SOT-23	JCET	SS8550LT1
10	RB7, RB8, RB9, RB10, RB11, RB12, RB13, RB14, RB15, RB16	750Ω	Film resistor, 1%	0603	Yageo	RC0603FR-07750RL
3	R32, R40, R46	100Ω	Film resistor, 1%	1206	Yageo	RC1206FR-07100RL
13	RTU1, RTL1, RTU2, RTL2, RTU3, RTL3, RTU4, RTL4, R19, R20, R21, R22, R70	10kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710KL
11	R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17	20Ω	Film resistor, 1%	1206	Yageo	RC1206FR-0720RL
20	RB1, RB2, RB3, RB4, RB5, RB6, R18, R28, R39, R44, R45, R51, R52, R54, R55, R56, R57, R58, R59, R63	0Ω	Film resistor, 5%	0603	Royalohm	0603WAJ0000T5E
1	R29	20Ω	Film resistor, 5%	1206	Yageo	RC1206JR-0720RL
2	R30, R31	270Ω	Film resistor, 5%	2512	Yageo	RC2512JK-07270RL
7	R33, R50, R67, R72, R75, R90, R91	10MΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710ML
8	R34, R35, R36, R37, R43, R47, R48, R49	47Ω	Film resistor, 1%	0603	Yageo	RC1206FR-0747RL
2	R38, R42	100Ω	Film resistor, 1%	0603	Yageo	RC0603FR-07100RL
1	R41	1mΩ	Current-sense resistor, 1%	3920	Bourns	CSS2H-3920R-1L00F
1	R53	1kΩ	Film resistor, 5%	1206	Yageo	RC1206JR-071KL
3	R64, R73, R74	20MΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0720ML
1	R65	16Ω	Film resistor, 1%	0603	Yageo	RC0603FR-0716RL
1	R66	6.2MΩ	Film resistor, 1%	0603	Yageo	RC0603FR-076M2L
1	R71	300mΩ	Film resistor, 1%	2512	Yageo	RL2512FK-070R3L

EV2790-0002-FP-00A BILL OF MATERIALS *(continued)*

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	SW1	2.54mm	2-pin switch	SMD	Wurth	418121270802
1	SW2	2.54mm	9-pin switch	SMD	Wurth	418121270809
1	U1	MP2790	7-cell to 10-cell, high-accuracy battery monitoring and protection IC	TQFP-48 (7mmx 7mm)	MPS	MP2790DFP-0002

EV2790-0000/0002-FP-00A BILL OF MATERIALS

Recommended Components for the External MOSFET Balancing Circuit (Components Not Installed on the Standard Board)

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
10	M1, M2, M3, M4, M5, M6, M7, M8, M15, M16	50V	N-channel MOSFET, 3.5mΩ, 0.2A	SOT-23	LRC	LBSS138LT1G
20	RF1, RE1, RF2, RE2, RF3, RE3, RF4, RE4, RF5, RE5, RF6, RE6, RF7, RE7, RF8, RE8, RF15, RE15, RF16, RE16	100Ω	Film resistor, 1%	1206	Yageo	RC1206FR-07100RL
9	RG1, RG2, RG3, RG4, RG5, RG6, RG7, RG14, RG15, RG16	10kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710KL
9	DG1, DG2, DG3, DG4, DG5, DG6, DG7, DG14, DG15, DG16	5.6V	Zener diode, 5mA	SOD-323	Diodes, Inc.	BZT52C5V6S-7-F

EV2790-0000/0002-FP-00A BILL OF MATERIALS

Recommended Components for the VTOP UVLO Deglitch Circuit (Components Not Installed on the Standard Board)

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	M20	-100V	P-channel MOSFET, 1.2Ω, 1A	SOT-23	Analog Power	AM2371P
2	D12, D14	16V	Zener diode, 5mA, 500mW	SOD-123	Diodes, Inc.	BZT52C16-7-F
1	D13	75V	Diode, 300mA	SOD-323	Diodes, Inc.	1N4148WS
3	R76 ,R77, R80	10MΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710ML
1	R78	0Ω	Film resistor, 5%	0603	Royalohm	0603WAJ0000T5E
1	R79	20kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0720KL
1	C44	10nF	Capacitor, 250V, X7R	0805	Murata	GRM21BR72E103KW03

EV2790-0000/0002-FP-00A BILL OF MATERIALS

Recommended Components for the DSCHG Fast Turn-Off and Anti-Reverse Connection Circuit (Components Not Installed on the Standard Board)

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	C45	10nF	Capacitor, 250V, X7R	0805	Murata	GRM21BR72E103KW03
4	D20, D21, D23, D24	75V	Diode, 300mA	SOD-323	Diodes, Inc.	1N4148WS
1	D25	16V	Zener diode, 5mA, 500mW	SOD-123	Diodes, Inc.	BZT52C16-7-F
1	D19	100V	Schottky diode, 1A	SOD-123-2	ST	BAT41ZFILM
1	D22	4.7V	Zener diode, 5mA	SOD-323	Diodes, Inc.	BZT52C4V7S
4	D28, D29, D30, D31	5V	ESD diode, 5V	SOD-323	NXP	PESD5V0V1BA
1	M24	-100V	P-channel MOSFET, 1.2Ω, 1A	SOT-23	Analog Power	AM2371P
2	Q4, Q5	-80V	Transistor, 0.5A, PNP	SOT-23	Diodes, Inc.	MMBTA56LT1G
1	Q6	80V	Transistor, 0.5A, NPN	SOT-23	ON Semiconductor	MMBTA06
1	R85	200kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-07200KL
1	R87	47Ω	Film resistor, 1%	1206	Yageo	RC1206FR-0747RL
2	R84, R86	2kΩ	Film resistor, 1%	0805	Yageo	RC0805FR-072KL
2	R88, R89	1MΩ	Film resistor, 1%	0603	Yageo	RC0603FR-071ML

EV2790-0000/0002-FP-00A BILL OF MATERIALS

Recommended Components for High-Voltage Charger Circuit (Components Not Installed on the Standard Board)

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
3	D15, D16, D18	68V	Zener diode, 1.8mA	SOD-123-2	Onsemi	MMSZ5266BT1G
1	D17	82V	Zener diode, 1.5mA	SOD-123-2	Onsemi	MMSZ5268BT1G
3	R81, R82, R83	200kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-07200KL
3	M21, M22, M23	250V	N-channel MOSFET, 7.8mΩ, 2.3nc, 30mA	SOT-23	Infineon	BSS139H6327

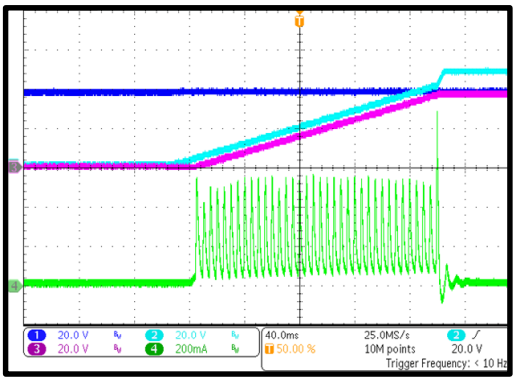
EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board. V_{TOP} = 37.5V, T_A = 25°C, unless otherwise noted.

DSCHG Soft Start

PACK+ is connected to a 1mF capacitor, DSCHG slope = 0.2V/ms

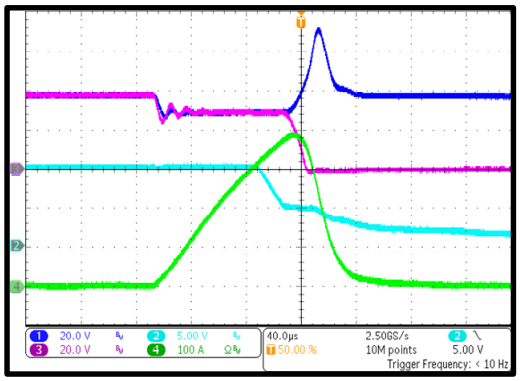
CH1: V_{MID}
CH2: V_{DSCHG}
CH3: V_{PACK+}
CH4: I_{DSCHG}



DSCHG Fast-Off in Short-Circuit

$R_{SRP-SRN}$ = 1mΩ, SC threshold = 99mV, deglitch off, 4 paralleled CRSS042N10N devices act as the DSCHG N-channel MOSFETs (typical C_{ISS} = 27088pF)

CH1: V_{MID}
CH3: V_{PACK+}
CH2: V_{GS_DSCHG}
CH4: I_{DSCHG}



PCB LAYOUT (MP2790-0000-FP-00A)

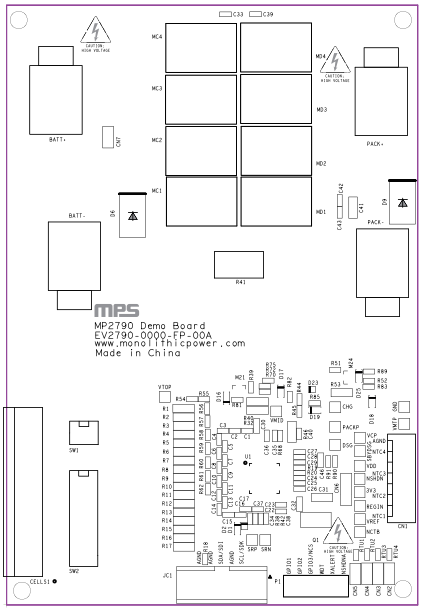


Figure 52: Top Silk

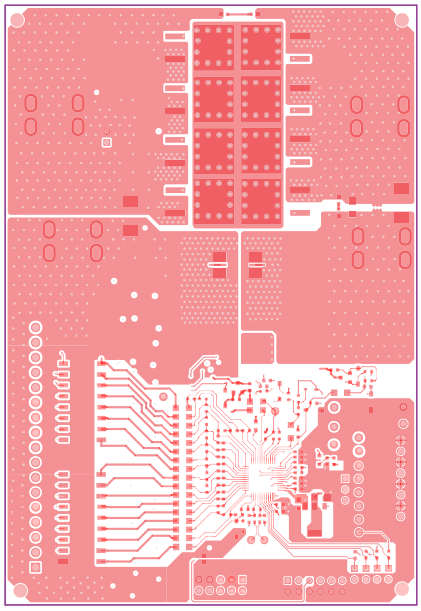


Figure 53: Top Layer

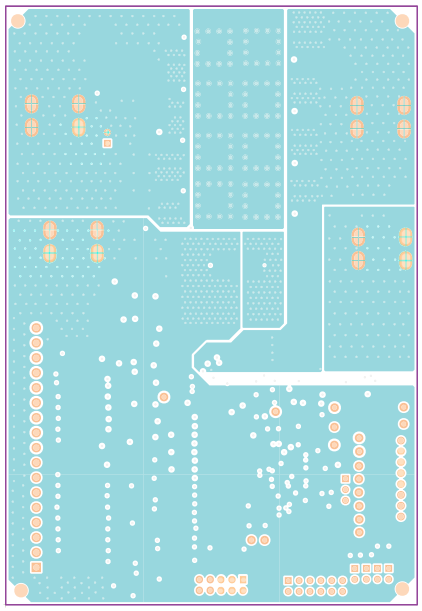


Figure 54: Mid-Layer 1

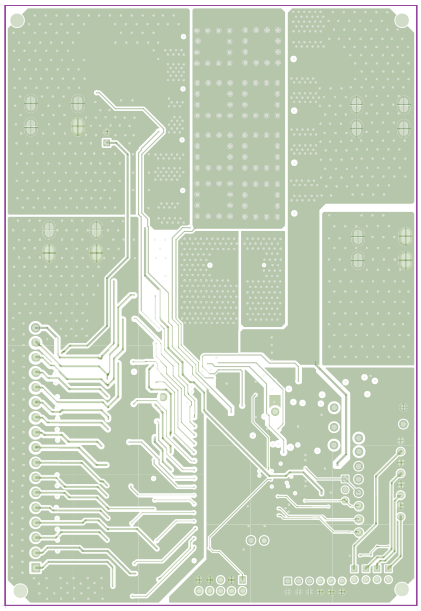


Figure 55: Mid-Layer 2

PCB LAYOUT (MP2790-0000-FP-00A) *(continued)*

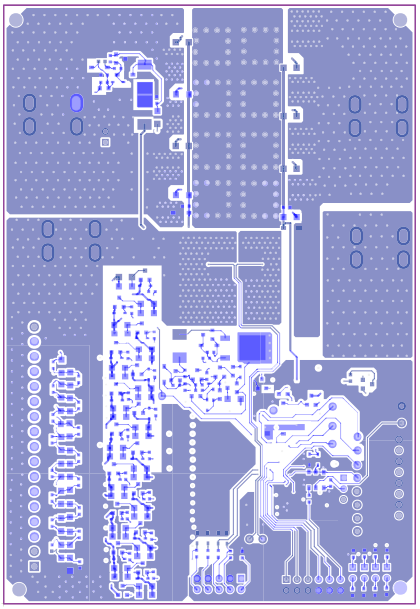


Figure 56: Bottom Layer

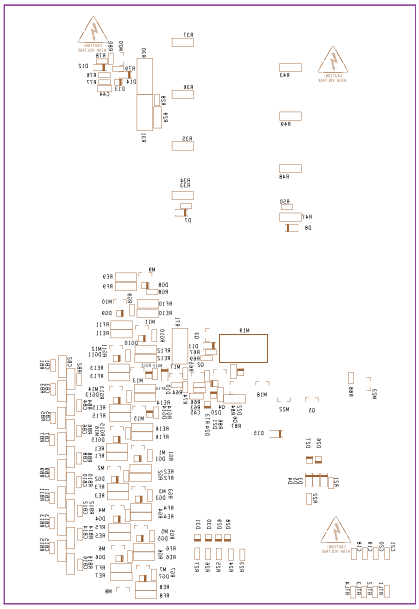


Figure 57: Bottom Silk

PCB LAYOUT (MP2790-0002-FP-00A)

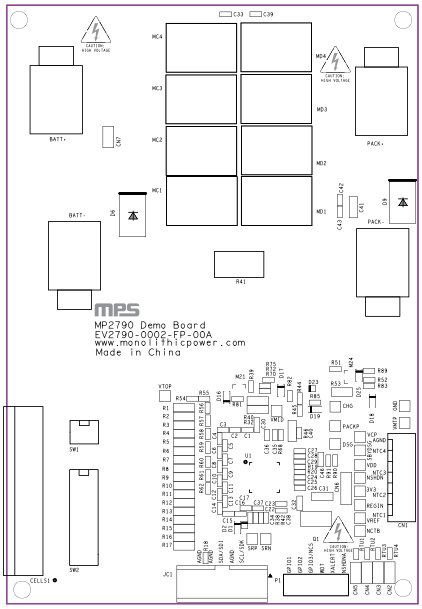


Figure 58: Top Silk

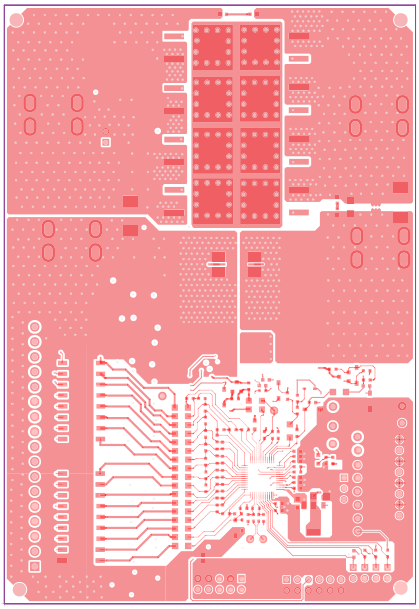


Figure 59: Top Layer

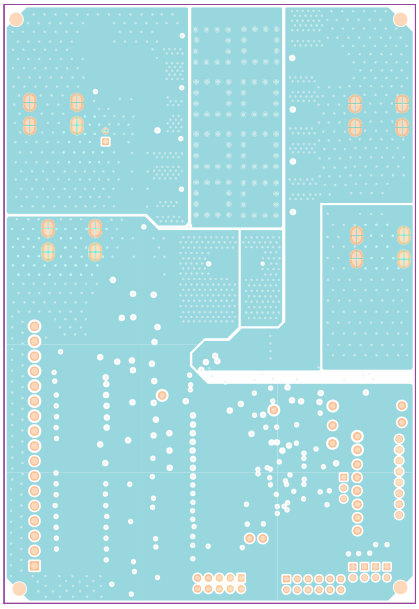


Figure 60: Mid-Layer 1

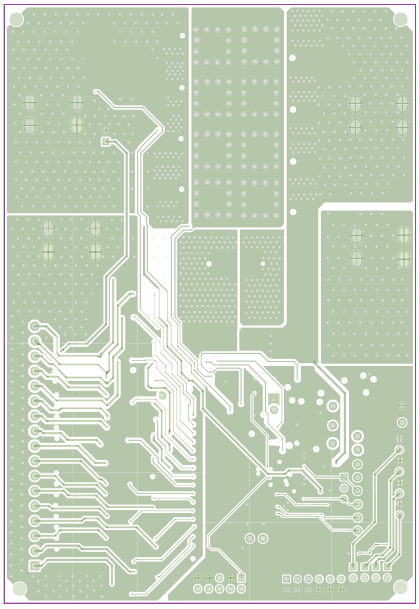


Figure 61: Mid-Layer 2

PCB LAYOUT (MP2790-0002-FP-00A) *(continued)*

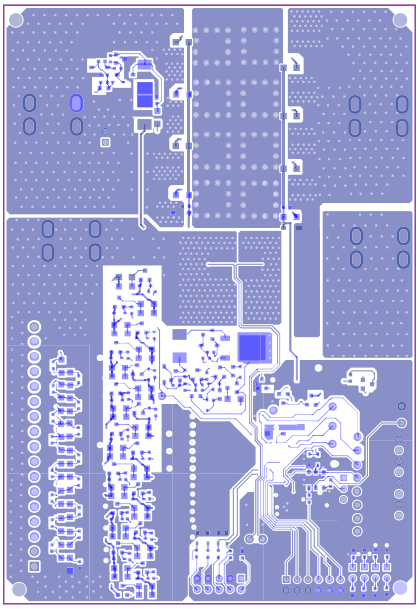


Figure 62: Bottom Layer

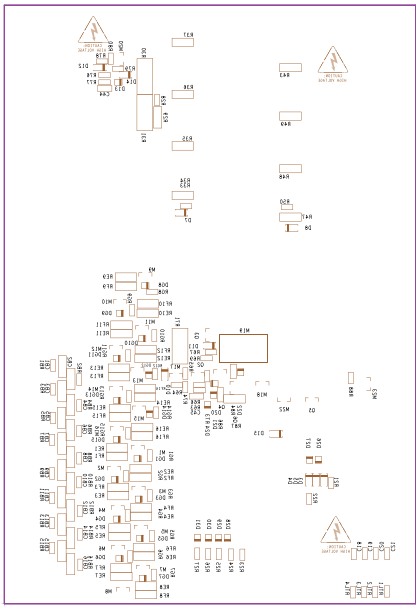


Figure 63: Bottom Silk

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	8/4/2023	Initial Release	-