EV2790-0000-FP-00B

4-Cell to 10-Cell, High-Accuracy Battery Monitor and Protector with Coulomb Counting and I²C Evaluation Board

DESCRIPTION

The EV2790-0000-FP-00B is an evaluation board designed to demonstrate the capabilities of the MP2790, a robust battery management device. The MP2790 provides a complete analog front-end (AFE) monitoring and protection solution. It is designed for multiple-cell series battery management systems (BMS). The device supports I²C communication.

The MP2790 supports connections for 4-cell to 10-cell series battery packs, with an absolute voltage exceeding 80V on particular pins.

The MP2790 integrates two separate analog-to-digital converters (ADCs). The first ADC measures each channel's differential cell voltage (up to 10 channels), die temperature, and 4-channel temperatures via external negative temperature coefficient (NTC) thermistors. The second ADC measures the charge and discharge current via an external current-sense resistor. The dual ADC architecture enables synchronous voltage and current measurements for cell and pack impedance monitoring.

The MP2790 includes high-side MOSFET (HS-FET) drivers for independent charge (CHG) and discharge (DSG) control.

The DSG MOSFET driver includes a configurable soft start (SS) that provides a controlled turn-on, eliminating the need for an external pre-charge circuit. The DSG MOSFET driver also incorporates protections such as reporting discharging over-current (DOC), short-circuit, battery under-voltage (UV), over-temperature (OT), and under-temperature (UT) faults. The CHG MOSFET drivers incorporates protections such as reporting charging over-current (COC), short-circuit, battery over-voltage (OV), OT, and UT faults. All of these protections have configurable thresholds.

Internal passive balancing MOSFETs can be used to equalize mismatched cells, supporting up to 58mA. The MP2790 provides the option to drive external balancing transistors (MOSFET or BJT).

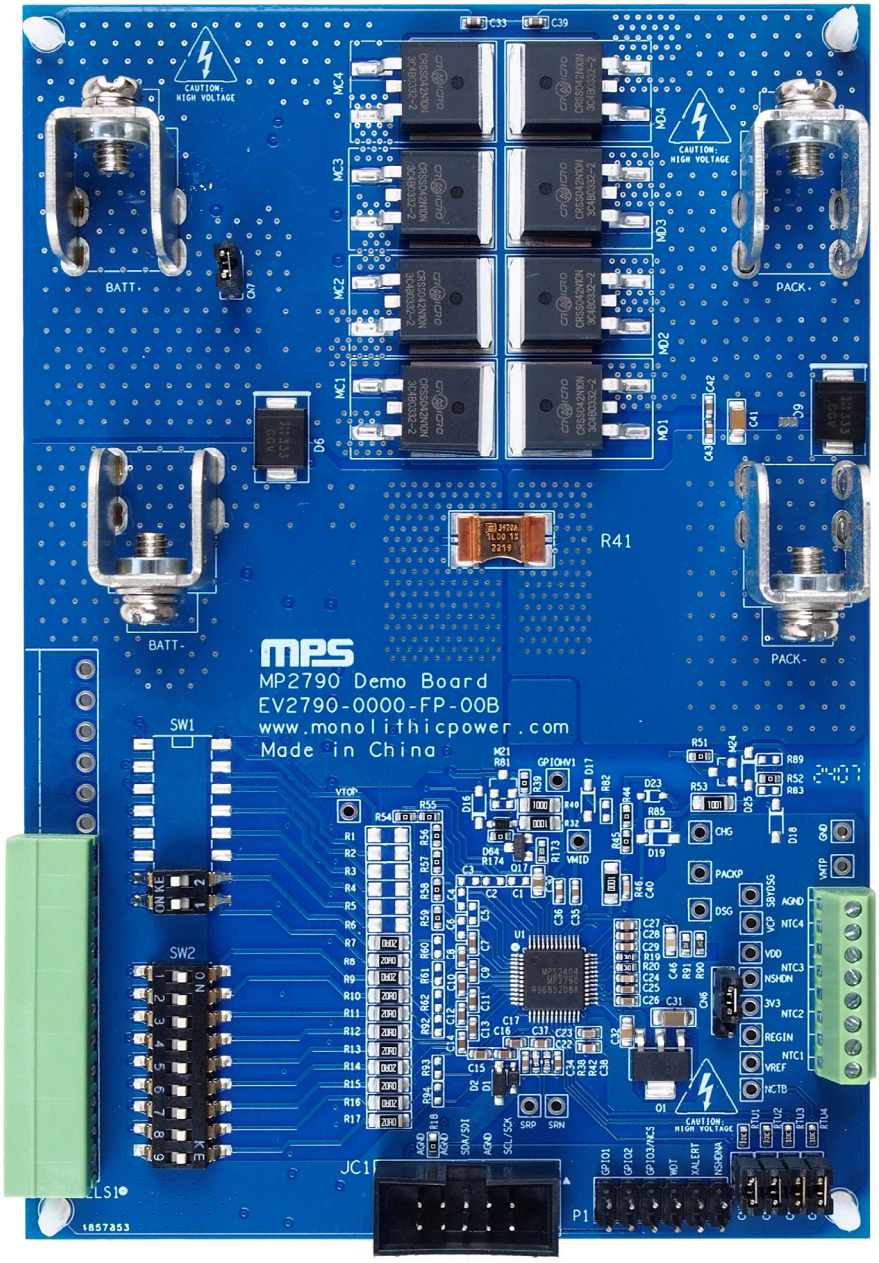
The MP2790 has optimized baseline current consumption dependent on the mode. It is available in a TQFP-48 (7mmx7mm) package.

PERFORMANCE SUMMARY

Specifications are at T_A = -40°C to +85°C, unless otherwise noted.

Parameters	Conditions	Value
Battery pack voltage range		10V to 47V
Cell voltage range		0V to 5V
Continuous charge current		0A to 70A
Continuous discharge current		0A to 70A
Supported cells in series		4 cells to 10 cells

EV2790-0000-FP-00B EVALUATION BOARD



LxWxH (14cmx9.6cmx1.5cm)

Board Number	MPS IC Number
EV2790-0000-FP-00B	MP2790DFP-0000 (1)

Note:

1) "0000" is the default configuration code that supports I²C communication. For custom options, contact an MPS FAE to obtain an "xxxx" value.

QUICK START GUIDE

The EV2790-0000-FP-00B is designed to evaluate the MP2790, a robust battery management device. The MP2790 can monitor the analog front-end (AFE) and provide protections. The evaluation board includes the MP2790, power MOSFETs, a current-sense resistor, a bipolar junction transistor (BJT), external balance resistors, balancing BJTs, and other components. This complete solution protects the battery from the following: over-current (OC), short-circuit, under-voltage (UV), over-voltage (OV), unbalanced cell, and high-/low-temperature conditions.

The EV2790-0000-FP-00B can be set to support 4-cell to 10-cell series connections, synchronous voltage and current measurements, and robust hardware protections with configurable thresholds. Adding external balancing BJTs allows the device to support a higher balancing current.

Evaluation Platform Preparation

1. To use the evaluation platform, the following is required: a computer with at least one USB port, a USB cable, and a USB-to-I²C communication kit (EVKT-USBI2C-02) (see Figure 1).

Figure 1: USB-to-I²C Communication Kit (EVKT-USBI2C-02)

2. Install the MP2790 graphical user interface (GUI), which can be downloaded from the MPS website. The software is supported by Windows XP, 7, or later versions.
3. To check that the software is installed properly, open the GUI by clicking on the “Programming Tool MP2790 V1.1.exe” file.
4. To set up the board using the cell simulator shunt (i.e. without a real battery pack) (see Figure 2 on page 4), follow the steps below:
   a. Short CN7, and turn the SW1 and SW2 channels on.
   b. Apply a DC power supply between BATT+ and BATT-.
   c. Adjust the power supply to be about 37.5V/1A.
   d. Connect the USB-to-I²C communication kit to JC1. Carefully consider where SCL and SDA are positioned.

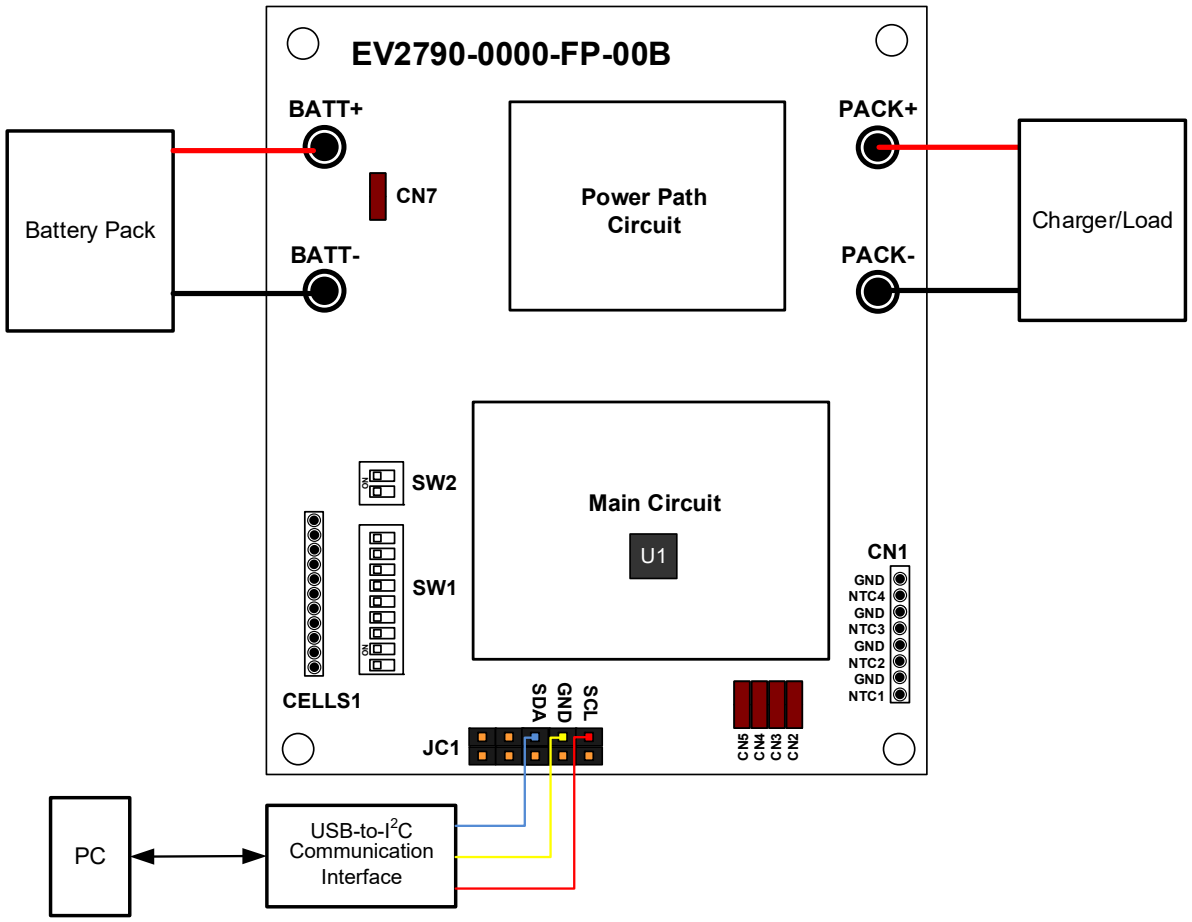


Figure 2: Equipment Set-Up for the MP2790DFP-0000

5. By default, the evaluation board has 10 cells in series. To use the cell simulator shunt and evaluate the device with a lower number of cells in series, short circuit the corresponding channels:

   a. If more than 5 cells (but fewer than 10 cells in series) are used, directly connect all the upper unused cell channels to the practical maximum cell channel. For example, if only 8 cells are used, BATT8~BATT10 should be connected together (see Figure 3).

   a. If fewer than 6 series cells are used, directly connect all the upper unused cell channels to the practical maximum cell channel, and connect all lower unused cell channels to the practical minimum cell channel. For example, if only 4 cells are used, BATT6~BATT10 should be connected together, and BATT0~BATT2 should be connected together (see Figure 3).

   Figure 3 shows the 4-cell and 8-cell series connection with the cell simulator shunt. The DC power supply voltage between BATT+ and BATT- should be decreased depending on the number of cells in series.

4-Cell Series Connection **8-Cell Series Connection**

Figure 3: 4-Cell and 8-Cell Series Connections

6. The open-wire detection and cell-balancing functions cannot be tested using the cell simulator shunt. A real battery pack is required to evaluate these features. Figure 4 shows the MP2790DFP-0000 equipment set-up with a battery pack.

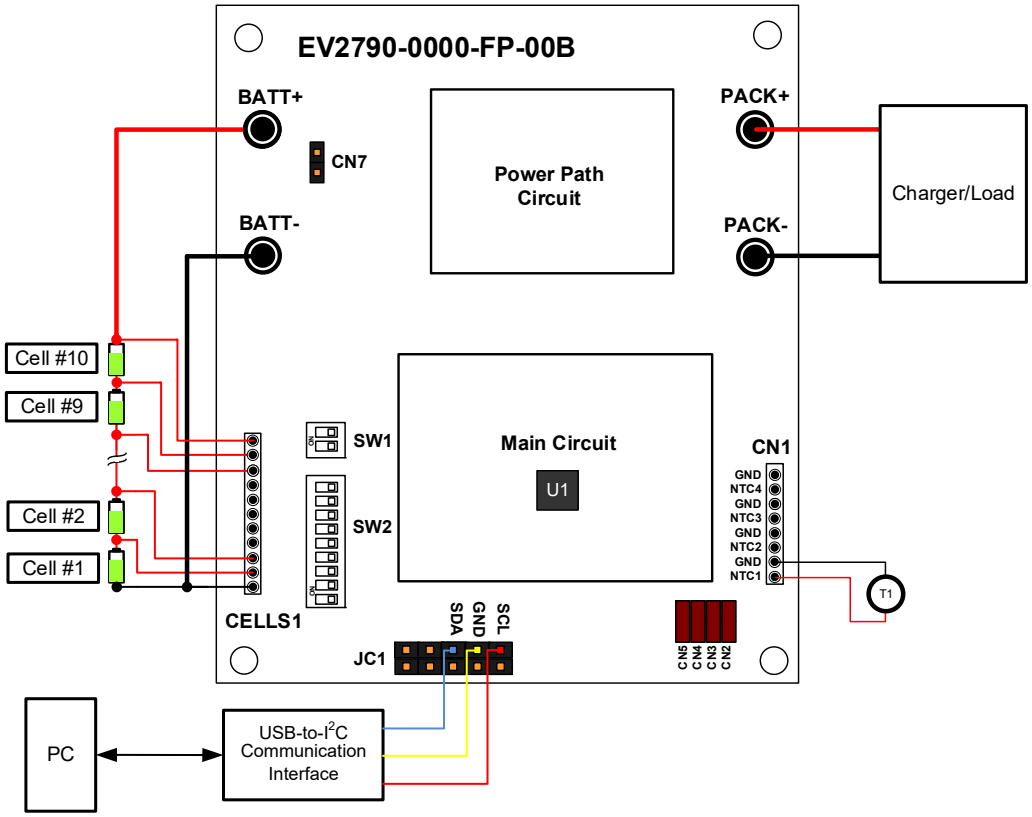


Figure 4: Equipment Set-Up for the MP2790DFP-0000 with a Battery Pack

To set up the board using a battery pack, follow the steps below:

a. Remove the CN7 jumper, then turn off the SW1 and SW2 channels.

b. If the application has fewer than 10 cells in series (but more than 5 cells), use 0Ω resistors to short all unused cell channels to the practical maximum cell channel.

c. If the application has fewer than 6 series cells, use 0Ω resistors to short all the upper unused cell channels to the practical maximum cell channel, and short all lower unused cell channels to the practical minimum cell channel.

   For example, when only 8 cells in series are used, short C8~C10 together by adding 0Ω resistors to R61~R62. When only 4 cells in series are used, short C0~C2 and C6~C16 together by adding 0Ω resistors to R60~R62, and R92~R94. If the application has 10 cells in series, skip the shorting step.

d. Connect the cell terminal (CELLS1) to each cell sensing point. If the number of cells in series is below 10, then float the connectors' higher channels.

e. Remove CN2, CN3, CN4, and CN5. Connect and locate the temperature sensors to support up to four NTCs.

f. Connect the battery terminals to:

   i. Positive (+): BATT+

   ii. Negative (-): BATT-

g. Connect the charger (or the load) terminals to:

   i. Positive (+): PACK+

   ii. Negative (-): PACK-

7. The evaluation board has bypass P-channel MOSFETs to achieve pre-charging and pre-discharging, as controlled by GPIO1 and GPIO2, respectively.

   a. In safe mode, turn on the P-channel MOSFET using GPIO2 to power PACK with low-power consumption, or turn on the P-channel MOSFET using GPIO1 to power BATT to protect the charge (CHG) MOSFETs.

   b. If this function is not used, set the GPIO1 and GPIO2 outputs to a low level. It is recommended to use GPIO2 to control the pre-discharge circuits when discharge (DSG) soft start does not work.

   c. Choose the appropriate package for the current-limit resistors, according to the maximum pre-charge and pre-discharge current (see Figure 46 on page 25).

8. Connect SDA, SCL, and GND to the USB-to-I²C communication kit. Carefully consider where SCL and SDA are positioned.

9. Connect the USB cable to the PC, turn on the computer, and launch the MP2790 GUI.

10. Figure 5 shows the main window of the MP2790 evaluation GUI. If the previous steps are correct, “MP2790 Demo board: Connected” should be displayed in the lower left corner. Otherwise, “MP2790 Demo board: Disconnected!” is displayed.

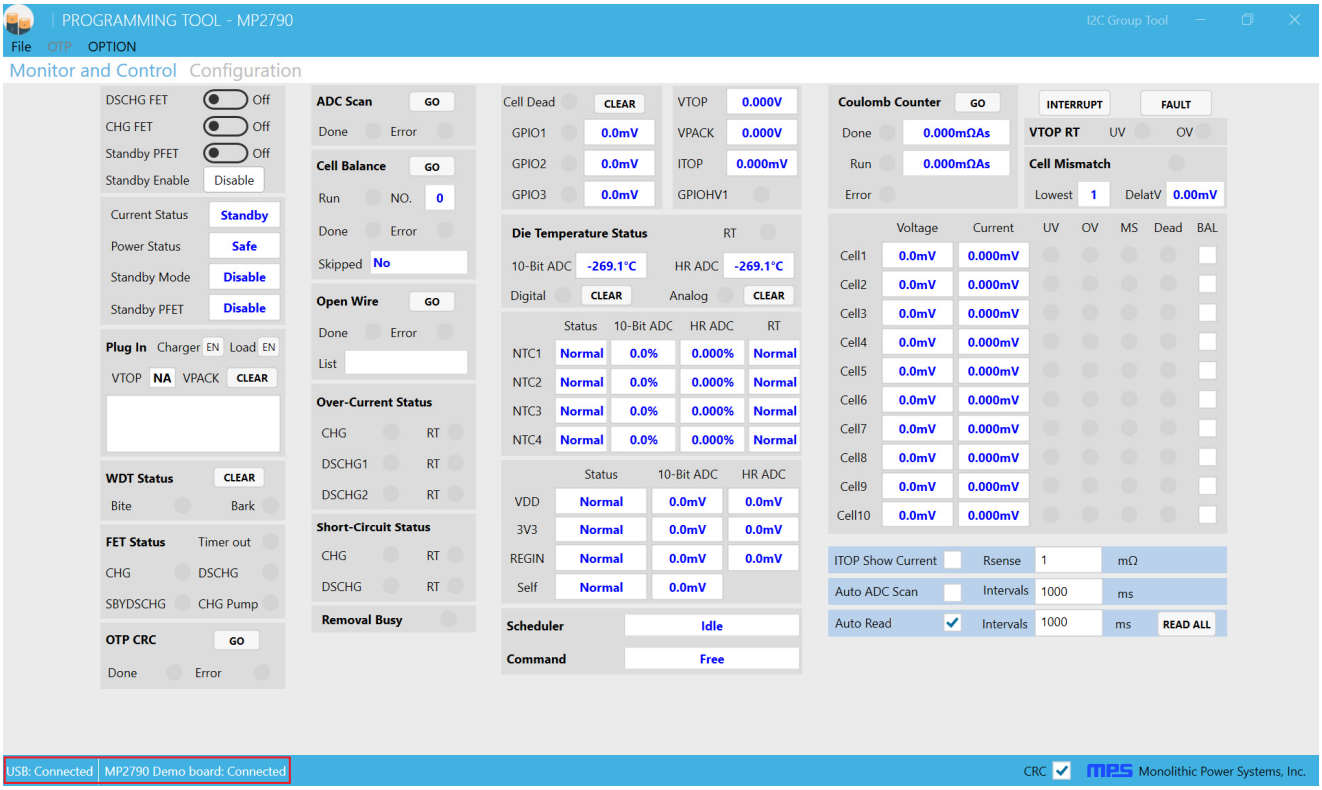


Figure 5: MP2790 Evaluation GUI

PROCEDURE

1. Ensure that all the connections (e.g. between the USB-to-I²C communication kit and the EV2790-0000-FP-00B) are successful.
2. Click on the Configuration tab to view the device configurations (see Figure 6). The software should automatically read all the configurations. Items with a lock symbol can be configured as read-only.

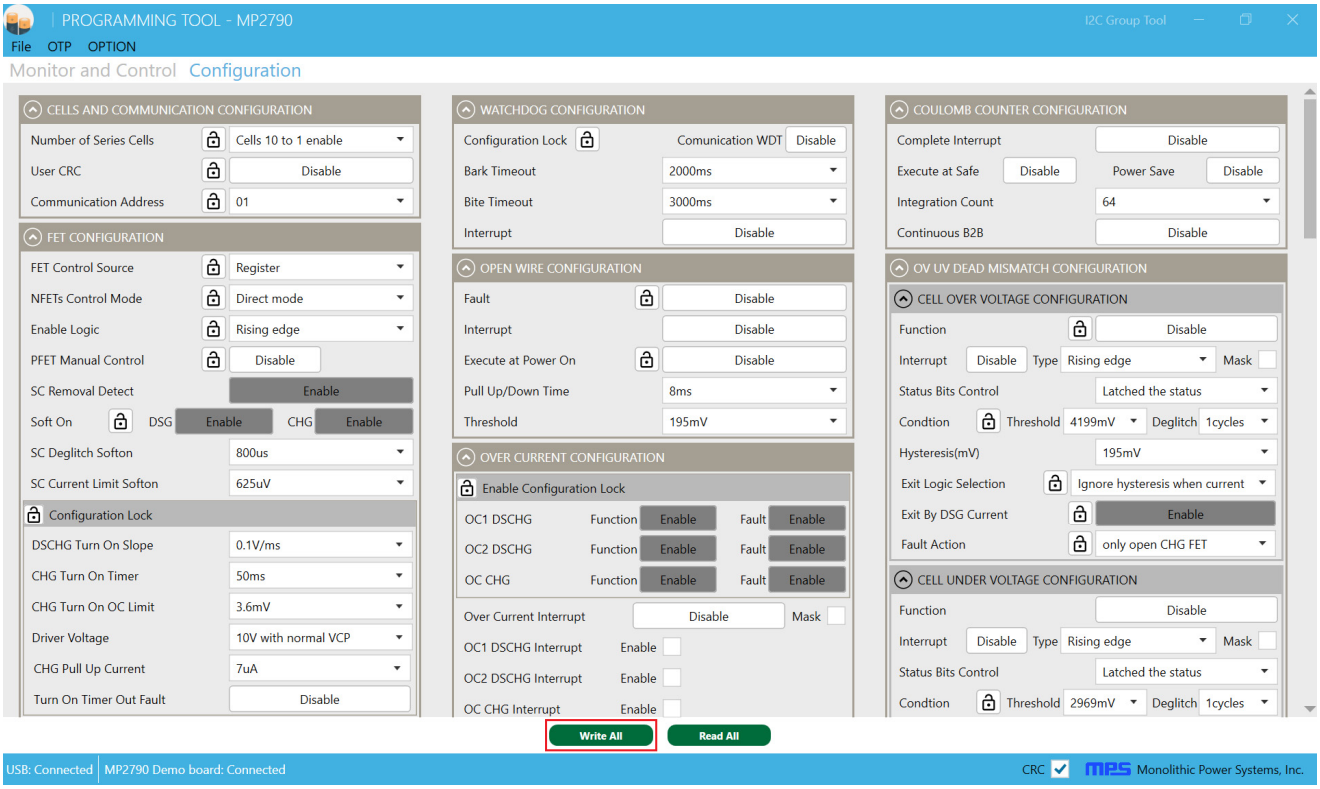


Figure 6: Configuration View

3. Configure the protection thresholds, enable all relevant functions, and set the corresponding faults.
4. Click the “Write All” button to write the configurations into the register, then click on the Monitor and Control tab to switch the view.
5. Turn the N-channel MOSFETs on.
6. Click the “Read All” button. The MOSFET status should be displayed in green for the CHG, DSG, and CHG Pump MOSFET statuses, and the power status should be set to the normal B status (see Figure 5 on page 6).
7. Click the “Go” button to scan the analog-to-digital converter (ADC) (see Figure 5 on page 6). The ADC result should be updated to the corresponding register.
8. Click the “Read All” button again. The updated values should be displayed in the GUI. If the “Auto Read” checkbox is selected, then it is not required to click the “Read All” button (see Figure 5 on page 6).

9. Figure 7 shows how to configure the cells and communication parameters.

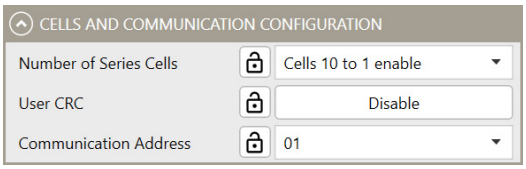


Figure 7: Cell and Communication Configuration

a. Number of Series Cells: The number of cells in series can be set between 4 and 10.

b. User CRC: To enable the cyclic redundancy check (CRC) function, select the “CRC” checkbox at the bottom right of the GUI window. Otherwise, the configuration value cannot be written to the register.

c. Communication Address: The default slave address is 01h, and the configurable communication address range is between 00h and 7Fh. After changing this value, the new address should be used for the next communication. For devices with different “-xxxx” suffixes, the default address may be different. The GUI automatically scans the address. This function can be disabled by not selecting “Monitor chip connection” under the Option tab.

10. Figure 8 shows how to configure the MOSFET parameters.

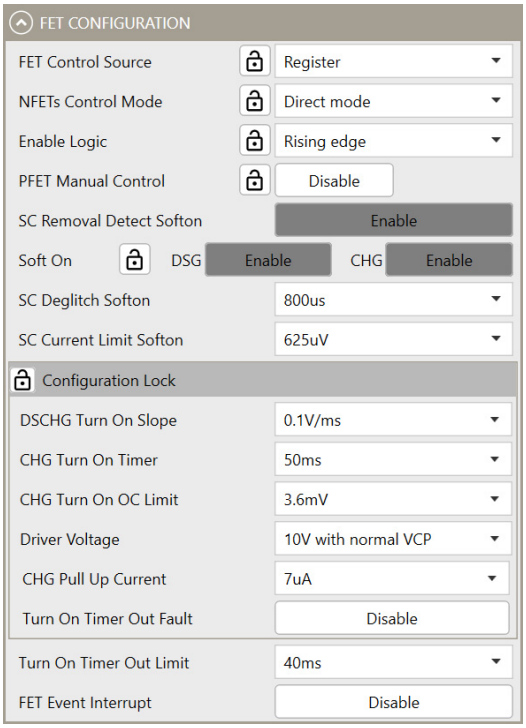


Figure 8: MOSFET Configurations

a. FET Control Source: The MOSFET control source can be set to GIPO control or register control.

b. NFETs Control Mode: The control mode of the N-channel MOSFETs can be set to simple or direct mode. In direct mode with GPIO control, GPIO1 controls the DSG MOSFET, while GPIO2 controls the CHG MOSFET.

c. Enable Logic: The enable logic can be set to rising edge active or level active.

d. SC Removal Detection Soft Start (SS): This function enables the short-circuit detection sequence that occurs before the DSG MOSFET turns on.

e. SC Deglitch SS and SC Current Limit SS: When enabled, the DSG MOSFET is protected from the inrush current when charging a large capacitive load. These two settings protect the DSG MOSFET while it ramps up during SS.

f. DSG Turn-On Slope: The DSG turn-on slope ranges between 0.1V/ms and 1.6V/ms.

g. CHG Turn-On Over-Current Limit (OCL): OCL during SS can be set to 3.6mV or 4.8mV.

h. Driver Voltage: The gate-to-source voltage (V_{GS}) for the CHG and DSG MOSFETs ranges between 5V and 7V (lower) or 7V and 12V (normal).

i. CHG Pull-Up Current: The CHG pin's output current (I_{OUT}) during the CHG soft-start time (t_{SS}) can be set 3μA and 10μA to control the CHG MOSFET driver voltage's rising slope.

11. Figure 9 shows how to configure the power status parameters.

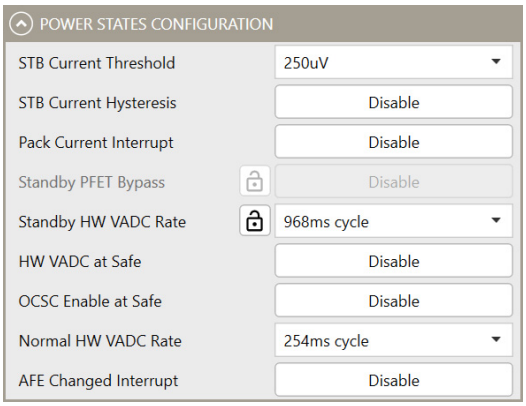


Figure 9: Power Status Configurations

a. HW VADC at Safe: If protections are required in safe mode, enable this function to ensure that the voltage can be monitored for protections.

b. Standby HW VADC Rate: The standby HW voltage ADC (VADC) rate can be used with voltage protection monitoring to refresh the ADC result while in safe or standby mode. This rate can be configured to refresh the voltage protection reading every 254ms, 492ms, or 968ms.

c. Normal HW VADC Rate: The normal HW VADC rate can be used with voltage protection monitoring to refresh the ADC result while in normal mode. This rate can be configured to refresh the voltage protection reading every 135ms or 254ms.

12. Figure 10 shows how to configure the plug-in detection parameters.

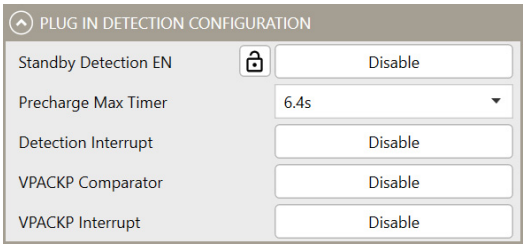


Figure 10: Plug-In Detection Configurations

a. Pre-Charge Max Timer: The PACKP pre-charge expiration timer can be set between 0.2s and 24s.

b. VPACKP Comparator: Enables the V_{PACK} vs. V_{TOP} comparator. When disabled, the comparator can still be enabled internally for other functions, such as plug-in detection.

13. Figure 11 shows how to configure the GPIOx pins (where x = 1, 2, or 3).

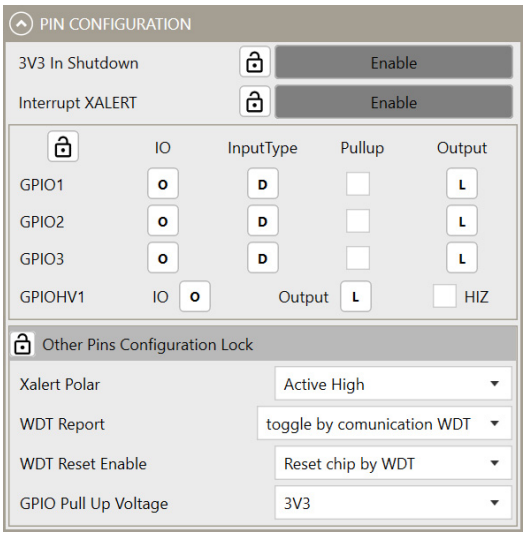


Figure 11: GPIOx Pin Configurations

a. IO: The GPIOx pins can be set to act as inputs or outputs. If they are set to inputs, they cannot be left floating and must be connected to a high or low level. Otherwise, GPIOx can consume excess power.

   GPIO2 can control the pre-discharge circuit. Pull up GPIO2 to turn on the P-channel MOSFET; set the GPIO2 output low to turn it off.

   GPIO1 can control the pre-charge circuit. Pull up GPIO1 to turn on the P-channel MOSFET and set the GPIO1 output low to turn off (see Figure 46 on page 25).

b. Input Type: Defines whether the input type for GPIO1x is a digital input or a buffered ADC input.

c. Pull-Up: Enables GPIOx's pull-up capability. When enabled, GPIOx is pulled up to 3V3 or REGIN via an internal 20kΩ resistor.

d. Output: GPIOx's target output level can be set high or low. This configuration bit is only effective when the corresponding GPIOx is used as a digital output.

e. GPIOHV1: GPIOHV1's target level can be set high or low. This configuration bit is only effective when GPIOHV1 is used as a digital output and GPIOHV1_HZ = 0. If "HIZ" is selected, then GPIOHV1 is in high-impedance (Hi-Z) mode. In this mode, the MP2790 ignores GPIOHV1_O and the GPIOHV1 output is always at Hi-Z. If "HIZ" is not selected, then GPIOHV1 is controlled in output mode following GPIOHV1_O, and its output is low.

f. GPIO Pull-Up Voltage: Sets the GPIOx pull-up voltage to 3V3 or REGIN.

14. Figure 12 shows how to configure the ADC scan parameters.

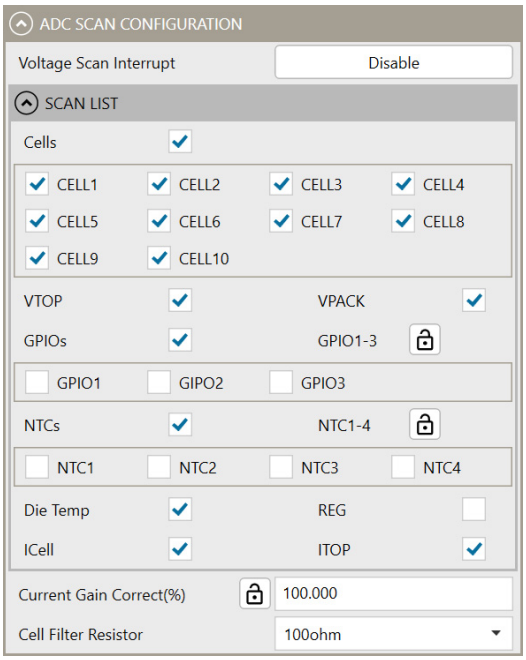


Figure 12: ADC Scan Configurations

a. Select a checkbox to enable the related parameter. If a parameter is enabled, that parameter is read and updated during the high-resolution VADC scan. If disabled, the parameter is excluded from the high-resolution VADC scan.

b. The cell ADC scan list should exclude CELL1 manually when 5 cells are enabled (CELL_S_CTRL = 4) and exclude CELL1 and CELL2 manually when 4 cells are enabled (CELL_S_CTRL = 3).

c. Current Gain Correct (%): Compensates for the sense resistor and surface-mounted technology (SMT) variation. The correction is applied to both Coulomb counting and synchronous current ADC readings. The correction is not applied to short-circuit or OC detection. The configuration range is between 87.5% and 112.476%.

d. Cell Filter Resistor: The default value is 100Ω, and the ADC cell readings are not compensated. This configuration should be set to 1kΩ when a 1kΩ filtering resistor is used (e.g. for external balancing), which compensates for the ADC cell readings to remove the drop caused by the input current during ADC conversion.

15. Figure 13 shows how to configure the watchdog.

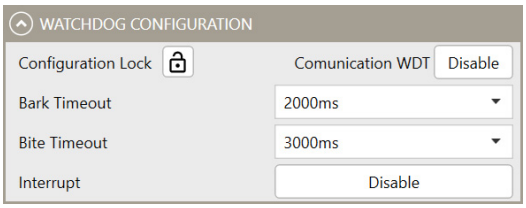


Figure 13: Watchdog Timer Configurations

a. Bark Timeout: The delay between the last watchdog reset and the interrupt bite can be set between 25ms and 3200ms.

b. Bite Timeout: The delay between the bark and watchdog timer (WDT) pulse ranges between 25ms and 3200ms.

16. Figure 14 shows how to configure open-wire parameters.

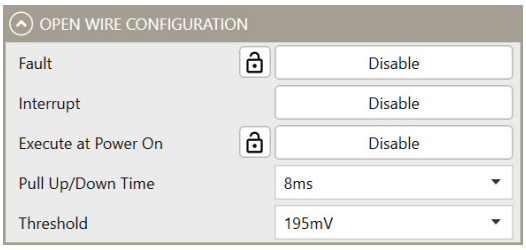


Figure 14: Open-Wire Configurations

a. Execute at Power-On: Enables open-wire detection during the start-up sequence (while exiting shutdown mode).

b. Pull-Up/-Down Time: The length of each pull-up and pull-down phase can be set between 1ms and 16ms.

c. Threshold: The open-wire detection threshold for the detection sequence can be set between 39mV and 625mV.

17. Figure 15 shows how to configure Coulomb counting.

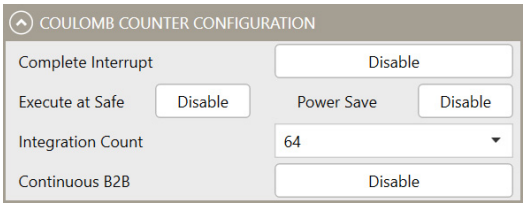


Figure 15: Coulomb Counting Configurations

a. Power Save: If enabled, the Coulomb counter operates in power-save mode; if disabled, power-save mode is not used. Power-save mode reduces overall current consumption at the expense of accuracy.

b. Integration Count: The Coulomb counter integration length sets the number of time slots, which are each 32ms. The length can be set between 1 (32ms) and 64 (2048ms). This register should only be updated when Coulomb counting is not active.

c. Continuous B2B: Enables back-to-back accumulation mode. When enabled, a new Coulomb counting conversion automatically starts after the most recent conversion is complete.

18. Figure 16 shows how to configure OC parameters.

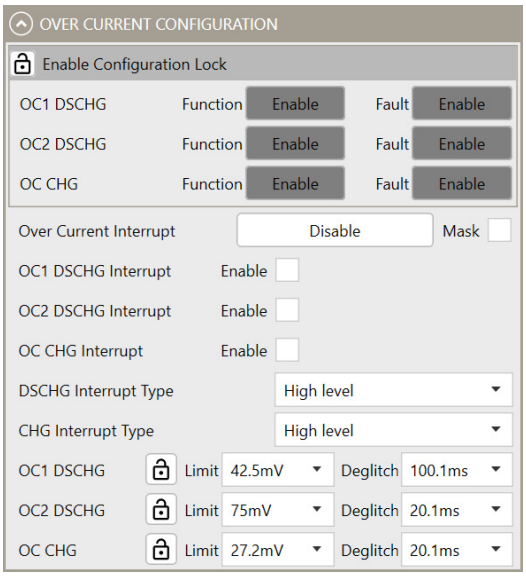


Figure 16: Over-Current Configurations

a. Select the OC interrupt “Mask” checkbox to enable this function. When enabled, the OC interrupt flag is cleared and the interrupt pin goes low, unless other interrupts are pending. When disabled, an OC condition can trigger the interrupt flag.

b. OC1 and OC2 DSCHG Limit: The 1x range can be set between 2.5mV and 80mV, while the 3x range can be set between 7.5mV and 240mV.

c. OC1 and OC2 DSCHG Deglitch: The OCx (where x = 1 or 2) DSG time ranges between 0.1ms and 2520.1ms. The external filter circuit determines whether the response time is about 100μs after the OC condition is detected.

d. OC CHG Limit: The 1x range can be set between 1.6mV and 51.2mV, while the 3x range can be set between 4.8mV and 153.6mV.

e. OC CHG Deglitch: The OC CHG deglitch time can be set between 0.1ms and 2520.1ms. The external filter circuit determines whether the response time is about 100μs after the OC condition is detected.

19. Figure 17 shows how to configure the short-circuit parameters.

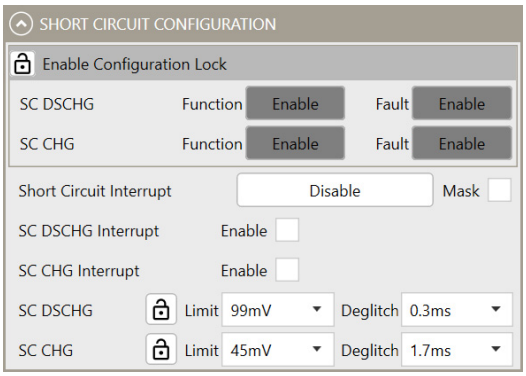


Figure 17: Short-Circuit Configurations

a. Select the short-circuit interrupt “Mask” checkbox to enable this function. When enabled, the short-circuit interrupt flag is cleared and the interrupt pin goes low, unless other interrupts are pending. When disabled, the short-circuit condition can trigger the interrupt flag.

b. SC DSCHG Limit: The 1x range can bet set between 5.5mV and 176mV, while the 3x range can be set between 16.5mV and 528mV.

c. SC DSCHG Deglitch: The short-circuit DSG deglitch time ranges between 0.1ms and 25.5ms. The external filter circuit determines whether the response time is about 100µs after the SC condition is detected.

d. SC CHG Limit: The 1x range can be set between 2.5mV and 80mV, while the 3x range can be set between 7.5mV and 240mV.

e. SC CHG Deglitch: The short-circuit CHG deglitch time ranges between 0.1ms and 25.5ms. The external filter circuit determines whether the response time is about 100µs after the SC condition is detected.

20. Figure 18 shows how to configure the short-circuit removal parameters.

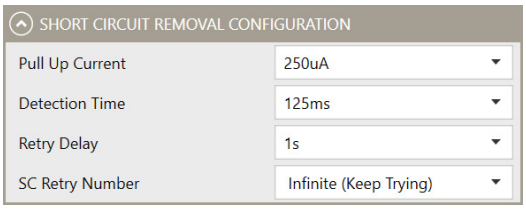


Figure 18: Short-Circuit Removal Configurations

a. Pull Up Current: The pull-up current during short-circuit removal detection can be set to 250µA, 500µA, or 750µA.

b. Detection Time: The detection time can be set to 125ms, 250ms, 500ms, or 1s.

c. Retry Delay: The retry delay between the short-circuit removal detections can be set between 1s and 25s.

d. SC Retry Number: The short-circuit retry number can be set to 1, 2, 4, or to infinite (keep trying).

21. Figure 19 shows how to configure the negative temperature coefficient (NTC), with NTCx (where x = 1, 2, 3, or 4).

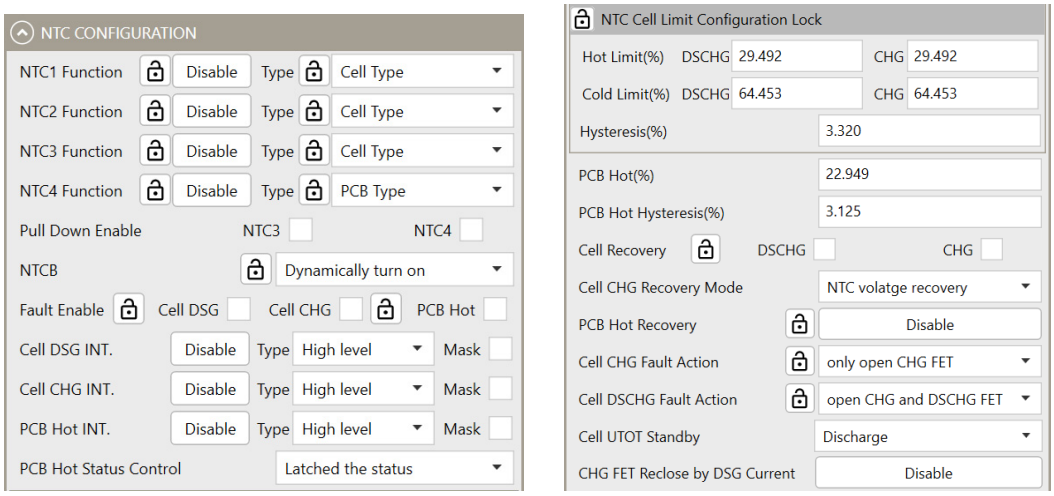


Figure 19: NTC Configurations

a. NTC Type: The NTC can be set to monitor the cells (Cell Type) or the PCB (PCB Type).

b. Pull Down Enable: Enables NTC3 and NTC4 to be pulled down.

c. NTCB: NTCB is set to dynamically turn on. NTCB is dynamically biased during ADC conversions of the NTC channels; if NTCB is continuously on, current consumption increases.

d. PCB Hot Status Control: The PCB hot status control can be set to show the latched status (which goes to the interrupt controller) or show the real-time status.

e. NTC Cell Limit: The NTC cell limit can be set to be between 0% and 99.9% of NTCB.

f. Hysteresis (%): The hysteresis can be set to be between 0% and 6.055% of NTCB.

g. Cell CHG Recovery Mode: Defines the recovery logic from NTC hot/cold conditions in charge mode. Set the NTC_CHG_REC_MODE bit to 0 for NTC voltage recovery. Set it to 1 for NTC voltage recovery or charger removed recovery.

h. Cell CHG Fault Action: Set the NTC_CELL_CHG_ACTION bit to 0 to only turn off the CHG MOSFET; if an NTC hot/cold fault occurs during charging, set the NTC_CELL_CHG_ACTION bit to 1 to turn off both the CHG and DSG MOSFETs. It is recommended to turn off the CHG MOSFET only.

i. Cell DSG Fault Action: Set the NTC_CELL_DSG_ACTION bit to 0 to only turn off the DSG MOSFET; if an NTC hot/cold fault occurs during discharging, set the NTC_CELL_DSG_ACTION bit to 1 to turn off both the CHG and DSG MOSFETs. It is recommended to turn off both MOSFETs.

j. Cell UTOT Standby: Determines if the standby current is a charge current or discharge current in response to an NTC charge or discharge fault.

k. CHG FET Reclose by DSG Current: Enables the additional recovery logic from an NTC hot/cold condition in charge mode, which allows for CHG MOSFET fault auto-recovery if $V_{PACK} < V_{TOP}$, or if the battery pack current state is set to discharge. This setting is only valid when NTC_CELL_CHG_REC = 1 and NTC_CELL_CHG_ACTION = 0.

22. Figure 20 shows how to configure the die temperature parameters.

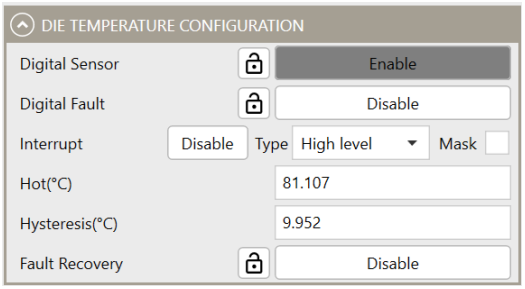


Figure 20: Die Temperature Configurations

a. Hot (°C): The resolution is 0.474°C.

b. Hysteresis (°C): The hysteresis ranges between 0°C and 14.692°C.

23. Figure 21 on page 16 shows how to configure the cell-balancing parameters.

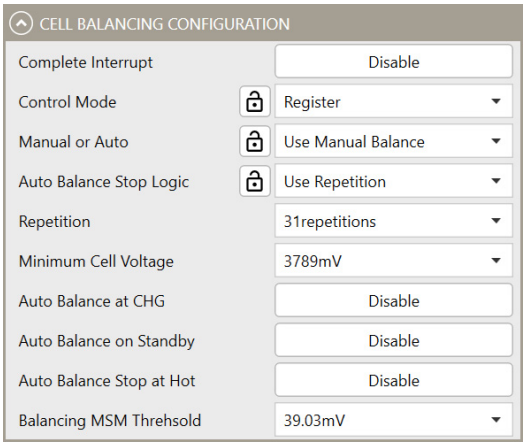


Figure 21: Cell-Balancing Configurations

a. Control Mode: The control mode can be set to register control or GIPO3 control when using automatic balancing.

b. Manual or Auto: The balancing mode can be configured for manual balancing or automatic balancing.

c. Auto-Balance Stop Logic: Only used when automatic balancing is enabled. If set to "Use Repetition," balancing uses repetition to control the number of balance iterations. If set to "Use List," balancing continues until the balancing list is empty. To stop constant automatic cell-balancing before the balancing list is empty, change this bit to disabled.

d. Repetition: The number of repetitions for each execution of the balancing list can be set between 0 and 31 repetitions. If 31 repetitions are selected, then 32 balancing cycles are executed.

e. Minimum Cell Voltage: The qualifying minimum cell voltage to run automatic balancing can be set between 2500mV and 4961mV. When a cell is below this level, it is excluded from the balancing list. All other qualifying cells can execute balancing.

f. Balancing MSM Threshold: The balancing MSM threshold is used by the automatic balancing algorithm, and can be set between 19.5mV and 87.855mV.

24. Figure 22 shows how to configure the cell OV parameters.

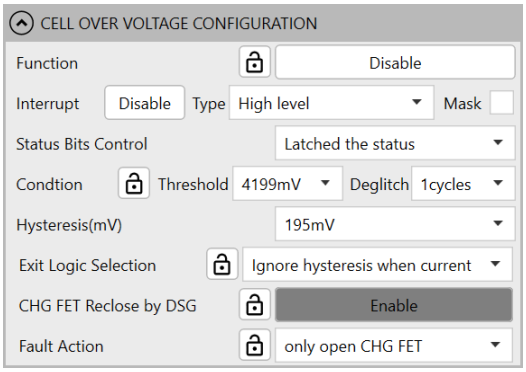


Figure 22: Cell Over-Voltage Configurations

a. Threshold: The cell OV threshold can be set between 0mV and 4980.15mV.

b. Hysteresis (mV): The OV hysteresis can be set between 0mV and 292.5mV.

c. Exit Logic Selection: The exit logic can be set to either “Ignore Hysteresis when current is discharged” or “Ignore Hysteresis when V_{PACK} < V_{TOP}”. It is recommended to choose the former logic when the fault action is set to “only open CHG FET” and “CHG FET Reclose by DSG” is enabled. Otherwise, choose the latter logic when the fault action is set to “open CHG and DSCHG FET.”

d. CHG FET Reclose by DSG: When enabled, if the battery pack’s current status is in a discharge state and the cell voltage is below the OV threshold, then the CHG MOSFET turns on.

e. Fault Action: The CHG MOSFET is off, or both MOSFETs are off.

25. Figure 23 shows how to configure the cell UV parameters.

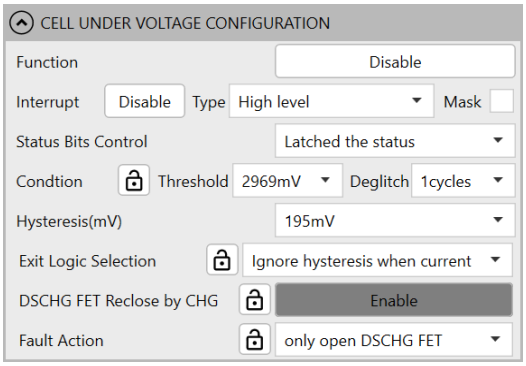


Figure 23: Cell Under-Voltage Configurations

a. Threshold: The cell UV threshold can be set between 0mV and 4980.15mV.

b. Hysteresis (mV): The UV hysteresis ranges between 0mV and 292.5mV.

c. Exit Logic Selection: The exit logic can be set to either “Ignore Hysteresis when current is charged” or “Ignore Hysteresis when V_{PACK} > V_{TOP}”. It is recommended to choose the former logic when the fault action is set to “Only open DSCHG FET” and “DSCHG FET Reclose by CHG” is enabled; otherwise, choose the latter logic when the fault action is set to “open CHG and DSCHG FET.”

d. DSCHG FET Reclose by CHG: When enabled, if the battery pack’s current status is in a charge state and the cell voltage exceeds the UV threshold, then the DSG MOSFET turns on.

e. Fault Action: The DSG MOSFET is off, or both FETs are off.

26. Figure 24 shows how to configure the cell mismatch parameters, where the cell mismatch threshold (Threshold) ranges between 0mV and 1211mV.

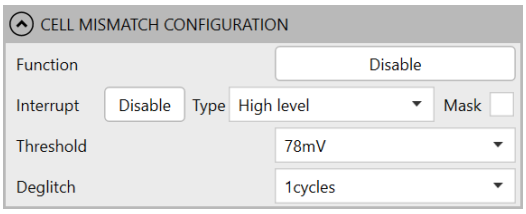


Figure 24: Cell Mismatch Configurations

27. Figure 25 shows how to configure the dead cell parameters, where the dead cell threshold (Threshold) ranges between 0mV and 2480mV.

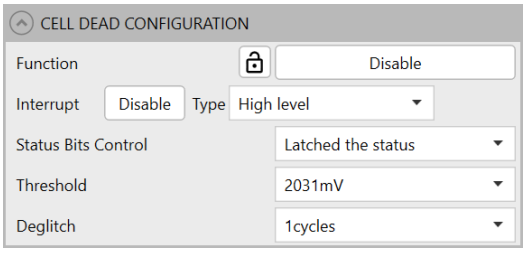


Figure 25: Dead Cell Configurations

28. Figure 26 shows how to configure the TOP pin voltage (V_{TOP}) UV parameters.

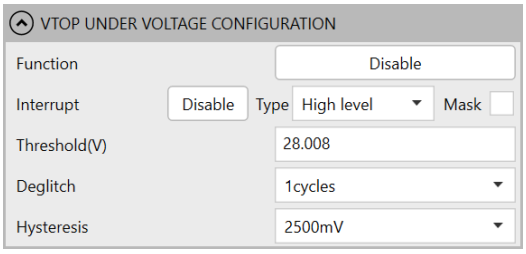


Figure 26: V_{TOP} Under-Voltage Configurations

a. Threshold (V): The V_{TOP} UV threshold can be set between 0V and 79.98V.

b. Hysteresis: The V_{TOP} hysteresis can be set between 0mV and 4922mV.

29. Figure 27 shows how to configure the V_{TOP} OV parameters.

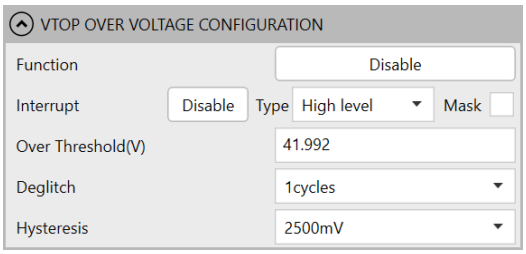


Figure 27: V_{TOP} Over-Voltage Configurations

a. OV Threshold (V): The V_{TOP} OV threshold can be set between 0V and 79.98V.

b. Hysteresis: The V_{TOP} hysteresis can be set between 0mV and 4922mV.

30. Figure 28 shows how to configure the REGIN, 3V3, VDD, and ADC self-test checks.

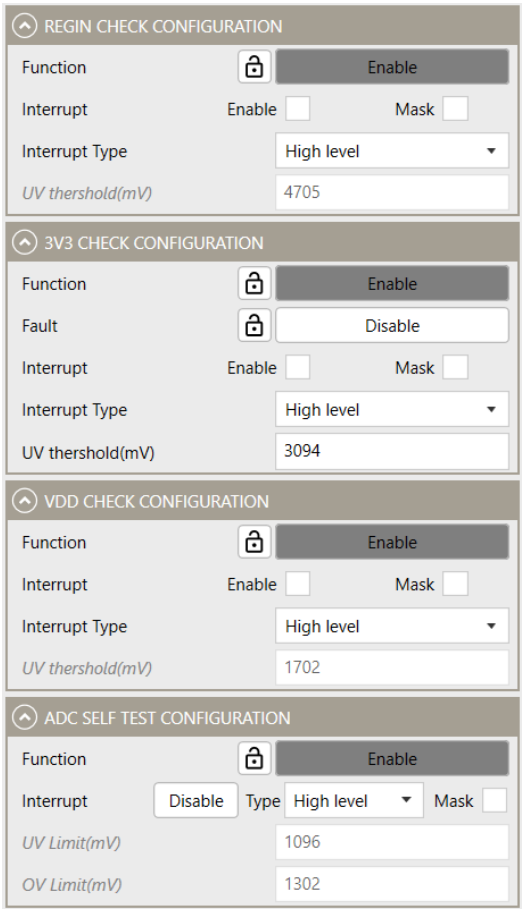


Figure 28: REGIN, 3V3, VDD, ADC Self-Test Check Configuration

31. Figure 29 shows how to configure the non-volatile memory (NVM) CRC.

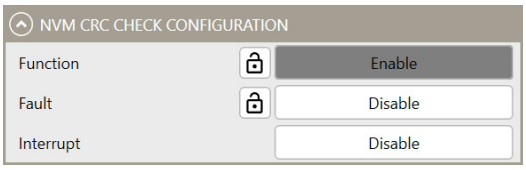


Figure 29: NVM CRC Configuration

32. Figure 30 shows how to configure direct mode MOSFET control.

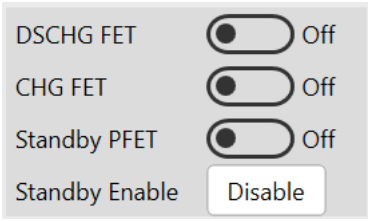


Figure 30: Direct Mode MOSFET Control

33. Figure 31 shows how to configure simple mode MOSFET control. Modify the control mode on the configuration tab, and then the options on the control tab change accordingly.

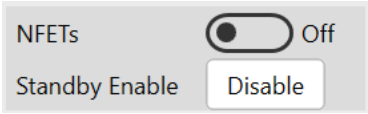


Figure 31: Simple Mode MOSFET Control

34. Figure 32 shows how to configure the status monitor.

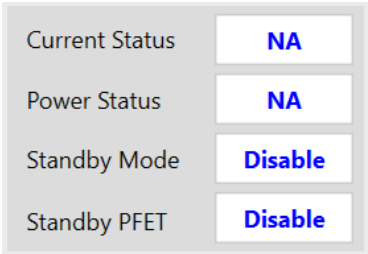


Figure 32: Status Monitor

35. Figure 33 shows how to configure the plug-in detection control and monitor.

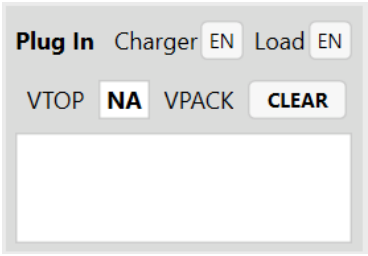


Figure 33: Plug-In Detection Control and Monitor

36. Figure 34 shows the watchdog status monitor.

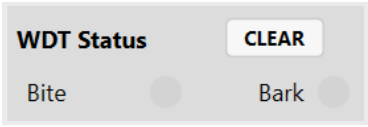


Figure 34: Watchdog Status Monitor

37. Figure 35 shows the MOSFET status monitor.

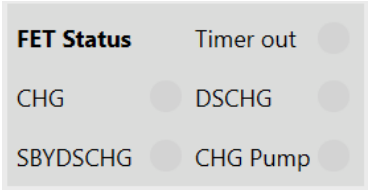


Figure 35: MOSFET Status Monitor

38. Figure 36 shows how to configure the ADC, cell-balancing, and the open-wire control and monitor.

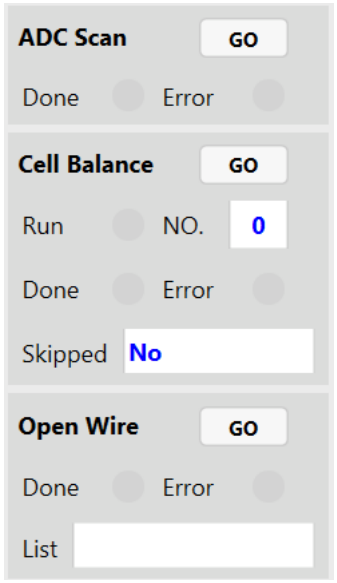


Figure 36: ADC, Cell-Balancing, and Open Wire Control and Monitor

39. Figure 37 shows the OC and short-circuit status monitor.

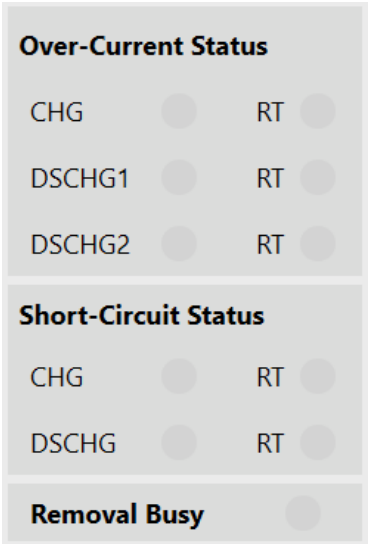


Figure 37: Over-Current and Short-Circuit Status Monitor

40. Figure 38 shows the GPIO and V_{TOP} status monitor.

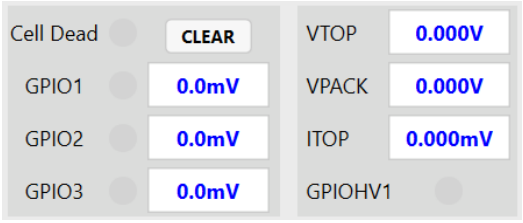


Figure 38: GPIO and V_{TOP} Status Monitor

41. Figure 39 shows the die temperature monitor.

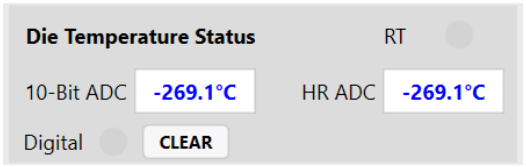
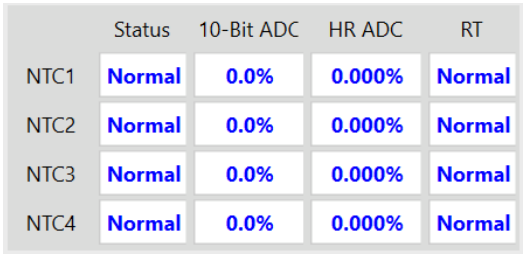


Figure 39: Die Temperature Monitor

42. Figure 40 shows the NVM CRC monitor.

Figure 40: NVM CRC Monitor

43. Figure 41 shows the NTC monitor.



	Status	10-Bit ADC	HR ADC	RT
NTC1	Normal	0.0%	0.000%	Normal
NTC2	Normal	0.0%	0.000%	Normal
NTC3	Normal	0.0%	0.000%	Normal
NTC4	Normal	0.0%	0.000%	Normal

Figure 41: NTC Monitor

44. Figure 42 shows the NTC functional block diagram.

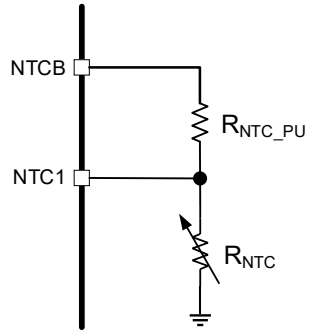


Figure 42: NTC Functional Block Diagram

The NTC resistance (R_{NTC}) can be estimated with Equation (1):

$$R_{NTC}=\frac{A \times R_{NTC\_PUP}}{32768 - A} \quad (1)$$

Where *A* is the NTC ADC reading, and R_{NTC_PU} is the NTC pull-up resistor (10kΩ is recommended).

The ambient temperature (T, in Kelvin) can be calculated with Equation (2):

$$T=\frac{1}{\frac{1}{T_0}+\frac{1}{B}\ln\frac{R_{NTC}}{R_0}} \quad (2)$$

Where R_0 is the NTC resistance when the ambient temperature is T_0 (in Kelvin), and *B* is the thermistor constant (in Kelvin).

For example, if the NTC ADC reading (*A*) is 9830 (0x2666) for the thermistor NCP18XH103, R_0 is 10kΩ at 25°C (298.15K), and *B* is 3380K, then R_{NTC} = 4.285kΩ and T = 322K. This means that if the NTC ADC reading is 9830, then the ambient temperature is about 49°C.

45. Figure 43 shows the low-dropout (LDO) monitor.

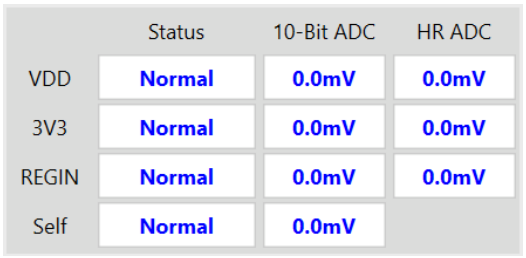


Figure 43: LDO Monitor

46. Figure 44 shows the cell ADC monitor.

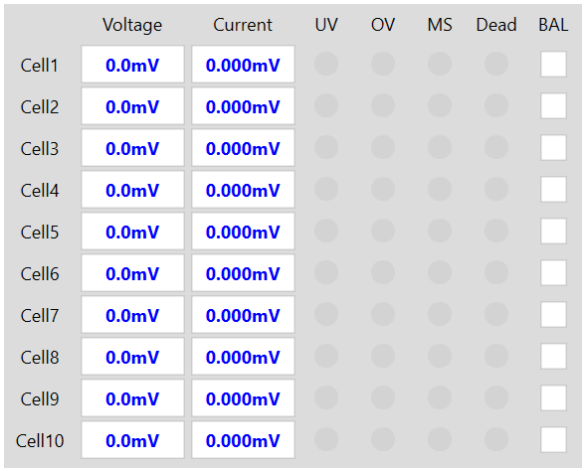


Figure 44: Cell ADC Monitor

EVALUATION BOARD SCHEMATICS

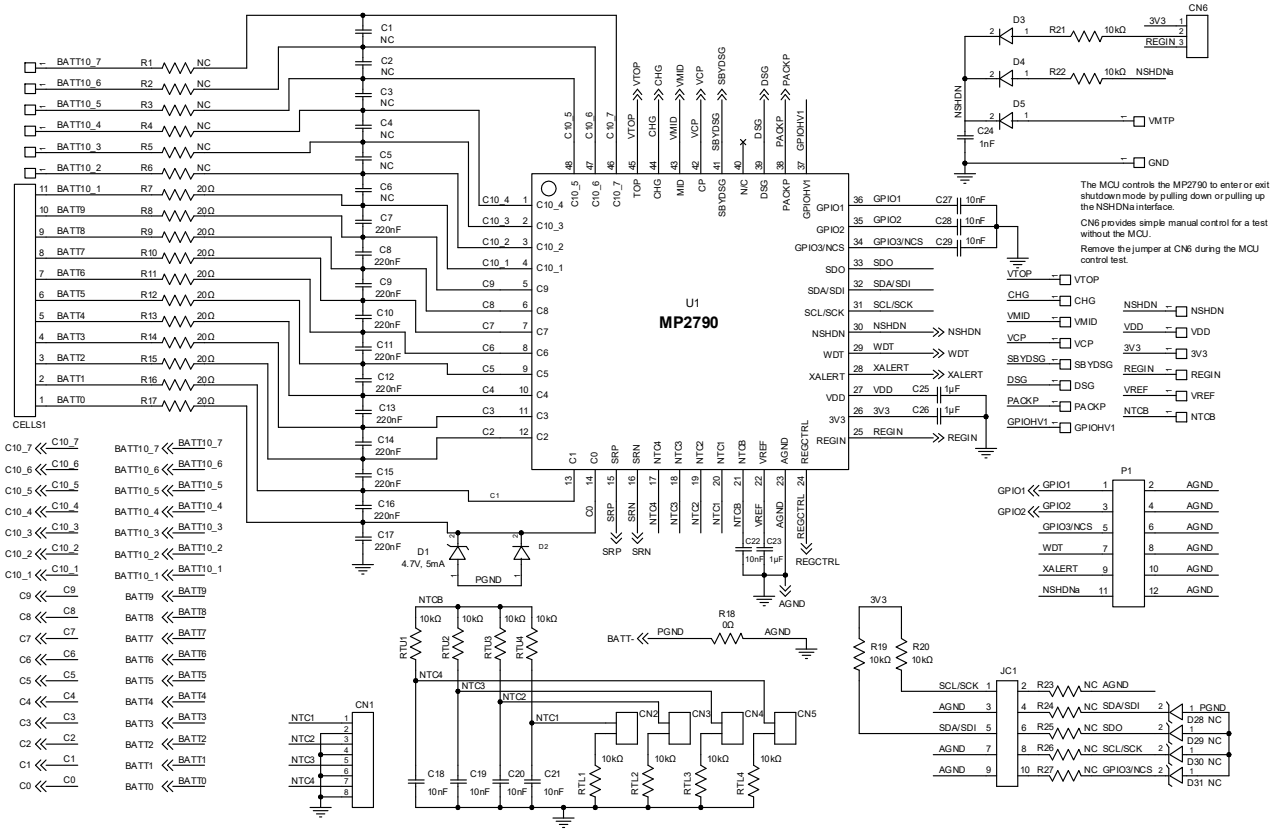


Figure 45: Evaluation Board Schematic (IC and Connector)

EVALUATION BOARD SCHEMATICS *(continued)*

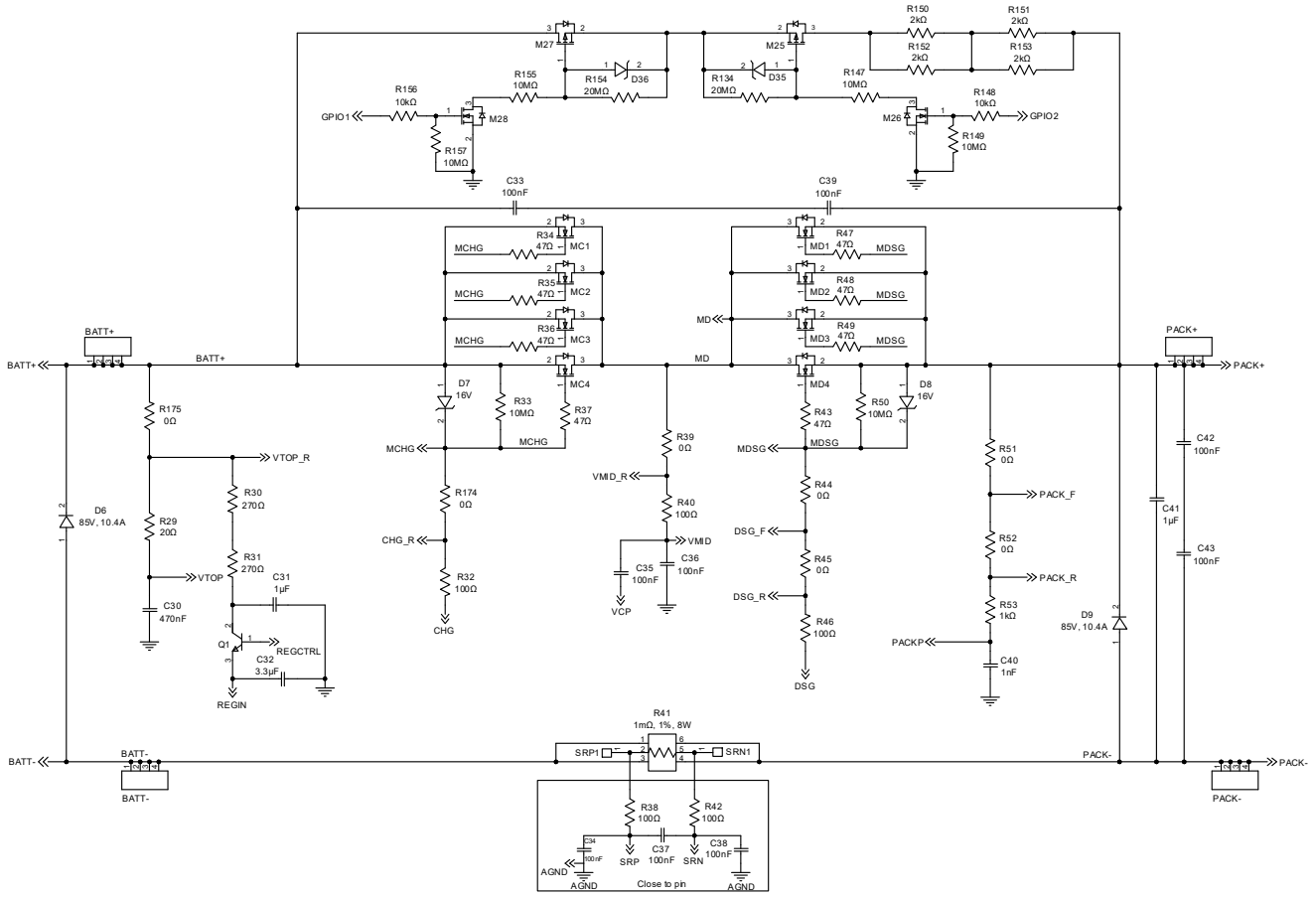


Figure 46: Evaluation Board Schematic (Power Path)

EVALUATION BOARD SCHEMATICS *(continued)*

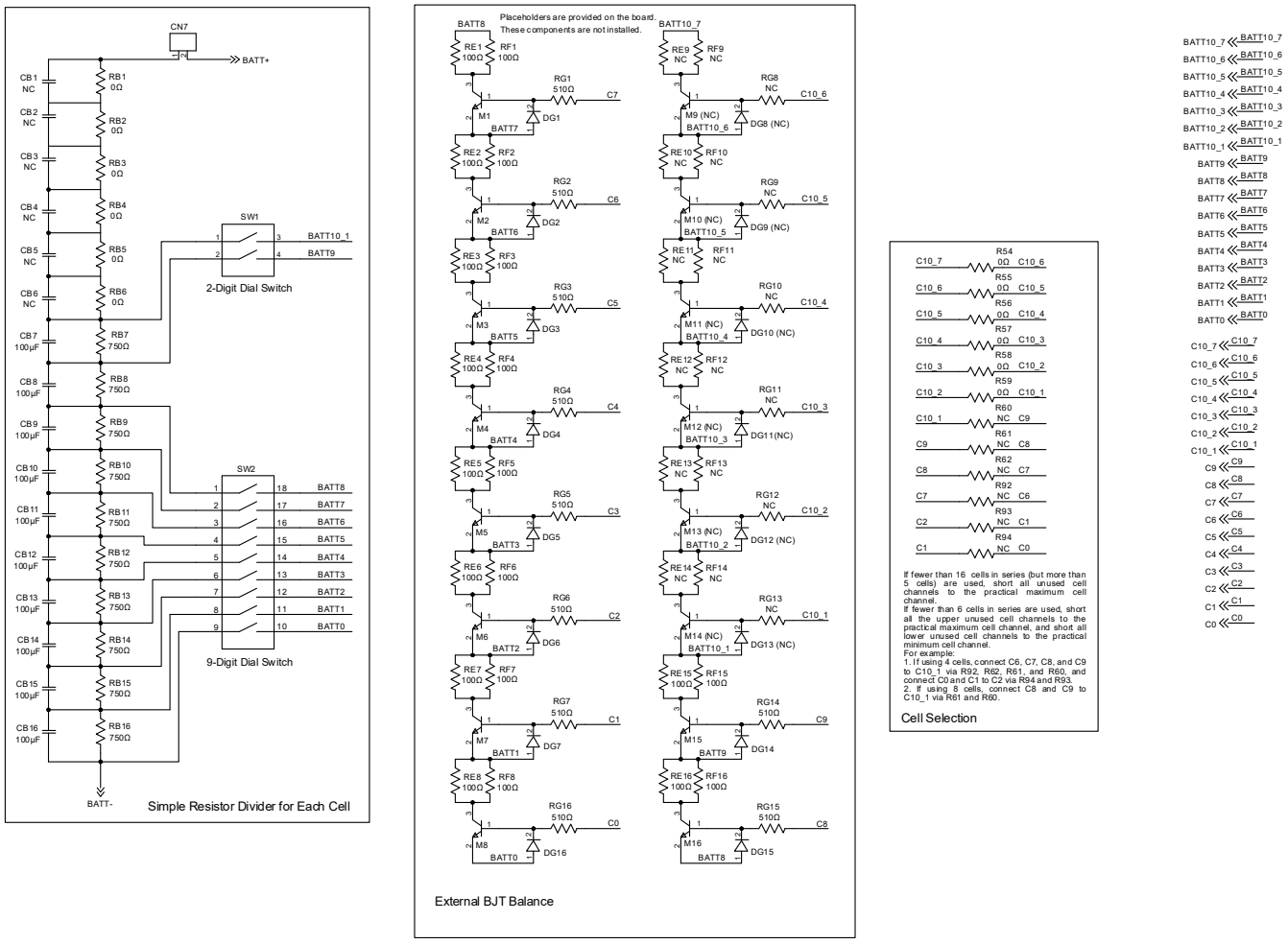


Figure 47: Evaluation Board Schematic (Battery Connection)

EVALUATION BOARD SCHEMATICS *(continued)*

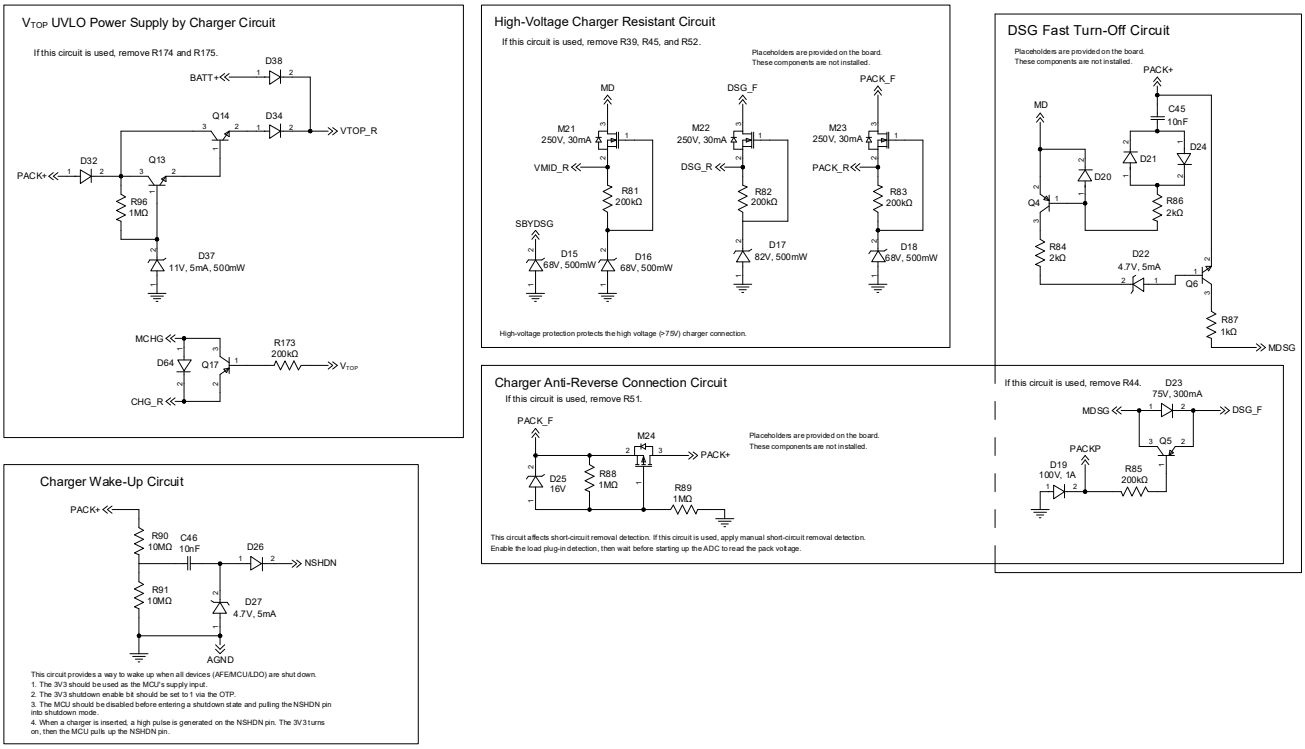


Figure 48: Evaluation Board Schematic (Additional Circuit)

EV2790-0000-FP-00B BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
4	PACK-, PACK+, BATT-, BATT+	12mmx 18mm	Connector	DIP	Zhengyou	PCB_50
10	CB7, CB8, CB9, CB10, CB11, CB12, CB13, CB14, CB15, CB16	100µF	Capacitor, 6.3V, X6T	1206	Murata	GRM31CD80J107 ME39L
1	CN1	2.54mm	8-pin connector	DIP	Wurth	691210910008
5	CN2, CN3, CN4, CN5, CN7	2.54mm	2-pin connector	DIP	Wurth	60900213421
1	CN6	2.54mm	3-pin connector	DIP	Wurth	60900213421
1	CELLS1	3.5mm	11-pin connector	DIP	KEFA	KF2EDGR-3.5-11P
11	C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17	220nF	Capacitor, 50V, X7R	0603	Murata	GRM188R71H224K AC4D
8	C18, C19, C20, C21, C22, C27, C28, C29	10nF	Capacitor, 25V, X7R	0603	Wurth	885012206065
3	C23, C25, C26	1µF	Capacitor, 16V, X7R	0603	Wurth	885012206052
2	C24, C40	1nF	Capacitor, 100V, X7R	0603	Murata	GRM188R72A102K A01D
1	C30	470nF	Capacitor, 100V, X7R	0805	Murata	GRM21BR72A474K A73L
2	C31, C41	1µF	Capacitor, 100V, X7R	1206	Murata	GRM31CR72A105 KA01L
1	C32	3.3µF	Capacitor, 16V, X5R	0805	Murata	GRM21BR61C335 KA88
9	C33, C34, C35, C36, C37, C38, C39, C42, C43	100nF	Capacitor, 100V, X7R	0603	Wurth	885012206120
1	C46	10nF	Capacitor, 250V, X7R	0805	Murata	GRM21BR72E103K W03
2	D1, D27	4.7V	Zener diode, 5mA	SOD-323	Diodes, Inc.	BZT52C4V7S
4	D2, D3, D4, D5	30V	Schottky diode, 0.5A	SOD-123	JCET	B0530W
2	D6, D9	85V	TVS diode, 10.4A	DO-214AB	Diodes, Inc.	SMCJ85A-13-F
4	D7, D8, D35, D36	16V	Zener diode, 5mA/500mW	SOD-123	Diodes, Inc.	BZT52C16-7-F
3	D32, D34, D38	75V	Diode, 0.15A	SOD-123	JCET	1N4148W
2	D26, D64	75V	Diode, 300mA	SOD-323	Diodes, Inc.	1N4148WS
1	D37	11V	Zener diode, 5mA/500mW	SOD-123	Diodes, Inc.	BZT52C11

EV2790-0000-FP-00B BILL OF MATERIALS *(continued)*

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	JC1	2.54mm	2 x 5-pin connector	DIP	Wurth	61201021621
8	MD1, MC1, MD2, MC2, MD3, MC3, MD4, MC4	100V	N-channel MOSFET, 3.6mΩ, 90nC, 120A	TO-263	Crmicro	CRSS042N10N
2	M25, M27	-100V	P-channel MOSFET, 3.7nC, 1300mΩ, 1A	SOT-23	Analog Power	AM2371P-T1-PF
2	M26, M28	100V	N-channel MOSFET, 6000mΩ, 170mA	SOT-23	Analog Power	LBSS123LT1G
1	P1	2.54mm	2 x 6-pin connector	DIP	Any	2X6_180D_2.54mm
1	Q1	100V	Transistor, NPN, 6A, 3W	SOT-23	Zetex	FZT853TA
2	Q13, Q14	80V	Transistor, 0.5A, NPN	SOT-23	onsemi	MMBTA06LT1G
1	Q17	-80V	Transistor, 0.5A, PNP	SOT-23	onsemi	MMBTA56LT1G
10	RB7, RB8, RB9, RB10, RB11, RB12, RB13, RB14, RB15, RB16	750Ω	Film resistor, 1%	0603	Yageo	RC0603FR-07750RL
3	R32, R40, R46	100Ω	Film resistor, 1%	1206	Yageo	RC1206FR-07100RL
14	RTU1, RTL1, RTU2, RTL2, RTU3, RTL3, RTU4, RTL4, R19, R20, R21, R22, R148, R156	10kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710KL
12	R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R29	20Ω	Film resistor, 1%	1206	Yageo	RC1206FR-0720RL
2	R30, R31	270Ω	Film resistor, 5%	2512	Yageo	RC2512JK-07270RL
8	R33, R50, R90, R91, R147, R149, R155, R157	10MΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710ML
8	R34, R35, R36, R37, R43, R47, R48, R49	47Ω	Film resistor, 1%	0603	Yageo	RC1206FR-0747RL
2	R38, R42	100Ω	Film resistor, 1%	0603	Yageo	RC0603FR-07100RL
20	RB1, RB2, RB3, RB4, RB5, RB6, R18, R39, R44, R45, R51, R52, R54, R55, R56, R57, R58, R59, R174, R175	0Ω	Film resistor, 5%	0603	Yageo	RC0603FR-070RL

EV2790-0000-FP-00B BILL OF MATERIALS *(continued)*

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	R41	1mΩ	Current-sense resistor, 1%	3920	Bourns	CSS2H-3920R-1L00F
1	R53	1kΩ	Film resistor, 5%	1206	Yageo	RC1206JR-071KL
1	R173	200kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-07200KL
1	R96	1MΩ	Film resistor, 1%	0603	Yageo	RC0603FR-071ML
2	R134, R154	20MΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0720ML
4	R150, R151, R152, R153	2kΩ	Film resistor, 5%	2512	Yageo	RC2512JK-072KL
1	SW1	2-pin switch	Button	SMD	Any	418121270802
1	SW2	9-pin switch	Button	SMD	Any	418121270809
1	U1	MP2790DFP-0000	4-cell to 10-cell, high-accuracy battery monitoring and protection IC with Coulomb counting	TQFP-48 (7mmx 7mm)	MPS	MP2790DFP-0000

EV2790-0000-FP-00B BILL OF MATERIALS *(continued)*

Recommended components for the external BJT balancing circuit (components not Installed on the standard board).

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
10	M1, M2, M3, M4, M5, M6, M7, M8, M15, M16	80V	Transistor, 0.5A, NPN	SOT-23	onsemi	MMBTA06LT1G
20	RF1, RE1, RF2, RE2, RF3, RE3, RF4, RE4, RF5, RE5, RF6, RE6, RF7, RE7, RF8, RE8, RF15, RE15, RF16, RE16	100Ω	Film resistor, 1%	1206	Yageo	RC1206FR-07100RL
10	RG1, RG2, RG3, RG4, RG5, RG6, RG7, RG14, RG15, RG16	510Ω	Film resistor, 1%	0603	Yageo	RC0603FR-07510RL
10	DG1, DG2, DG3, DG4, DG5, DG6, DG7, DG14, DG15, DG16	75V	Diode, 0.15A	SOD-323	JCET	1N4148WS

EV2790-0000-FP-00B BILL OF MATERIALS *(continued)*

Recommended components for the DSG fast turn-off and charger anti-reverse connection circuit (components not installed on the standard board).

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	C45	10nF	Capacitor, 250V, X7R	0805	Murata	GRM21BR72E103KW03
4	D20, D21, D23, D24	75V	Diode, 300mA	SOD-323	Diodes, Inc.	1N4148WS
1	D25	16V	Zener diode, 5mA/500mW	SOD-123	Diodes, Inc.	BZT52C16-7-F
1	D19	100V	Schottky diode, 1A	SOD-123-2	ST	BAT41ZFILM
1	D22	4.7V	Zener diode, 5mA	SOD-323	Diodes, Inc.	BZT52C4V7S
1	M24	-100V	P-channel MOSFET, 3.7nC, 1300mΩ, 1A	SOT-23	Analog Power	AM2371P-T1-PF
2	Q4, Q5	-80V	Transistor, 0.5A, PNP	SOT-23	onsemi	MMBTA56LT1G
1	Q6	80V	Transistor, 0.5A, NPN	SOT-23	onsemi	MMBTA06LT1G
1	R85	200kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-07200KL
1	R87	1kΩ	Film resistor, 1%	1206	Yageo	RC1206FR-0747RL
2	R84, R86	2kΩ	Film resistor, 1%	0805	Yageo	RC0805FR-072KL
2	R88, R89	1MΩ	Film resistor, 1%	0603	Yageo	RC0603FR-071ML

EV2790-0000-FP-00B BILL OF MATERIALS *(continued)*

Recommended components for the high-voltage charger resistant circuit (components not installed on the standard board).

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
3	D15, D16, D18	68V	Zener diode, 1.8mA	SOD-123-2	onsemi	MMSZ5266BT1G
1	D17	82V	Zener diode, 1.5mA	SOD-123-2	onsemi	MMSZ5268BT1G
3	R81, R82, R83	200kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-07200KL
3	M21, M22, M23	250V	N-channel MOSFET, 7.8mΩ, 2.3nC, 30mA	SOT-23	Infineon	BSS139H6327

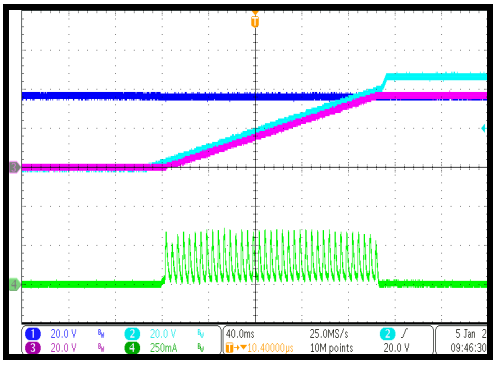
EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board. V_{TOP} = 37.5V, T_A = 25°C, unless otherwise noted.

DSG Soft Start

PACK+ is connected to a 1mF capacitor,
DSG slope = 0.2V/ms

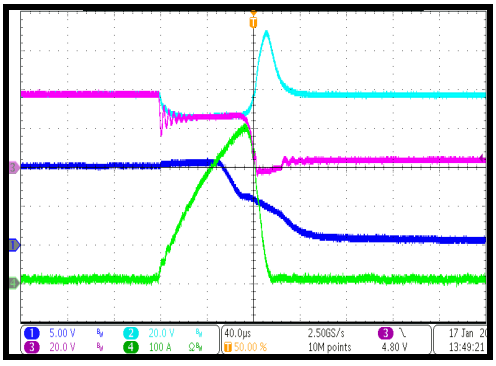
CH1: V_{MID}
CH2: V_{DSG}
CH3: V_{PACK+}
CH4: I_{TOP}



DSG Fast-Off in Short Circuit

$R_{SRP-SRN}$ = 1mΩ,
short-circuit threshold = 55mV,
deglitch off, four paralleled CRSS042N10N devices act as the DSG N-channel MOSFETs (typical C_{ISS} = 27088pF)

CH3: V_{PACK+}
CH2: V_{MID}
CH1: V_{GS-DSG}
CH4: I_{TOP}



PCB LAYOUT

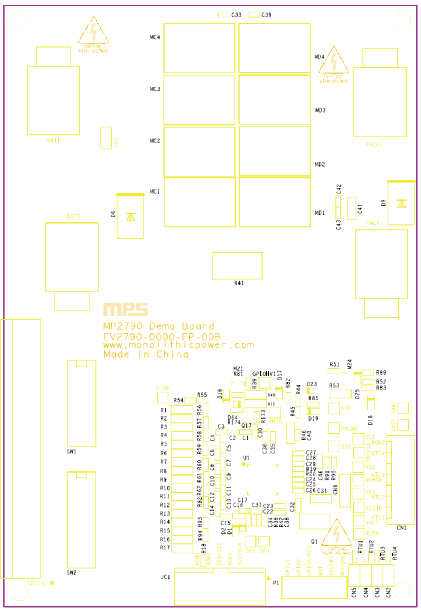


Figure 49: Top Silk

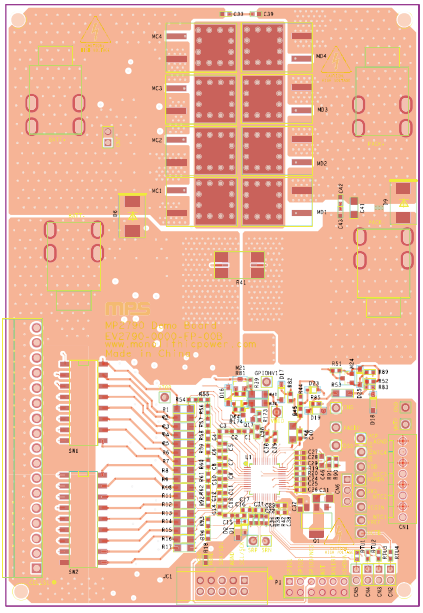


Figure 50: Top Layer

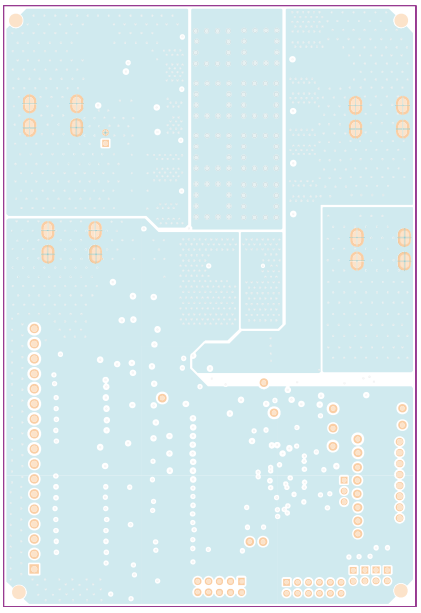


Figure 51: Mid-Layer 1

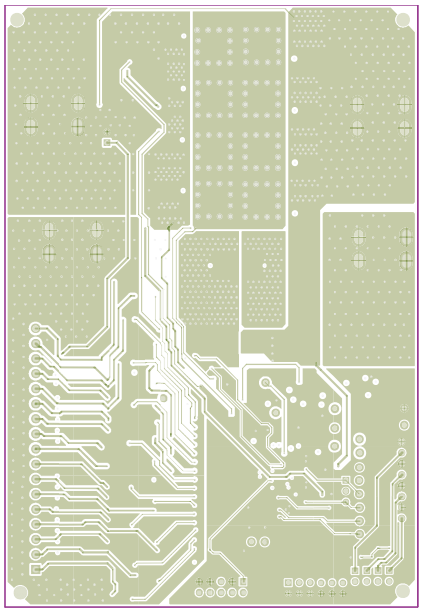


Figure 52: Mid-Layer 2

PCB LAYOUT *(continued)*

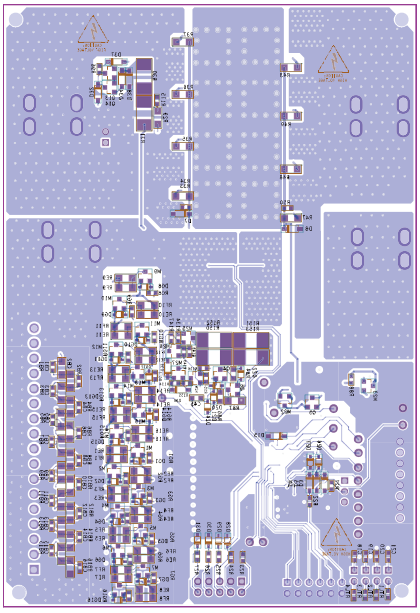


Figure 53: Bottom Layer

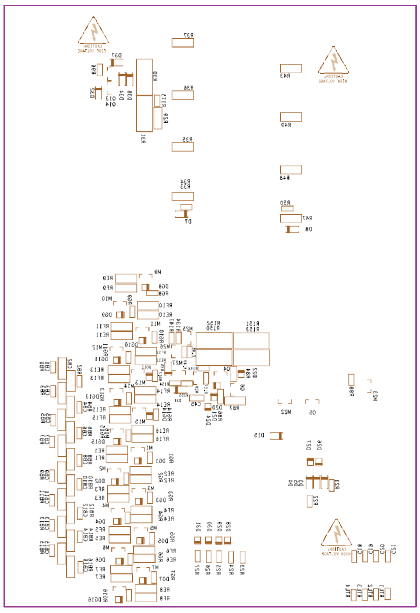


Figure 54: Bottom Silk

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	8/2/2024	Initial Release	-