



EV2702-RP-00A

26V, 1A, Linear Charger

with Configurable JEITA and EN Control

Evaluation Board

DESCRIPTION

The EV2702-RP-00A is an evaluation board designed to demonstrate the capabilities of the MP2702, a 26V, 1A, highly integrated linear charger for Li-ion and Li-polymer batteries.

The MP2702 has a dedicated ISET pin to set the charge current (I_{CC}) by connecting a resistor from this pin to ground. The USBM pin sets the input current limit (I_{IN_LIM}) prior to setting I_{CC} . The MP2702 also has a minimum input voltage limit (V_{IN_LIM}) to reduce I_{CC} when the input power is overloaded.

The MP2702 has a dedicated EN pin to enable or disable charging. After charging is disabled, the quiescent current in either the IN or BATT pin is minimized.

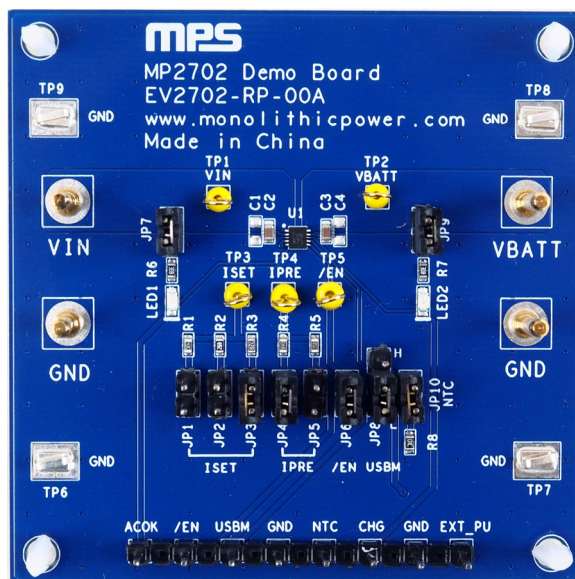
The MP2702 supports a fully customizable JEITA profile with configurable temperature windows and actions.

The EV2702-RP-00A supports an operating voltage up to 6V, and its absolute maximum input voltage (V_{IN}) can be up to 26V.

PERFORMANCE SUMMARY

Parameters	Conditions	Value
Input voltage (V_{IN}) range		4V to 6V
Battery charge regulation voltage (V_{BATT_REG})	$V_{IN} = 5V$	4.2V
Charge current (I_{CC})	$V_{BATT} = 4V$	0.02A to 1A

EVALUATION BOARD



LxWxH (6.3cmx6.3cmx1.3cm)

Board Number	MPS IC Number
EV2702-RP-00A	MP2702GRP

QUICK START GUIDE

The EV2702-RP-00A evaluation board is designed for the MP2702 as a single-cell linear charger. Its layout accommodates most commonly used capacitors. The charge-full voltage is preset to 4.2V.

Table 1 lists the jumper set-ups for the EV2702-RP-00A.

Table 1: Jumper Installations

Jumper	Description	Factory Setting
JP1	ISET resistor selection 1: $I_{CC} = 20\text{mA}$	Off
JP2	ISET resistor selection 2: $I_{CC} = 300\text{mA}$	Off
JP3	ISET resistor selection 3: $I_{CC} = 1\text{A}$	On
JP4	IPRE resistor selection 1: $I_{PRE} = 10\%$ of I_{CC}	On
JP5	IPRE resistor selection 2: $I_{PRE} = 20\%$ of I_{CC}	Off
JP6	External /EN pin control: pull low or float to enable charging	On
JP7	/ACOK pull-up	On
JP8	External USBM pin control	Low
JP9	/CHG pull-up	On
JP10	NTC setting: fixed 10k Ω pull-down	On

Start-Up Procedure

To set up the EV2702-RP-00A, refer to Figure 1 on page 3 and follow the guidelines below:

- Set the battery simulator output to be between 0V and 4.2V with a current limit at 3A, then turn off the battery simulator output.
- Set the DC power source to 5V with an output current limit set to 2A, then turn off the DC power source.
- Connect the battery simulator terminals to:
 - Positive (+): VBATT
 - Negative (-): GND
- Connect the DC power source terminals to:
 - Positive (+): VIN
 - Negative (-): GND
- Set the fast charge current using JP1, JP2, and JP3.
- Set the pre-charge current using JP4 and JP5.
- Set the input current limit (I_{IN_LIM}) using JP8 (USBM). Connect JP8 to logic low to follow the ISET setting. Connect JP8 to logic high to set I_{IN_LIM} to 500mA. Float JP8 to set I_{IN_LIM} to 100mA. If connecting JP8 to high logic, an external 3V pull-up voltage must be connected between EXT_PU and GND on the board.
- Turn on the battery simulator.
- Turn on the DC power source. The IC should start up automatically.

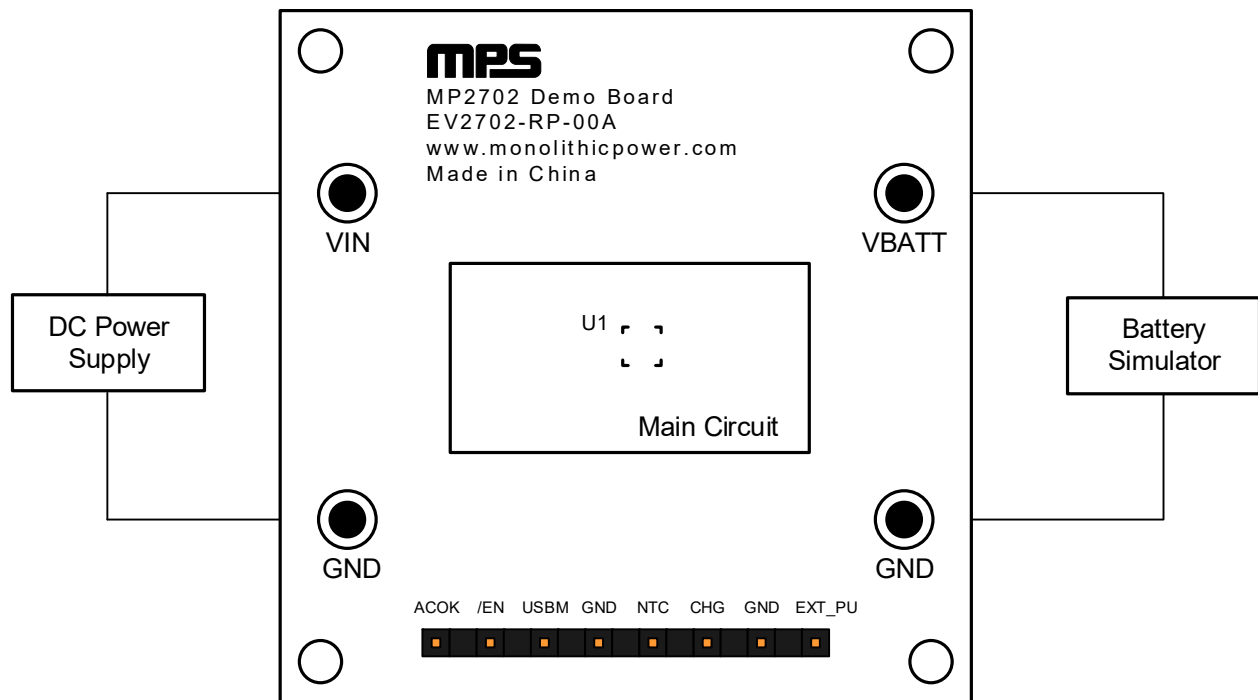


Figure 1: Test Set-Up for the MP2702

EVALUATION BOARD SCHEMATIC

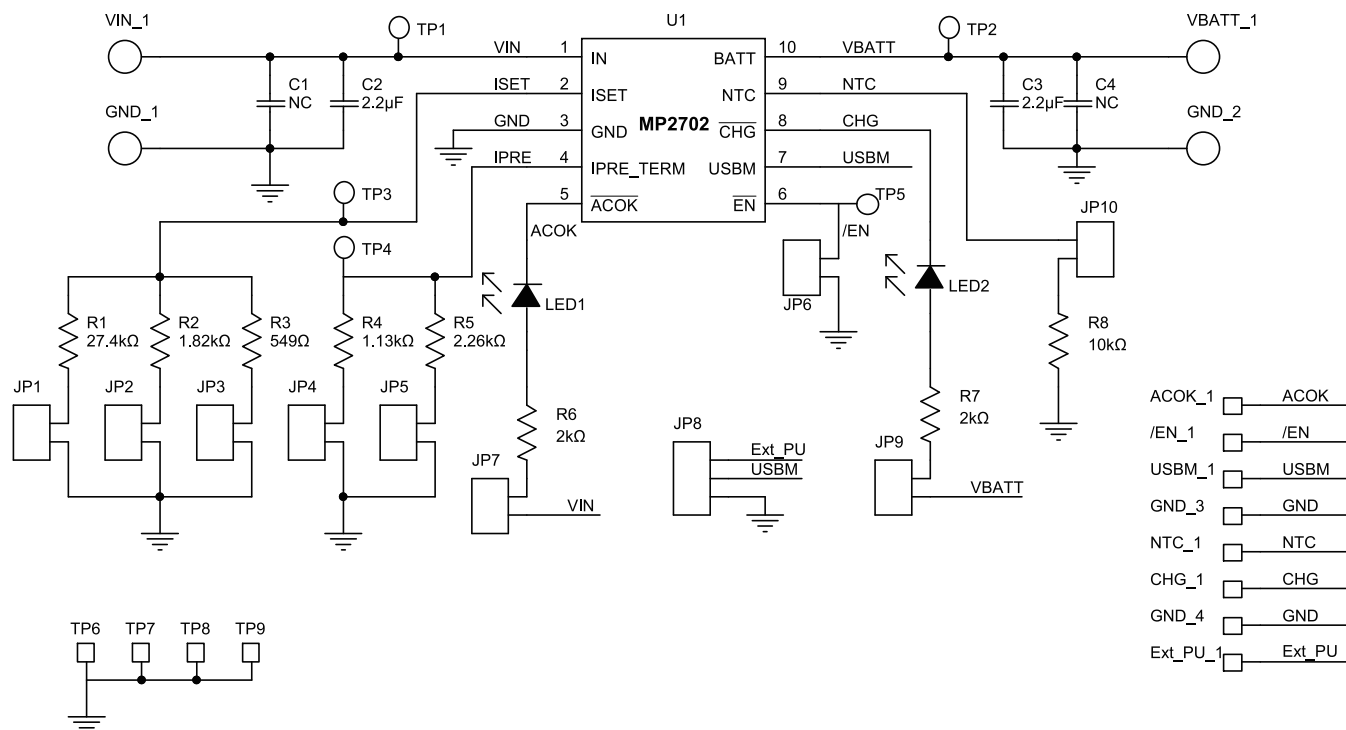


Figure 2: Evaluation Board Schematic

EV2702-RP-00A BILL OF MATERIALS

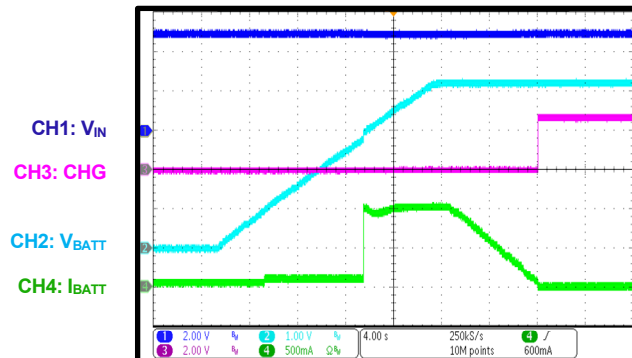
Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
2	C1, C4	NC	Ceramic capacitor, 50V, X5R	0805		
2	C2, C3	2.2μF	Ceramic capacitor, 50V, X5R	0603	Murata	GRM188R61H225KE11D
1	R1	27.4kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0727K4L
1	R2	1.82kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-071K82L
1	R3	549Ω	Film resistor, 1%	0603	Yageo	RC0603FR-07549RL
1	R4	1.13kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-071K13L
1	R5	2.26kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-072K26L
2	R6, R7	2kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-072KL
1	R8	10kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710KL
1	LED1	50mW	Red LED	0805	Baihong	BL-HUE35A-AV-TRB
1	LED2	50mW	Green LED	0805	Baihong	BL-HGE35A-AV-TRB
4	VIN_1, VBATT_1, GND_1, GND_2	2mm	Connector	DIP	Any	
9	JP1, JP2, JP3, JP4, JP5, JP6, JP7, JP9, JP10	2.54mm	Row connector	DIP	Any	
1	JP8	2.54mm	Row connector	DIP	Any	
7	JP3, JP4, JP6, JP7, JP8, JP9, JP10	2.54mm	Shunt connector	DIP	Any	
8	USBM_1, NTC_1, Ext_PU_1, CHG_1, ACOK_1, /EN_1, GND_3, GND_4	2.54mm	Row connector	DIP	Any	
5	TP1, TP2, TP3, TP4, TP5	1mm	Test point yellow	DIP	Any	
4	TP6, TP7, TP8, TP9	2.8mmx 3.8mm	Test point ground	SMD	Any	
1	U1	MP2702	26V, 1A, linear charger	QFN-10 (2.0mmx 2.5mm)	MPS	MP2702GRP

EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board. $V_{IN} = 5V$, $V_{BATT} = 0V$ to $4.2V$, $I_{CC} = 1A$, $V_{IN_LIM} = 4.5V$, $T_A = 25^{\circ}C$, unless otherwise noted.

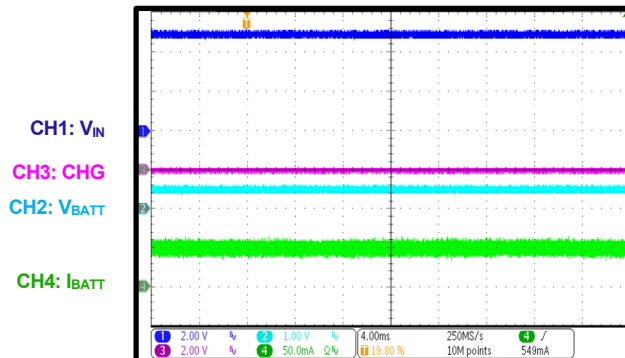
Battery Charge Profile

$V_{IN} = 5V$, $I_{PRE} = 10\%$ of I_{CC} , $I_{CC} = 1A$



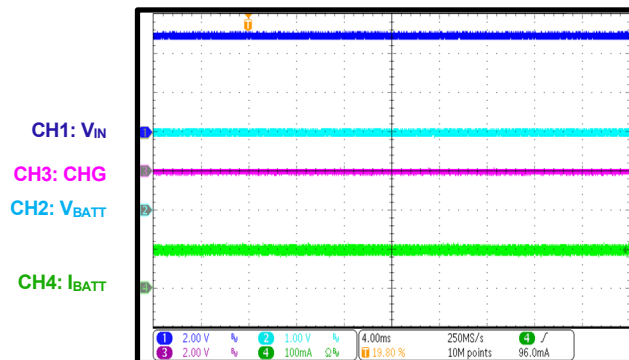
Trickle Charge

$V_{IN} = 5V$, $V_{BATT} = 0.5V$, $I_{TC} = 50mA$



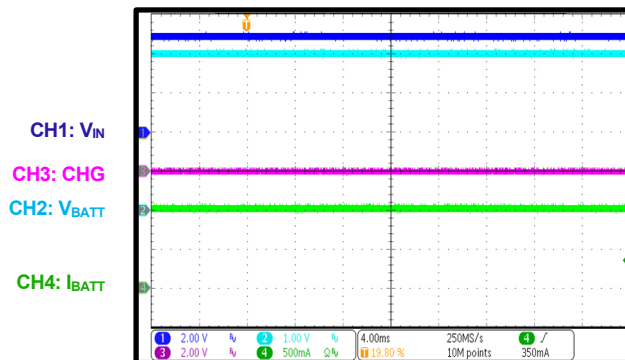
Pre-Charge

$V_{IN} = 5V$, $V_{BATT} = 2V$, $I_{PRE} = 100mA$



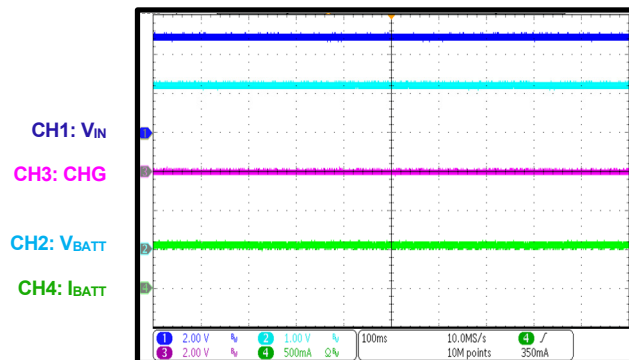
Constant Current Charge

$V_{IN} = 5V$, $V_{BATT} = 4V$, $I_{CC} = 1A$



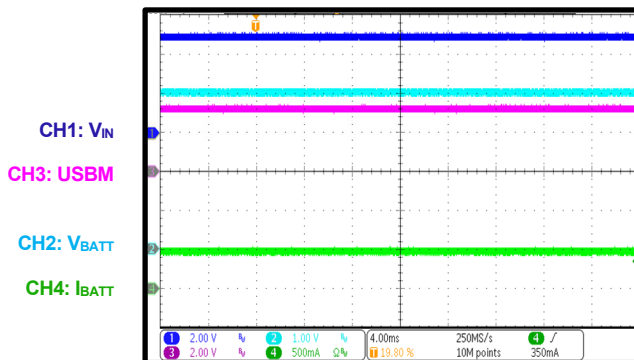
Constant Voltage Charge

$V_{IN} = 5V$, $V_{BATT} = 4.185V$, $I_{CC} = 1A$



Input Current Limit

$V_{IN} = 5V$, $V_{BATT} = 4V$, $I_{CC} = 1A$, USBM = high

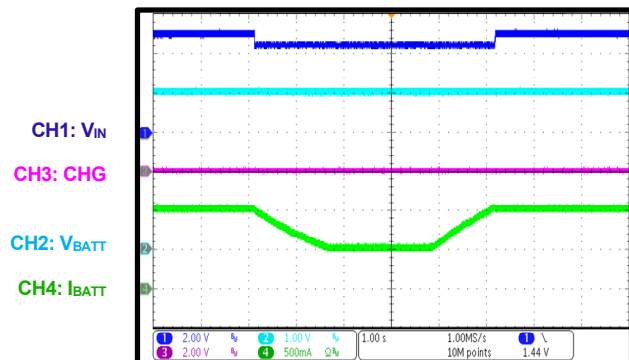


EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. $V_{IN} = 5V$, $V_{BATT} = 0V$ to $4.2V$, $I_{CC} = 1A$, $V_{IN_LIM} = 4.5V$, $T_A = 25^{\circ}C$, unless otherwise noted.

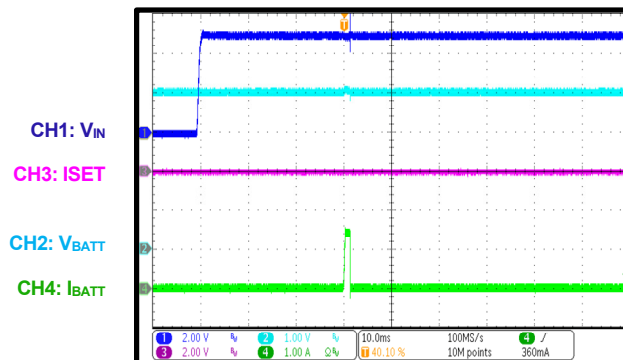
Input Voltage Limit

$V_{IN} = 5V$ (1A to 0.5A to 1A), $V_{IN_LIM} = 4.5V$,
 $V_{BATT} = 4V$, $I_{CC} = 1A$



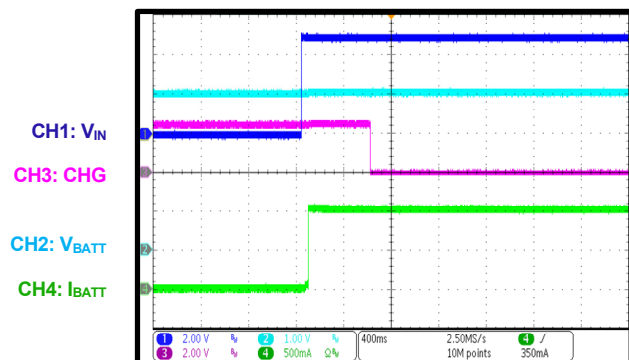
Start-Up with ISET Short

$V_{IN} = 5V$, $V_{BATT} = 4V$, ISET short



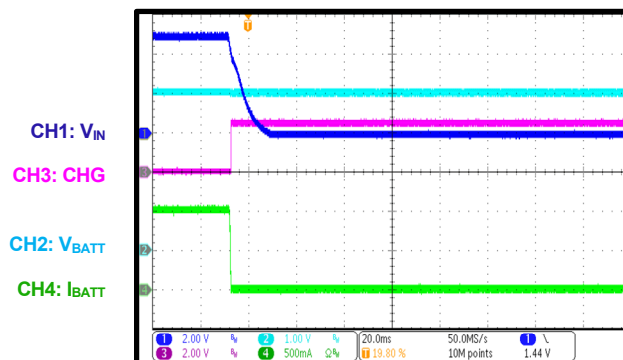
Start-Up

$V_{IN} = 5V$, $V_{BATT} = 4V$, $I_{CC} = 1A$



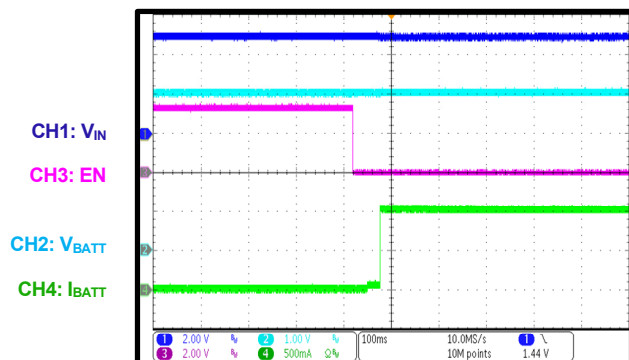
Shutdown

$V_{IN} = 5V$, $V_{BATT} = 4V$, $I_{CC} = 1A$



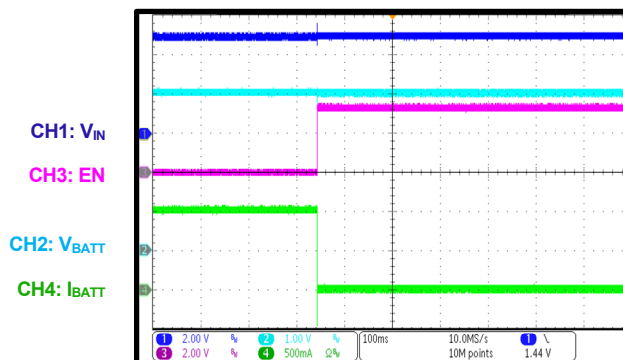
Charge Enabled by EN

$V_{IN} = 5V$, $V_{BATT} = 4V$, $I_{CC} = 1A$



Charge Disabled by EN

$V_{IN} = 5V$, $V_{BATT} = 4V$, $I_{CC} = 1A$



PCB LAYOUT

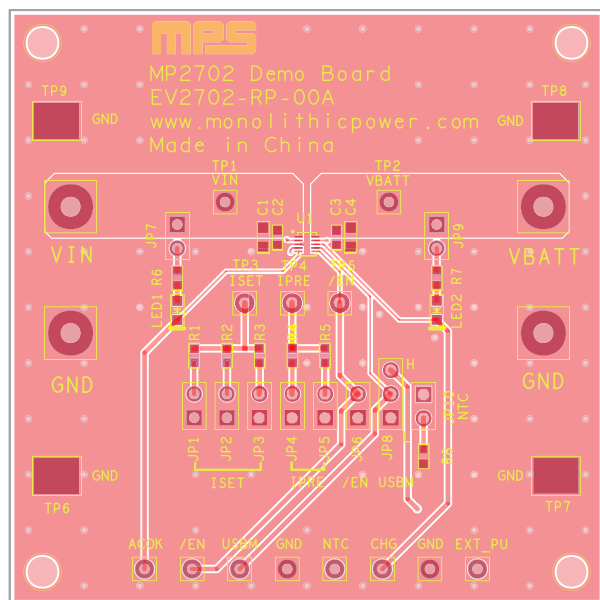


Figure 3: Top Layer

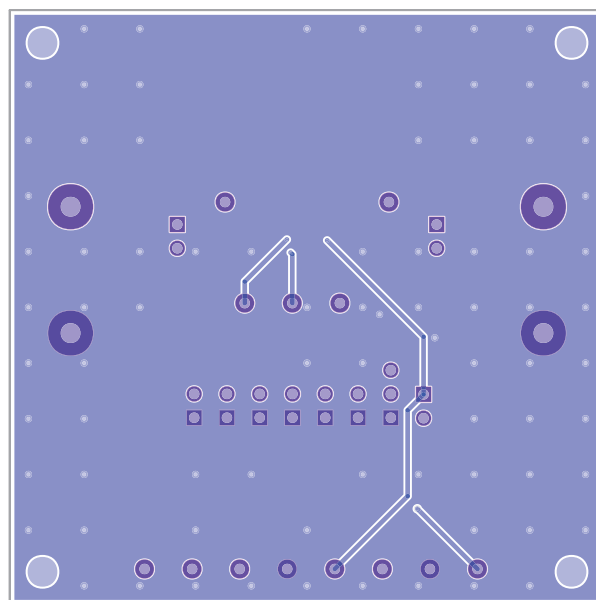


Figure 4: Bottom Layer



REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	2/23/2023	Initial Release	-

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