MPQ3446

55V, Wide-Input, Current Mode Synchronous Boost Controller, AEC-Q100 Qualified

DESCRIPTION

The MPQ3446 is a high-efficiency, current-mode, synchronous boost controller with a wide 6V to 55V input voltage (V_{IN}) range. It can operate with multiple phases for high-power applications. The MPQ3446 also has the capability to drive 10V MOSFETs, greatly improving efficiency and minimizing power loss.

The MPQ3446 provides either an I^2C (default) or SPI interface to configure some key operating parameters, such as the switching frequency (f_{SW}), current limit, light-load mode, frequency spread spectrum (FSS), dead time (DT), soft-start time (t_{SS}), and slope compensation. f_{SW} can be adjusted from 250kHz to 2.5MHz or directly synchronized to an external source.

Protection features include under-voltage lockout (UVLO), current limiting, and thermal shutdown.

The MPQ3446 is available in a QFN-21 (5mmx5mm) package with wettable flanks, and is available in AEC-Q100 Grade 1.

FEATURES

- Designed for Automotive Applications
  - Supports 3V Cold Crank
  - 6V to 55V Wide Input Voltage (V_{IN}) Range
  - -40°C to +150°C Operating Junction Temperature (T_J)
  - Available in AEC-Q100 Grade 1

FEATURES *(continued)*

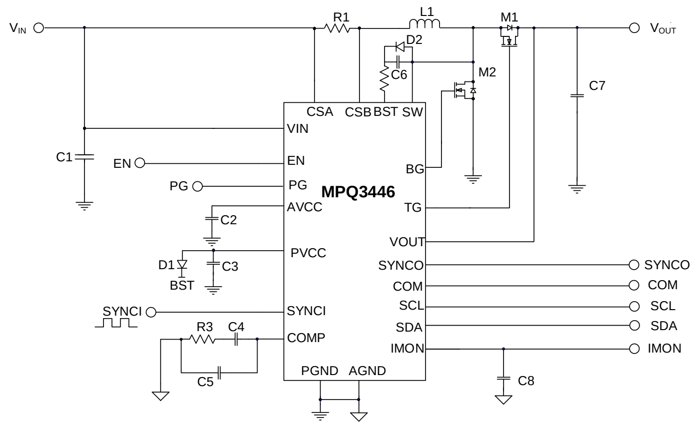
- Configurable via the I^2C or SPI Interface
  - Switching Frequency (f_{SW})
  - Slope Compensation
  - Current Limit Reference
  - Selectable Light-Load Mode
  - Pulse-Skip Modulation (PSM) for Ultra-Light Loads
  - Dead Time (DT)
  - SYNCIN Phase and Frequency Division
  - Synchronous or Non-Synchronous Operation
  - Frequency Spread Spectrum (FSS)
- Additional Features
  - 10V Gate Driving Capability
  - 250kHz to 2.5MHz f_{SW} Synchronizable to an External Clock
  - Clock SYNC Out
  - Thermal Warning and Thermal Shutdown
  - Power Good (PG) Indicator
  - Multi-Phase Capability
  - Available in a QFN-21 (5mmx5mm) Package with Wettable Flanks
- Functional Safety System Design Capable
  - MPSafe™ Compatible – Functional Safety Supporting Document Available

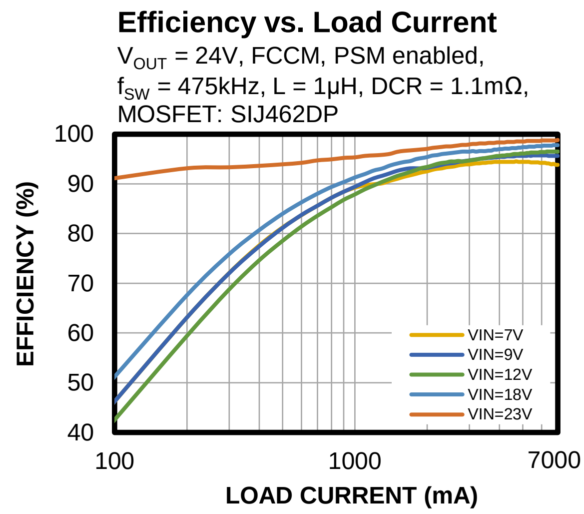
MPSafe™ FuSa Compatible

APPLICATIONS

- Automotive Infotainment and Advanced Driver-Assistance Systems (ADAS) Systems
- Automotive Audio Amplifiers
- Automotive Power Systems

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ3446GUE-xxxx-AEC1***,****	QFN-21 (5mmx5mm)	*See Below*	2

* For Tape & Reel, add suffix -Z (e.g. MPQ3446GUE-xxxx-AEC1-Z).

** Moisture Sensitivity Level Rating

*** "xxxx" is the configuration code identifier for the register settings stored in the OTP register. Each "x" can be a hexadecimal value between 0 and F. The default code is "0000". Please contact an MPS FAE to create this unique number.

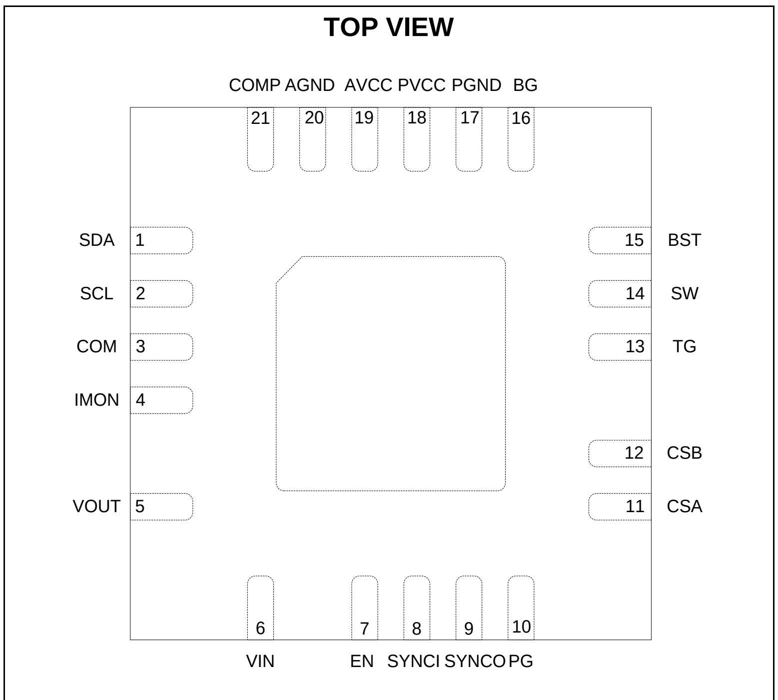
**** Wettable Flank

TOP MARKING

```
MPSYYWW
 MP3446
LLLLLLL
      E
```

MPS: MPS prefix
YY: Year code
WW: Week code
MP3446: Part number
LLLLLLL: Lot number
E: Wettable Flank

PACKAGE REFERENCE



QFN-21 (5mmx5mm)

PIN FUNCTIONS

Pin	Name	Description
1	SDA	**I^2C serial data or SPI bus serial data input.**
2	SCL	**I^2C serial clock or SPI BUS serial clock.**
3	COM	**SPI chip selection signal.** If the I^2C interface is used, float this pin or connect it to AGND.
4	IMON	**Input current monitor output or SPI slave data output.** The IMON pin voltage (V_{IMON}) is proportional to the (V_{CSA} - V_{CSB}) voltage to indicate the input average current. Connect a 1nF to 10nF decoupling capacitor between IMON and AGND. For the SPI interface, the IMON pin is the SPI slave data output.
5	VOUT	**Output voltage (V_{OUT}) feedback.** The VOUT pin senses V_{OUT} for voltage regulation.
6	VIN	**Input supply.** The VIN pin supplies power to the converter. Place a 0.1µF decoupling capacitor as close as possible between PGND and the IC to reduce switching spikes.
7	EN	**Enable.** Pull the EN pin above 1.2V to enable the power stage; pull this pin below 1V to stop switching. Do not float this pin.
8	SYNCI	**Synchronized signal input pin.** Apply a 250kHz to 2.5MHz external clock signal to synchronize the switching frequency (f_{SW}). Do not float this pin; connect it to AGND if not used.
9	SYNCO	**Synchronized clock signal output pin.** The SYNCO pin outputs an out-of-phase 0° or 180° clock to the other devices.
10	PG	**Power good indicator.** The PG pin is an open-drain output. If the PG pin is used, connect a pull-up resistor to the power source. PG is pulled high if V_{OUT} is within 96% to 104% of the nominal voltage. PG is pulled low when V_{OUT} is above 105% or below 95% of the nominal voltage. Float this pin if it is not used.
11	CSA	**Current-sense (CS) pin A.** The voltage sensed between the CSA and CSB pins determines the external CS signal.
12	CSB	**Current-sense pin B.** The voltage sensed between the CSA and CSB pins determines the external CS signal.
13	TG	**Top gate driver output.** The TG pin drives the gate of the top N-channel synchronous MOSFET. The TG driver draws power from the bootstrap (BST) capacitor (C_{BST}) and returns to the SW pin. It provides a floating drive to the top N-channel MOSFET. For non-synchronous applications, the TG pin is disabled.
14	SW	**Switch node.** Connect the SW pin to the switch node of the power supply. The switch node is the junction of the power inductor, low-side MOSFET (LS-FET) drain, high-side MOSFET (HS-FET) source, and C_{BST}. The high-side (HS) driver is referenced to this pin.
15	BST	**Bootstrap (BST).** Connect a bypass capacitor between the BST and SW pins to form a floating supply to power the TG driver. An external diode must be placed between the PVCC and BST pins to charge C_{BST} while the LS-FET is on; a 1N4148 diode is recommended. Add an external diode between the SW and BST pins to prevent the BST-SW voltage (V_{BST-SW}) from being discharged to less than -0.3V by the leakage current at the BST pin under no switching conditions; a 1N4148 diode is also recommended.
16	BG	**Bottom gate driver output**. Connect the BG pin to the gate of the bottom synchronous N-channel MOSFET.
17	PGND	**Power ground.** The PGND pin is a high-current ground reference for the internal LS-FET driver.
18	PVCC	**Internal power bias supply.** Decouple the PVCC pin with a 4.7µF to 10µF ceramic capacitor, placed as close to PVCC as possible.
19	AVCC	**Internal analog bias supply.** Decouple the AVCC pin with a 1µF to 10µF ceramic capacitor, placed as close to AVCC as possible.
20	AGND	**Analog ground.** Connect the AGND pin to the analog ground plane through a wide, short path.

PIN FUNCTIONS *(continued)*

Pin	Name	Description
21	COMP	**Internal error amplifier (EA) output.** Connect the compensation network between the COMP and AGND pins. See the Compensation Components section on page 40 for more information on selecting the components for this pin. For multi-phase applications, connect COMP from the master device to the slave device(s) to share the loop control information.
-	Exposed pad	The exposed pad has no internal electrical connection to ground. Connect the exposed pad to the ground plane to optimize thermal performance. The pad can be floated regardless of thermal performance.

ABSOLUTE MAXIMUM RATINGS (1)

VIN, CSA, CSB, SW, VOUT ....-0.3V to +60V
BST, TG…………….... ....-0.3V to SW +14V
PVCC, BG…………….. ....-0.3V to +14V
All other pins………….. ....-0.3V to +7V
Continuous power dissipation (T_A = 25°C) (2)
QFN-21 (5mmx5mm) 3.5W
Junction temperature (T_J) ....150°C
Lead temperature…….. ....260°C
Storage temperature.... ....-65°C to +150°C

ESD Ratings

Human body model (HBM)…………… Class D (3)
Charged-device model (CDM)……..Class C2b (4)

Recommended Operating Conditions

Supply voltage (V_{IN})…. ....6V to 55V
Minimum V_{IN} for start-up 6.5V
Output voltage (V_{OUT}) setting ....Up to 55V
Operating junction temp (T_J) .... -40°C to +150°C

Thermal Resistance	***θJA***	***θJC***	
JESD51-7……………………...	36	8	°C/W (5)

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance $θ_{JA}$, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / $θ_{JA}$. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Per AEC-Q100-002.
4) Per AEC-Q100-011.
5) Obtained on a JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application. The value of $θ_{JC}$ shows the characterization parameter from junction-to-case bottom.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Power Supply						
Shutdown current	I_{SHDN_GND}	V_{EN} = 0V, V_{IN} = V_{OUT} = 12V		20	35	μA
V_{IN} under-voltage lockout (UVLO) rising threshold	$V_{IN\_UVLO\_R}$		2.8	3.1	3.4	V
V_{IN} UVLO falling threshold	$V_{IN\_UVLO\_F}$		2.25	2.55	2.85	V
VCC Supply						
PVCC regulation voltage	V_{PVCC}	PVCC_LVL = 1, I_{PVCC} = 0mA	9	10	11	V
		PVCC_LVL = 1, I_{PVCC} = 100mA	9	10	11	V
PVCC UVLO rising threshold	$V_{PVCC\_UVLO\_R}$	PVCC_LVL = 1, PVCC_UVLO = 0	4.6	5	5.4	V
		PVCC_LVL = 1, PVCC_UVLO = 1	6.1	6.5	6.9	V
PVCC UVLO falling threshold	$V_{PVCC\_UVLO\_F}$	PVCC_LVL = 1, PVCC_UVLO = 0	4.4	4.8	5.2	V
		PVCC_LVL = 1, PVCC_UVLO = 1	5.9	6.3	6.7	V
PVCC UVLO hysteresis	$V_{PVCC\_UVLO\_HYS}$			200		mV
PVCC pull-down resistor		EN = 0, PVCC > 1V		40		kΩ
PVCC dropout voltage	V_{PVCC_DROP}	V_{IN} - PVCC, I_{PVCC} = 100mA			2.6	V
		V_{OUT} - PVCC, I_{PVCC} = 100mA			2.6	V
AVCC regulation voltage	V_{AVCC}		4.5	5	5.5	V
AVCC UVLO rising threshold	$V_{AVCC\_UVLO\_R}$		3.1	3.3	3.5	V
AVCC UVLO falling threshold	$V_{AVCC\_UVLO\_F}$		2.85	3.05	3.25	V
AVCC UVLO hysteresis	$V_{AVCC\_UVLO\_HYS}$			250		mV
AVCC pull-down resistor		EN = 0, AVCC > 1V		40		kΩ
AVCC dropout voltage	V_{AVCC_DO}	PVCC - AVCC, I_{AVCC} = 5mA			1.2	V
Output Voltage (V_{OUT}) Regulation						
V_{OUT} accuracy (6)	V_{OUT_ACC}	T_J = 25°C	-1%		+1%	V_{OUT}
		T_J = -40°C to +150°C	-2%		+2%	V_{OUT}
Power Good (PG)						
PG rising threshold	PG_{RISING}	V_{OUT} rising	94	96	98	%
		V_{OUT} falling	102	104	106	%
PG falling threshold	$PG_{FALLING}$	V_{OUT} falling	93	95	97	%
		V_{OUT} rising	103	105	107	%
PG sink capability		I_{PG} = 4mA			200	mV
Switching Behavior						
TG source resistance	R_{TG_SOURCE}	V_{BST} - V_{SW} = 10V		2.5		Ω
TG sink resistance	R_{TG_SINK}	V_{BST} - V_{SW} = 10V		1.5		Ω
BG source resistance	R_{BG_SOURCE}	V_{PVCC} = 10V		2.5		Ω
BG sink resistance	R_{BG_SINK}	V_{PVCC} = 10V		1		Ω
Switching frequency (6)	f_{SW}	Set via OTP register 0x00h, bits[6:0]	225	250	275	kHz
			427	475	523	
			900	1000	1100	
			1800	2000	2200	
Minimum off time (7)	t_{OFF_MIN}			80	100	ns
Minimum on time (7)	$t_{ON\_MIN\_BG}$			90	150	ns

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Maximum duty cycle	D_{MAX}	MAX_DUTY, bit[0] = 0, DEAD_TIME = 00	82	86	90	%
		MAX_DUTY, bit[0] = 1, DEAD_TIME = 00		90		%
Dead time (DT)		Set via the I²C, C_{LOAD} = 4.7nF, (BG falling 50% to TG rising 50%), DEAD_TIME = 00		40		ns
		DEAD_TIME = 01		60		ns
		DEAD_TIME = 10		80		ns
		DEAD_TIME = 11		100		ns
Enable (EN)						
Enable turn-on threshold	V_{ENTH_R}	V_{EN} rising	1.1	1.2	1.3	V
Enable turn-off threshold	V_{ENTH_F}	V_{EN} falling	0.9	1	1.1	V
Enable threshold hysteresis	V_{ENTH_HYS}			200		mV
Enable pull-up current	I_{EN_PLUP}	V_{EN} = 0V, 5V		0.5	2	μA
Synchronization						
SYNCI high voltage	V_{SYNCH}		2			V
SYNCI low voltage	V_{SYNCL}				0.8	V
SYNCIN frequency range	f_{SYNC}		-20%		+20%	f_{SW}
SYNCIN frequency division		SYNCI_DIV = 1		0.5		f_{SYNC}
SYNCIN phase		SYNCI_PHASE = 0		0		deg
		SYNCI_PHASE = 1		180		deg
SYNCO high voltage		I_{SYNCO} = 1mA (source)	AVCC - 0.25	AVCC - 0.15		V
SYNCO low voltage		I_{SYNCO} = -1mA (sink)		0.15	0.25	V
Communications Enable						
COM high voltage	V_{COMH}		2			V
COM low voltage	V_{COML}				0.8	V
Current Sense (CS) and Limit						
Peak current limit reference voltage (V_{REF})	V_{REF_CLP}	V_{CSA} - V_{CSB}, ILIM_REF = 000	18	25	32	mV
		V_{CSA} - V_{CSB}, ILIM_REF = 001	42	50	58	mV
		V_{CSA} - V_{CSB}, ILIM_REF = 010	65	75	85	mV
		V_{CSA} - V_{CSB}, ILIM_REF = 011	90	100	110	mV
		V_{CSA} - V_{CSB}, ILIM_REF = 111	180	200	220	mV
Valley current limit V_{REF}	V_{REF_CLV}	V_{CSA} - V_{CSB}, V_{REF_CLP} < 100mV	60%	80%	100%	V_{REF_CLP}
		V_{CSA} - V_{CSB}, V_{REF_CLP} ≥ 100mV	68%	80%	92%	V_{REF_CLP}
Reverse current limit V_{REF}	V_{REF_CLN}		15%	30%	50%	V_{REF_CLP}
Zero-current detection (ZCD) voltage	V_{ZCD}		-1	6	+13	mV
CS error amplifier (EA) gain	K_{CS}		9	10	11	V/V
Control						
V_{CSA} - V_{CSB} to V_{IMON} gain		V_{REF_CLP} ≤ 100mV, V_{CSA} - V_{CSB} = 0.5 x V_{REF_CLP}		25		V/V
		V_{REF_CLP} > 100mV, V_{CSA} - V_{CSB} = 0.5 x V_{REF_CLP}		12.5		V/V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Error Amplifier (EA)						
Transconductance	g_M		1	2	3	mA/V
COMP voltage	V_{COMP}	V_{CSA} - V_{CSB} = 0V		1		V
COMP source current	I_{COMP_SRC}	V_{COMP} = 1.25V	120			μA
COMP sink current	I_{COMP_SNK}	V_{COMP} = 0.95V	120			μA
Thermal Protection						
Thermal warning (7)	T_{TW}		105	125	145	°C
Thermal warning hysteresis (7)	T_{TW_HYS}			20		°C
Thermal shutdown (7)	T_{TSD}		150	170	190	°C
Thermal shutdown hysteresis (7)	T_{TSD_HYS}			20		°C
I²C Interface Specifications						
Input logic low	V_{IL}	V_{IO} = 3.3V	0		0.4	V
Input logic high	V_{IH}	V_{IO} = 3.3V	2.1			V
Output logic low	V_{OL}	I_{LOAD} = 3mA			0.4	V
SCL clock frequency	f_{SCL}				400	kHz
SCL high time	t_{HIGH}		0.6			μs
SCL low time	t_{LOW}		1.3			μs
Data set-up time	t_{SU_DAT}		100			ns
Data hold time	t_{HD_DAT}		0		0.9	μs
Set-up time for a repeated start command	t_{SU_STA}		0.6			μs
Hold time for a start command	t_{HD_STA}		0.6			μs
Bus free time between a start and a stop command	t_{BUF}		1.3			μs
Set-up time for a stop command	t_{SU_STO}		0.6			μs
SCL and SDA rise time	t_R		20		300	ns
SCL and SDA fall time	t_F		20 x (V_{DD} / 5.5V)		300	ns
Suppressed spike pulse width	t_{SP}		0		50	ns
Capacitance bus for each bus line	C_B				400	pF

Notes:

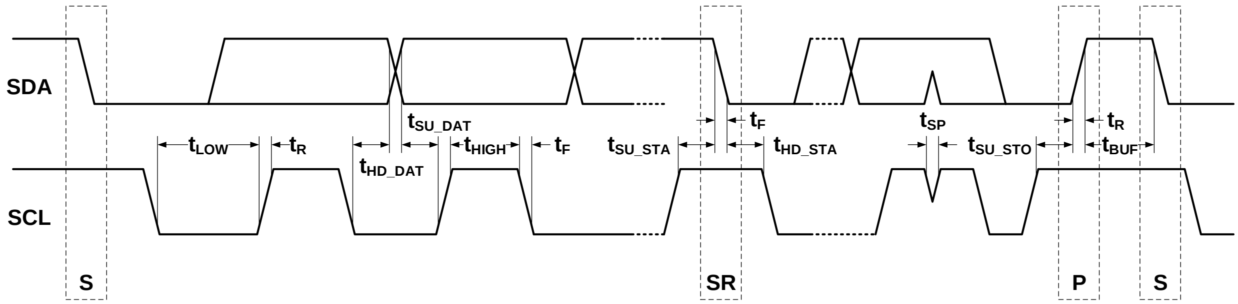
6) Not tested in the entire option range. Only guaranteed for the specified option, which is the default values pre-configured in the OTP register.
7) Guaranteed by design and characterization.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Conditions	Min	Typ	Max	Units
SPI Interface Specifications						
SCL period	t_{SPI}		250			ns
SCL low time	t_{SCLL}			125		ns
SCL high time	t_{SCLH}			125		ns
Time between SCL falling edge and IMON data valid	t_{SOV}	Falling IMON < 0.8V, rising IMON > 2V	0		50	ns
SDA set-up time before SCL rising edge	t_{SIS}		30			ns
SDA hold time after SCL rising edge	t_{SIH}		30			ns
COM set-up time before first SCL falling edge	t_{SCS}		125			ns
COM hold time after last SCL rising edge	t_{HCS}		62.5			ns
Delay between COM rising edge and IMON tri-state	t_{SOTRI}				120	ns
High-level V_{IN}	V_{IN_HIGH}	COM, SCL, SDA; V_{IO} = 3.3V, 5V	2			V
Low-level V_{IN}	V_{IN_LOW}	COM, SCL, SDA; V_{IO} = 3.3V, 5V			0.8	V
V_{IN} hysteresis	V_{IN_HYS}	COM, SCL, SDA; V_{IO} = 3.3V, 5V	130		280	mV
IMON output low voltage	V_{OUT_LOW}	AVCC = 5V, I_{SO} = 20mA			0.6	V
IMON capacitance		Pull-up resistor = 250Ω			50	pF
Minimum time between two SPI commands	$t_{MIN2SPI}$		40			µs
COM deglitch time	t_{CSN_FILTER}		50		85	ns

I²C TIMING DIAGRAM



S: Start Command
SR: Repeated Start Command
P: Stop Command

Figure 1: I²C-Compatible Interface Timing Diagram

SPI TIMING DIAGRAM

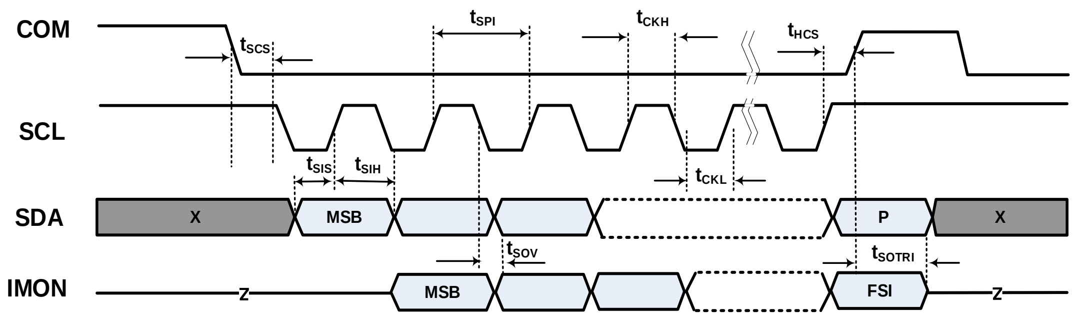
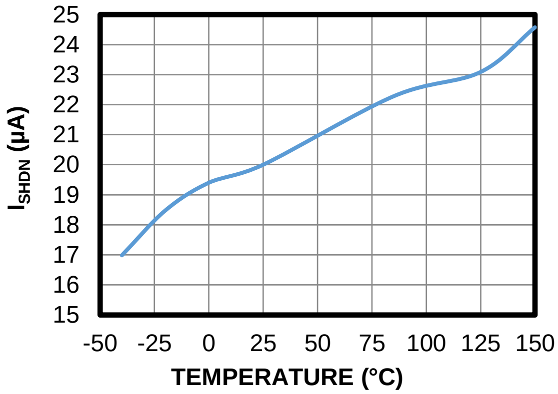


Figure 2: SPI-Compatible Interface Timing Diagram

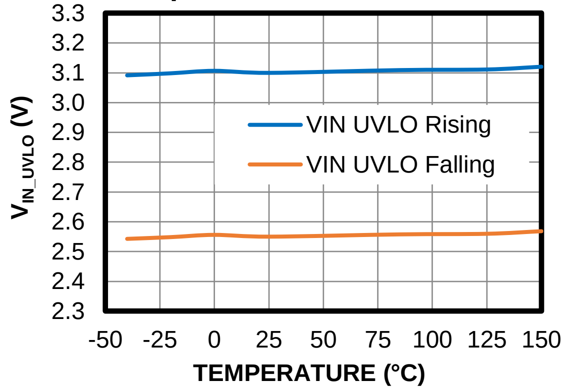
TYPICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +150°C, unless otherwise noted.

Shutdown Current vs. Temperature

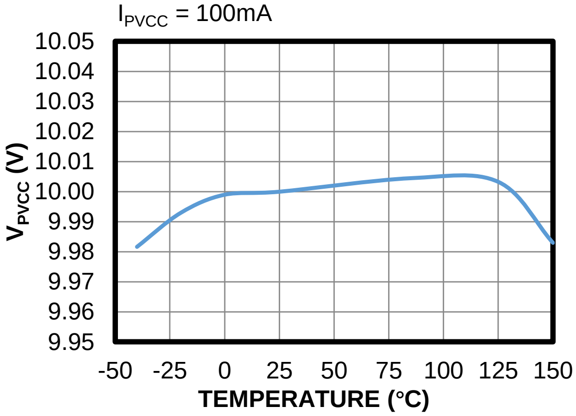


V_{IN} UVLO Threshold vs. Temperature



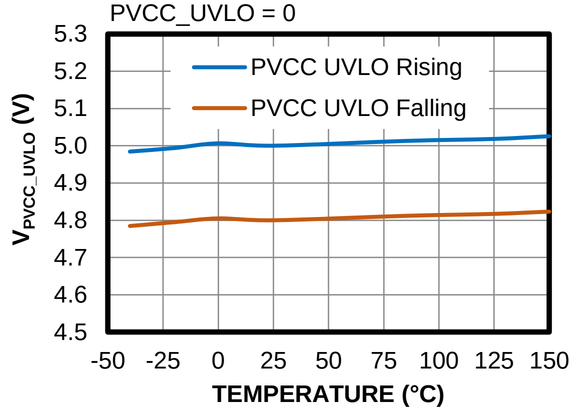
PVCC Regulation Voltage vs. Temperature

I_{PVCC} = 100mA



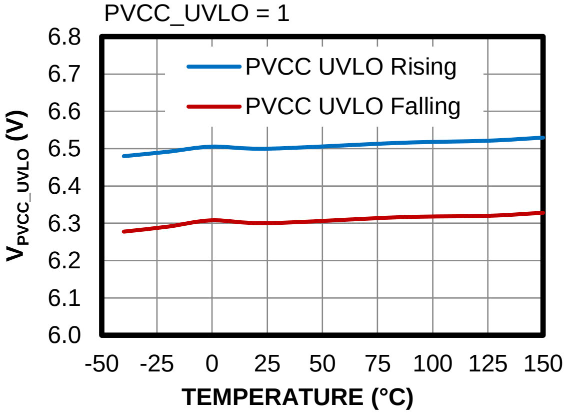
PVCC UVLO Threshold vs. Temperature

PVCC_UVLO = 0

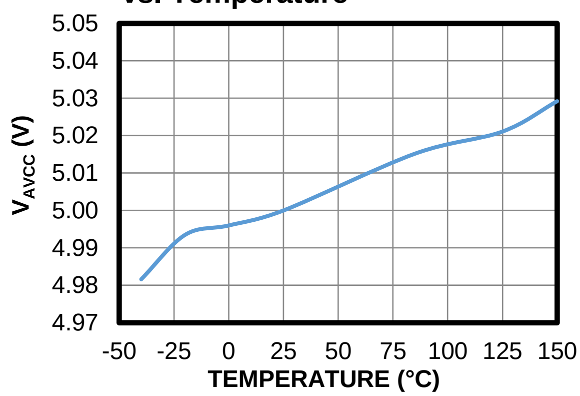


PVCC UVLO Threshold vs. Temperature

PVCC_UVLO = 1

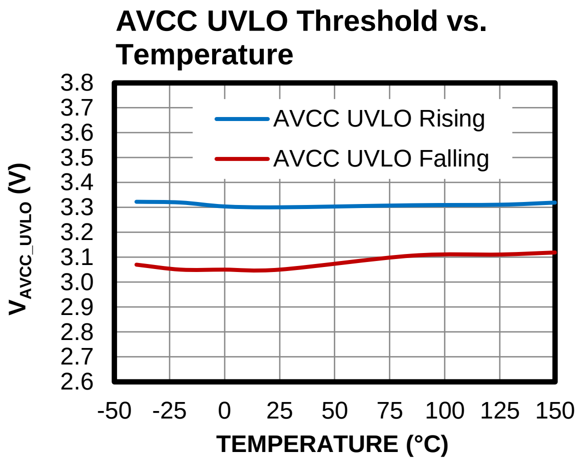


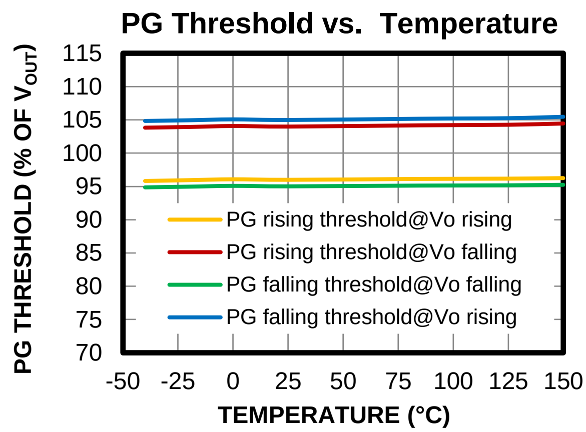
AVCC Regulation Voltage vs. Temperature

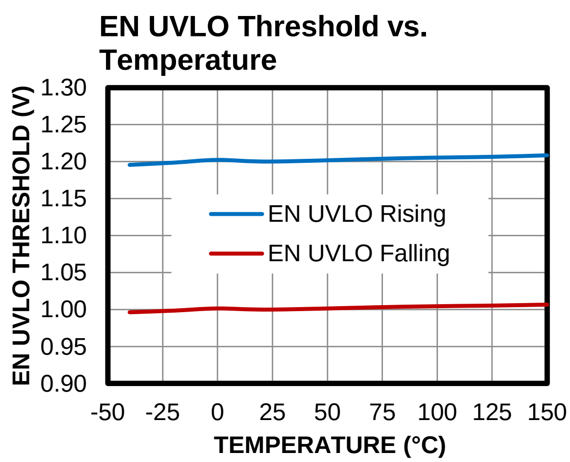


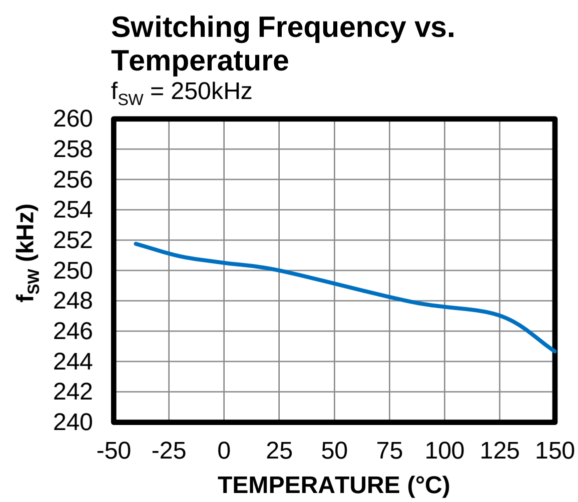
TYPICAL CHARACTERISTICS *(continued)*

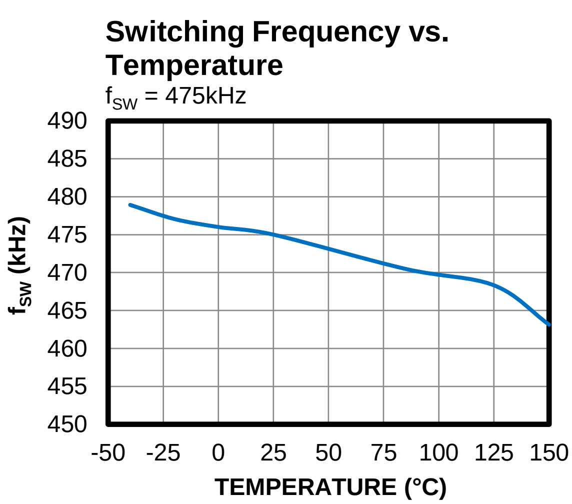
V_{IN} = 12V, T_J = -40°C to +150°C, unless otherwise noted.

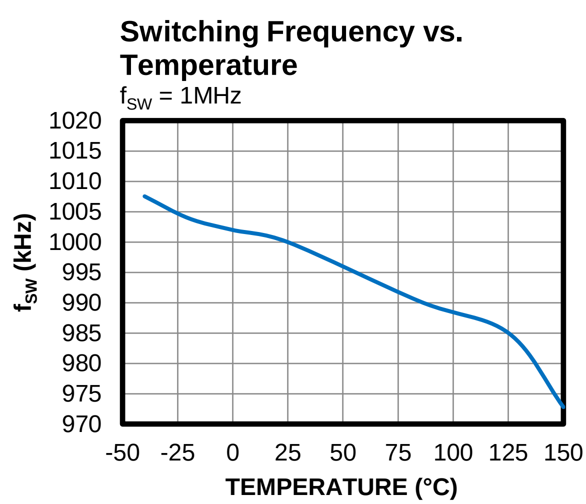










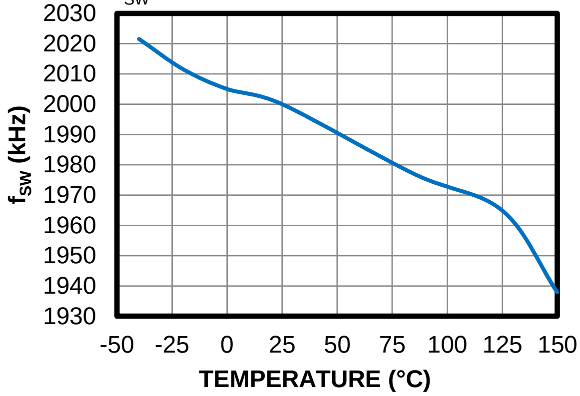


TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +150°C, unless otherwise noted.

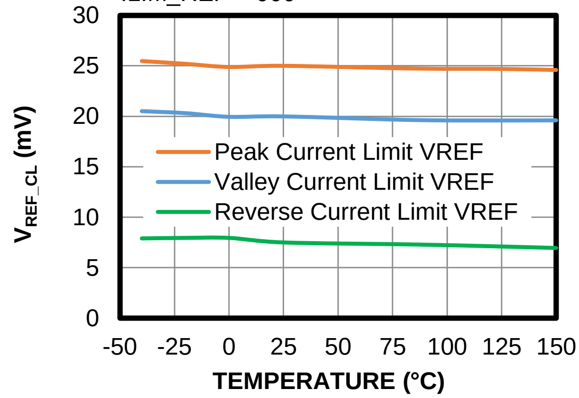
Switching Frequency vs. Temperature

f_{SW} = 2MHz



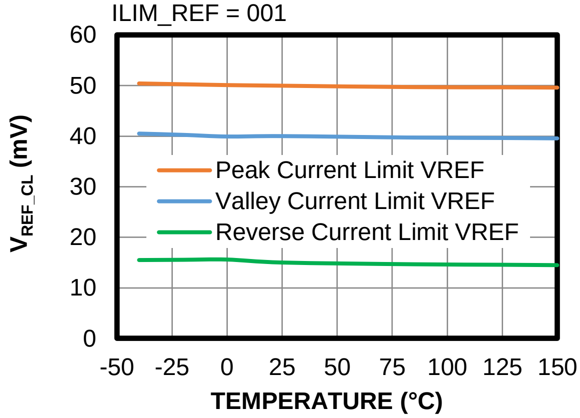
Current Limit V_{REF} vs. Temperature

ILIM_REF = 000



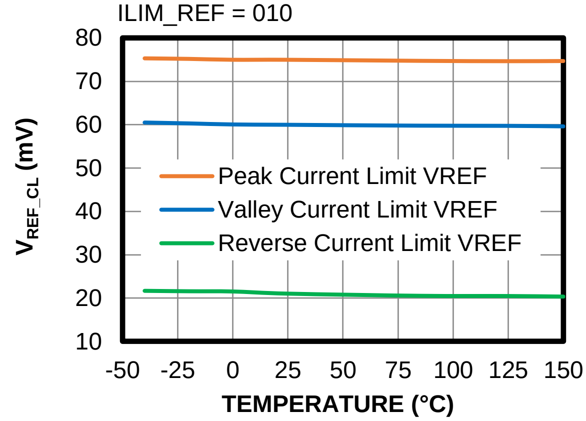
Current Limit V_{REF} vs. Temperature

ILIM_REF = 001



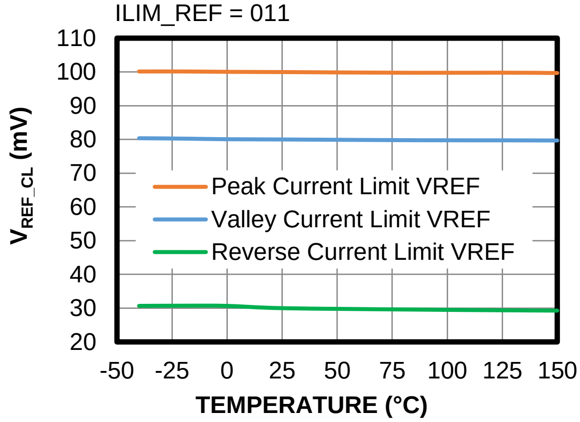
Current Limit V_{REF} vs. Temperature

ILIM_REF = 010



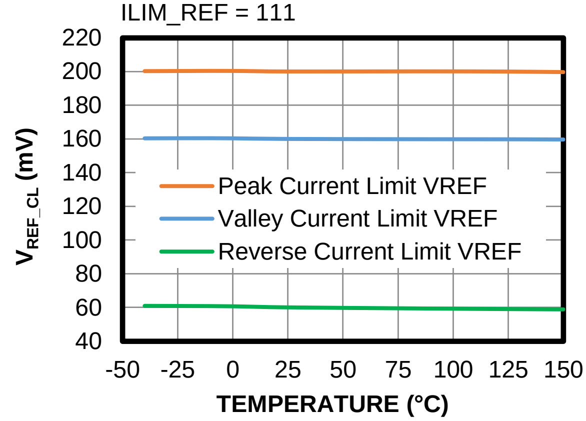
Current Limit V_{REF} vs. Temperature

ILIM_REF = 011



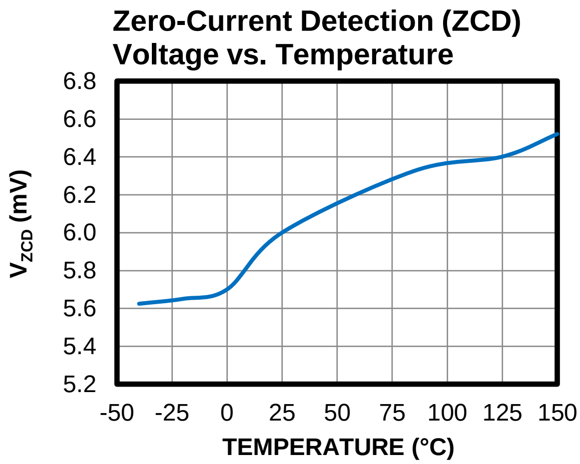
Current Limit V_{REF} vs. Temperature

ILIM_REF = 111



TYPICAL CHARACTERISTICS *(continued)*

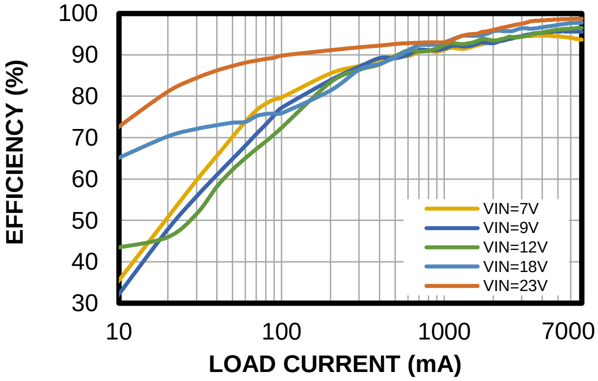
V_{IN} = 12V, T_J = -40°C to +150°C, unless otherwise noted.



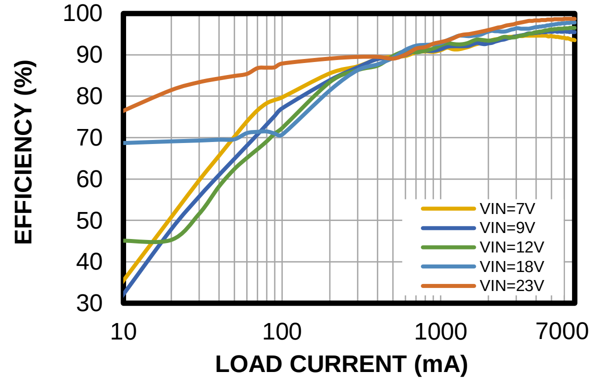
TYPICAL PERFORMANCE CHARACTERISTICS

V_{EN} = 5V, V_{IN} = 12V, V_{OUT} = 24V, L = 1µH (8), T_A = 25°C, unless otherwise noted.

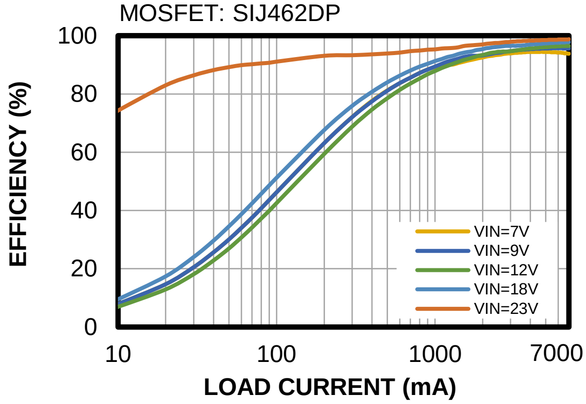
Efficiency vs. Load Current
V_{OUT} = 24V, DCM, PSM enabled,
f_{SW} = 475kHz, L = 1µH (DCR = 1.1mΩ),
MOSFET: SIJ462DP



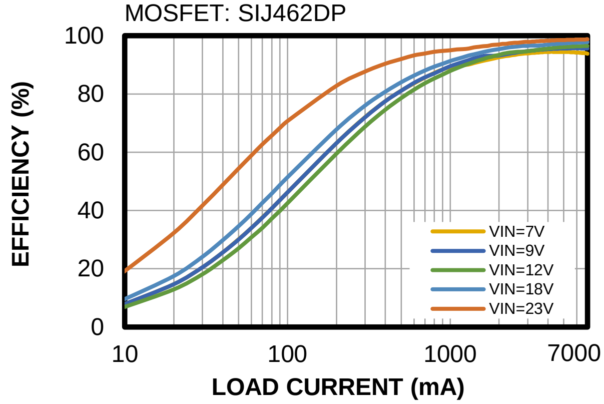
Efficiency vs. Load Current
V_{OUT} = 24V, DCM, PSM disabled,
f_{SW} = 475kHz, L = 1µH (DCR = 1.1mΩ),
MOSFET: SIJ462DP



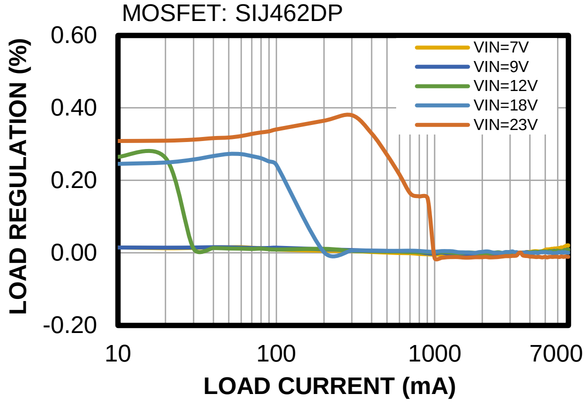
Efficiency vs. Load Current
V_{OUT} = 24V, FCCM, PSM enabled,
f_{SW} = 475kHz, L = 1µH (DCR = 1.1mΩ),
MOSFET: SIJ462DP



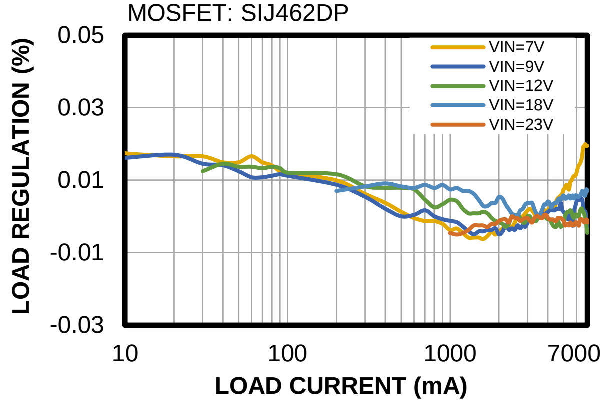
Efficiency vs. Load Current
V_{OUT} = 24V, FCCM, PSM disabled,
f_{SW} = 475kHz, L = 1µH (DCR = 1.1mΩ),
MOSFET: SIJ462DP



Load Regulation
V_{OUT} = 24V, DCM, PSM enabled,
f_{SW} = 475kHz, L = 1µH (DCR = 1.1mΩ),
MOSFET: SIJ462DP



Load Regulation
V_{OUT} = 24V, DCM, PSM disabled,
f_{SW} = 475kHz, L = 1µH (DCR = 1.1mΩ),
MOSFET: SIJ462DP

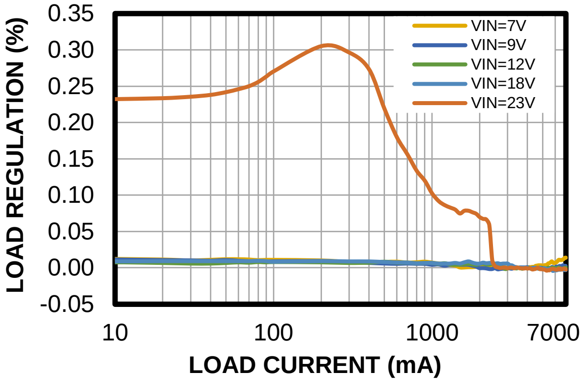


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{EN} = 5V, V_{IN} = 12V, V_{OUT} = 24V, L = 1µH [8], T_A = 25°C, unless otherwise noted.

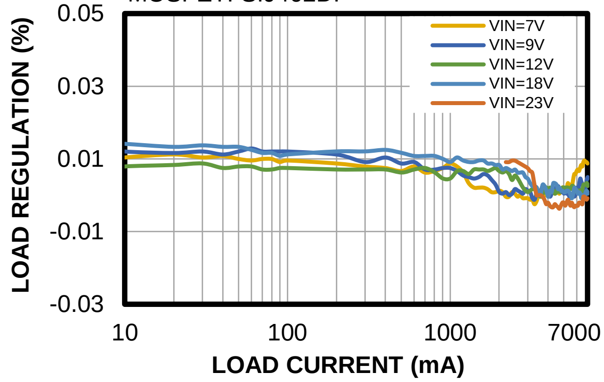
Load Regulation

V_{OUT} = 24V, FCCM, PSM enabled,
f_{SW} = 475kHz, L = 1µH (DCR = 1.1mΩ),
MOSFET: SIJ462DP



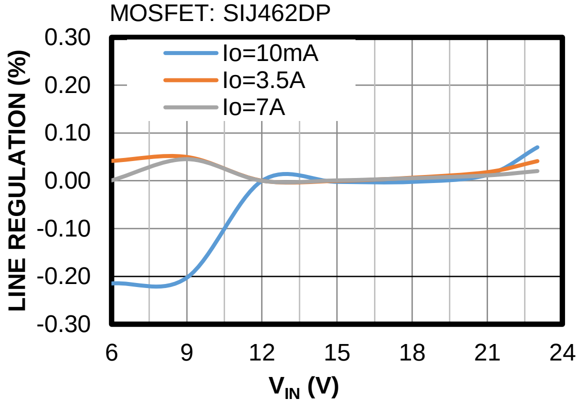
Load Regulation

V_{OUT} = 24V, FCCM, PSM disabled,
f_{SW} = 475kHz, L = 1µH (DCR = 1.1mΩ),
MOSFET: SIJ462DP



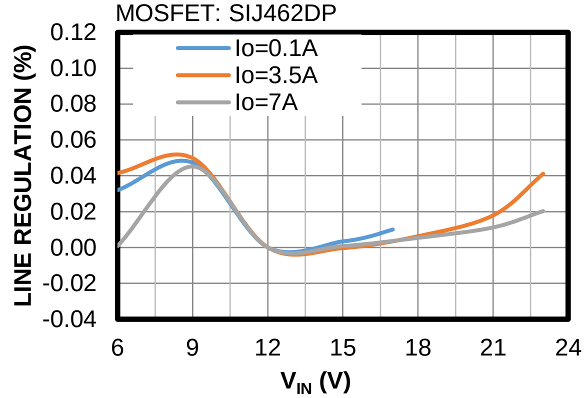
Line Regulation

V_{OUT} = 24V, DCM, PSM enabled,
f_{SW} = 475kHz, L = 1µH (DCR = 1.1mΩ),
MOSFET: SIJ462DP



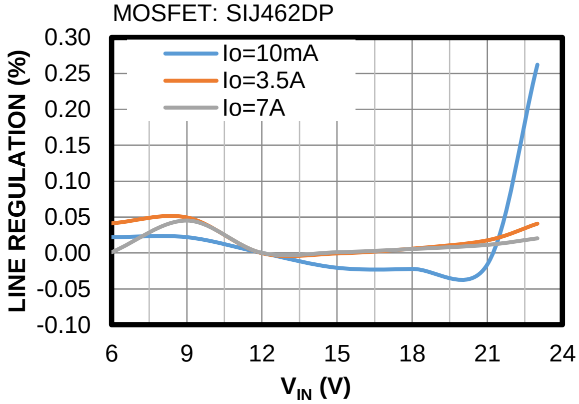
Line Regulation

V_{OUT} = 24V, DCM, PSM disabled,
f_{SW} = 475kHz, L = 1µH (DCR = 1.1mΩ),
MOSFET: SIJ462DP



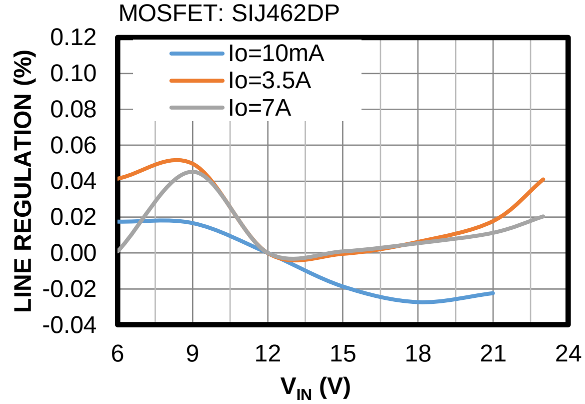
Line Regulation

V_{OUT} = 24V, FCCM, PSM enabled,
f_{SW} = 475kHz, L = 1µH (DCR = 1.1mΩ),
MOSFET: SIJ462DP



Line Regulation

V_{OUT} = 24V, FCCM, PSM disabled,
f_{SW} = 475kHz, L = 1µH (DCR = 1.1mΩ),
MOSFET: SIJ462DP



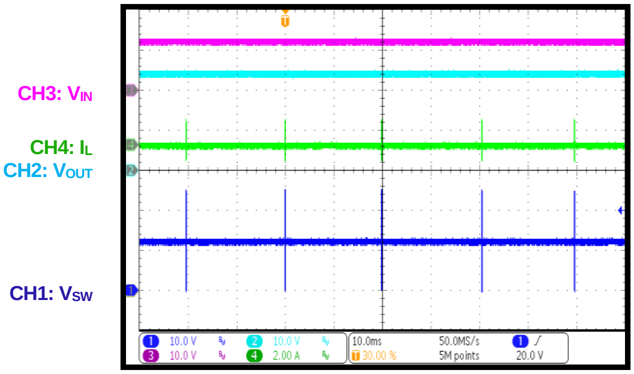
Note:

8) Inductor information: XAL1010-102MEB, DCR = 1.1mΩ.

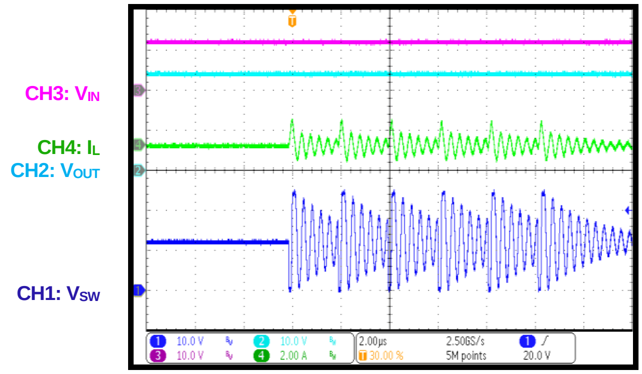
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{EN} = 5V, V_{IN} = 12V, V_{OUT} = 24V, L = 1µH (8), f_{SW} = 475kHz, T_A = 25°C, unless otherwise noted.

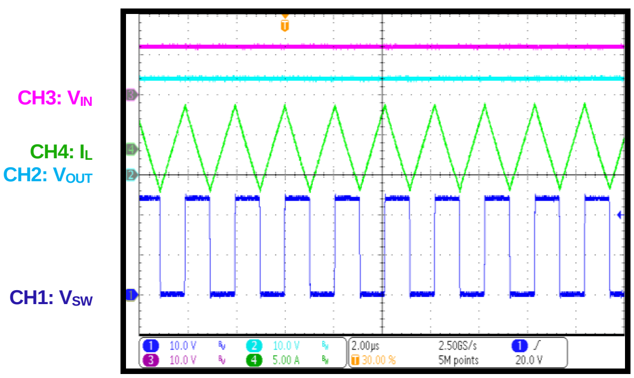
Steady State
I_{OUT} = 0A, DCM



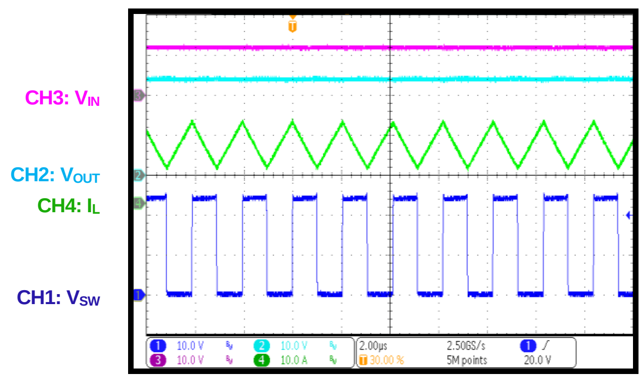
Steady State
I_{OUT} = 0A, DCM, zoom in



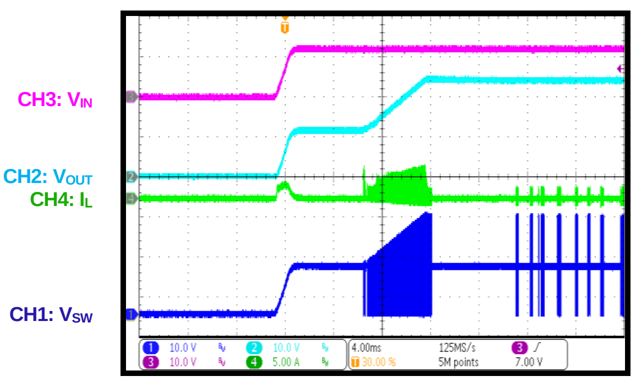
Steady State
I_{OUT} = 0A, FCCM



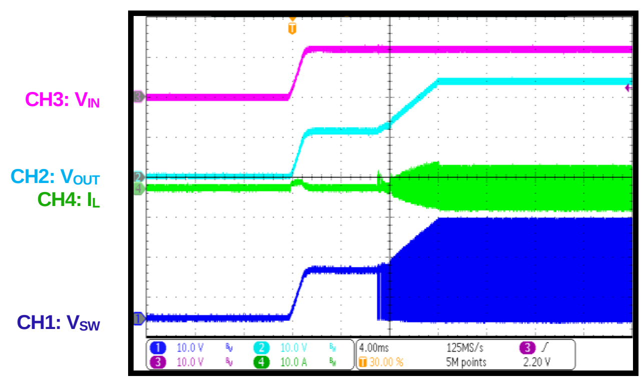
Steady State
I_{OUT} = 7A



Start-Up through VIN
I_{OUT} = 0A, DCM



Start-Up through VIN
I_{OUT} = 0A, FCCM

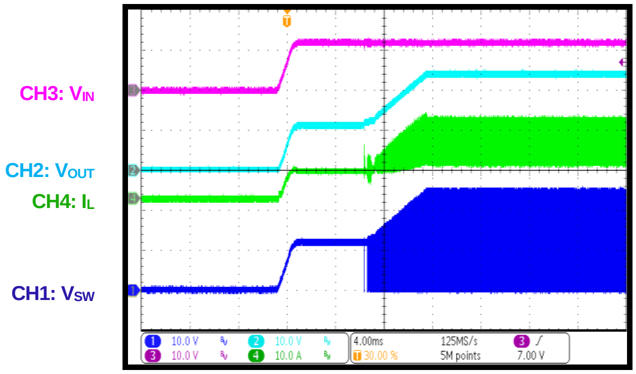


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{EN} = 5V, V_{IN} = 12V, V_{OUT} = 24V, L = 1µH [8], f_{SW} = 475kHz, T_A = 25°C, unless otherwise noted.

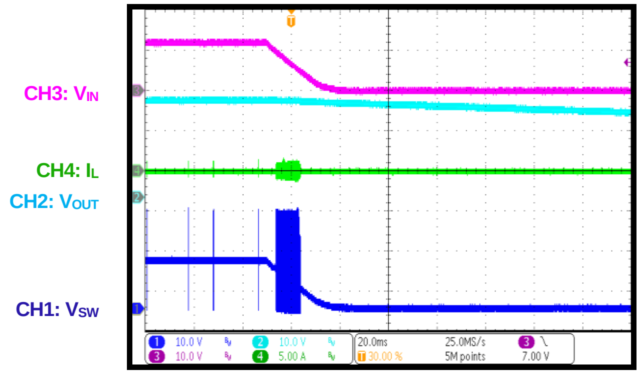
Start-Up through VIN

I_{OUT} = 7A



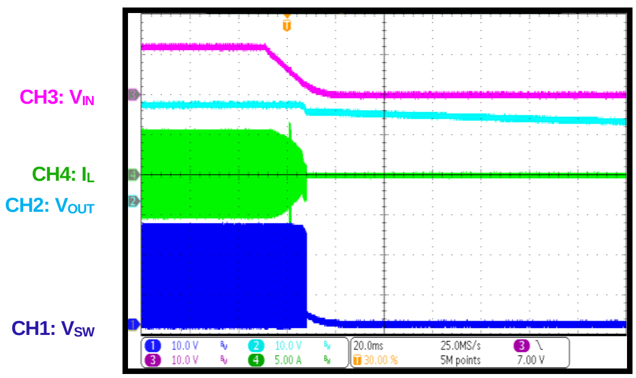
Shutdown through VIN

I_{OUT} = 0A, DCM



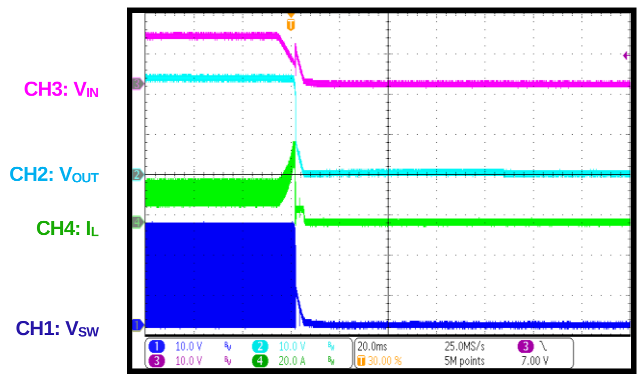
Shutdown through VIN

I_{OUT} = 0A, FCCM



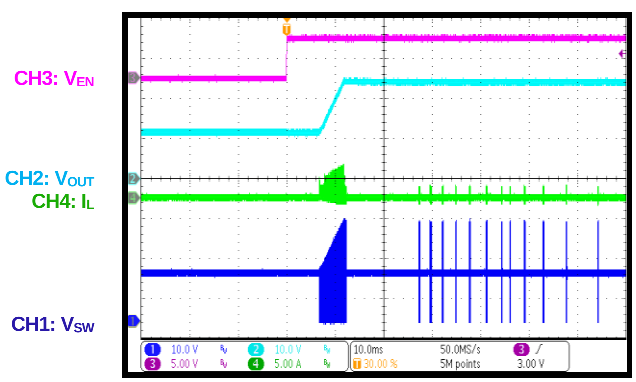
Shutdown through VIN

I_{OUT} = 7A



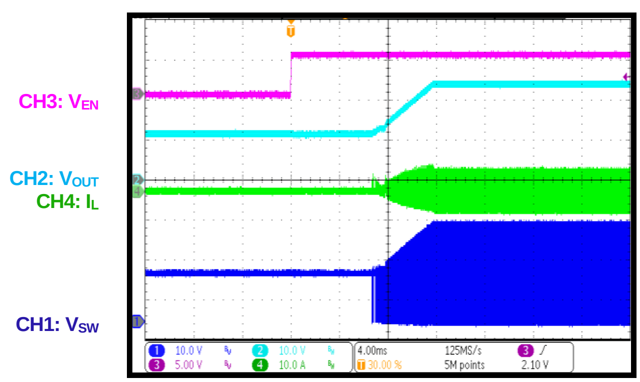
Start-Up through EN

I_{OUT} = 0A, DCM



Start-Up through EN

I_{OUT} = 0A, FCCM

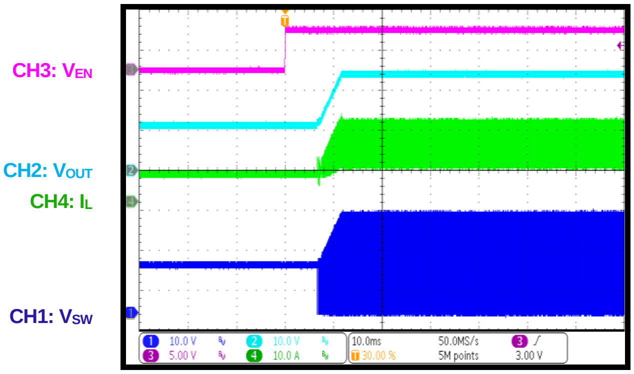


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{EN} = 5V, V_{IN} = 12V, V_{OUT} = 24V, L = 1µH [8], f_{SW} = 475kHz, T_A = 25°C, unless otherwise noted.

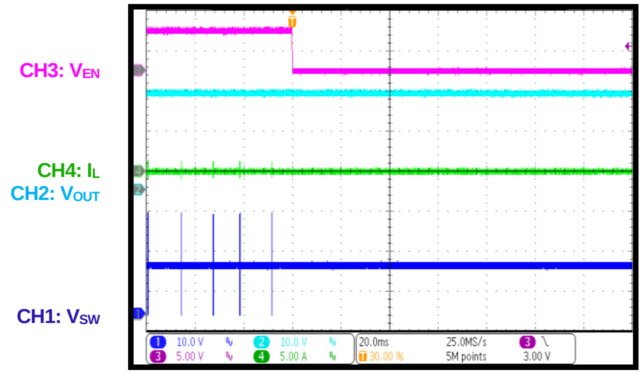
Start-Up through EN

I_{OUT} = 7A



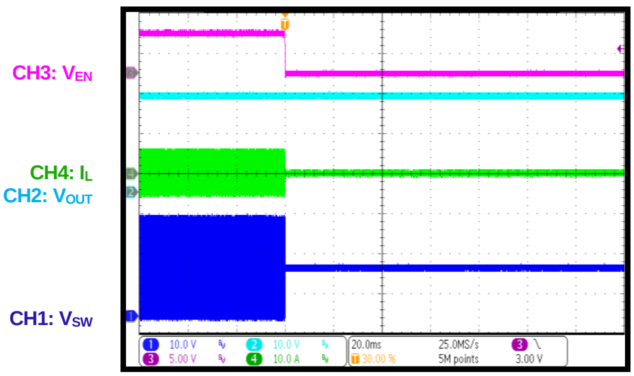
Shutdown through EN

I_{OUT} = 0A, DCM



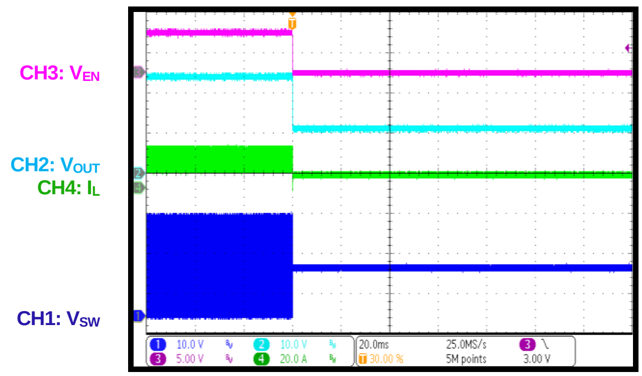
Shutdown through EN

I_{OUT} = 0A, FCCM



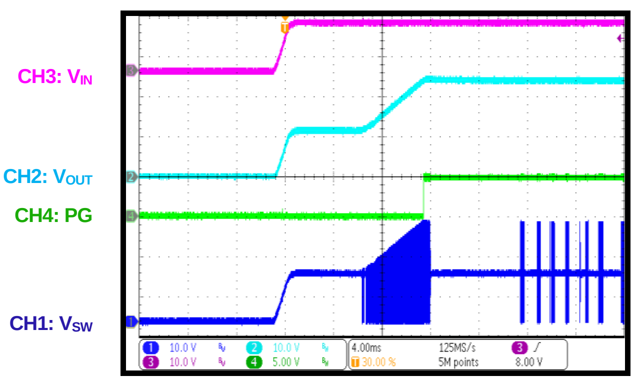
Shutdown through EN

I_{OUT} = 7A



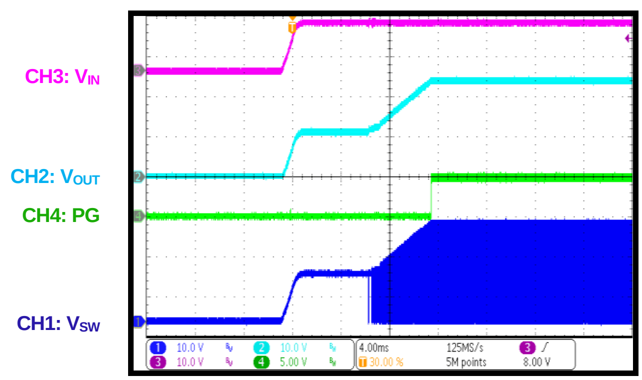
PG in Start-Up through VIN

I_{OUT} = 0A, DCM



PG in Start-Up through VIN

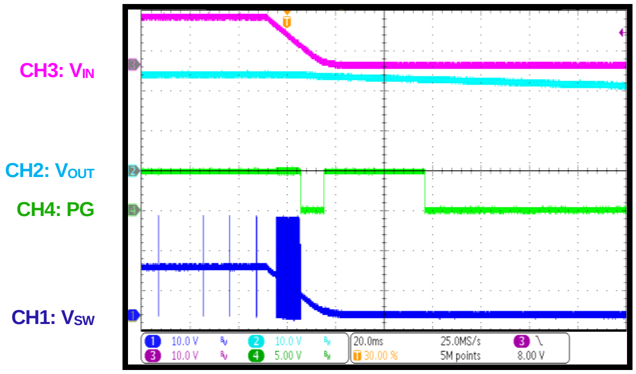
I_{OUT} = 7A



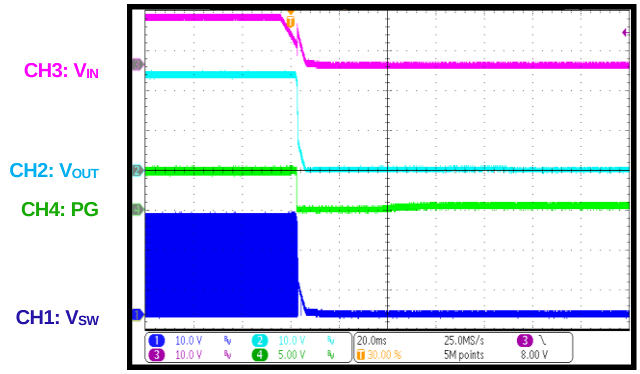
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{EN} = 5V, V_{IN} = 12V, V_{OUT} = 24V, L = 1µH [8], f_{SW} = 475kHz, T_A = 25°C, unless otherwise noted.

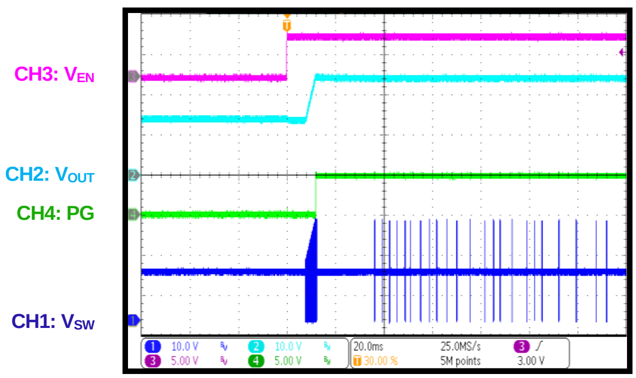
PG in Shutdown through VIN
I_{OUT} = 0A, DCM



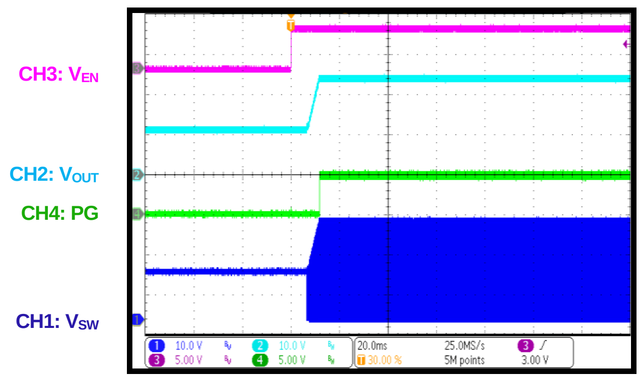
PG in Shutdown through VIN
I_{OUT} = 7A



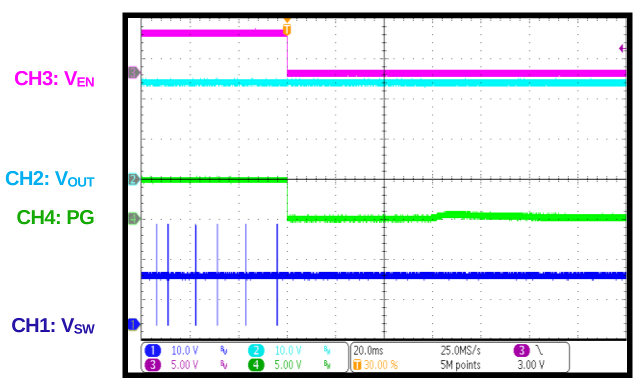
PG in Start-Up through EN
I_{OUT} = 0A, DCM



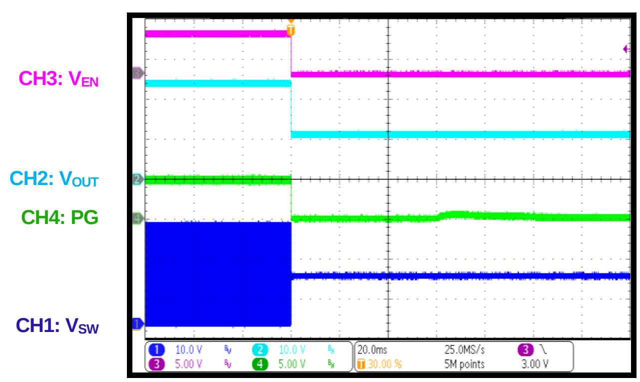
PG in Start-Up through EN
I_{OUT} = 7A



PG in Shutdown through EN
I_{OUT} = 0A, DCM



PG in Shutdown through EN
I_{OUT} = 7A

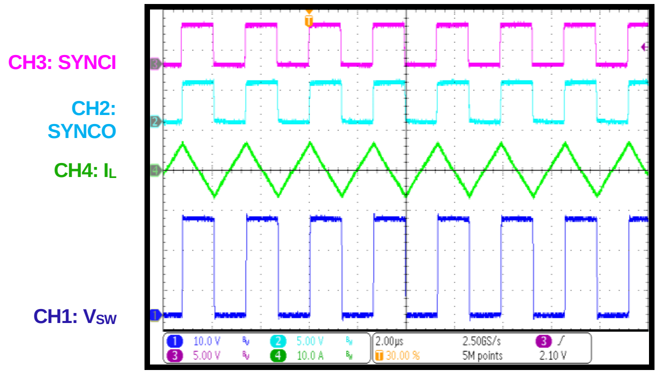


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{EN} = 5V, V_{IN} = 12V, V_{OUT} = 24V, L = 1µH (8), f_{SW} = 475kHz, T_A = 25°C, unless otherwise noted.

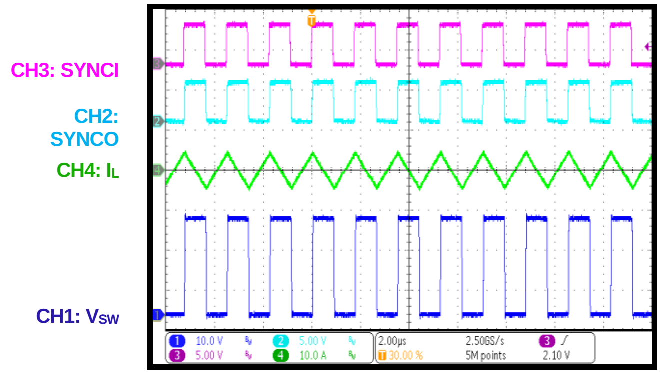
SYNCI and SYNCO Operation

I_{OUT} = 0A, SYNCI = 380kHz



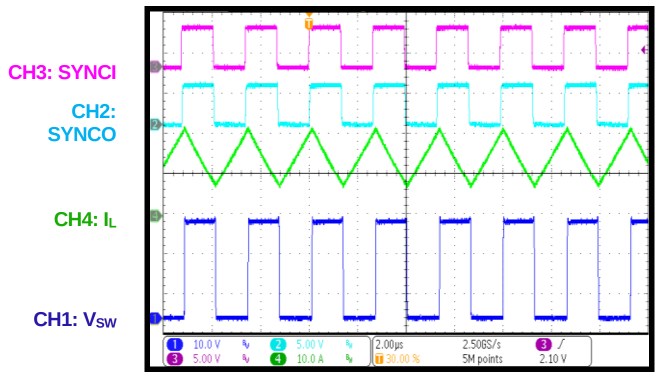
SYNCI and SYNCO Operation

I_{OUT} = 0A, SYNCI = 570kHz



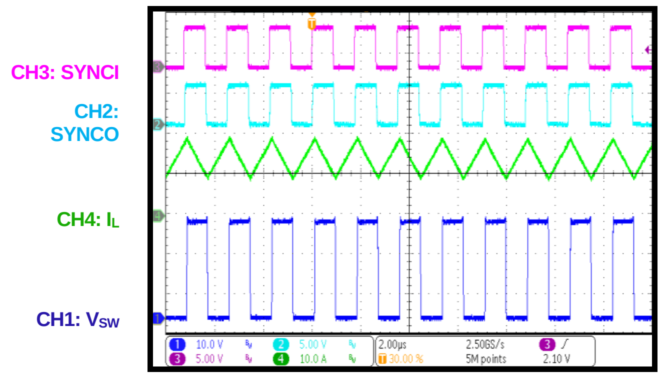
SYNCI and SYNCO Operation

I_{OUT} = 7A, SYNCI = 380kHz



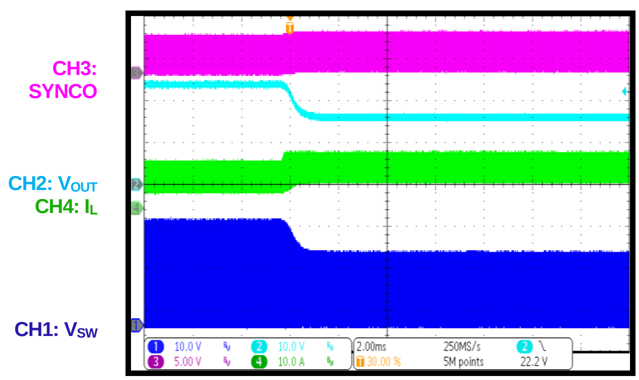
SYNCI and SYNCO Operation

I_{OUT} = 7A, SYNCI = 570kHz



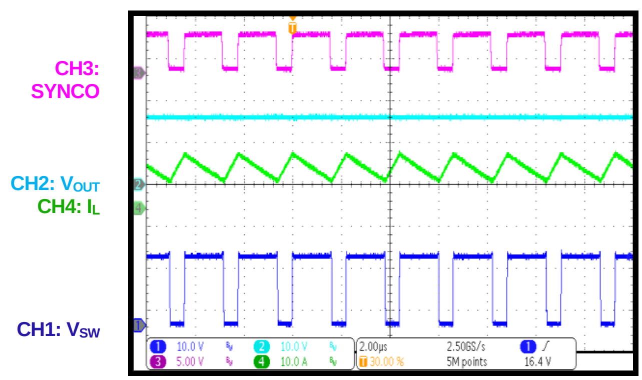
OCP Entry

I_{LIM} = 25mV, R_{SENSE} = 2mΩ, I_{OUT} = 3.5A to 7A



OCP Steady State

I_{LIM} = 25mV, R_{SENSE} = 2mΩ, I_{OUT} = 7A

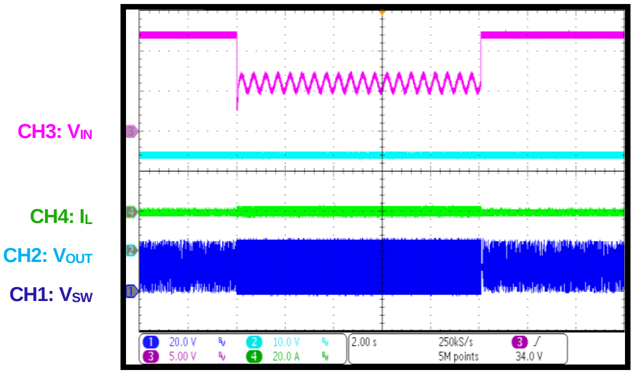


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{EN} = 5V, V_{IN} = 12V, V_{OUT} = 24V, L = 1µH [(8)], f_{SW} = 475kHz, T_A = 25°C, unless otherwise noted.

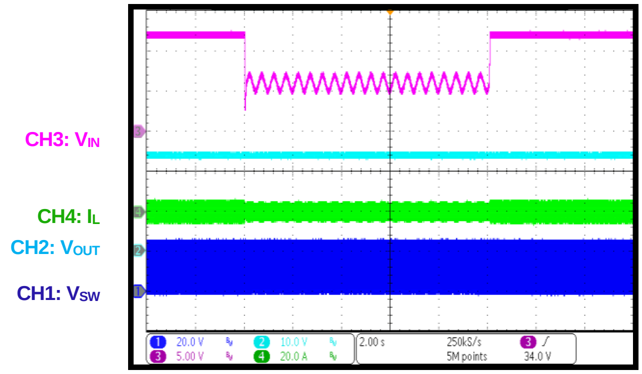
Cold Crank

V_{IN} = 12V to 3V to 6V, I_{OUT} = 0A, DCM



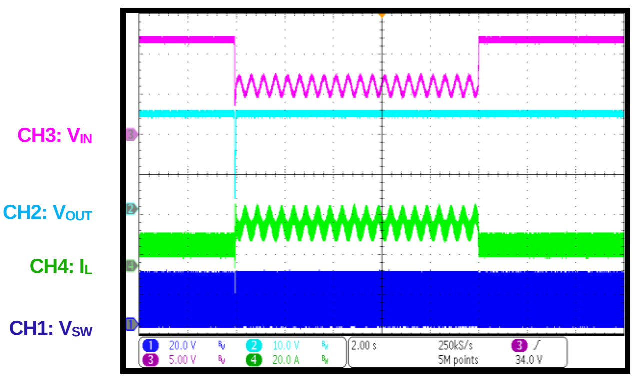
Cold Crank

V_{IN} = 12V to 3V to 6V, I_{OUT} = 0A, FCCM



Cold Crank

V_{IN} = 12V to 3V to 6V, I_{OUT} = 5A

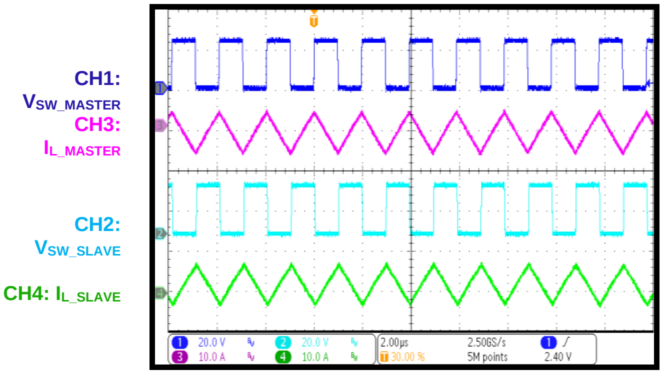


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{EN} = 5V, V_{IN} = 12V, V_{OUT} = 24V, L = 1µH [8], f_{SW} = 475kHz, dual-phase, T_A = 25°C, unless otherwise noted.

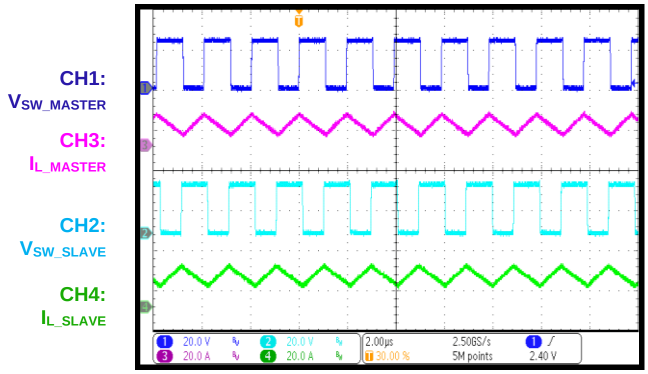
Steady State

I_{OUT} = 0A



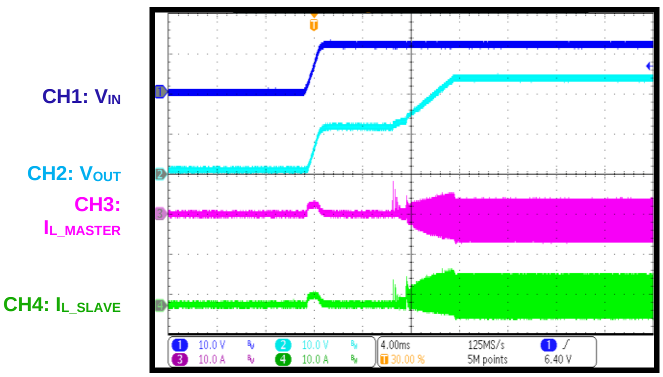
Steady State

I_{OUT} = 14A



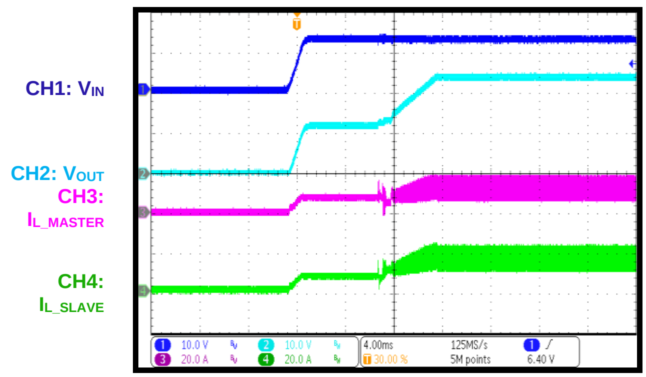
Start-Up through VIN

I_{OUT} = 0A



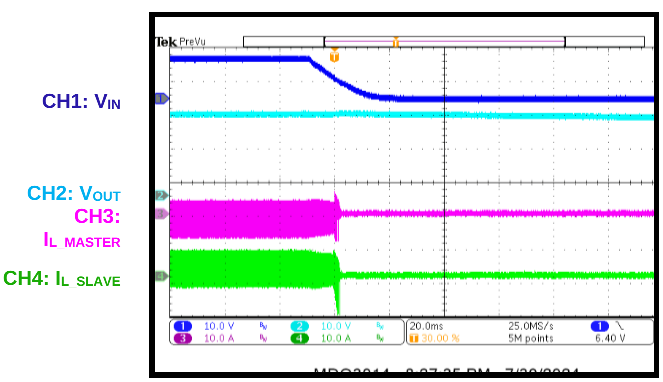
Start-Up through VIN

I_{OUT} = 14A



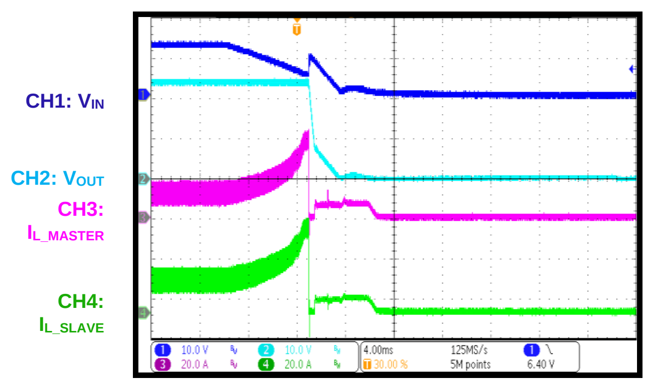
Shutdown through VIN

I_{OUT} = 0A



Shutdown through VIN

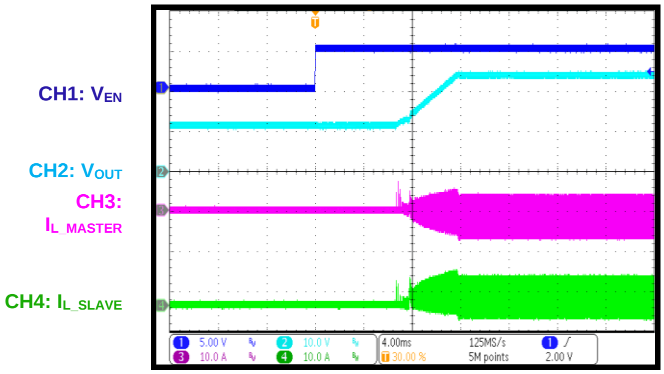
I_{OUT} = 14A



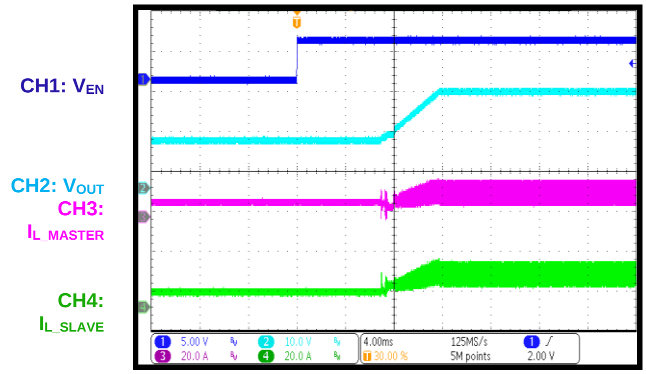
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{EN} = 5V, V_{IN} = 12V, V_{OUT} = 24V, L = 1µH [(8)], f_{SW} = 475kHz, dual-phase, T_A = 25°C, unless otherwise noted.

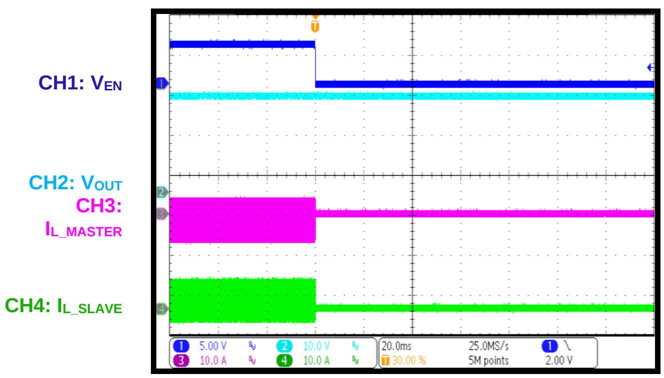
Start-Up through EN
I_{OUT} = 0A



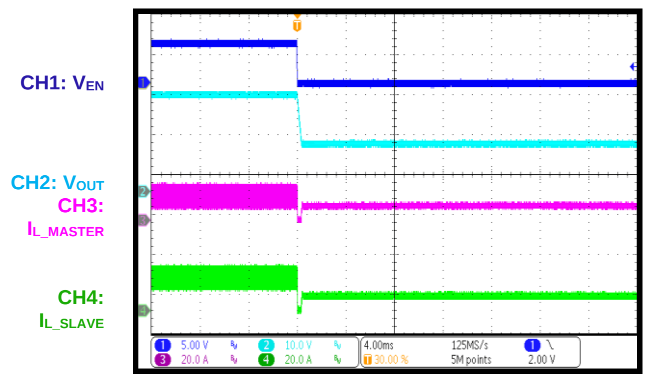
Start-Up through EN
I_{OUT} = 14A



Shutdown through EN
I_{OUT} = 0A



Shutdown through EN
I_{OUT} = 14A



FUNCTIONAL BLOCK DIAGRAM

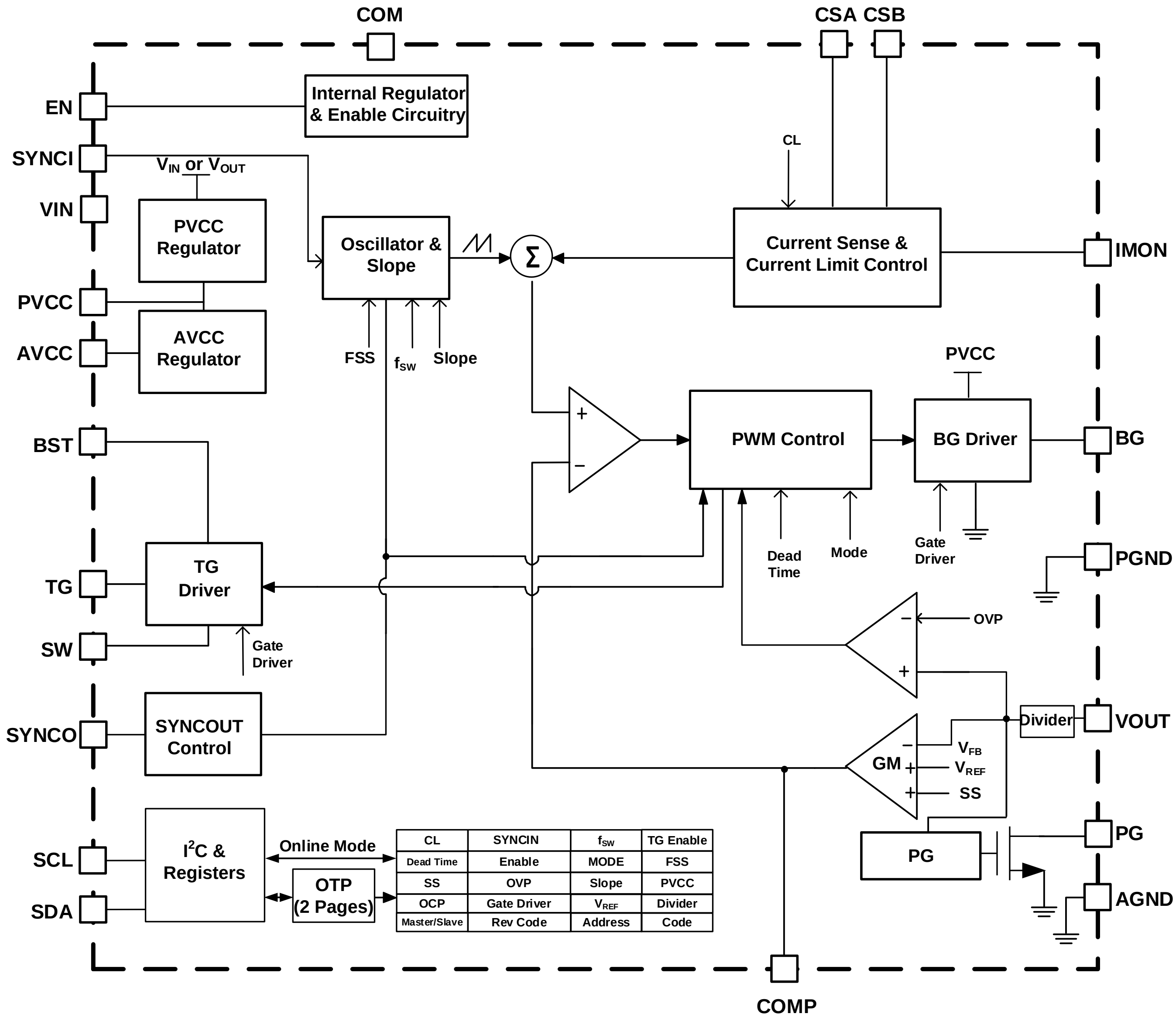


Figure 3: Functional Block Diagram for the I²C Interface

FUNCTIONAL BLOCK DIAGRAM *(continued)*

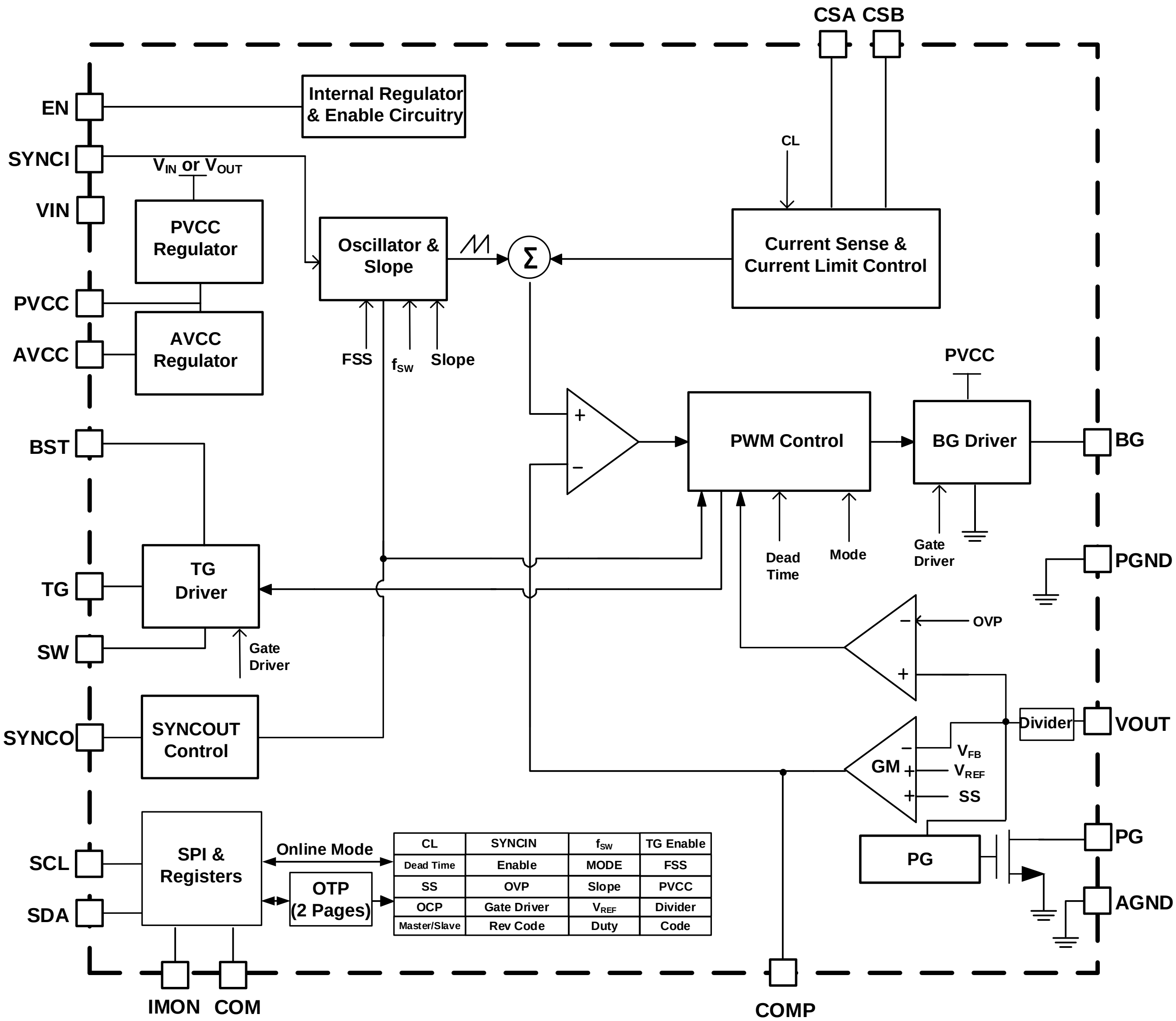


Figure 4: Functional Block Diagram for the SPI Interface

OPERATION

The MPQ3446 is a 6V to 55V, wide-input, synchronous boost controller, and features all of the functions necessary to implement a highly efficient synchronous boost regulator. The regulator control method is based on peak current mode control. The switching frequency (f_{SW}) can be adjusted from 250kHz to 2.5MHz or directly synchronized to an external source. The MPQ3446's 180° shifted clock output enables easy two-phase configuration.

The MPQ3446's operation can be understood by referring to the Functional Block Diagrams (see Figure 3 on page 25 and Figure 4 on page 26).

Normal Operation

The MPQ3446 uses a constant-frequency, peak current mode architecture to regulate the output voltage (V_{OUT}).

In boost operation mode, the N-channel low-side MOSFET (LS-FET, M2) is driven via the BG pin and turns on at the beginning of each cycle to increase the current limit. The BG pin's typical minimum on time is about 90ns. The inductor current (I_L) ripple is sensed back as the voltage difference across the CSA and CSB pins (V_{SENSE}). V_{SENSE} is then amplified and compared to the error voltage (V_{COMP}), which is an amplified error signal between the reference voltage (V_{REF}) and the feedback voltage (V_{FB}). When these two voltages are the same, the pulse-width modulation (PWM) comparator turns off M2 and forces I_L into the output capacitor (C_{OUT}) through the high-side MOSFET (HS-FET, M1).

This causes I_L to decrease. The TG pin's typical minimum on time is about 80ns. The peak I_L (I_{PK}) is controlled by V_{COMP}, which in turn is controlled by V_{OUT}. I_L regulates V_{OUT} to satisfy the load. Current mode regulation improves the transient response and control loop stability.

Light-Load Operation

The MPQ3446 features two light-load operation modes: discontinuous conduction mode (DCM) and forced continuous conduction mode (FCCM). DCM and FCCM can be configured via register USER00 (00h), bit[10]. In DCM, the MPQ3446 employs a zero-current detection (ZCD) circuit. Once I_L falls below the ZCD level, TG turns off until the next clock cycle. In FCCM, the MPQ3446 works with a fixed preset frequency at any load. I_L is permitted to go negative while maintaining the switching frequency (f_{SW}) constant even under no-load conditions.

Pulse-Skip Modulation (PSM)

If register USER02 (02h), bit[10] is set to 0, the MPQ3446 employs pulse-skip modulation (PSM). When PSM is enabled and V_{COMP} drops to the clamp level during no-load or ultra-light load conditions, switching is temporarily stopped.

The stopped power stage does not resume until V_{OUT} drops below its target. Then V_{COMP} exits from the clamp level and the power stage resumes normal operation. The part keeps switching until V_{COMP} drops back to the clamped level. If the output current (I_{OUT}) is high enough that V_{COMP} is no longer dropped to the clamp level, the MPQ3446 enters DCM or continuous conduction mode (CCM) and achieves a constant f_{SW}. PSM can be used to minimize power loss, improve efficiency, and decrease the V_{OUT} ripple during ultra-light load conditions.

Maximum Duty Cycle

When designing a boost converter, the maximum duty cycle (D_{MAX}) should be reviewed at the minimum supply voltage ($V_{IN(MIN)}$). D_{MAX} can be set to 86% or 90% via register USER02 (02h), bit[8]. The $V_{IN(MIN)}$ value required to reach the target V_{OUT} can be estimated with Equation (1):

$$\begin{aligned} V_{IN(MIN)} &= V_{OUT}\,(1-D_{MAX}) + I_{IN(MAX)} x (R_{DCR} + R_{SENSE}) \\ &+ I_{IN(MAX)} x R_{DS(ON)\_H} x (1-D_{MAX}) + R_{DS(ON)\_L} x D_{MAX} \end{aligned} \quad (1)$$

Where $I_{IN(MAX)}$ is the maximum input current (I_{IN}), R_{DCR} is the DC inductor resistance, R_{SENSE} is the current-sense resistor, $R_{DS(ON)\_H}$ is the HS-FET on resistance, and $R_{DS(ON)\_L}$ is the LS-FET on resistance.

Over-Current Protection (OCP)

The MPQ3446 supports configurable cycle-by-cycle current limiting. Register USER01, bits[13:11] determine the desired current limit level. R_{SENSE} should be placed between the

CSA and CSB pins to detect I_L. Once the sense voltage (V_{SENSE}) exceeds the current limit reference (I_{LIM_REF}), BG turns off and TG turns on to discharge I_L until I_L ramps down to the valley current limit. Then the part begins the next charging cycle. The valley current limit is 80% of the MPQ3446's peak current limit, and automatically adjusts according to the peak current limit register setting. A small, 300ns deglitch time for both the peak current limit and valley current limit can avoid mistriggering during high-current operation.

Reverse Current Limit

The MPQ3446 has a reverse current limit, for which the value is 30% of the set peak current limit. In FCCM, if the reverse current exceeds the reverse current threshold, the device terminates the switching cycle and both the HS-FETs and LS-FETs remain off for the rest of the switching cycle. The current limit prevents the reverse current from dropping too low and damaging the components.

Configurable Frequency and Frequency Spread Spectrum (FSS)

f_{SW} can be adjusted to be between 250kHz and 2.5MHz, and can be configured via register USER00 (00h), bits[6:0].

To optimize EMI performance, the MPQ3446 features frequency spread spectrum (FSS). The FSS modulation frequency and modulation range are set via register USER03 (03h), bits[15:14] and bits[13:12], respectively. Once FSS is enabled and configured via register OTP_USER_RESERVE (1Eh), bit[4], triangular frequency modulation mode is used to vary f_{SW} within a certain range above or below the reference frequency. f_{SW} varies from its lowest value to its highest value, then drops back to its lowest value in a whole modulation cycle. Figure 5 shows FSS.

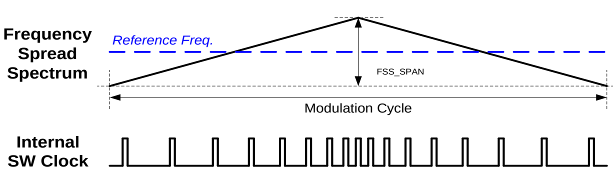


Figure 5: Frequency Spread Spectrum

IMON

The IMON pin outputs a voltage proportional to the voltage sensed back between the CSA and CSB pins (V_{SENSE}). Connect a 1nF to 10nF decoupling capacitor between the IMON and AGND pins to filter the noise at IMON.

When V_{SENSE} exceeds 15mV, if $V_{REF\_CLP} \leq$ 100mV is selected, the gain of (V_{CSA} - V_{CSB}) to V_{IMON} is about 25. If V_{REF_CLP} > 100mV is selected, the gain of (V_{CSA} - V_{CSB}) to V_{IMON} is about 12.5. Figure 6 shows the relationship between V_{IMON} and I_{IN}.

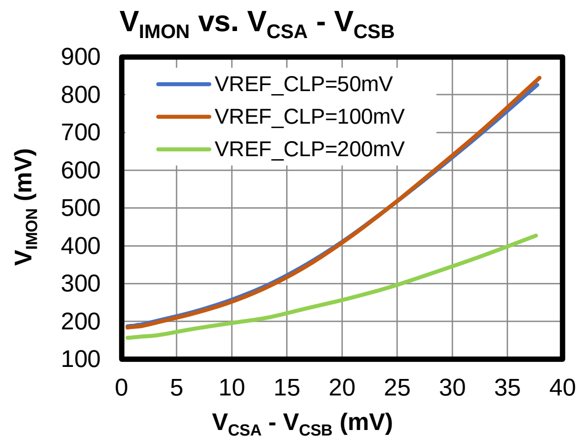


Figure 6: V_{IMON} vs. V_{CSA} - V_{CSB}

Current Sense and Slope Compensation

The MPQ3446 features a high-side (HS) current-sense (CS) amplifier with a gain of 10. I_L is sensed back between the CSA and CSB pins for closed-loop regulation and over-current protection (OCP). Place R_{SENSE} in series with the inductor for good CS accuracy.

The MPQ3446 provides an internal slope compensation ramp to prevent subharmonic oscillation at high duty cycles. For duty cycles greater than 50%, peak current mode regulators are subject to subharmonic oscillation. Subharmonic oscillation is normally characterized by observing alternating wide and narrow duty cycles. Slope compensation can eliminate subharmonic oscillation by adding an artificial ramp to the sensed I_L. The device generates the slope compensation ramp using a sawtooth current source. This current flows through an internal resistor, and the slope compensation can be configured via register USER01 (01h), bits[2:0].

The slope compensation is from 0.1V x f_{SW} (typical) to 0.8V x f_{SW} (typical) with a 0.1V step.

COMP

The MPQ3446 includes internal feedback (FB) resistors that are set based on the V_{OUT} selection configured via register USER02 (02h), bits[7:0]. The FB resistor divider connects to an internal transconductance error amplifier (EA). The internal transconductance EA source and sink currents are proportional to the difference between the FB resistor divider voltage (V_{FB}) and internal V_{REF}. The EA output connects to the COMP pin, allowing the use of a Type 2 loop compensation network (see Figure 7). R_{COMP}, C_{COMP}, and C_{POLE} loop compensation components configure the EA gain and phase characteristics to achieve a stable loop response.

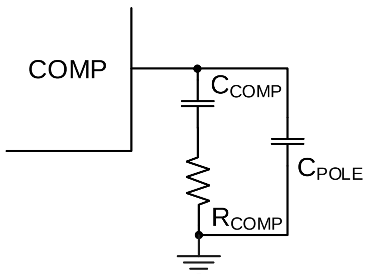


Figure 7: Compensation Network

VCC Power

The PVCC pin powers the MPQ3446's internal driver circuits, while the AVCC pin powers the rest of the blocks. The PVCC power is regulated to 10V from the VIN or VOUT pin, and requires a minimum 4.7μF high-quality, low-ESR ceramic capacitor for decoupling. The PVCC under-voltage lockout (UVLO) threshold can be configured via register USER00 (00h), bit[11]. The AVCC pin is regulated to 5V from the PVCC pin, and requires a minimum 1μF ceramic capacitor for decoupling.

Soft Start (SS)

The MPQ3446 provides an internal soft start (SS) to control the V_{OUT} slew rate under low V_{IN} conditions. With the proper slew rate control and output filtering capacitor selection, the inrush current at V_{IN} can be well controlled. V_{OUT} slew rate control can be configured using register USER01 (01h), bits[10:8] via the I^2C or SPI.

BG, TG, and BST Functionality

The MPQ3446 generates two complementary gate driver signals to control the LS-FET and HS-FET via the BG and TG pins, respectively. The BG pin is directly powered from PVCC, while the TG pin is powered by the floating capacitor (C_{BST}) across the BST and SW pins. An external low-leakage diode must be placed between the PVCC and BST pins to charge C_{BST} while the LS-FET is on, a 1N4148 is recommended. It is also recommended to place a 1N4148 diode between the BST and SW pins to prevent BST-SW voltage (V_{BST-SW}) from being discharged to less than -0.3V.

Enable (EN)

The EN pin enables and disables the MPQ3446. When the applied voltage exceeds the 0.8V threshold, the MPQ3446 starts up some of the internal circuitry (micro-power mode). If the EN voltage (V_{EN}) exceeds the 1.2V threshold, the MPQ3446 enables all functions and starts boost operation. If V_{EN} falls below the 1.0V threshold, boost operation turns off. To completely shut down the MPQ3446, pull EN below the 0.5V shutdown level. Do not float the EN pin if it is not used.

SYNCI and SYNCO

f_{SW} can be synchronized to the falling edge of the clock signal applied at the SYNCI pin. The recommended SYNCI frequency range is 250kHz to 2.5MHz. Ensure that the SYNCI frequency is ±20% of the range of the internal oscillator. There is no other special limit on the SYNCI pulse width and off time, but there is always parasitic capacitance of the pad. If the pulse width or off time is too short, a clear rising and falling edge may not be seen due to parasitic capacitance. A pulse or off time longer than 100ns is recommended.

The SYNCO can reflect the frequency and phase of internal oscillator. The phase shift from SYNCI in clock to SYNCO can be set to 0° or 180° via register 00h, bit[8], while SYNCO can be the same or half of SYNCI frequency or setting swtiching frequency via register USER00 (00h), bit[9]. The MPQ3446 can also synchronize with another phase of the MPQ3446 or another power device altogether.

Power Good (PG)

The PG pin is an open-drain output and requires a pull-up resistor to the AVCC pin. PG is pulled high if V_{OUT} is within 96% to 104% of its nominal voltage, and is pulled low when V_{OUT} is above 105% or below 95% of its nominal voltage.

Under-Voltage Lockout (UVLO)

The MPQ3446 features input UVLO protection to ensure reliable output power (P_{OUT}). Assuming the PVCC and EN pins are active, the MPQ3446 powers on when V_{IN} exceeds the UVLO rising threshold (typically 3.1V). The device stops switching when V_{IN} falls below the UVLO falling threshold (typically 2.55V). This prevents the device from operating at an insufficient voltage.

Start-Up and Shutdown

If V_{IN}, V_{PVCC}, and V_{EN} exceed their respective thresholds, the chip starts up. The reference block starts first, generating a stable V_{REF} and current, then the internal regulator for the PVCC and AVCC pins is enabled. The regulator provides a stable supply for all operating circuitries.

Before the power stage begins switching, the digital controller accesses the one-time programmable (OTP) memory to load all the programmed data. It takes about 2ms to 3ms to preload all the settings to the part.

Four major events can shut down the power stage and reinitiate SS for the part:

- V_{OUT} drops below 50% of the V_{OUT} target
- PVCC/AVCC drops below the UVLO threshold
- The junction temperature (T_J) reaches the thermal shutdown threshold
- An issue is detected in the OTP circuit

If EN is pulled low, the part initiates a shutdown sequence. The driver, analog blocks, digital controller, and base circuitries (such as bandgap reference and monitors) turn off in that order.

Over-Voltage Protection (OVP)

If V_{OUT} exceeds the preset over-voltage protection (OVP) threshold (120% of the typical V_{OUT} by default), the part stops switching to avoid overcharging V_{OUT}. A deglitch time (about 60μs) is added to prevent mistriggering when the V_{OUT} is approaching the threshold. The OVP threshold can be set by via register USER01 (01h), bits[4:3]. Once V_{OUT} drops below 103% of the typical V_{OUT}, the part resumes normal operation with HS-FET and LS-FET switching to regulate the output.

Thermal Warning and Thermal Shutdown

Thermal warning is indicated and can be read via the I^2C or SPI interface. The warning status is shown in register SYSTEM01 (07h), bit[1] if the silicon die temperature exceeds its upper threshold (typically 125°C). The warning bit is set until T_J drops below the lower hysteresis level (105°C).

If T_J exceeds 170°C, thermal shutdown triggers to protect the part. If the junction overheats and thermal shutdown reaches its threshold, the device enters a low-power shutdown state with the MOSFET driver disabled. At the same time, register SYSTEM01 (07h), bit[0] is set to 1 and can be read via the I^2C or SPI interface. Once T_J drops below 150°C, the part exits the shutdown state, register SYSTEM01 (07h), bit[0] clears back to 0, and the part reinitiates SS.

I²C INTERFACE

The MPQ3446 features an I²C interface to configure some key parameters.

I²C Serial Interface Description

The I²C is a two-wire, bidirectional serial interface that consists of a data line (SDA) and a clock line (SCL). When the lines are idle, they are externally pulled to a bus voltage (V_{BUS}). A master device connects to the line and generates the SCL signal and device address to arrange the communication sequence. The MPQ3446 interface is an I²C slave device that supports fast mode (400kHz). The I²C interface adds flexibility to the power supply solution. V_{OUT}, the transition slew rate, and other parameters can be instantaneously controlled via the I²C interface. It is recommended to leave trim options for more I²C addresses to preserve the possibility of multiple ICs communicating in one system. Set the 4MSB to 0100b to make the device compatible with PMBus protocols.

Start and Stop Commands

The master device signals the start (S) and stop (P) commands to signify the beginning and end of the I²C transfer, respectively. A start command is defined as the SDA line transitioning from high to low while the SCL line is high. A stop command is defined as the SDA line transitioning from low to high while the SCL line is high. Figure 8 shows the start and stop conditions.

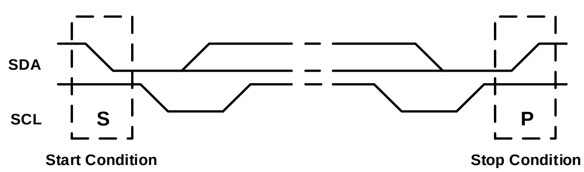


Figure 8: Start and Stop Conditions

The master device then generates the SCL clocks and transmits the device address and the read/write (R/W) direction bit to the SDA line.

Data Transfer

Every byte on the SDA line must be 8 bits long. Each byte must be followed by an acknowledge (ACK) bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse, so that it remains stable low during the high period of the clock pulse.

I²C Update Sequence

The MPQ3446 requires a start command, a valid I²C address, a register address byte, and a data byte for a single data update. After receiving each byte, the MPQ3446 acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MPQ3446, and the part performs an update on the falling edge of the LSB byte.

SPI INTERFACE

SPI Serial Interface Description

The MPQ3446 features a four-wire SPI interface with CPOL = CPHA = 1 (SPI mode 3, clock idle high, sample data at the rising edge).

The MPQ3446 uses the COM (active low), SCL (serial clock), SDA (serial data input), and IMON (serial data output) pins to configure the SPI interface. Communication starts when COM is pulled low via the SPI master device, and stops when COM is pulled high. The SPI master device also controls the SCL pin. Both the SDA and IMON pins are driven at SCL's falling edge, and should be captured at SCL's rising edge. The COM pin is kept low while sending data.

The features of SPI are:

- 24-bit frame size
- Up to 4MHz clock speed
- The command and data are shifted as MSB first, LSB last
- The SDA line is sampled on SCL's rising edge
- The IMON line is shifted out on SCL's falling edge

The SPI master device should meet the following criteria:

- The SPI does not support back-to-back frame operation. After each SPI transfer, the COM pin must go from low to high, then back to low, before the next SPI transfer can start.
- The minimum time between two SPI commands, during which the COM pin must remain high, is 40µs.

REGISTER MAP

Command Code	Command Name	Type	Bytes	Page 0
00h	USER00	R/W	2	✓
01h	USER01	R/W	2	✓
02h	USER02	R/W	2	✓
03h	USER03	R/W	2	✓
06h	SYSTEM00	R/W	2	✓
07h	SYSTEM01	R/W	2	✓
08h	MASTER_SLAVE_KEY	R/W	2	✓
1Eh	OTP_USER_RESERVE	R/W	2	✓

PAGE 0 REGISTER MAP FOR MPQ3446-0000

USER00 (00h)

Format: Unsigned binary

The USER00 command configures the master/slave mode, enables and disables the device, and sets the mode under light loads. It can also set PVCC parameters, boost switching frequency (f_{SW}), and clock synchronicity for multi-phase applications.

Bits	Access	Bit Name	Description
15	R/W	MASTER_SLAVE	Controls the master/slave mode. 1'b 0: Master (default) 1'b 1: Slave
14	R/W	DIS_BOOST	Enables and disables the converter. 1'b 0: Enabled (default) 1'b 1: Disabled
13	R/W	FORCEVIN	Forces V_{IN} to be the main power source for the PVCC low-dropout regulator (LDO). 1'b 0: Follow the internal decision logic (default) 1'b 1: Force V_{IN} to be the main power source
12	R/W	RESERVED	Reserved.
11	R/W	PVCC_UVLO	Sets the PVCC under-voltage lockout (UVLO) level. 1'b 0: 5V (default) 1'b 1: 6.5V
10	R/W	FCCM	Sets the control mode under light loads. 1'b 0: DCM 1'b 1: FCCM (default)
9	R/W	SYNCI_DIV	Selects the CLK synchronicity during multi-phase operation. 1'b 0: 1x (default) 1'b 1: 0.5x
8	R/W	SYNCI_PHASE	Selects the CLK synchronicity during multi-phase operation. 1'b 0: 0° (default) 1'b 1: 180°
7	R/W	RESERVED	Reserved.
6:0	R/W	FS	Sets the switching frequency (f_{SW}). LSB = 25kHz, MSB = 1600kHz. f_{SW} = bits[6:0] x 25kHz + 200kHz For example: 7'b 0000010: f_{SW} = 250kHz 7'b 0001011: f_{SW} = 475kHz (default) 7'b 0100000: f_{SW} = 1MHz 7'b 1010000: f_{SW} = 2.2MHz

USER01 (01h)

Format: Unsigned binary

The USER01 command configures the current limit, soft-start time (t_{SS}), PG function, bypass threshold, and boost slope compensation.

Bits	Access	Bit Name	Description
15:14	R/W	RESERVED	Reserved.

13:11	R/W	ILIM_REF	Sets the current limit threshold. 3'b 000: 25mV 3'b 001: 50mV (default) 3'b 010: 75mV 3'b 011: 100mV 3'b 100: 125mV 3'b 101: 150mV 3'b 110: 175mV 3'b 111: 200mV
10:8	R/W	TSS	Sets the V_{OUT} slew rate (using the look-up table). The controlled slew rates are described as follows: 3'b 000: 20.0000 (V/ms) 3'b 001: 10.0000 (V/ms) 3'b 010: 5.00000 (V/ms) 3'b 011: 2.50000 (V/ms) (default) 3'b 100: 1.25000 (V/ms) 3'b 101: 0.62500 (V/ms) 3'b 110: 0.31250 (V/ms) 3'b 111: 0.15625 (V/ms)
7:5	R/W	RESERVED	Reserved.
4:3	R/W	OVP THRESHOLD	Sets the boost over-voltage protection (OVP) threshold. 2'b 00: 105% 2'b 01: 110% 2'b 10: 115% 2'b 11: 120% (default)
2:0	R/W	SLOPE_COMP	Selects the boost slope compensation. 3'b 000: 0.1V/T 3'b 001: 0.2V/T (default) 3'b 010: 0.3V/T 3'b 011: 0.4V/T 3'b 100: 0.5V/T 3'b 101: 0.6V/T 3'b 110: 0.7V/T 3'b 111: 0.8V/T

USER02 (02h)

Format: Unsigned binary

The USER02 command configures the device output voltage (V_{OUT}), dead time, and duty-related parameters. It can also activate boost TG control and enable pulse-skip mode (PSM).

Bits	Access	Bit Name	Description
15	R	RESERVED	Reserved. Always reads as 0.
14	R/W	TG_ENABLE	Sets boost TG control. 1'b 0: Turn-off TG control (asynchronous) 1'b 1: Turn-on TG control (synchronous) (default)
13:12	R/W	DEAD_TIME	Sets the dead time for TG/BG. 2'b 00: 40ns (default) 2'b 01: 60ns 2'b 10: 80ns 2'b 11: 100ns
11	R/W	RESERVED	Reserved.

10	R/W	PULSE_SKIP	Enables PSM. 1'b 0: Enable PSM (default) 1'b 1: Disable PSM
9	R/W	RESERVED	Reserved.
8	R/W	MAX_DUTY	Sets the maximum duty cycle. 1'b 0: 86% (default) 1'b 1: 90%
7:0	R/W	DVS_VOUT	Sets the boost controller's V_{OUT}. Bits[7:6] set the ratio of the feedback resistor divider (FB DIV) connected to the EA. Set via the look-up table, nonlinear control. FB DIV = (1/10)x, (1/20)x, (1/40)x, (1/50)x. Bits[5:0] set the internal V_{REF} for the EA. Range 1: Boost V_{OUT} = 6V - 12V (V_{REF} = 0.6V to 1.23V, FB DIV = (1/10)x, step = 10mV/LSB) Range 2: Boost V_{OUT} = 12V - 24V (V_{REF} = 0.6V to 1.23V, FB DIV = (1/20)x, step = 10mV/LSB) Range 3: Boost V_{OUT} = 24V - 48V (V_{REF} = 0.6V to 1.23V, FB DIV = (1/40)x, step = 10mV/LSB) Range 4: Boost V_{OUT} = 48.5 - 55V (V_{REF} = 0.97V to 1.6V, FB DIV = (1/50)x, step = 10mV/LSB) Equation for V_{OUT} DVS control (default Boost V_{OUT} = 9V): 8'd000–8'd060: Boost V_{OUT} = 6V + 0.1 x value of (DVS_VOUT, bits[5:0]) 8'd061–8'd063: Boost V_{OUT} = 12V (remains as-is) 8'd064–8'd124: Boost V_{OUT} = 12V + 0.2 x value of (DVS_VOUT, bits[5:0]) 8'd125–8'd127: Boost V_{OUT} = 24V (remains as-is) 8'd128–8'd188: Boost V_{OUT} = 24V + 0.4 x value of (DVS_VOUT, bits[5:0]) 8'd189–8'd191: Boost V_{OUT} = 48V (remains as-is) 8'd192–8'd205: Boost V_{OUT} = 48.5V + 0.5 x value of (DVS_VOUT, bits[5:0])

USER03 (03h)

Format: Unsigned binary

The USER03 command configures the frequency spread spectrum (FSS) parameters and I²C address.

Bits	Access	Bit Name	Description
15:14	R/W	FSS_FREQ	Controls the FSS behavior. 2'b 00: 1.95kHz 2'b 01: 3.90kHz 2'b 10: 7.80kHz (default) 2'b 11: 15.6kHz
13:12	R/W	FSS_SPAN	Controls the FSS behavior. 2'b 00: ±6.25% of f_{SW} (default) 2'b 01: ±12.5% of f_{SW} 2'b 10: ±18.75% of f_{SW} 2'b 11: ±25% of f_{SW}
11:4	R/W	SLAVE_ADDR_KEY	Sets the I²C address access unlock key. Set these bits to 8'h A8.
3:0	R/W	ADDRESS_CODE	Sets the I²C address (default 4'h 8).

SYSTEM00 (06h)

Format: Unsigned binary

The SYSTEM00 command configures different protections for the MPQ3446.

Bits	Access	Bit Name	Description
15:13	R	RESERVED	Reserved.

12	R/W	BOOST_OCP_EN	Enables boost over-current protection (OCP). 1'b 0: Disabled 1'b 1: Enabled (default)
11	R/W	BOOST_VOUT_UV_EN	Enables boost output under-voltage protection (UVP). 1'b 0: Disabled (default) 1'b 1: Enabled
10:0	R	RESERVED	Reserved.

SYSTEM01 (07h)

Format: Unsigned binary

The SYSTEM01 command configures thermal shutdown protection and indicates the PVCC source and thermal status in real time.

Bits	Access	Bit Name	Description
15:4	R	RESERVED	Reserved.
3	R/W	THER_SD_EN	Enables thermal shutdown. 1'b 0: Disabled 1'b 1: Enabled (default)
2	R	PVCC_POWER	Real-time PVCC source indicator (V_{IN} or V_{OUT}). 1'b0: V_{OUT} (default) 1'b1: V_{IN}
1	R	THER_WARN	Real-time thermal warning indicator. 1'b 0: No thermal warning (default) 1'b 1: Thermal warning
0	R	THER_SD	Real-time thermal shutdown indicator. 1'b 0: No thermal shutdown (default) 1'b 1: Thermal shutdown

MASTER_SLAVE_KEY (08h)

Format: Unsigned binary

The MASTER_SLAVE_KEY command is used to unlock the master/slave setting.

Bits	Access	Bit Name	Description
15:0	R/W	MASTER_SLAVE_KEY	MASTER_SLAVE unlock key; set these bits to 16'h BC8A.

OTP_USER_RESERVE (1Eh)

Format: Unsigned binary

The OTP_USER_RESERVE command enables FSS.

Bits	Access	Bit Name	Description
15:5	R	RESERVED	Reserved.
4	R/W	FSS_EN	1'b 0: Enable FSS (default) 1'b 1: Disable FSS
3:0	R	RESERVED	Reserved.

APPLICATION INFORMATION

Selecting the Input Capacitor

The input capacitors reduce the V_{IN} ripple. Use a low-ESR capacitor with a >4.7µF value to minimize noise. High-quality ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors also suffice.

To ensure stable operation, place the input capacitors as close to the IC as possible. Since the input capacitors absorb the input switching current, they require an adequate ripple current rating. Use a capacitor with an RMS current rating greater than the inductor ripple current.

It is strongly recommended to place a small, high-quality ceramic 0.1µF capacitor as close to the IC as possible to absorb high-frequency switching noise.

Selecting the Output Capacitor

The output capacitors smooth the V_{OUT} ripple (V_{RIPPLE}) and provide a charging source during load transient conditions. Output capacitors also reduce V_{OUT} overshoot if the load suddenly disconnects. Use ceramic, tantalum or low-ESR electrolytic capacitors. For the best result, use low-ESR capacitors to minimize V_{RIPPLE}. The C_{OUT} characteristics also affect the regulatory control system's stability. For ceramic capacitors, the capacitance dominates the impedance at f_{SW}, and V_{RIPPLE} is mostly independent of the ESR. V_{RIPPLE} can be estimated with Equation (2):

$$V_{RIPPLE} \cong I_{LOAD} x \frac{1 - \frac{V_{IN}}{V_{OUT}}}{C_{OUT} \times f_{SW}} \qquad (2)$$

Where V_{RIPPLE} is the output voltage ripple, V_{IN} and V_{OUT} are the DC input and output voltages respectively, I_{LOAD} is the load current, f_{SW} is the switching frequency, and C_{OUT} is the output capacitance.

For tantalum or low-ESR electrolytic capacitors, the ESR dominates the impedance at f_{SW}. V_{RIPPLE} can be calculated with Equation (3):

$$V_{RIPPLE} \cong I_{LOAD} \times \frac{1 - \frac{V_{IN}}{V_{OUT}}}{C_{OUT} \times f_{SW}} + \frac{I_{LOAD} \times R_{ESR} \times V_{OUT}}{V_{IN}} \qquad (3)$$

Where R_{ESR} is the equivalent series resistance (ESR) of C_{OUT}.

The C_{OUT} ripple current rating must be enough to handle the output ripple current (I_{RIPPLE}). By using multiple output capacitors, I_{RIPPLE} can be split. In practice, ceramic capacitors are placed closer to the LS-FET and HS-FET than the electrolytic capacitors to absorb the majority of I_{RIPPLE}. It is recommended to use low-ESR electrolytic capacitors to ensure I_{RIPPLE} capability and also use some additional 10µF ceramic capacitors, placed close to the switching components, to minimize switching noise. It is also strongly recommended to place a small, high-quality ceramic 0.1µF capacitor as close to the IC as possible to absorb high-frequency switching noise.

Selecting the Inductor

The inductor forces V_{OUT} to exceed V_{IN}. A larger-value inductor results in less ripple current and reduces the peak inductor current (I_{L_PK}); this reduces the stress on the internal N-channel MOSFET. However, a larger-value inductor is also physically larger, has a higher series resistance, and/or lower saturation current. Choosing a low-DCR inductor can help achieve higher efficiency.

A good rule of thumb is to allow the peak-to-peak ripple current to equal 30% to 50% of the maximum I_{IN}. During normal boost operation, make sure that I_{L_PK} is below 75% of the current limit to prevent regulator losses from the current limit. Make sure that the inductor does not saturate under the worst-case load transient and start-up conditions. The required inductance (L) can be calculated with Equation (4):

$$L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT} \times f_{SW} \times \Delta I} \qquad (4)$$

Where ΔI is the peak-to-peak inductor ripple current, and ΔI = (30% to 50%) x I_{IN}.

The maximum input current ($I_{IN(MAX)}$) can be calculated with Equation (5):

$$I_{IN(MAX)} = \frac{V_{OUT} \times I_{LOAD(MAX)}}{V_{IN} \times \eta} \qquad (5)$$

Where $I_{LOAD(MAX)}$ is the maximum load current, ΔI is peak-to-peak inductor ripple current, ΔI = (30% to 50%) x I_{IN}, η is the efficiency, and I_{IN} is the average input current with the maximum load.

Selecting the Current-Sense Resistor (R_{SENSE})

The MPQ3446 features current limit (I_{LIM}) options from 25mV to 200mV, with a 25mV step. Ensure that the application can deliver a full load of current across the full operating temperature range when setting I_{LIM}.

The current-sense resistor (R_{SENSE}) monitors the inductor current (I_L). Its value is chosen based on the I_{LIM} threshold. The relationship between the peak current (I_{PK}) and R_{SENSE} can be calculated with Equation (6):

$$R_{SENSE} = \frac{V_{ILIM}}{I_{PK}} \quad (6)$$

The maximum peak I_{IN} capability should be 30% to 50% greater than the required peak current at low V_{IN} and full loads to account for tolerances.

A higher R_{SENSE} increases power loss across the resistor. Considering I_{OUT}, efficiency, and I_{LIM} threshold, the recommended value for R_{SENSE} is between 2mΩ and 5mΩ.

Selecting the Power MOSFET

The MPQ3446 can drive a wide variety of N-channel power MOSFETS. The critical parameters when selecting a MOSFET are:

- Maximum drain-to-source voltage ($V_{DS(MAX)}$)
- Maximum drain current ($I_{D(MAX)}$)
- On resistance ($R_{DS(ON)}$)
- Total gate charge (Q_G)
- Turn-on threshold (V_{TH})

Two N-channel MOSFETs must be selected as the controllers for the HS-FET and LS-FET.

Ideally, the off-state voltage across the MOSFET equals the boost V_{OUT}. Considering the voltage spike when it turns off, $V_{DS(MAX)}$ should be greater than 1.5 times V_{OUT}.

The maximum current through the power MOSFET occurs when V_{IN} is at its minimum and P_{OUT} is at its maximum. The peak and average currents through the MOSFET can be calculated with Equation (7) and Equation (8), respectively:

$$I_{IN(PEAK)} = I_{IN(AVERAGE)} + \frac{1}{2}\Delta I_{IN} \quad (7)$$

$$I_{IN(AVERAGE)} = \frac{V_{OUT} \times I_{LOAD}(max)}{V_{IN}(min) \times \eta} \quad (8)$$

Where ΔI_{IN} = (30% to 50%) x $I_{IN(AVERAGE)}$.

The current rating of the MOSFET should be greater than 1.5 x $I_{IN(PEAK)}$.

The MOSFETs' $R_{DS(ON)}$ determines the conduction loss. The low-side (LS) conduction loss can be calculated with the Equation (9) and Equation (10):

$$P_{COND(LS)} = (1 - \frac{V_{IN}}{V_{OUT}}) \times I_{IN^2} \times R_{DS(ON)\_L} \times 1.3 \quad (9)$$

$$I_{IN} = \frac{I_{OUT} \times V_{OUT}}{V_{IN}} \quad (10)$$

The high-side (HS) conduction loss can be calculated with Equation (11):

$$P_{COND(HS)} = \frac{V_{IN}}{V_{OUT}} \times I_{IN^2} \times R_{DS(ON)\_H} \times 1.3 \quad (11)$$

Where the factor of 1.3 accounts for the increase in the N-channel MOSFET $R_{DS(ON)}$ due to heating. Alternatively, the factor of 1.3 can be eliminated and the N-channel MOSFET's high-temperature $R_{DS(ON)}$ can be estimated using the $R_{DS(ON)}$ vs. temperature curves in the N-channel MOSFET datasheet. A smaller $R_{DS(ON)}$ can achieve better efficiency.

Q_G is required to estimate the turn-on and turn-off loss, which affect the switching loss. A small Q_G causes a fast turn-on/-off speed, which decreases the switching loss. A very small Q_G causes the negative spike of SW, so it is important to choose a suitable MOSFET based on the specifications.

V_{TH} is also important. GATE is powered via PVCC, so V_{TH} must be less than PVCC.

Selecting the BST Components

The bootstrap capacitor (C_{BST}) between the BST and SW pins supplies the gate current to charge the HS-FET device gate during each cycle's turn-on period. The recommended C_{BST} is 0.1µF. C_{BST} should be a good quality, low-ESR, ceramic capacitor located at the pins of the device to minimize potentially damaging voltage transients caused by trace inductance.

A low-leakage diode between PVCC and BST pins is required to ensure that the BST voltage (V_{BST}) is high enough under all conditions. A 1N4148 or diode with similar leakage characteristics is recommended. The D_{BST} voltage rating should be greater than the peak SW node voltage. The D_{BST} leakage current should be low enough for the BST charge pump to maintain a sufficient HS driver supply voltage at high temperatures. A 1N4148 diode is also recommended between the BST and SW pins to prevent the BST-SW voltage (V_{BST-SW}) from being discharged to less than -0.3V.

Compensation Components

The transconductance EA (COMP) output is used to compensate for the regulation control system. The system uses two poles and one zero to stabilize the control loop. The poles are F_{P1}, which is set by C_{OUT} and the load resistance, and F_{P2}, which starts from the origin. The zero (F_{Z1}) is set by both the compensation capacitor (C_{COMP}) and the compensation resistor (R_{COMP}). F_{P1} and F_{Z1} can be calculated with Equation (12) and Equation (13), respectively:

$$F_{P1} = \frac{1}{2 \times \pi \times C_{OUT} \times R_{LOAD}} \tag{12}$$

$$F_{Z1} = \frac{1}{2 \times \pi \times C_{COMP} \times R_{COMP}} \tag{13}$$

Where R_{LOAD} is the load resistance.

The DC mid-band loop gain can be calculated with Equation (14):

$$A_{VDC} = \frac{0.5 \times G_{EA} \times V_{IN} \times R_{LOAD} \times V_{REF} \times R_{COMP}}{V_{OUT}^2 \times R_{SENSE} \times G_{SENSE}} \tag{14}$$

Where V_{REF} is the voltage reference, G_{SENSE} is the current-sense amplifier gain, and G_{EA} is the EA transconductance.

In this example, the ESR zero locates at a very high frequency and is not taken into design consideration.

There is also a right half-plane zero (F_{RHPZ}) that exists in CCM step-up converters where I_L does not drop to 0A at each cycle. F_{RHPZ} can be calculated with Equation (15):

$$F_{RHPZ} = \frac{V_{IN}^2 \times R_{LOAD}}{2 \times \pi \times L \times V_{OUT}^2} \tag{15}$$

F_{RHPZ} increases the gain and reduces the phase simultaneously, resulting in a smaller phase and gain margin. The worst-case scenario occurs when V_{IN} is at its minimum and P_{OUT} is at its maximum.

To achieve system stability, place F_{Z1} close to F_{P1} to cancel the pole. R_{COMP} is adjusted to change the voltage gain. Ensure that the bandwidth (F_C) is about 1/10 of the lower value of the ESR zero or F_{RHPZ}. R_{COMP} and C_{COMP} can be calculated with Equation (16) and Equation (17):

$$\frac{1}{2 \times \pi \times C_{OUT} \times R_{LOAD}} = \frac{1}{2 \times \pi \times C_{COMP} \times R_{COMP}} \tag{16}$$

$$R_{COMP} = \frac{V_{OUT}^2 \times 2 \times \pi \times C_{OUT} \times F_C \times R_{SENSE} \times G_{SENSE}}{G_{EA} \times V_{REF} \times V_{IN}} \tag{17}$$

If the ESR zero is in a relatively low-frequency region and results in an insufficient gain margin, an optional capacitor (C_{POLE}) should be added between COMP and GND. Then a pole formed between C_{POLE} and R_{COMP} should be placed at the ESR zero to cancel the adverse effect. C_{POLE} can be calculated with Equation (18):

$$C_{POLE} = \frac{1}{2 \times \pi \times R_{COMP} \times F_{ESRZ}} \tag{18}$$

Interleaved Boost

For dual-phase applications, after unlocking the master/slave setting via register MASTER_SLAVE_KEY (08h), set one phase as the master and the other as the slave via register USER00 (00h), bit[15]. Once set to slave mode, the internal EA is disabled. Connect the slave phase COMP to the master phase so the COMP voltage (V_{COMP}) is used as the reference of the PWM comparator and compared to the current-sense signal to determine when the LS-FET turns off. Figure 9 on page 41 shows the typical circuit for dual-phase application.

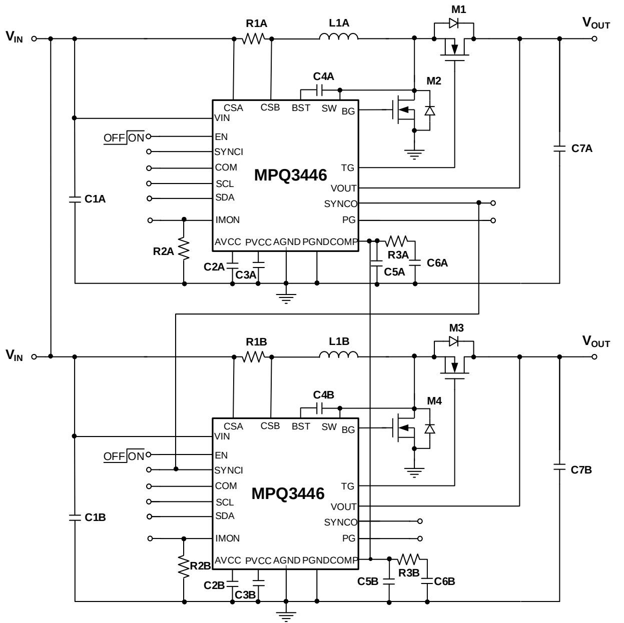


Figure 9: Dual-Phase Configuration

Connect SYNCI of the slave device to SYNCO of the master device. To achieve 180° phase shift operation for the master and slave devices, follow the steps below:

1. Set the master device's SYNCI division = 0.5, and set the slave device's SYNCI division = 1.
2. Set the master device's SYNCI phase = 180°, and set the slave device's SYNCI phase = 0°.

Figure 10 shows SYNCI and SYNCO.

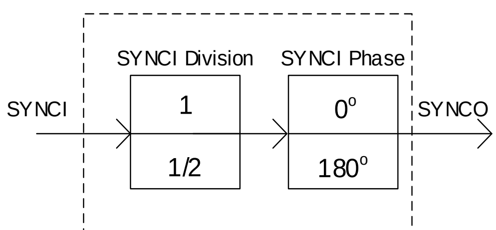


Figure 10: SYNCI and SYNCO

Similarly, when four phases are operating in parallel, the four phases can be interleaved via a proper connection and the SYNCI phase and SYNCI division register setting. Figure 11 shows four-phase configuration.

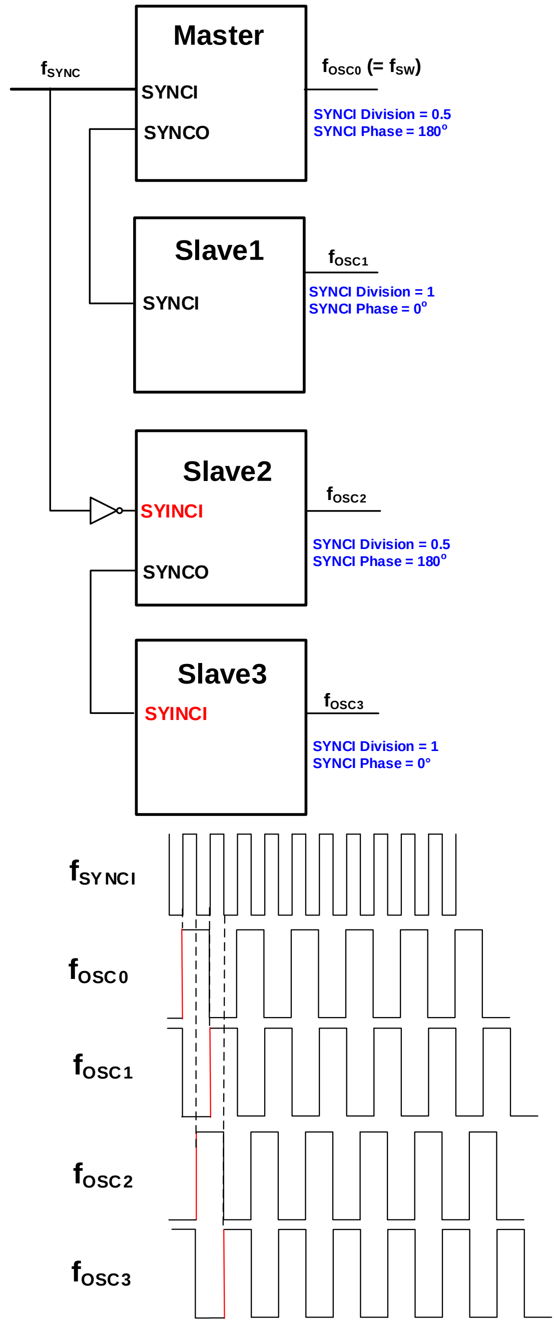


Figure 11: Four-Phase Configuration

Non-Synchronous Applications

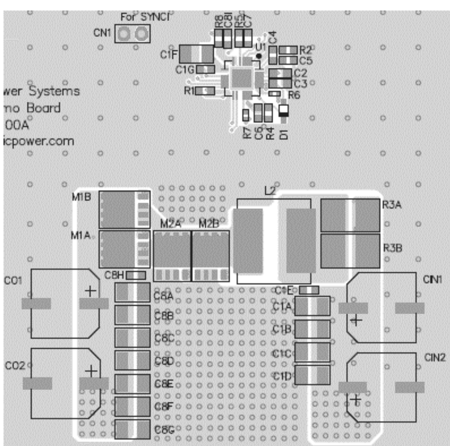
When using the MPQ3446 in non-synchronous applications, the HS-MOSFET should be replaced with a diode, and the TG pin must be disabled through via USER02 (02h), bit[14] to prevent generation of the HS drive signal. Figure 14 on page 43 shows the typical application circuit for the MPQ3446 in non-synchronous applications.

PCB Layout Guidelines

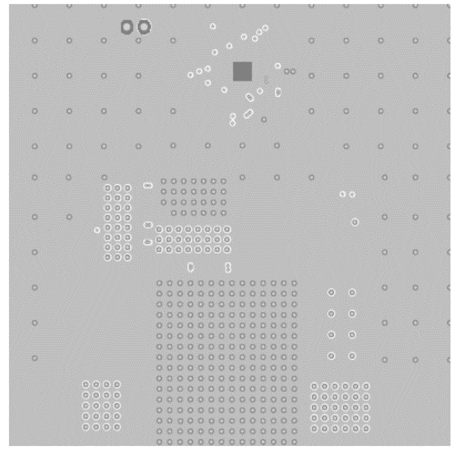
Effective PCB layout is critical for stable operation and low noise in high-frequency switching regulators. In a boost controller, the primary switching loop consists of the output capacitor (C_{OUT}) and the switching between MOSFETs. Minimizing the loop area reduces the stray inductance and minimizes noise. In particular, placing high-quality ceramic output capacitors as close to this loop before the bulk aluminum output capacitors to minimize the output voltage ripple and ripple current of the aluminum capacitors.

For the best results, refer to Figure 12 and follow the guidelines below:

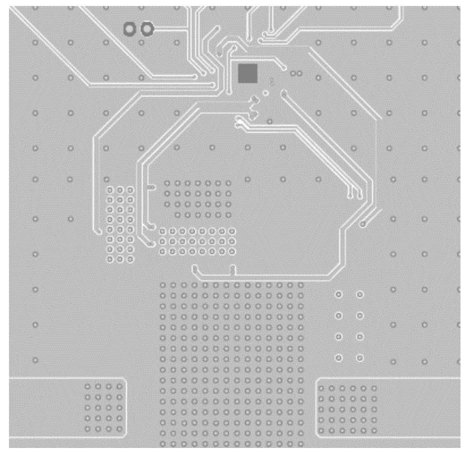
1. Place all components as close to the IC as possible.
2. Keep the path between L1, M1, M2, and C_{OUT} extremely short to minimize noise and ringing.
3. Place C_{IN} close to the VIN pin to maximize decoupling.
4. Tie the C_{IN} and C_{OUT} ground returns close to the GND pin.



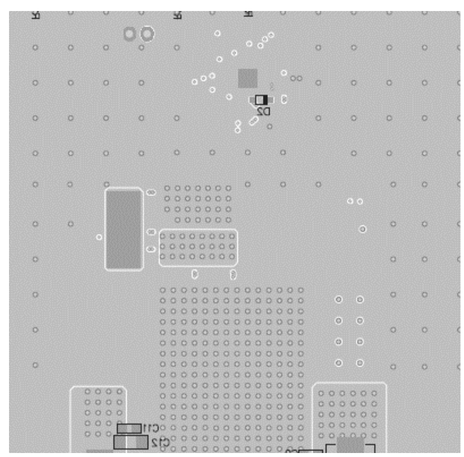
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 12: Recommended PCB Layout (9)

Note:

9) The recommended PCB layout is based on Figure 13 on page 43.

TYPICAL APPLICATION CIRCUITS

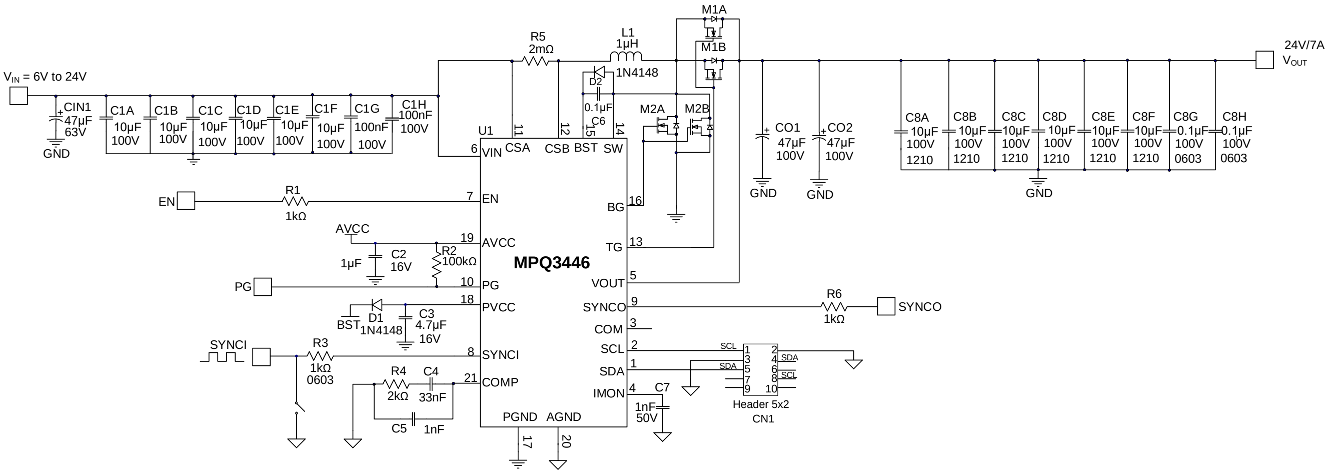


Figure 13: Typical Application Circuit (V_{OUT} = 24V, I_{OUT} = 7A, f_{SW} = 475kHz, Synchronous Application, I^2C Interface)

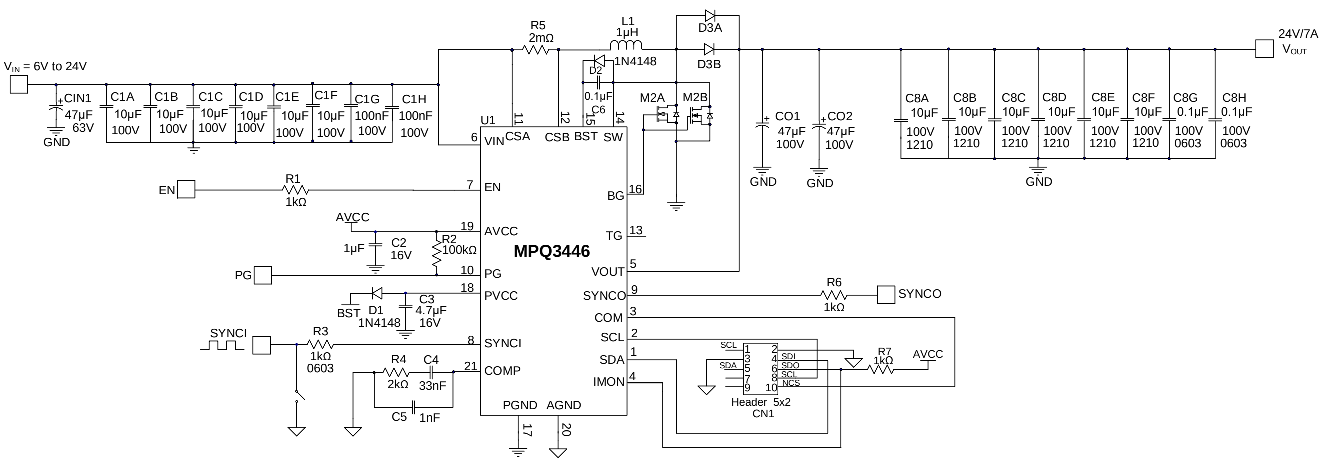


Figure 14: Typical Application Circuit (V_{OUT} = 24V, I_{OUT} = 7A, f_{SW} = 475kHz, Non-Synchronous Application, SPI Interface)

TYPICAL APPLICATION CIRCUITS *(continued)*

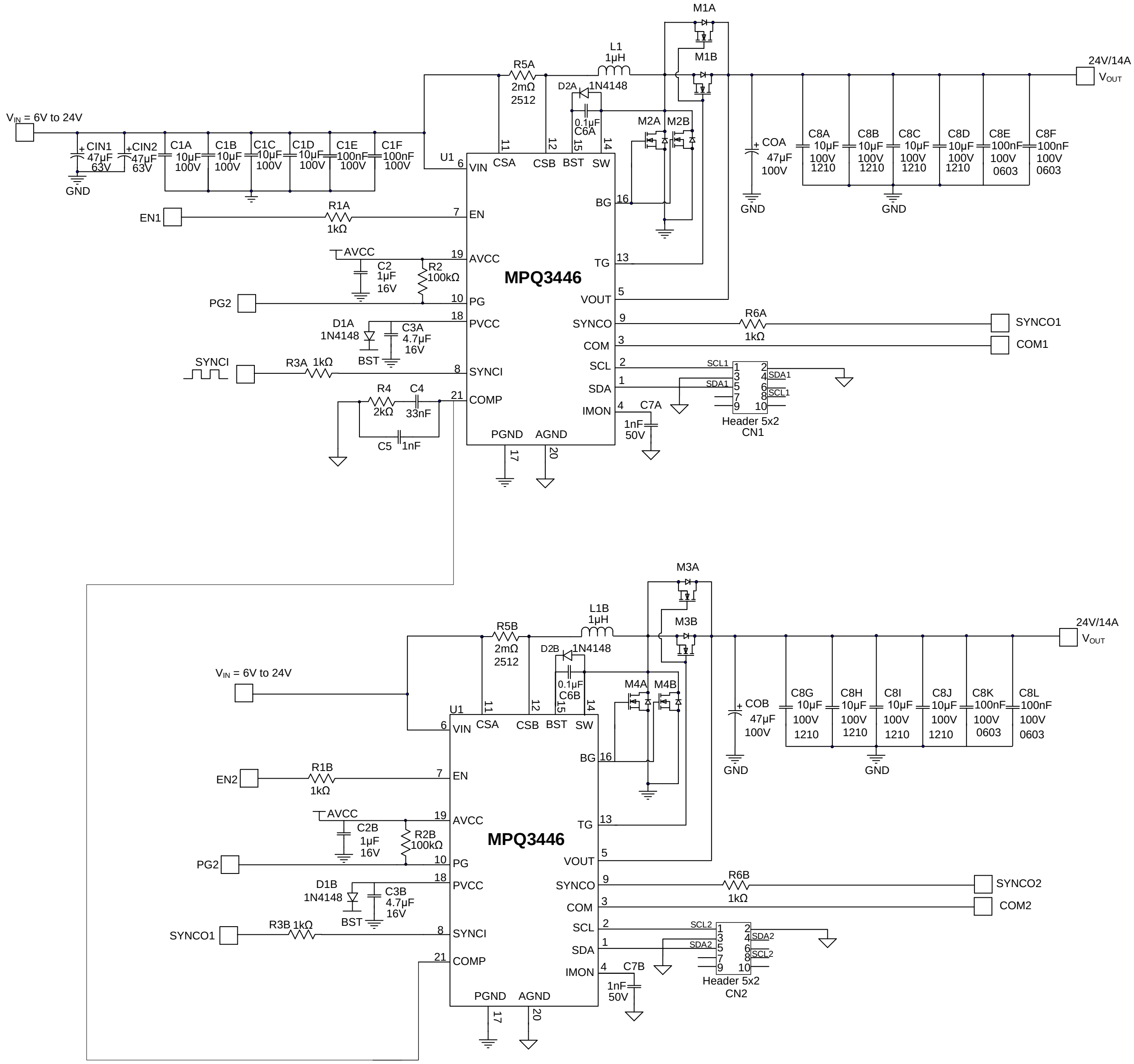
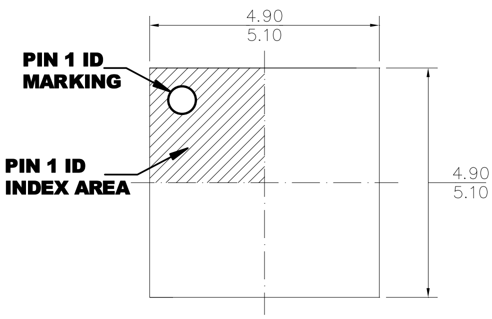


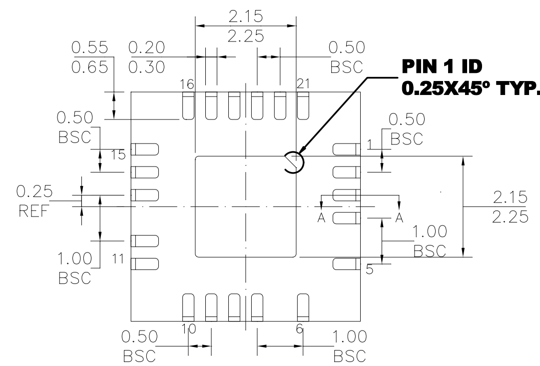
Figure 15: Typical Application Circuit (V_{OUT} = 24V, I_{OUT} = 14A, f_{SW} = 475kHz, Dual-Phase, I²C Interface)

PACKAGE INFORMATION

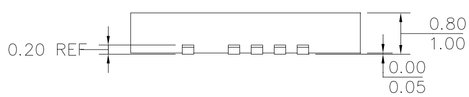
QFN-21 (5mmx5mm)
Wettable Flank



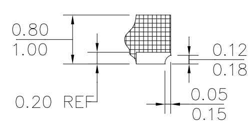
TOP VIEW



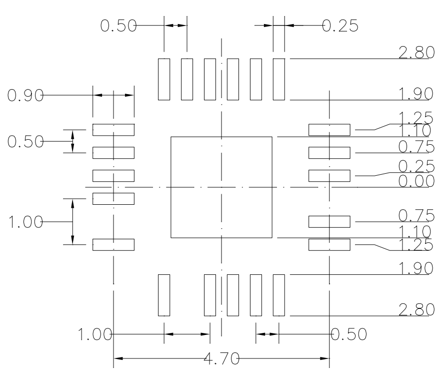
BOTTOM VIEW



SIDE VIEW



SECTION A-A

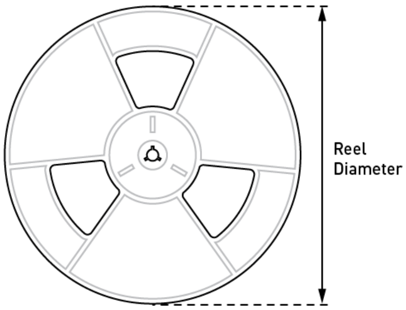


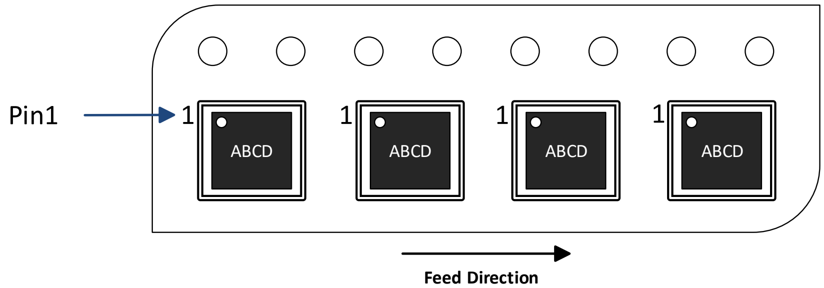
RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION





Part Number	Package Description	Quantity /Reel	Quantity /Tube	Quantity /Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ3446GUE-xxxx-AEC1-Z	QFN-21 (5mmx5mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	4/1/2025	Initial Release	-