



The Future of Analog IC Technology®

MPQ20051

Low Noise, High PSRR, 1A
Linear Regulator
AEC-Q100 Qualified

DESCRIPTION

The MPQ20051 is a low-dropout linear regulator that supplies up to 1A current with a 140mV dropout voltage. The externally-adjustable output voltage has a range of 0.8V to 5V from an input voltage of 2.5V to 5.5V.

An internal PMOS pass element allows for a low 130µA ground current, making the MPQ20051 suitable for battery-powered devices. Other features include low-power shutdown, and short-circuit and thermal protection.

The MPQ20051 is available in 3mm x 3mm 8-pin QFN package.

FEATURES

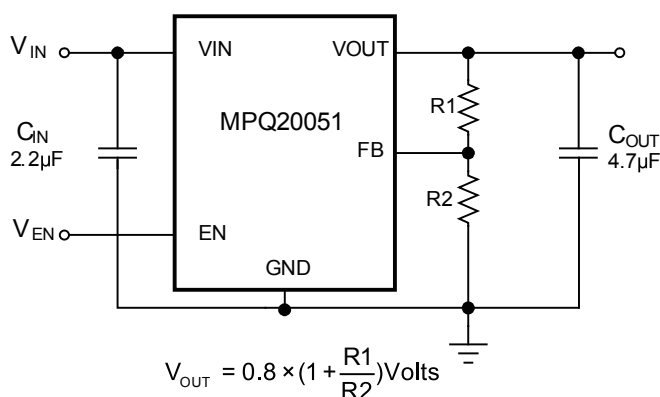
- Guaranteed Industrial/Automotive Temp Range Limits
- Up to 1A Output Current
- Low 140mV Dropout at 1A
- Low 130µA Ground Current
- Output Voltage Available from 0.8V to 5V
- Low Noise: 13µV_{RMS} typical (10Hz to 100kHz)
- 63dB PSRR @1kHz
- Stable with Ceramic Capacitor
- Excellent Load/Line Transient Response
- Current Limiting and Thermal Protection
- Available in 3mm x 3mm 8-pin QFN Package
- Available in AEC-Q100 Qualified Grade 1

APPLICATIONS

- Automotive/Industrial Power System
- Notebook Computers
- Cordless Telephones
- Cellular Phones
- Wireless Communication Equipments

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TYPICAL APPLICATION



ORDERING INFORMATION

| Part Number | Package | Top Marking | MSL Rating |
|------------------|----------------|-------------|------------|
| MPQ20051DQ-AEC1* | QFN-8(3mmx3mm) | See Below | Level1 |
| MPQ20051DQ** | QFN-8(3mmx3mm) | | |

* For Tape & Reel, add suffix -Z (e.g. MPQ20051DQ-AEC1-Z)
 For RoHS compliant packaging, add suffix -LF (e.g. MPQ20051DQ-AEC1-LF-Z).

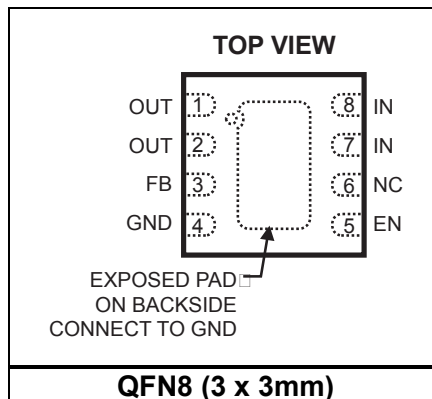
** For Tape & Reel, add suffix -Z (e.g. MPQ20051DQ-Z)
 For RoHS compliant packaging, add suffix -LF (e.g. MPQ20051DQ-LF-Z).

TOP MARKING

ABRY
LLL

ABR: product code
 Y: year code
 LLL: lot number

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

VIN, EN, FB to GND -0.3V to +6V
 OUT to GND.....-0.5V to (VIN + 0.5V)
 Continuous Power Dissipation (TA=25°C) ⁽²⁾
 QFN8 (3x3mm)2.0W
 Junction Temperature..... 150°C
 Storage Temperature Range.....-65°C to 150°C
 Lead Temperature (Soldering, 10sec).....260°C

ESD SUSCEPTIBILITY⁽³⁾

HBM (Human Body Mode)..... 2kV
 CDM (Charged Device Mode) 750V

Recommended Operating Conditions ⁽⁴⁾

Supply Input Voltage..... 2.5V to 5.5V
 Enable Input Voltage 0V to 5.5V
 Operating Junction Temp. (TJ). -40°C to +125°C

Thermal Resistance ⁽⁵⁾ θ_{JA} θ_{JC}
 QFN-8 (3mmx3mm)50 12... °C/W

Notes:

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature TJ (MAX), the junction-to-ambient thermal resistance θ_{JA} , and the ambient temperature TA. The maximum allowable continuous power dissipation at any ambient temperature is calculated by PD (MAX) = (TJ (MAX)-TA)/ θ_{JA} . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) Devices are ESD sensitive. Handling precaution recommended.
- 4) The device is not guaranteed to function outside of its operating conditions.
- 5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

$V_{IN}=V_{OUT}+0.5V$ or $V_{IN}=2.5V$, $EN=V_{IN}$, $T_J=-40^{\circ}C$ to $+125^{\circ}C$ Typical values are at $T_J=25^{\circ}C$, unless otherwise specified

| Parameter | Condition | Min | Typ | Max | Units | |
|---|---|----------------------------------|-------|------|---------------|---------|
| Input Voltage | | 2.5 | | 5.5 | V | |
| Input Under Voltage Lockout | V_{IN} rising | 1.95 | | 2.3 | V | |
| Hysteresis of UVLO | | | 160 | | mV | |
| FB Voltage | $V_{OUT}=0.8V$, $I_{OUT}=1mA$ | $T_J=25^{\circ}C$ | 0.784 | 0.8 | 0.816 | V |
| | | $-40 \leq T_J \leq 125^{\circ}C$ | 0.776 | 0.8 | 0.824 | |
| Output Voltage Accuracy | $I_{OUT}=1mA$, $T_J=25^{\circ}C$ | -2 | | 2 | % | |
| | $I_{OUT}=1mA$, $-40 \leq T_J \leq 125^{\circ}C$ | -3 | | 3 | | |
| Maximum Output Current | Continuous, $V_{IN} \geq 2.5V$, $V_{OUT}=2.5V$ | 1 | | | A | |
| Short-Circuit Current Limit | $V_{OUT}=0$, $V_{IN} \geq 2.5V$ | 1.2 | 1.6 | 2.3 | A | |
| In-Regulation Current Limit | $V_{OUT}=2.5V$, V_{OUT} within 4% of normal output voltage $V_{IN}=5.5V$ | 1.4 | 2.2 | 3.0 | A | |
| Ground Current | $I_{OUT}=0.1mA$, $V_{OUT}=2.5V$ | | 130 | 200 | μA | |
| | $I_{OUT}=1A$, $V_{OUT}=2.5V$ | | 400 | 700 | | |
| Dropout Voltage ⁽⁶⁾ | $I_{OUT}=1A$, $V_{OUT}=2.5V$ | | 140 | 280 | mV | |
| | $I_{OUT}=750mA$, $V_{OUT}=2.5V$ | | 105 | 210 | | |
| | $I_{OUT}=500mA$, $V_{OUT}=2.5V$ | | 70 | 140 | | |
| Line Regulation ⁽⁷⁾ | $V_{OUT}=2.5V$, V_{IN} from $V_{OUT}+0.5V$ to $5.5V$, $I_{OUT}=100mA$, | -0.15 | | 0.15 | %/V | |
| Load Regulation ⁽⁸⁾ | I_{OUT} from 100mA to 1A, $V_{OUT}=2.5V$ | -0.5 | | 0.5 | % | |
| Output Voltage Noise ⁽⁹⁾ | $I_{OUT}=100mA$, f ranges from 10Hz to 100kHz | $V_{OUT}=1.1V$ | | 13 | μV_{RMS} | |
| | | $V_{OUT}=3.3V$ | | 35 | | |
| | | $V_{OUT}=5V$ | | 55 | | |
| PSRR ⁽⁹⁾ | $V_{IN} = 2.5V$, $V_{OUT} = 1.1V$, $I_{OUT} = 1A$ | $f=100Hz$ | | 65 | dB | |
| | | $f=1kHz$ | | 63 | | |
| | | $f=10kHz$ | | 63 | | |
| | | $f=1MHz$ | | 33 | | |
| Shutdown Supply Current | $V_{IN}=+5.5V$ | $T_J=25^{\circ}C$ | | 0.1 | 0.3 | μA |
| | | $-40 \leq T_J \leq 125^{\circ}C$ | | | | |
| EN Pin Current , Enabled | $V_{IN}=V_{EN}=+5.5V$ | | 0.1 | 0.3 | μA | |
| Feedback Pin Current | $V_{IN}=+5.5V$, $V_{FB}=6V$ | | 0.1 | 0.3 | μA | |
| Startup Time | $V_{OUT(NOM)}=2.5V$, $C_{OUT}=4.7\mu F$, $V_{OUT}=10\%$ to $90\%V_{OUT(NOM)}$ | | 45 | 100 | μs | |
| EN PIN Threshold | EN Logic High | 1.5 | | | V | |
| | EN Logic Low | | | 0.4 | | |
| Thermal Shutdown Temperature ⁽⁹⁾ | Typical thermal hysteresis $=20^{\circ}C$ | | 150 | | $^{\circ}C$ | |

Notes:

6) Dropout Voltage is defined as the input to output differential when the output voltage drops 100mV below its nominal value.

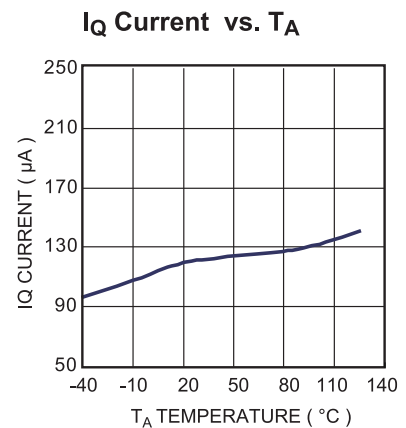
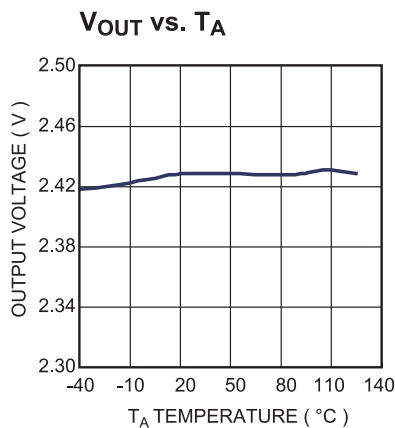
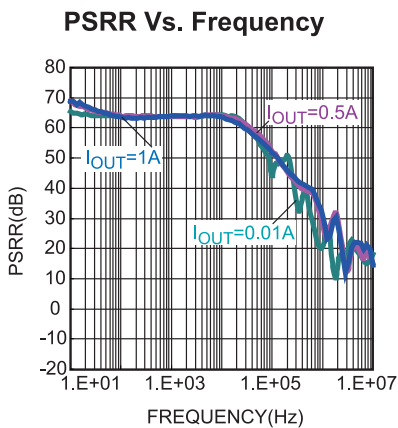
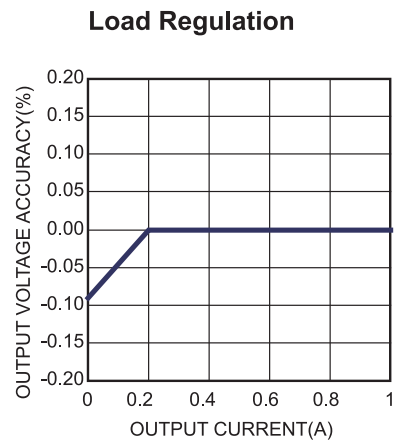
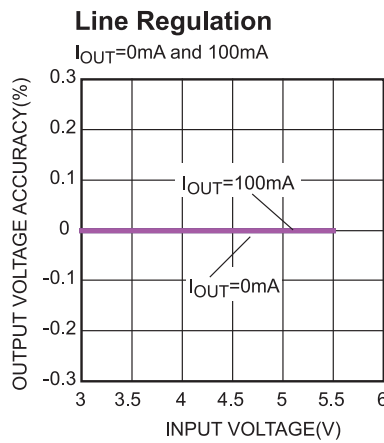
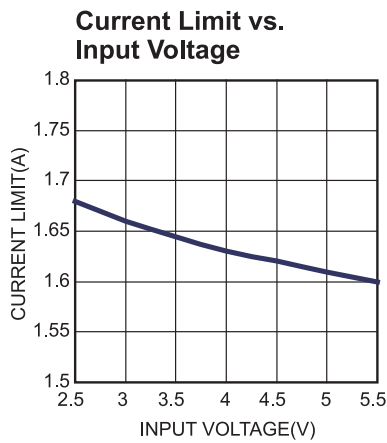
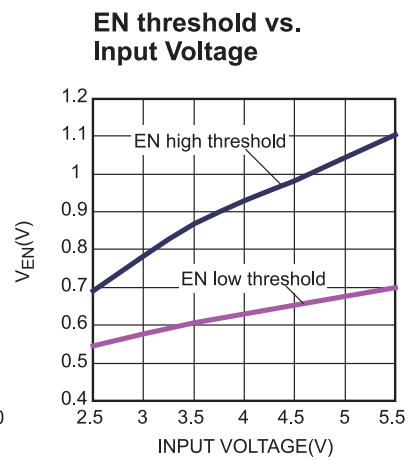
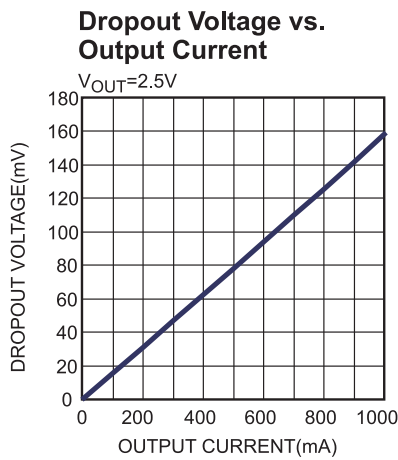
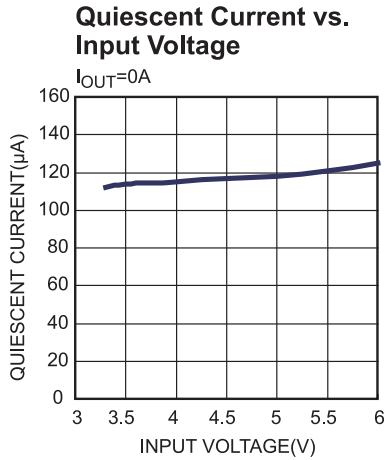
$$7) \text{ Line Regulation} = \frac{V_{OUT[V_{IN(MAX)}]} - V_{OUT[V_{IN(MIN)}]}}{[V_{IN(MAX)} - V_{IN(MIN)}] \times V_{OUT(NOM)}} \times (\% / V)$$

$$8) \text{ Load Regulation} = \frac{V_{OUT[I_{OUT(MAX)}]} - V_{OUT[I_{OUT(MIN)}]}}{V_{OUT(NOM)}} \times (\%)$$

9) Design guarantee, not production test.

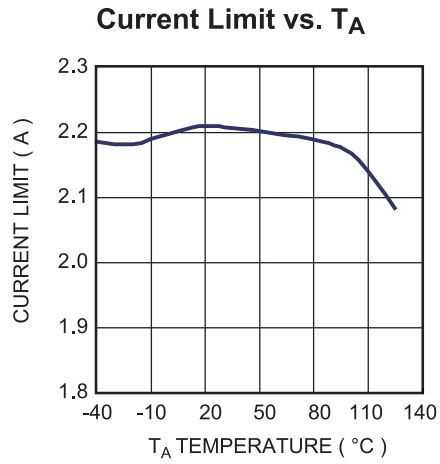
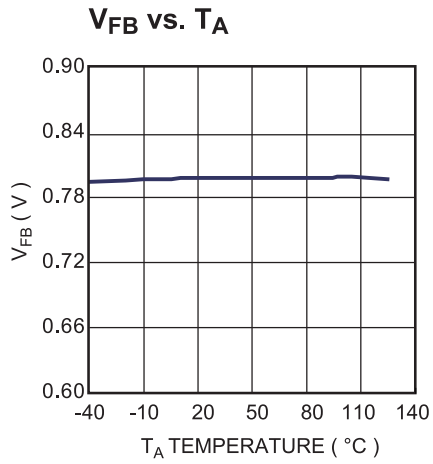
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 2.5V$, $V_{OUT} = 1.1V$, $C_{IN} = 2.2\mu F$, $C_{OUT} = 4.7\mu F$, $T_A = 25^\circ C$, unless otherwise noted.



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 2.5V$, $V_{OUT} = 1.1V$, $C_{IN}=2.2\mu F$, $C_{OUT}=4.7\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

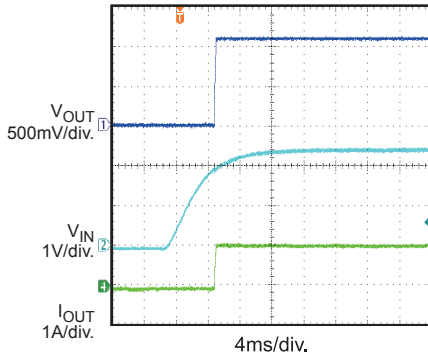


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 2.5V$, $V_{OUT} = 1.1V$, $C_{IN} = 2.2\mu F$, $C_{OUT} = 4.7\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

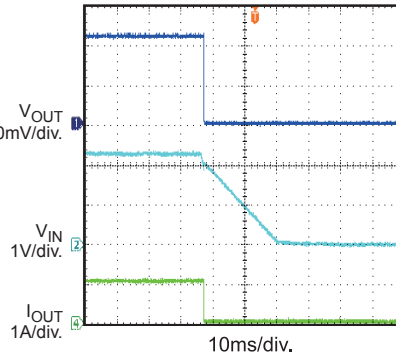
Input Power Start Up

$V_{IN} = 2.5V$, $V_{OUT} = 1.1V$, $I_{OUT} = 1A$,
with Resistor Load



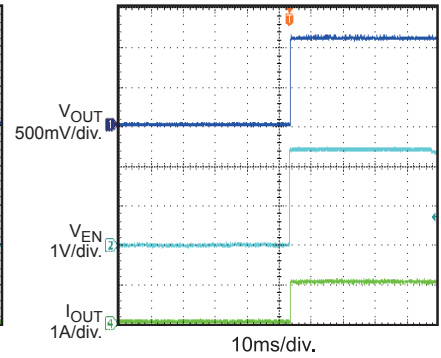
Input Power Shutdown

$V_{IN} = 2.5V$, $V_{OUT} = 1.1V$, $I_{OUT} = 1A$,
with Resistor Load



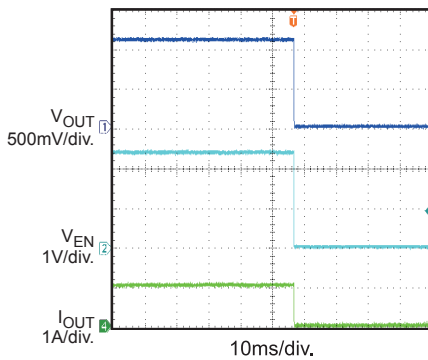
EN Start Up

$V_{EN} = 2.5V$, $V_{OUT} = 1.1V$, $I_{OUT} = 1A$,
with Resistor Load



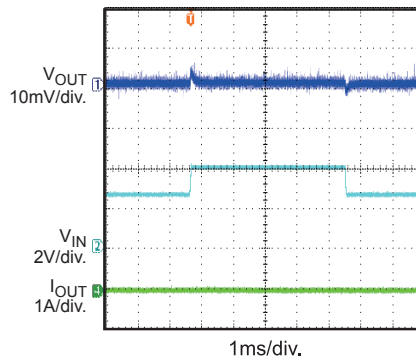
EN Shutdown

$V_{EN} = 2.5V$, $V_{OUT} = 1.1V$, $I_{OUT} = 1A$,
with Resistor Load

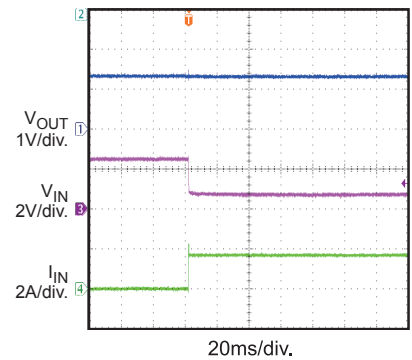


Line Transient

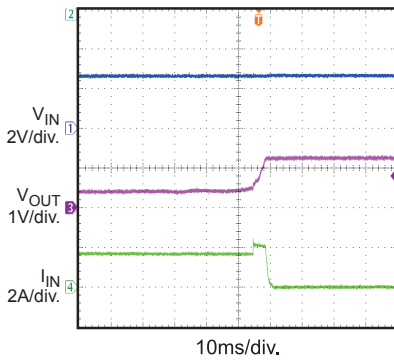
$V_{IN} = 2.5V$ to $4V$, $V_{OUT} = 1.1V$,
 $I_{OUT} = 10mA$, with Resistor Load



Short Output

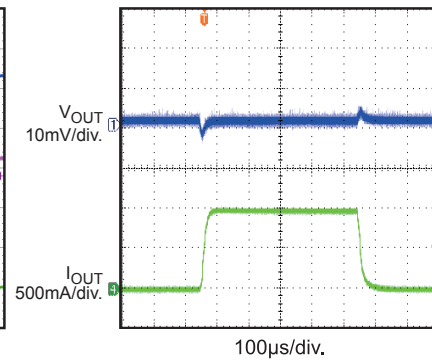


Short Output Recovery



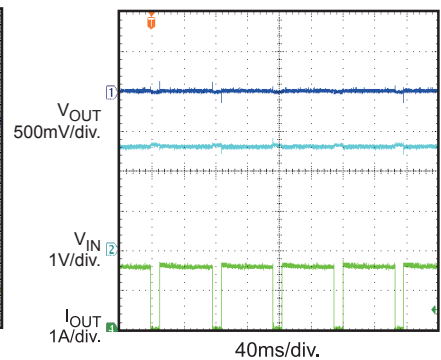
Over Current Protection Steady State

$V_{IN} = 2.5V$, $V_{OUT} = 1.1V$



Over Current Protection Steady State

$V_{IN} = 2.5V$, $V_{OUT} = 1.1V$



PIN FUNCTIONS

| Pin # | Name | Pin Function |
|-------|--------------------|--|
| 1, 2 | VOUT | Regulator output. Bypass with a standard 4.7 μ F ceramic capacitor to GND. Connect all the pins together externally. |
| 3 | FB | Feedback Input. Connect FB to the center point of the external resistor divider. The feedback threshold voltage is 0.8V. |
| 4 | GND Exposed pad | Ground. Connect exposed pad to GND plane for optimal thermal performance. |
| 5 | EN | Regulator Enable Control Input. Drive EN above 1.5V to turn on the MPQ20051. Drive EN below 0.4V to turn it off. Do not float the EN pin. |
| 6 | NC | No Connection. Leave this NC pin open. |
| 7, 8 | VIN | Regulator Input. Supply voltage ranges from 2.5V to 5.5V. Bypass with 2.2 μ F capacitor. These pins must be externally connected for proper operation even if they are internally connected. |

FUNCTIONAL BLOCK DIAGRAM

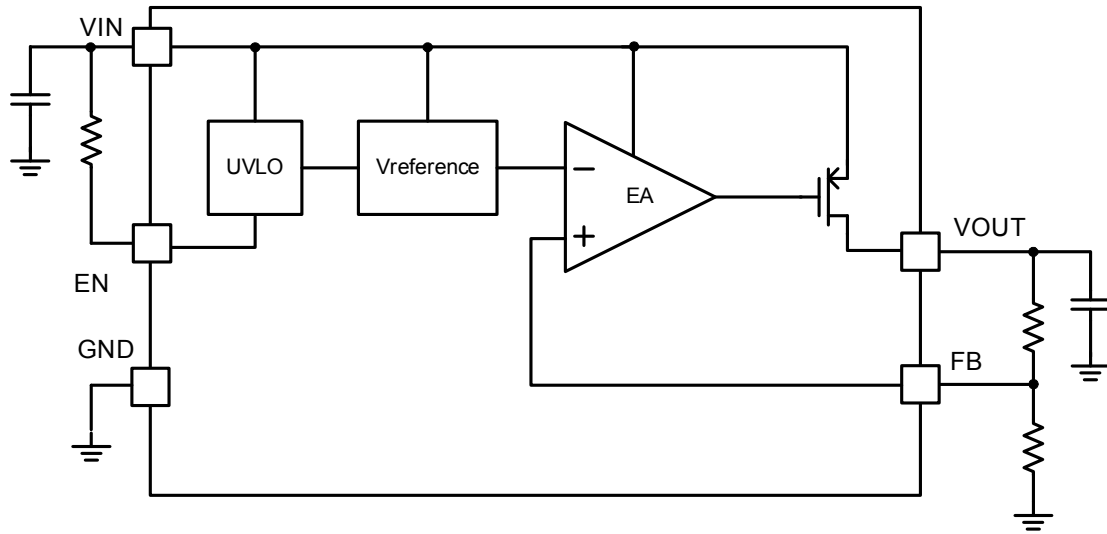


Figure 1—Functional Block Diagram

OPERATION

The MPQ20051 is a low-dropout linear regulator that can supply up to 1A current, which makes it suitable for very low voltage, low quiescent, low noise, and high PSRR applications such as wireless LAN transceivers, notebook computers, smartphones, and other low-power electronics.

The MPQ20051 uses an internal PMOS as the pass element and includes both thermal shutdown and an internal current-limiting circuit.

Dropout Voltage

Dropout voltage is the minimum input to output differential voltage required for the regulator to maintain an output voltage within 100mV of its nominal value. Because the PMOS pass element behaves as a low-value resistor, the dropout voltage of MPQ20051 is only 140mV.

Shutdown

The MPQ20051 can be switched ON or OFF by a logic input at the EN pin: Logic high turns the regulator on and logic low turns it off. Tie the EN pin to VIN if the application does not require the shutdown feature. Do not float the EN pin.

Current Limit

The MPQ20051 includes a current limit structure that monitors and controls the PMOS gate voltage to limit the guaranteed maximum output current to 1.6A.

Thermal Protection

Thermal protection turns off the PMOS when the junction temperature exceeds 150°C, allowing the IC to cool. When the IC's junction temperature drops by 20°C, the PMOS will turn on again. Thermal protection limits total power dissipation in the MPQ20051. For reliable operation, limit the junction temperature to a maximum of 125°C.

Load-Transient Considerations

The output response of the load-transient consists of a transient response and DC shift—the MPQ20051's excellent load regulation effectively limits the DC shift. The output voltage transient depends on the output capacitor's value and ESR. Increasing the capacitance and decreasing the ESR will improve the transient response.

APPLICATION INFORMATION

Setting the Output Voltage

The MPQ20051 has an externally-set output voltage with a range of 0.8V to 5V given a 2.5V to 5.5V input. Set the output voltage using a resistive voltage divider from the output voltage to the FB pin. The result of the voltage divider at the FB pin is:

$$V_{FB} = V_{OUT} \frac{R2}{R1 + R2}$$

Where V_{FB} is the feedback threshold voltage ($V_{FB} = 0.8V$), and V_{OUT} is the output voltage. Thus the output voltage is:

$$V_{OUT} = 0.8 \times \frac{R1 + R2}{R2}$$

$R2$ can go as high as 100k Ω , but typical applications use 10k Ω . After selecting $R2$, $R1$ is determined by:

$$R1 = R2 \times \left(\frac{V_{OUT} - V_{FB}}{V_{FB}} \right)$$

For example, for a 1.1V output voltage, $R2$ is 10k Ω , and $R1$ is 3.75k Ω . You can select a standard 3.75k Ω ($\pm 1\%$) resistor for $R1$.

Power Dissipation

The power dissipation for any package depends on the thermal resistance of the case and circuit board, the temperature differential between the junction and ambient air, and the rate of air flow. The power dissipation across the device can be represented by the equation:

$$P = (V_{IN} - V_{OUT}) \times I_{OUT}$$

The allowable power dissipation can be calculated using the following equation:

$$P_{(MAX)} = (T_{JUNCTION} - T_{AMBIENT}) / \theta_{JA}$$

Where $(T_{JUNCTION} - T_{AMBIENT})$ is the temperature differential between the junction and the surrounding environment, θ_{JA} is the thermal resistance from the junction to the ambient environment. Connecting the exposed GND pad to a large ground pad or plane helps to channel away heat.

Output Capacitor Selection

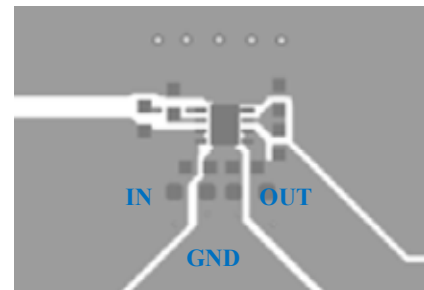
The MPQ20051 is specifically designed to work with a standard ceramic output capacitor to save space and improve performance. Use a 4.7 μF ceramic capacitor for most applications. Larger

output capacitors will improve load transient response and reduce noise at the cost of increased size.

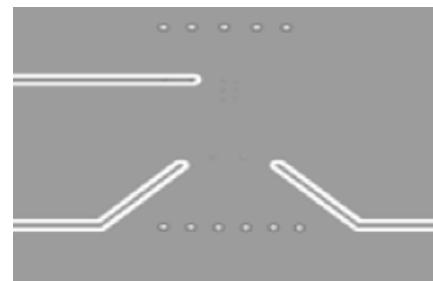
PCB Layout Guide

PCB layout is very important to achieve good regulation, ripple rejection, transient response and thermal performance. It is highly recommended to duplicate EVB layout for optimum performance. If change is necessary, please follow these guidelines and take Figure 2 for reference.

- 1) Input and output bypass ceramic capacitors are suggested to be put close to the IN Pin and OUT Pin respectively.
- 2) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
- 3) Connect IN, OUT and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.



Top Layer

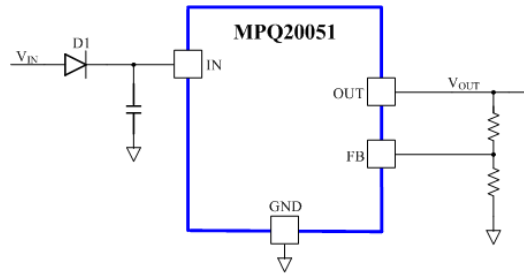


Bottom Layer

Figure 2: PCB Layout

External Reverse Voltage Protection

In some situations, e.g. a backup battery is connected as MPQ20051 load, the output voltage may be held up while the input is either pulled to ground to some intermediated voltage or is floating. Thus, the output voltage is higher than input voltage. Since MPQ20051 internal PMOS pass element has a body diode, a current will conduct from the output to input and is not internally limited. It's possible that the IC will be damaged by this unlimited reverse current. To avoid this, it's recommended to place an external diode at input like below.



Adding A Input Diode

Design Example

The detailed application schematic is shown in Figure 3. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more device applications, please refer to the related Evaluation Board Datasheets.

TYPICAL APPLICATION CIRCUITS

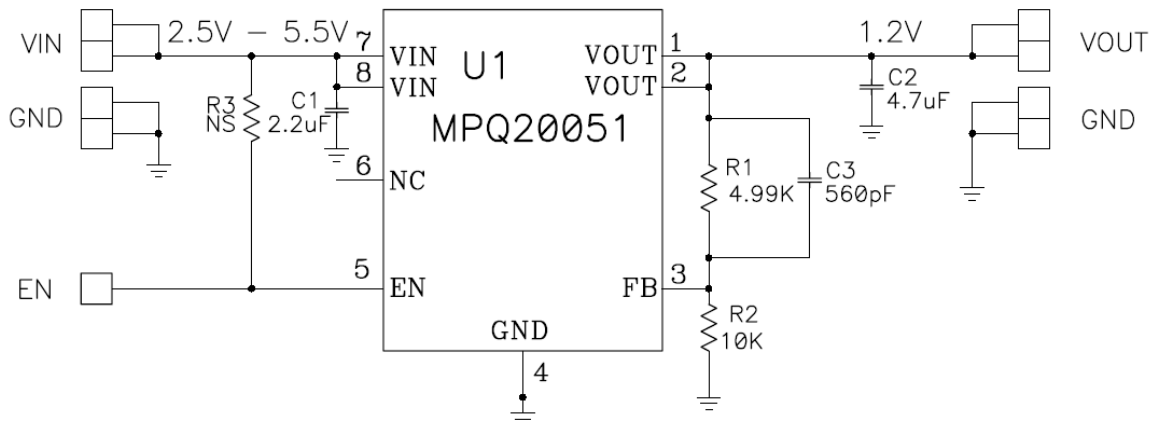
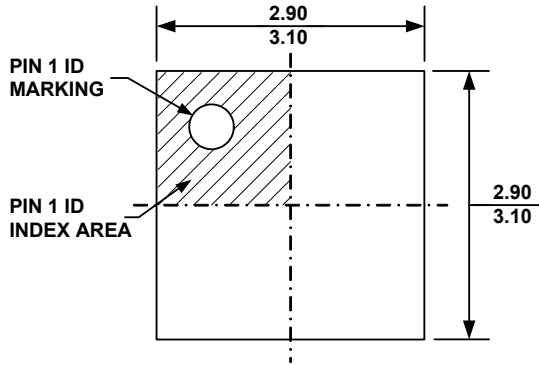


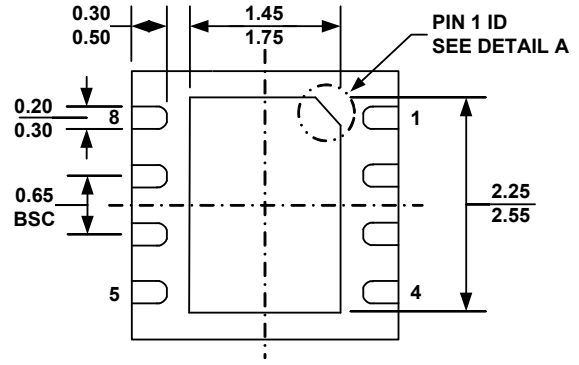
Figure 3: 1.2V Output Typical Application Schematic

PACKAGE INFORMATION

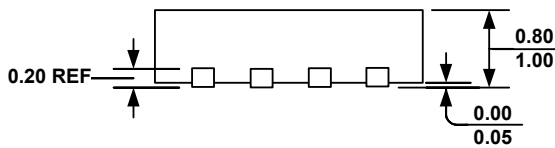
QFN-8 (3mm×3mm)



TOP VIEW



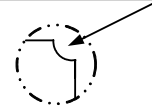
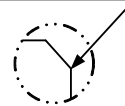
BOTTOM VIEW



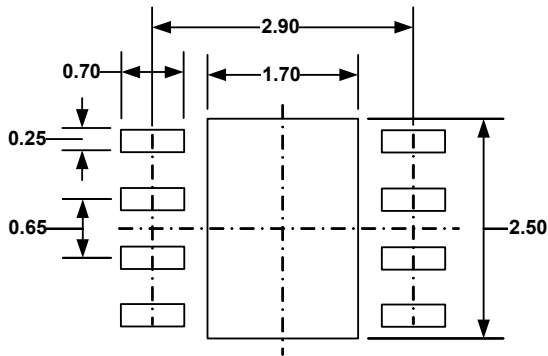
SIDE VIEW

PIN 1 ID OPTION A
0.30x45° TYP.

PIN 1 ID OPTION B
R0.20 TYP.



DETAIL A

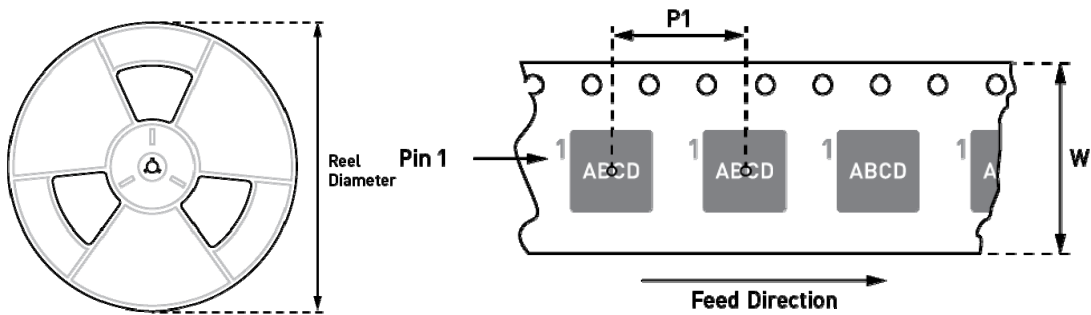


RECOMMENDED LAND PATTERN

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
- 4) JEDEC REFERENCE IS MO-229, VARIATION VEEC-2.
- 5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



| Part Number | Package Description | Quantity/Reel | Quantity/Tube | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch |
|-------------|---------------------|---------------|---------------|---------------|--------------------|--------------------|
| MPQ20051DQ | QFN 3x3 | 5000 | N/A | 13 in. | 12mm | 8mm |

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