MP9942

High Efficiency 2A, 36V, 410kHz Synchronous Step-Down Converter with Power Good

The Future of Analog IC Technology®

DESCRIPTION

The MP9942 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs. It offers a very compact solution to achieve a 2A continuous output current with excellent load and line regulation over a wide input supply range. The MP9942 has synchronous mode operation for higher efficiency over the output current load range.

Current-mode operation provides fast transient response and eases loop stabilization.

Full protection features include over-current protection and thermal shutdown.

The MP9942 requires a minimal number of readily-available standard external components, and is available in a space-saving 8-pin TSOT23 package.

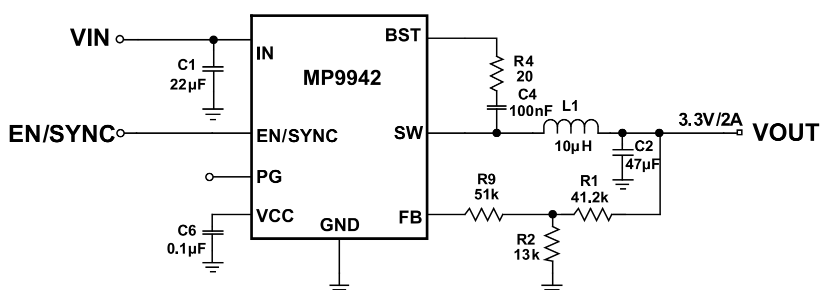
FEATURES

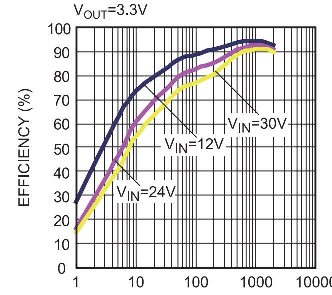
- Wide 4V to 36V Continuous Operating Input Range
- 90mΩ/55mΩ Low RDS(ON) Internal Power MOSFETs
- High-Efficiency Synchronous Mode Operation
- 410kHz Switching Frequency
- Synchronizes from 200kHz to 2.2MHz External Clock
- High Duty Cycle for Automotive Cold-crank
- Internal Power-Save Mode
- Internal Soft-Start
- Power Good Indicator
- Over-Current Protection with Hiccup
- Thermal Shutdown
- Output Adjustable from 0.8V
- Available in an 8-pin TSOT-23 package

APPLICATIONS

- Automotive
- Industrial Control System
- Distributed Power Systems

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MP9942GJ	TSOT23-8	*See Below*

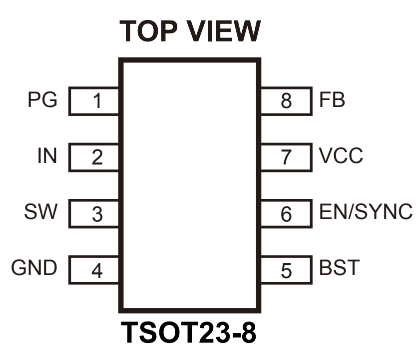
* For Tape & Reel, add suffix –Z (e.g. MP9942GJ–Z);

TOP MARKING

|ALLY

ALL: product code of MP9942GJ;
Y: year code;

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ....-0.3V to 40V
V_{SW} ....-0.3V to 41V
V_{BS} .... V_{SW}+6V
All Other Pins .... -0.3V to 6V (2)
Continuous Power Dissipation (T_A = +25°C) (3)
TSOT23-8 .... 1.25W
Junction Temperature ....150°C
Lead Temperature ....260°C
Storage Temperature................. -65°C to 150°C

Recommended Operating Conditions (4)

Continuous Supply Voltage V_{IN} ....4V to 36V
Output Voltage V_{OUT} ....0.8V to V_{IN}*D_{MAX}
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (5)

	θ_{JA}	θ_{JC}	
TSOT23-8	100	55	°C/W

Notes:

1) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) About the details of EN pin's ABS MAX rating, please refer to page 14, Enable/SYNC control section.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current (Shutdown)	I_{SHDN}	V_{EN} = 0V			8	μA
Supply Current (Quiescent)	I_Q	V_{EN} = 2V, V_{FB} = 1V		0.5	0.7	mA
HS Switch-ON Resistance	R_{ON_HS}	V_{BST-SW}=5V		90	155	mΩ
LS Switch-ON Resistance	R_{ON_LS}	V_{CC} =5V		55	105	mΩ
Switch Leakage	I_{LKG_SW}	V_{EN} = 0V, V_{SW} =12V			1	μA
Current Limit	I_{LIMIT}	Under 40% Duty Cycle	3	4.2	5.5	A
Oscillator Frequency	f_{SW}	V_{FB}=750mV	320	410	500	kHz
Fold-Back Frequency	f_{FB}	V_{FB}<400mV	70	100	130	kHz
Maximum Duty Cycle	D_{MAX}	V_{FB}=750mV, 410kHz	92	95		%
Minimum ON Time(6)	t_{ON_MIN}			70		ns
Sync Frequency Range	f_{SYNC}		0.2		2.4	MHz
Feedback Voltage	V_{FB}		780	792	804	mV
Feedback Current	I_{FB}	V_{FB}=820mV		10	100	nA
EN Rising Threshold	V_{EN_RISING}		1.15	1.4	1.65	V
EN Falling Threshold	$V_{EN\_FALLING}$		1.05	1.25	1.45	V
EN Threshold Hysteresis	V_{EN_HYS}			150		mV
EN Input Current	I_{EN}	V_{EN}=2V		4	6	μA
		V_{EN}=0		0	0.2	μA
VIN Under-Voltage Lockout Threshold-Rising	$INUV_{RISING}$		3.3	3.5	3.7	V
VIN Under-Voltage Lockout Threshold-Falling	$INUV_{FALLING}$		3.1	3.3	3.5	V
VIN Under-Voltage Lockout Threshold-Hysteresis	$INUV_{HYS}$			200		mV
VCC Regulator	V_{CC}	I_{CC}=0mA	4.6	4.9	5.2	V
VCC Load Regulation		I_{CC}=5mA		1.5	4	%
Soft-Start Period	t_{SS}	V_{OUT} from 10% to 90%	0.55	1.45	2.45	ms
Thermal Shutdown (6)	T_{SD}		150	170		°C
Thermal Hysteresis (6)	T_{SD_HYS}			30		°C
PG Rising Threshold	PG_{Vth_RISING}	as percentage of V_{FB}	86.5	90	93.5	%
PG Falling Threshold	$PG_{Vth\_FALLING}$	as percentage of V_{FB}	80.5	84	87.5	%

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
PG Threshold Hysteresis	PG_{Vth_HYS}	as percentage of V_{FB}		6		%
PG Rising Delay	PG_{Td_RISING}		40	90	160	μs
PG Falling Delay	$PG_{Td\_FALLING}$		30	55	95	μs
PG Sink Current Capability	V_{PG}	Sink 4mA		0.1	0.3	V
PG Leakage Current	I_{LKG_PG}			10	100	nA

Notes:

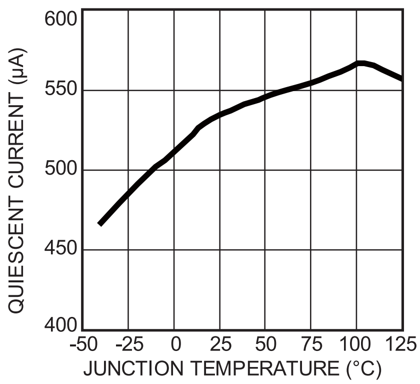
6) Derived from bench characterization. Not tested in production

PIN FUNCTIONS

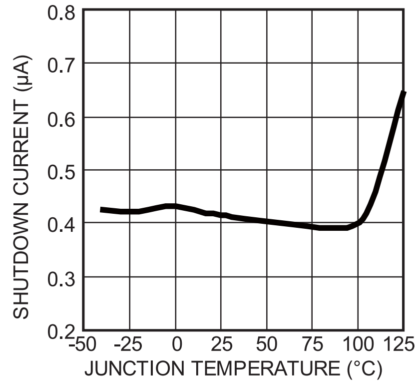
Package Pin #	Name	Description
1	PG	Power Good. The output of this pin is an open drain and goes high if the output voltage exceeds 90% of the nominal voltage.
2	IN	Supply Voltage. The MP9942 operates from a 4V to 36V input rail. Requires C1 to decouple the input rail. Connect using a wide PCB trace.
3	SW	Switch Output. Connect with a wide PCB trace.
4	GND	System Ground. This pin is the reference ground of the regulated output voltage, and PCB layout requires special care. For best results, connect to GND with copper traces and vias.
5	BST	Bootstrap. Requires a capacitor connected between SW and BST pins to form a floating supply across the high-side switch driver. A 20Ω resistor placed between SW and BST cap is strongly recommended to reduce SW spike voltage.
6	EN/SYNC	Enable/Synchronize. EN/SYNC high to enable the MP9942. Apply an external clock to the EN/SYNC pin to change the switching frequency.
7	VCC	Bias Supply. Decouple with 0.1µF-to-0.22µF capacitor. Select a capacitor that does not exceed 0.22µF
8	FB	Feedback. Connect to the tap of an external resistor divider from the output to GND, to set the output voltage. The frequency fold-back comparator lowers the oscillator frequency when the FB voltage is below 660mV to prevent current limit runaway during a short-circuit fault condition.

TYPICAL CHARACTERISTICS

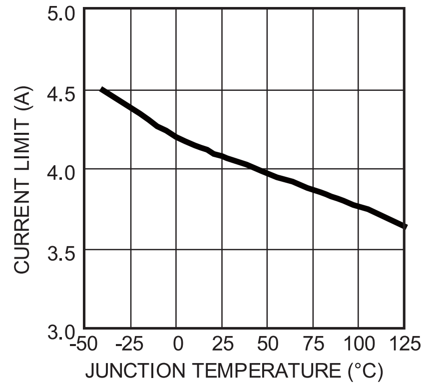
Quiescent Current vs. Junction Temperature
V_{IN}=12V



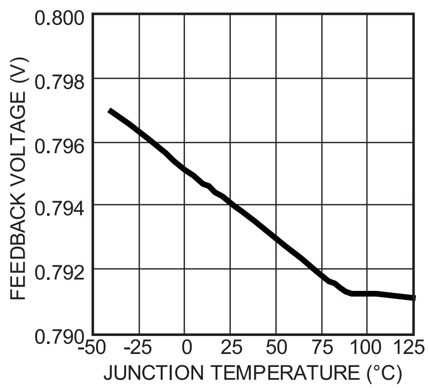
Shutdown Current vs. Junction Temperature
V_{IN}=12V



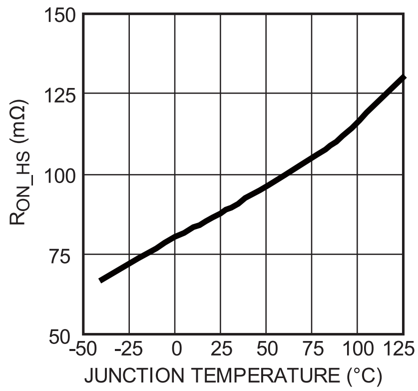
Current Limit vs. Junction Temperature
Duty Cycle=40%



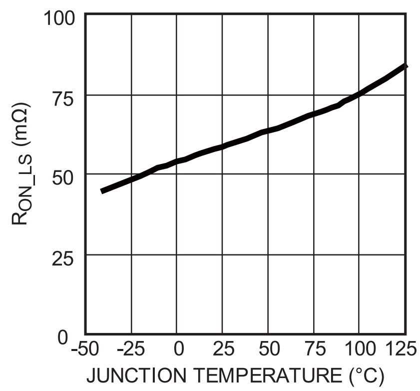
Feedback Voltage vs. Junction Temperature
V_{IN}=12V



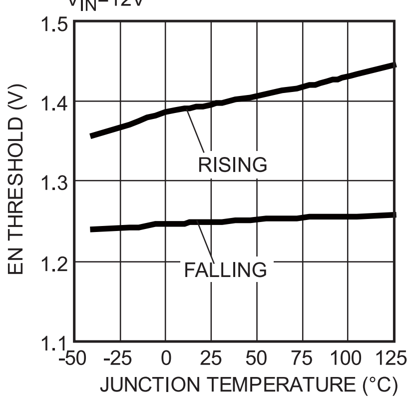
R_{ON-HS} vs. Junction Temperature
V_{IN}=12V, BST-SW=5V



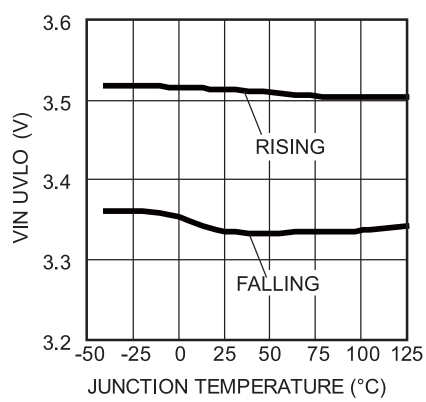
R_{ON-LS} vs. Junction Temperature
V_{IN}=12V, V_{CC}=5V



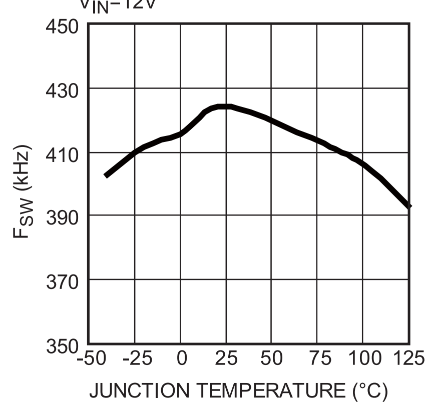
EN Threshold vs. Junction Temperature
V_{IN}=12V



V_{IN} UVLO vs. Junction Temperature

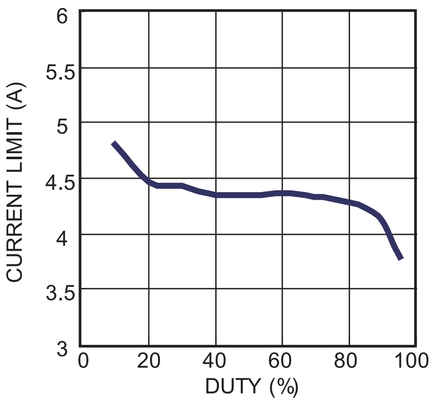


F_{SW} vs. Junction Temperature
V_{IN}=12V



TYPICAL CHARACTERISTICS *(continued)*

Current Limit vs. Duty
T_J=+25°C

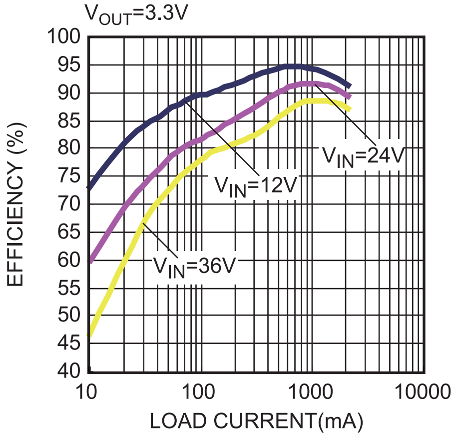


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH, R_{BST}=20Ω, T_A = +25°C, unless otherwise noted.

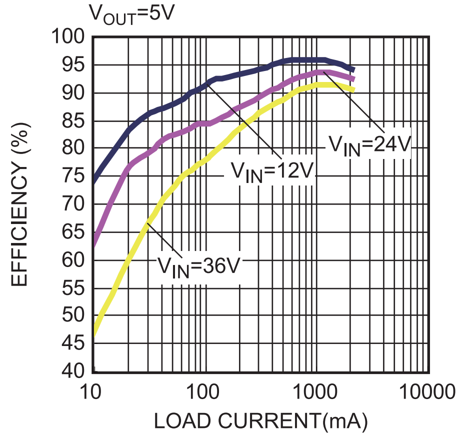
Efficiency vs. Load Current

V_{OUT}=3.3V

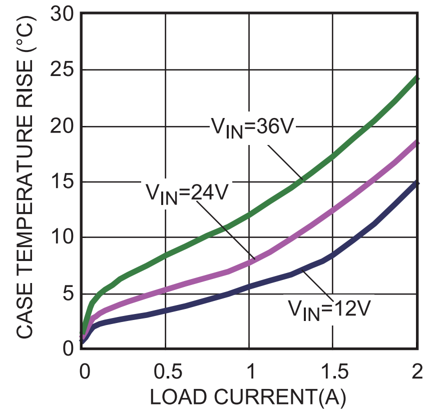


Efficiency vs. Load Current

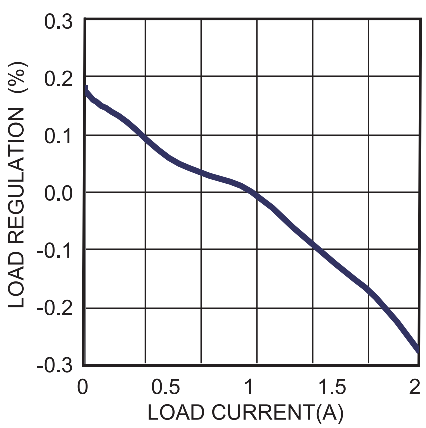
V_{OUT}=5V



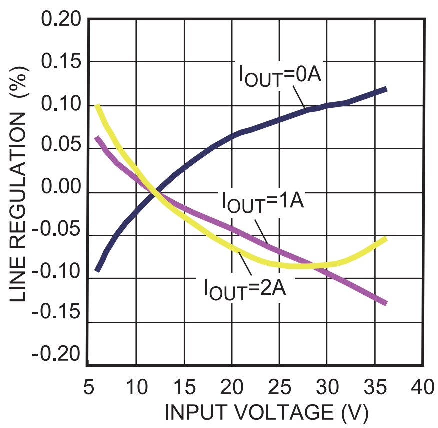
Thermal Rise



Load Regulation



Line Regulation

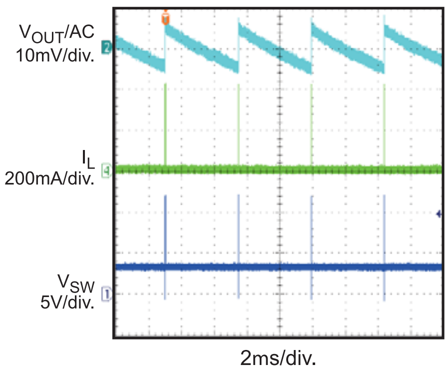


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH, R_{BST}=20Ω, T_A = +25°C, unless otherwise noted.

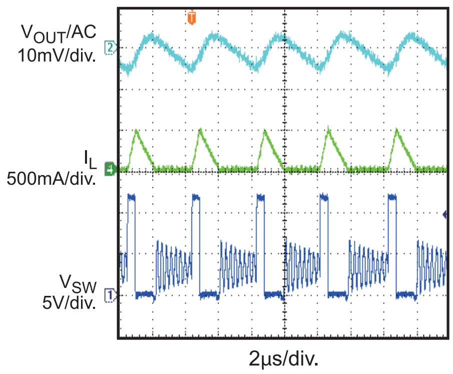
Steady State

I_{OUT}=0A



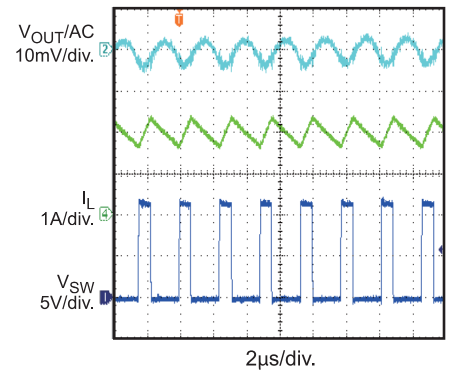
Steady State

I_{OUT} = 0.1A



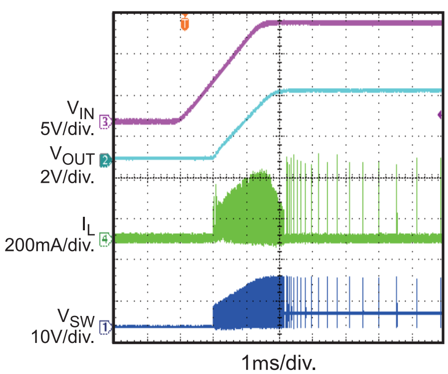
Steady State

I_{OUT}=2A



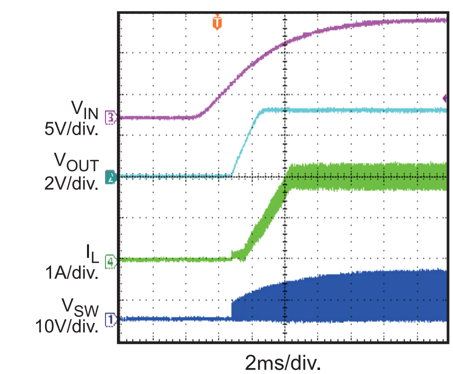
Startup through V_{IN}

I_{OUT}=0A



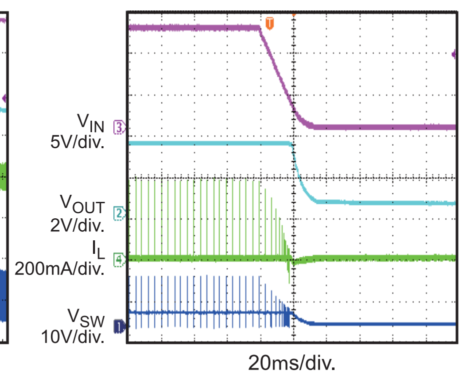
Startup through V_{IN}

I_{OUT}=2A



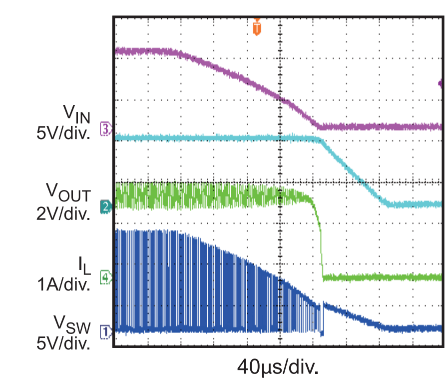
Shutdown through V_{IN}

I_{OUT}=0A



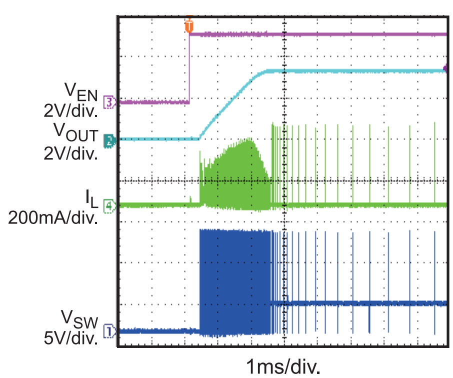
Shutdown through V_{IN}

I_{OUT}=2A



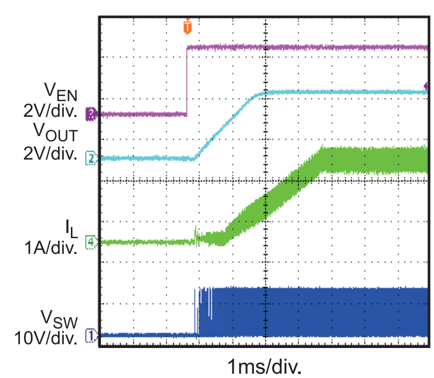
Startup Through EN

I_{OUT}=0A



Startup Through EN

I_{OUT}=2A

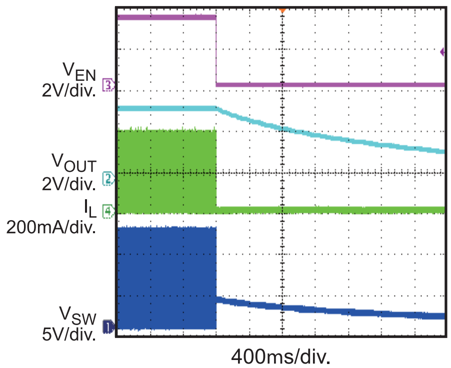


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH, R_{BST}=20Ω, T_A = +25°C, unless otherwise noted.

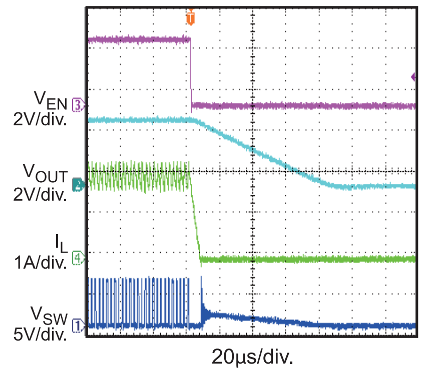
Shutdown Through EN

I_{OUT}=0A



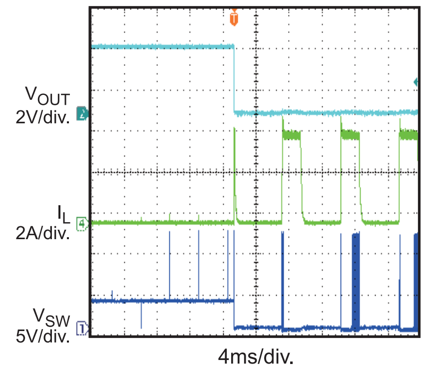
Shutdown Through EN

I_{OUT}=2A



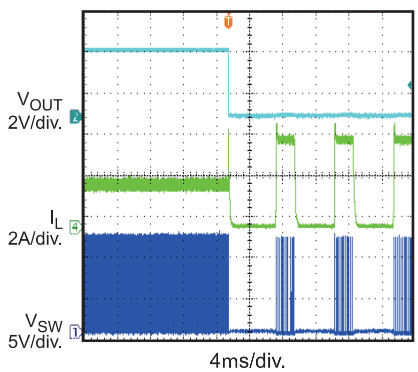
SCP Entry

I_{OUT}=0A to Short Circuit

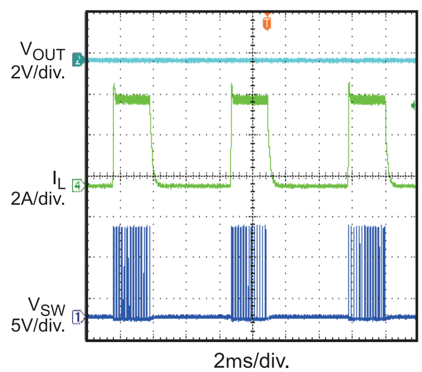


SCP Entry

I_{OUT}=2A to Short Circuit

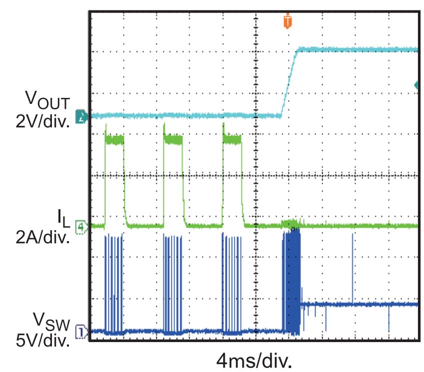


SCP Steady State



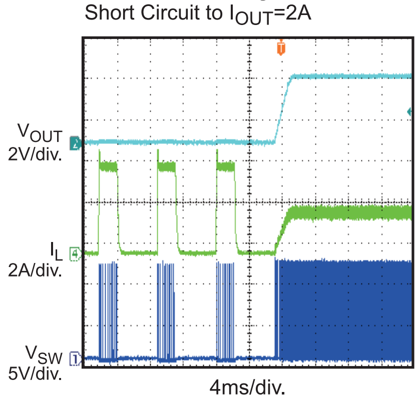
SCP Recovery

Short Circuit to I_{OUT}=0A



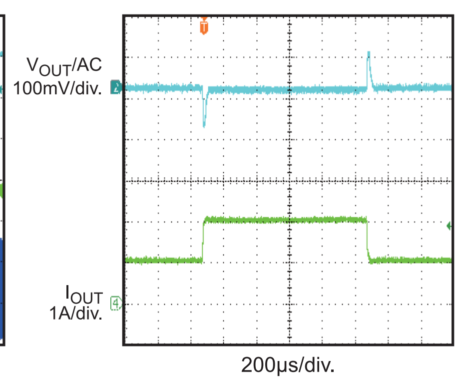
SCP Recovery

Short Circuit to I_{OUT}=2A



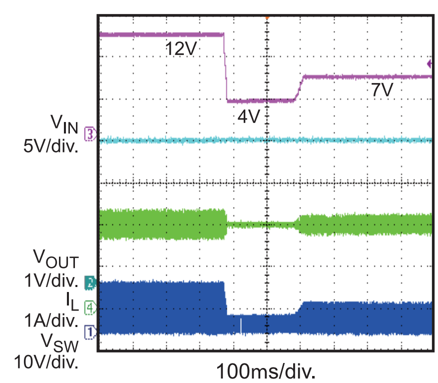
Load Transient

I_{OUT}=1A<->2A, 1.6A/µs



Cold-Crank

V_{OUT}=3.3V, I_{OUT}=2A

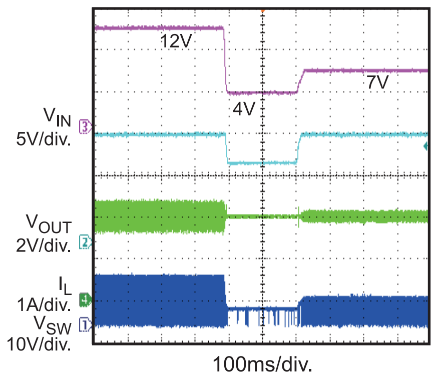


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH, R_{BST}=20Ω, T_A = +25°C, unless otherwise noted.

Cold-Crank

V_{OUT}=5V, I_{OUT}=2A



FUNCTIONAL BLOCK DIAGRAM

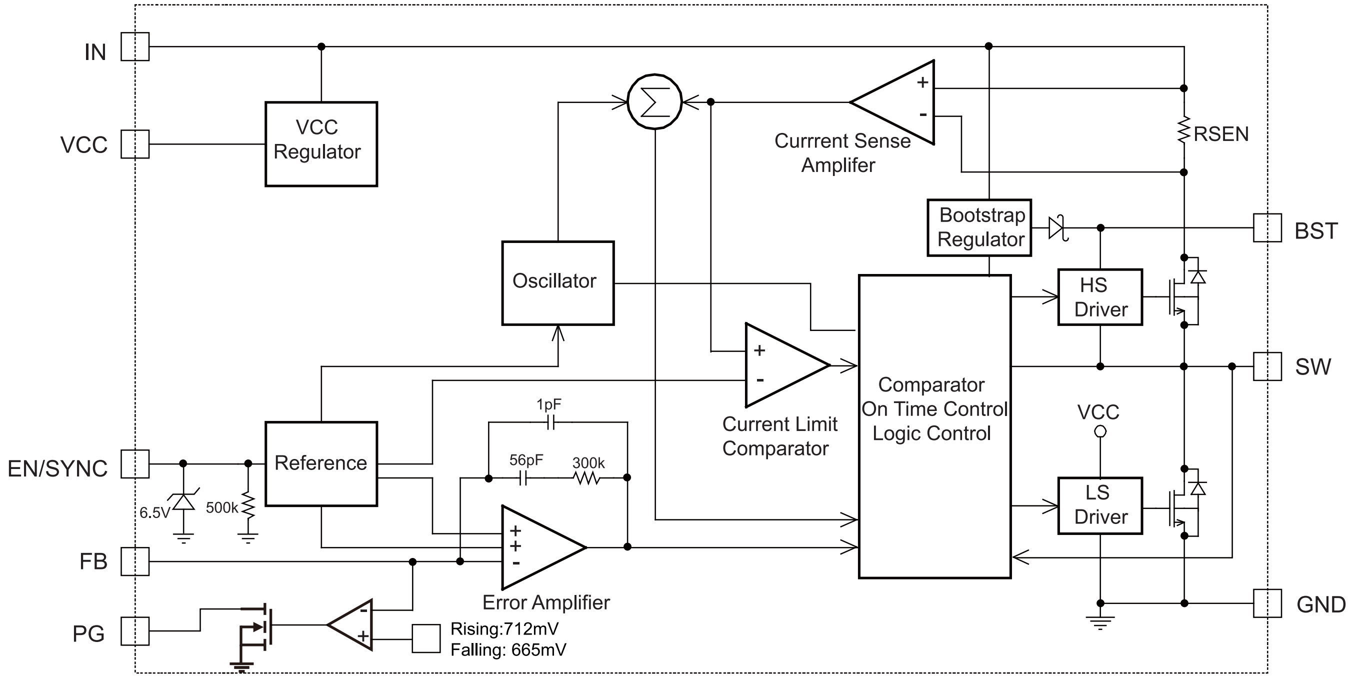


Figure 1: Functional Block Diagram

OPERATION

The MP9942 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs. It offers a very compact solution to achieve 2A continuous output current with excellent load and line regulation over a wide input supply range.

When MP9942 operates in a fixed-frequency, peak-current–control mode to regulate the output voltage, an internal clock initiates a PWM cycle. The integrated high-side power MOSFET turns on and remains on until its current reaches the value set by the COMP voltage. When the power switch is off, it remains off until the next clock cycle starts. If the current in the power MOSFET does not reach the current value set by COMP within 95% of one PWM period, the power MOSFET will be forced to turn off.

Internal Regulator

The 5V internal regulator power most of the internal circuitries. This regulator is supplied by the V_{IN} input and operates in the full V_{IN} range: When V_{IN} exceeds 5.0V, the output of the regulator is in full regulation; when V_{IN} falls below 5.0V, the output of the regulator decreases following the VIN. A 0.1uF decoupling ceramic capacitor is needed at the pin.

Error Amplifier

The error amplifier compares the FB pin voltage against the internal 0.792V reference (REF) and outputs a COMP voltage—this COMP voltage controls the power MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies the control loop design.

Power Save Mode for Light Load Condition

The MP9942 has AAM (Advanced Asynchronous Modulation) power-save mode for light load. The AAM threshold is fixed internally. Under the heavy load condition, the V_{COMP} is higher than V_{AAM}. When the clock goes high, the high-side power MOSFET turns on and remains on until $V_{ILsense}$ reaches the value set by the COMP voltage. The internal clock resets every time when V_{COMP} is higher than V_{AAM}.

Under the light load condition, the value of V_{COMP} is low. When V_{COMP} is less than V_{AAM} and V_{FB} is less than V_{REF}, V_{COMP} ramps up until it exceeds V_{AAM}. During this time, the internal clock is blocked, thus the MP9942 skips some pulses for PFM (Pulse Frequency Modulation) mode and achieves the light load power save.

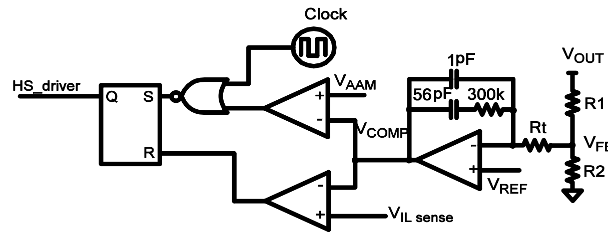


Figure 2: Simplified AAM Control Logic

Enable/SYNC control

EN/SYNC is a digital control pin that turns the regulator on and off: Drive EN/SYNC high to turn on the regulator, drive it low to turn it off. An internal 500kΩ resistor from EN/SYNC to GND allows EN/SYNC to be floated to shut down the chip.

The EN/SYNC pin is clamped internally using a 6.5V series Zener diode, as shown in Figure 3. Connect the EN/SYNC pin through a pullup resistor to any voltage connected to the V_{IN} pin—the pullup resistor limits the EN/SYNC input current to less than 100µA.

For example, with 12V connected to V_{IN}, $R_{PULLUP} \geq (12V – 6.5V) \div 100µA = 55kΩ$.

Connecting the EN/SYNC pin directly to a voltage source without any pullup resistor requires limiting voltage amplitude to ≤6V to prevent damage to the Zener diode.

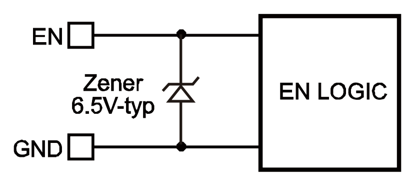


Figure 3: 6.5V-type Zener Diode

Connect an external clock with a range of 200kHz to 2.2MHz to synchronize the internal clock rising edge to the external clock rising edge. The pulse width of external clock signal should be less than 2µs.

Under-Voltage Lockout

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP9942 UVLO comparator monitors the output voltage of the internal regulator, VCC. The UVLO rising threshold is about 3.5V while its falling threshold is 3.3V.

Internal Soft-Start

The soft-start prevents the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) that ramps up from 0V to 1.2V. When SS is lower than REF, SS overrides REF so the error amplifier uses SS as the reference. When SS exceeds REF, the error amplifier uses REF as the reference. The SS time is internally set to 1.45ms.

Over-Current Protection and Hiccup

The MP9942 has cycle-by-cycle over current limit when the inductor current peak value exceeds the set current limit threshold. If the output voltage starts to drop until FB is below the Under-Voltage (UV) threshold—typically 84% below the reference—the MP9942 enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-shorted to ground. The average short-circuit current is greatly reduced to alleviate the thermal issue and to protect the regulator. The MP9942 exits the hiccup mode once the over-current condition is removed.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 170°C, it shuts down the whole chip. When the temperature drops below its lower threshold (typically 140°C) the chip is enabled again.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection, with a rising threshold of 2.2V and hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by V_{IN} through D1, M1, C4, L1 and C2 (Figure). If (V_{IN}-V_{SW}) exceeds 5V, U1 regulates M1 to maintain a 5V BST voltage across C4. A 20Ω resistor placed between SW and BST cap is strongly recommended to reduce SW spike voltage.

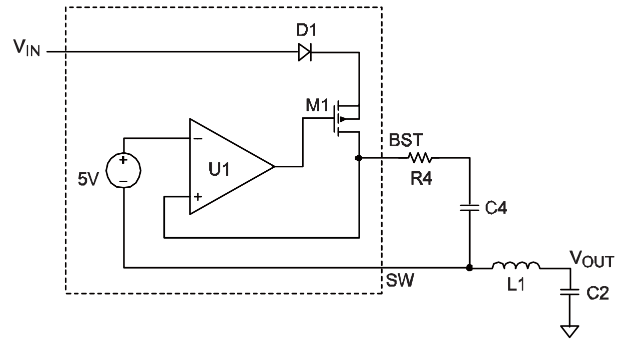


Figure 4: Internal Bootstrap Charging Circuit

Startup and Shutdown

If both V_{IN} and EN exceed their appropriate thresholds, the chip starts: The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries.

Three events can shut down the chip: EN low, V_{IN} low, and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

Power Good

The MP9942 has power good (PG) output. The PG pin is the open drain of a MOSFET. It should be connected to VCC or some other voltage source through a resistor (e.g. 100kΩ). In the presence of an input voltage, the MOSFET turns on so that the PG pin is pulled to low before SS is ready. After V_{FB} reaches 90%×REF, the PG pin is pulled high after a delay, typically 90µs. When V_{FB} drops to 84%×REF, the PG pin is pulled low. Also, PG is pulled low if thermal shutdown or EN is pulled low.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage (see Typical Application on page 1). Choose R1 around 41.2kΩ. R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.792V} - 1}$$

The T-type network—as shown in Figure —is highly recommended when V_{OUT} is low.

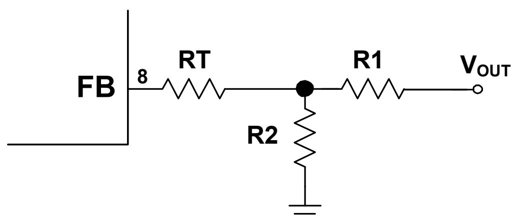


Figure 5: T-Type Network

RT+R1 is used to set the loop bandwidth. Basically, higher RT+R1, lower bandwidth. To ensure the loop stability, it is strongly recommended to limit the bandwidth lower than 40kHz based on the 410kHz default fsw. Table 1 lists the recommended T-type resistors value for common output voltages.

Table 1: Resistor Selection for Common Output Voltages (7)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	RT (kΩ)
3.3	41.2 (1%)	13 (1%)	51 (1%)
5	41.2 (1%)	7.68 (1%)	51 (1%)

Notes:

7) The feedback resistors in Table 1 are optimized for 410kHz switching frequency. The detailed schematic is shown on TYPICAL APPLICATION CIRCUITS.

Selecting the Inductor

Use a1μH-to-10μH inductor with a DC current rating of at least 25% percent higher than the maximum load current for most applications. For highest efficiency, an inductor with small DC resistance is recommended. For most designs, the inductance value can be derived from the following equation.

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Use a larger inductor for improved efficiency under light-load conditions—below 100mA.

VIN UVLO Setting

The MP9942 has internal fix under voltage lock out (UVLO) threshold: rising threshold is 3.5V while falling threshold is about 3.3V. For the application needs higher UVLO point, external resistor divider between EN/SYNC and IN as shown in Figure 6 can be used to get higher equivalent UVLO threshold.

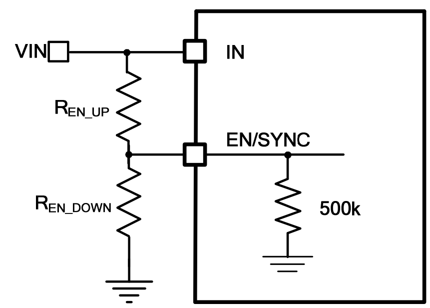


Figure 6: Adjustable UVLO using EN divider

The UVLO threshold can be computed from below two equations:

$$INUV_{RISING} = (1 + \frac{R_{EN\_UP}}{500k // R_{EN\_DOWN}}) \times V_{EN\_RISING}$$

$$INUV_{FALLING} = (1 + \frac{R_{EN\_UP}}{500k // R_{EN\_DOWN}}) \times V_{EN\_FALLING}$$

Where V_{EN_RISING}=1.4V, $V_{EN\_FALLING}$=1.25V.

When choose R_{EN_UP}, make sure it is big enough to limit the current flows into EN/SYNC pin lower than 100uA.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore requires a capacitor is to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Use ceramic capacitors with X5R or X7R dielectrics for best results because of their low ESR and small temperature coefficients.

For most application, a 22µF ceramic capacitor is sufficient to maintain the DC input voltage. And it is strongly recommended to use another lower value capacitor (e.g. 0.1µF) with small package size (0603) to absorb high frequency switching noise. Make sure place the small size capacitor as close to IN and GND pins as possible (see PCB LAYOUT section).

Since C1 absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worse case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, add a small, high quality ceramic capacitor (e.g. 1µF) placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where L_1 is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and the capacitance causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^{\,2} \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP9942 can be optimized for a wide range of capacitance and ESR values.

BST Resistor and External BST Diode

A 20Ω resistor in series with BST capacitor is recommended to reduce the SW spike voltage. Higher resistance is better for SW spike reduction, but will compromise the efficiency on the other hand.

An external BST diode can enhance the efficiency of the regulator when the duty cycle is high (>65%) or VIN is below 5V, and also help to avoid BST voltage insufficient at light load PFM operation. A power supply between 3.3V and 5V can be used to power the external bootstrap diode and VCC or VOUT is the good choice of this power supply in the circuit as shown in Figure 7.

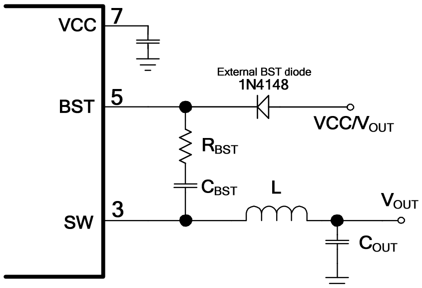


Figure 7: Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is 1N4148, and the BST capacitor value is 0.1μF to 1μF.

PCB Layout (8)

PCB layout, especially the input capacitor and VCC capacitor placement, is very important to achieve stable operation. For the best results, follow these guidelines:

1) Place the ceramics input capacitor as close to IN and GND pins as possible, especially the small package size (0603) input bypass capacitor. Keep the connection of input capacitor and IN pin as short and wide as possible.

2) Place the VCC capacitor to VCC pin and GND pin as close as possible. Make the trace length of VCC pin-VCC capacitor anode-VCC capacitor cathode-chip GND pin as short as possible.

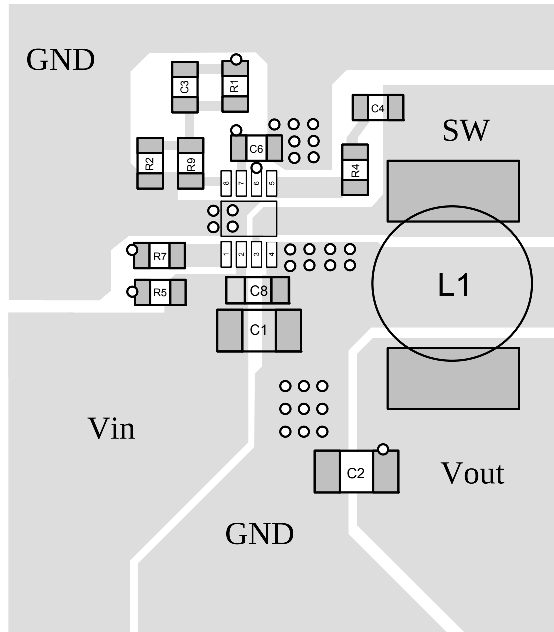
3) Use large ground plane directly connect to GND pin. Add vias near the GND pin if bottom layer is ground plane.

4) Route SW, BST away from sensitive analog areas such as FB.

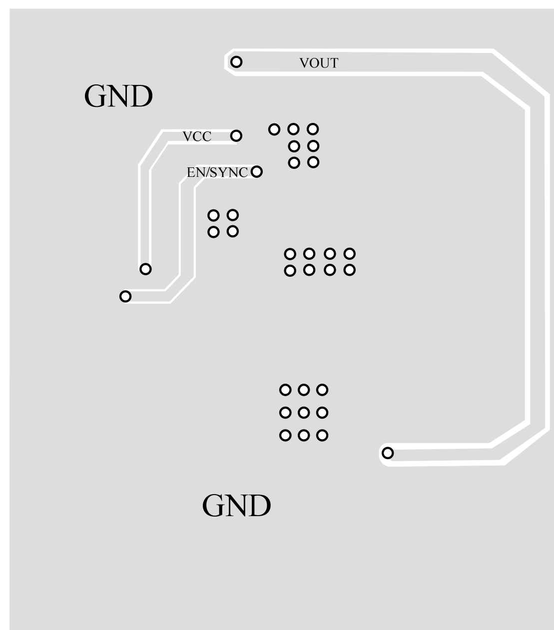
5) Place the T-type feedback resistor close to chip to ensure the trace which connects to FB pin as the short as possible.

Notes:

8) The recommended layout is based on the typical application circuit in Page 20.



Top Layer



Bottom Layer

Figure 8: Recommended PCB Layout

Design Example

Below is a design example following the application guidelines for the specifications:

Table 2—Design Example

V_{IN}	12V
V_{OUT}	3.3V
I_O	2A

The detailed application schematic is shown in Figure 9. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more device applications, please refer to the related Evaluation Board Datasheets.

TYPICAL APPLICATION CIRCUITS

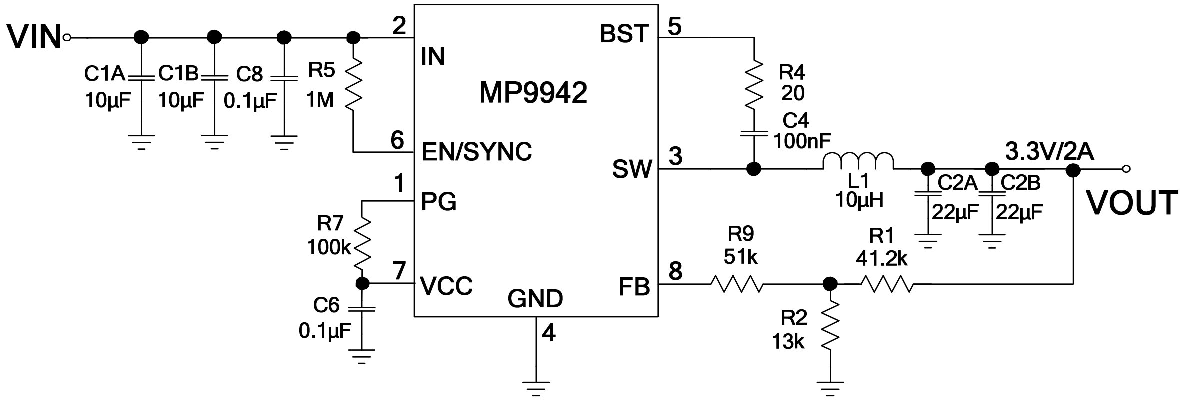
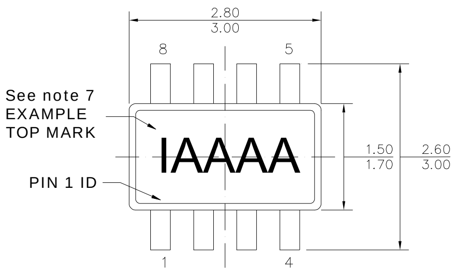


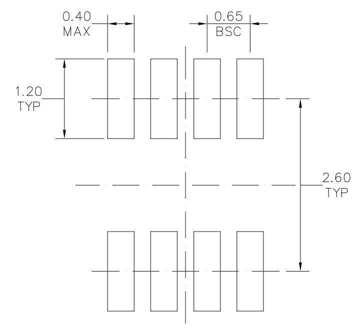
Figure 9: 12V_{IN}, 3.3V/2A Output

PACKAGE INFORMATION

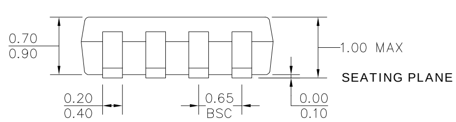
TSOT23-8



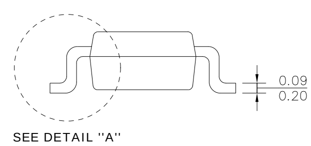
TOP VIEW



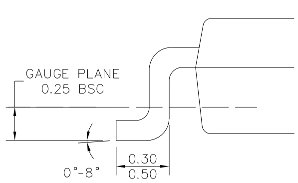
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL ''A''

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-193, VARIATION BA.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)