



The Future of Analog IC Technology®

MP8903

Low Dropout 150mA Linear Regulator

DESCRIPTION

The MP8903 is a 150mA low-dropout linear regulator that can operate from 2.7V to 6.5V input. It regulates the output with 2% accuracy and comes with preset 2.5V, 2.85V or 3.3V output. An external resistor divider may be used to adjust the output voltage from 1.25V to 5V.

The MP8903 has thermal protection to guard against harsh operating conditions, and is available in small QFN8 (2x2mm) and 5-pin TSOT23 packages.

FEATURES

- 2.7V to 6.5V Input Voltage Range
- Fixed Output Voltage Options of 2.5V, 2.85V or 3.3V
- Adjustable Output Voltage from 1.25V to 5V using an External Resistor Divider
- Low 100mV Dropout at 100mA Output
- 2% Accurate Output Voltage
- Stable With Low-ESR Output Capacitors
- Thermal Protection
- Available in Tiny QFN8 (2x2mm) and TSOT23-5 Packages

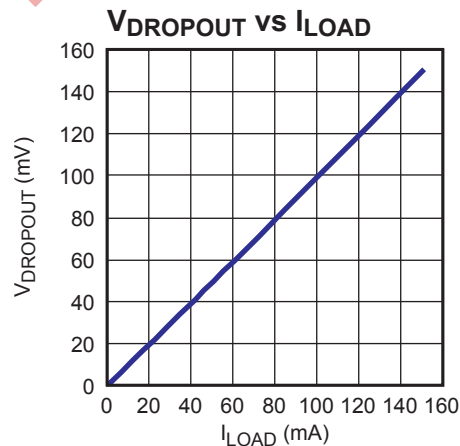
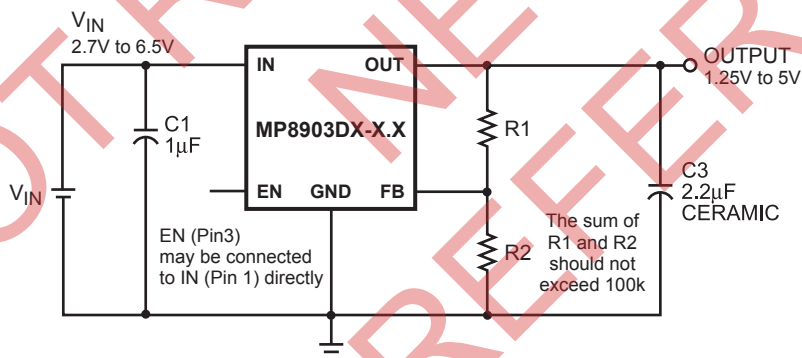
APPLICATIONS

- 802.11 PC Cards
- Mobile Handset PLL Power
- Audio Codec Power

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TYPICAL APPLICATION

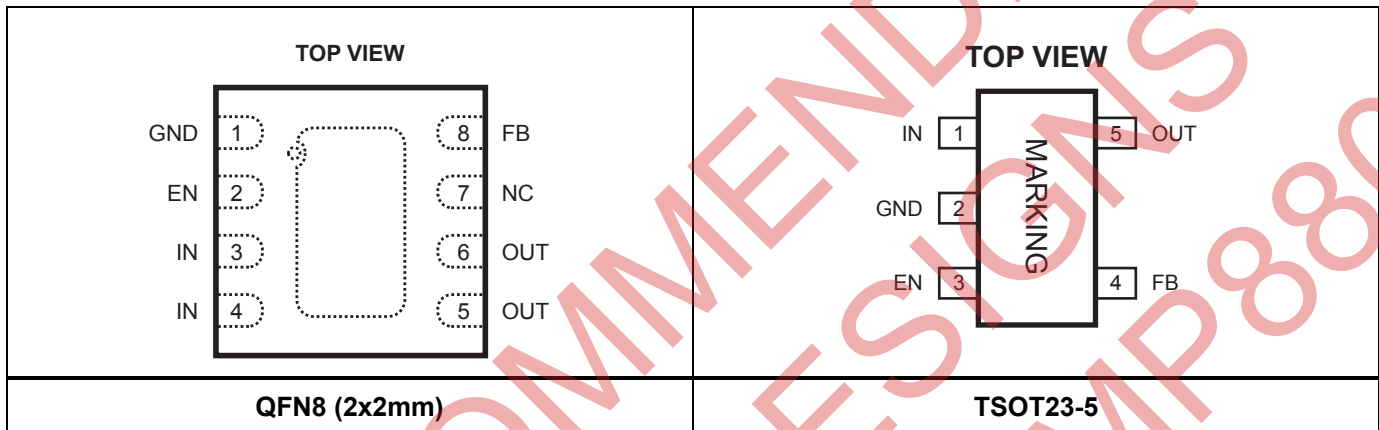


ORDERING INFORMATION

Part Number	Package	Top Marking	Free Air Temperature (T _A)
MP8903DG-2.5*	QFN8 (2x2mm)	R4	-40°C to +85°C
MP8903DG-2.85		R5	
MP8903DG-3.3		R6	
MP8903DJ-2.5	TSOT23-5	R4	
MP8903DJ-2.85		R5	
MP8903DJ-3.3		R6	

* For Tape & Reel, add suffix -Z (e.g. MP8903DG-2.85-Z);
 For RoHS Compliant Packaging, add suffix -LF (e.g. MP8903DG-2.85-LF-Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

IN Supply Voltage	-0.3V to +7.0V
FB Voltage	-0.3V to V _{OUT} + 0.3V
All Other Pins	-0.3V to +6V
Continuous Power Dissipation (T _A = +25°C) ⁽²⁾	
TSOT23-5	0.57W
QFN8 (2x2mm)	1.6W
Junction Temperature	150°C
Lead Temperature	260°C
Storage Temperature	-65°C to +150°C

Recommended Operating Conditions ⁽³⁾

Input Voltage	2.7V to 6.5V
Output Voltage	1.25V to 5V
Load Current	150mA Maximum
Operating Temperature	-40°C to +85°C
Maximum Junction Temp. (T _J)	+125°C

Thermal Resistance ⁽⁴⁾	θ _{JA}	θ _{JC}
TSOT23-5	220	110
QFN8 (2x2mm)	80	16

Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- Measured on JESD51-7 4-layer board.

ELECTRICAL CHARACTERISTICS
 $V_{IN} = 5V$, $T_A = +25^{\circ}C$, unless otherwise noted.

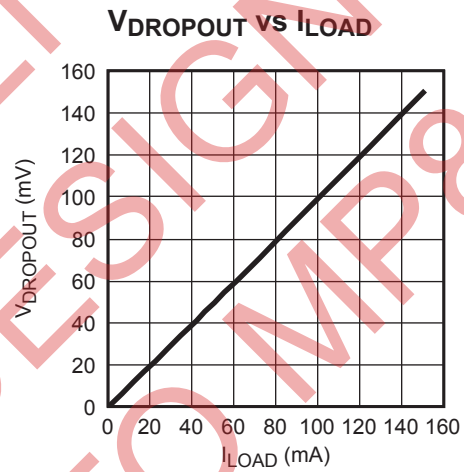
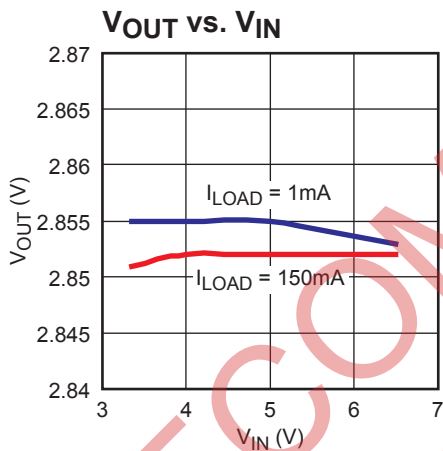
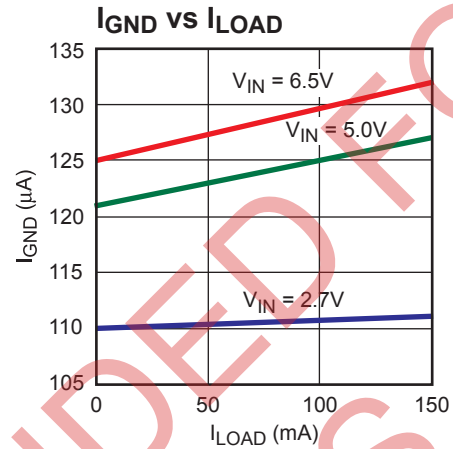
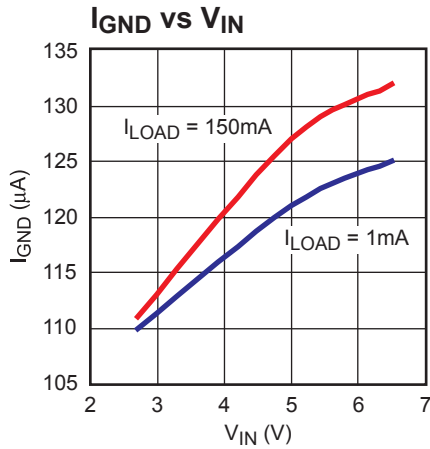
Parameter	Symbol	Condition	Min	Typ	Max	Units
Operating Voltage		$I_{OUT} = 1mA$	2.7		6.5	V
Output Voltage Accuracy		$I_{OUT} = 1mA$, $V_{OUT} = 1.5V$ to $5V$		± 1.0	± 2.0	%
Shutdown Current		$V_{EN} = 0V$, $V_{IN} = 5V$		0.1	1	μA
FB Regulation Voltage			1.197	1.222	1.246	V
		$-40^{\circ}C \leq T_A \leq +85^{\circ}C$	1.194	1.222	1.249	
Dropout Voltage ⁽⁶⁾		$I_{OUT} = 150mA$	$V_{OUT} = 3V$	150		mV
			$V_{OUT} = 4V$	125		
Line Regulation		$I_{OUT} = 1mA$, $V_{IN} = (V_{OUT} + 0.5V)$ to $6.5V$ ⁽⁷⁾		0.005	0.08	%/V
Load Regulation		$I_{OUT} = 1mA$ to $150mA$, $V_{IN} = V_{OUT} + 0.5V$ ⁽⁷⁾		0.001	0.02	%/mA
PSRR		$V_{IN} > V_{OUT} + 0.5V$, $C3 = 2.2\mu F$, $V_{IN(AC)} = 100mV$, $f = 1kHz$ ⁽⁵⁾		50		dB
		$V_{IN} > V_{OUT} + 0.5V$, $C3 = 2.2\mu F$, $V_{IN(AC)} = 100mV$, $f = 1MHz$ ⁽⁵⁾		20		dB
EN Input High Voltage			1.5			V
EN Input Low Voltage					0.4	V
EN Input Bias Current		$V_{EN} = 0V$		0.01	1	μA
Thermal Protection ⁽⁵⁾				155		$^{\circ}C$
Thermal Protection Hysteresis ⁽⁵⁾				30		$^{\circ}C$

Notes:

5) Parameter is guaranteed by design, not production tested.

6) Dropout Voltage is defined as the input to output differential when the output voltage drops 1% below its normal value.

 7) $V_{IN} = 2.7V$ for $V_{OUT} = 1.25V$ to $2.2V$

TYPICAL PERFORMANCE CHARACTERISTICS
 $V_{IN} = 4.5V$, $V_{OUT} = 2.85V$, $C1 = 1\mu F$, $C2 = 0.1\mu F$, $C3 = 2.2\mu F$, $T_A = +25^\circ C$ unless otherwise noted.


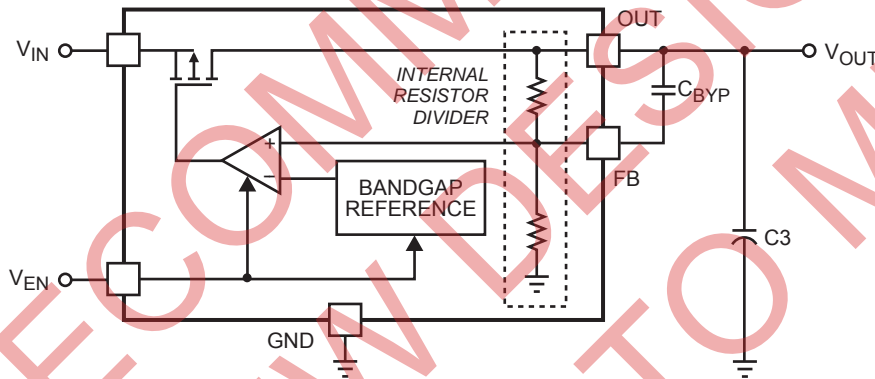
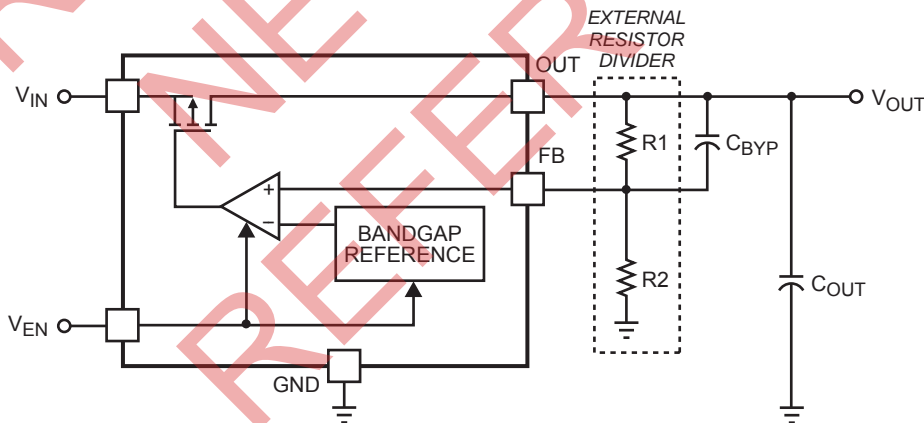
PIN FUNCTIONS

QFN8 (2x2mm) Pin #	TSOT23-5 Pin #	Name	Description
1	2	GND	Ground.
2	3	EN	Enable Input. Drive EN high to turn on the MP8903; low to turn it off. For automatic startup, connect EN to IN.
3, 4	1	IN	Power Source Input. IN supplies the internal power to the MP8903 and is the source of the pass transistor. Bypass IN to GND with a 1µF or greater capacitor.
5, 6	5	OUT	Regulator Output. OUT is the output of the linear regulator. Bypass OUT to GND with a 1µF or greater capacitor.
7		NC	No Connect.
8	4	FB	Feedback Input. Connect a resistive voltage divider from OUT to FB to set the output voltage. The OUT feedback threshold is 1.222V.

OPERATION

The MP8903 is a low-current, low-dropout linear regulator. The MP8903 uses a PMOS pass element and features internal thermal shutdown. The normally fixed output MP8903

may be converted to an adjustable output device by applying a resistor divider network as shown in Figure 2. An optional feed-forward capacitor, C_{BYP} , may be added for an improved transient response.


Figure 1—Fixed Output Regulator

Figure 2—Adjustable Regulator: $V_{OUT} = V_{FB} (1+(R1/R2))$

APPLICATION INFORMATION

Setting the Output Voltage

The fixed output voltage of the MP8903 is set to 2.5V, 2.85V or 3.3V, depending on the internal resistor divider (Figure 1). You can also adjust the output voltage by using an external resistor divider (R1 and R2 in Figure 2). However, the sum of R1 and R2 should not exceed 100kΩ in order to minimize the impact of the internal resistor divider. For an accurate output-voltage setting, use 10kΩ (±1%) for the low-side resistor R2 of the voltage divider, while the high-side resistor R1 can be determined by the equation:

$$R1 = R2 \times \left(\frac{V_{OUT} - V_{FB}}{V_{FB}} \right)$$

Where V_{FB} is the OUT feedback threshold voltage equal to 1.222V.

Example: For 2.5V Output

$$R1 = \frac{2.5V - 1.222V}{\left(\frac{1.222V}{10k\Omega} \right)} = 10.41k\Omega$$

You can select a standard 10.5kΩ (±1%) resistor for R1.

The following table lists the selected R1 values for some typical output voltages:

Table 1—Adjustable Output Voltage R1 Values

V _{OUT} (V)	R1 (Ω)	R2 (Ω)
1.25	232	10k
1.5	2.26k	
1.8	4.75k	
2	6.34k	
2.5	10.5k	
2.8	13k	
3	14.7k	
3.3	16.9k	
4	22.6k	
5	30.9k	

In Figures 3 and 4, C2 is added for an improved transient response.

Input Capacitor Selection

For proper operation, place a ceramic capacitor (C1) between 1μF and 10μF of dielectric type X5R or X7R between the input pin and ground. Larger values in this range will help improve line transient response at the drawback of increased size.

Output Capacitor Selection

For stable operation, use a ceramic capacitor (C3) of type X5R or X7R between 1μF and 10μF. Larger values in this range will help improve load transient response and reduce noise with the drawback of increased size. Output capacitors of other dielectric types may be used, but are not recommended as their capacitance can deviate greatly from their rated value over temperature.

To improve load transient response, add a small ceramic (X5R, X7R or Y5V dielectric) 100nF feed forward capacitor in parallel with R1. The feed forward capacitor is not required for stable operation.

TYPICAL APPLICATION CIRCUIT

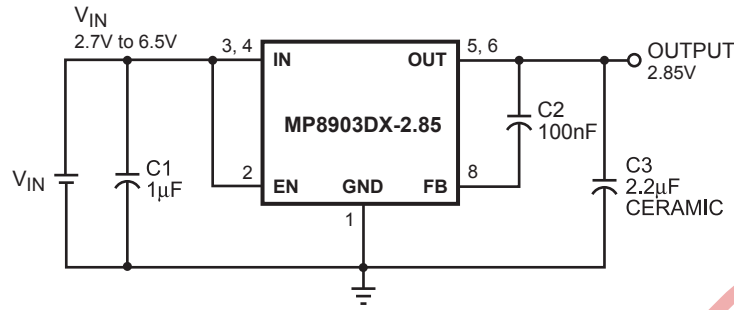


Figure 3—Typical Application Circuit (Fixed)

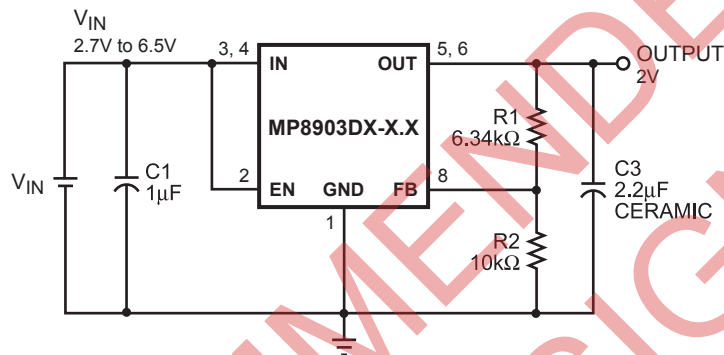


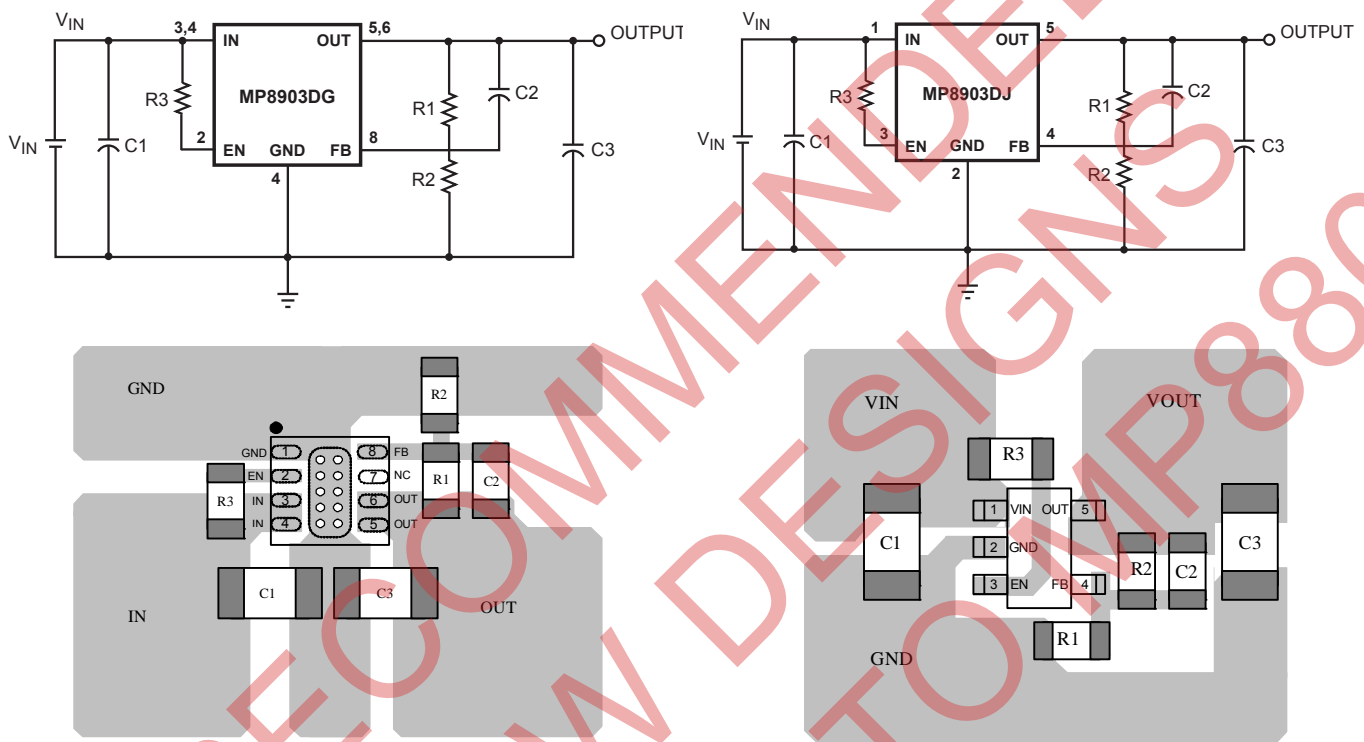
Figure 4—Typical Application Circuit (Adjustable)

PCB LAYOUT GUIDE

PCB layout is very important to achieve good regulation, ripple rejection, transient response and thermal performance. It is highly recommended to duplicate EVB layout for optimum performance.

If change is necessary, please follow these guidelines and take figure 5 for reference.

- 1) Input and output bypass ceramic capacitors are suggested to be put close to the IN Pin and OUT Pin respectively.
- 2) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
- 3) Connect IN, OUT and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.

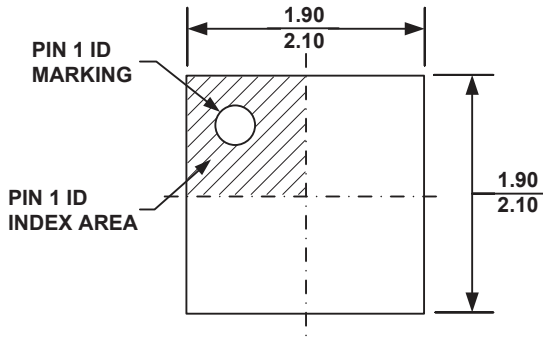


Top Layer

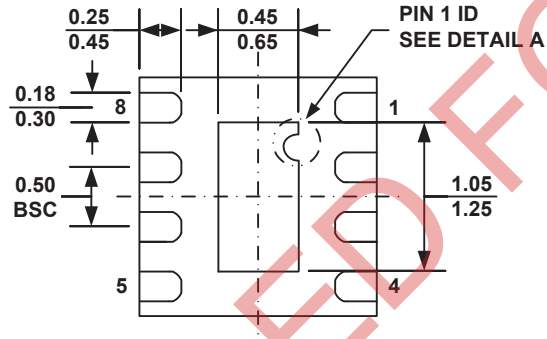
Figure 5—PCB Layout

PACKAGE INFORMATION

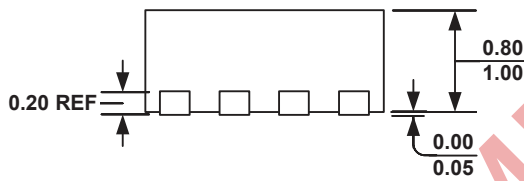
QFN8 (2x2mm)



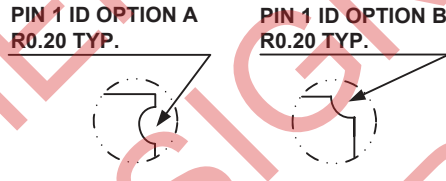
TOP VIEW



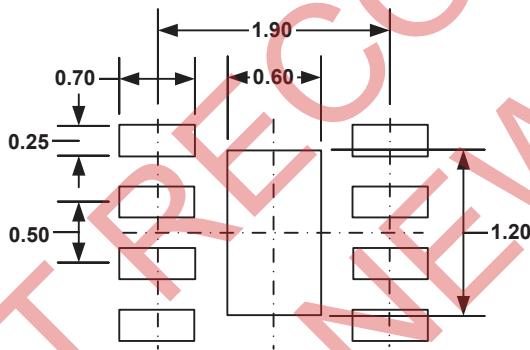
BOTTOM VIEW



SIDE VIEW



DETAIL A

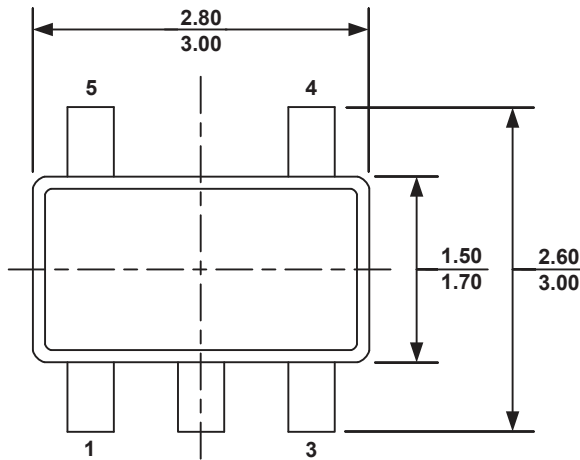


RECOMMENDED LAND PATTERN

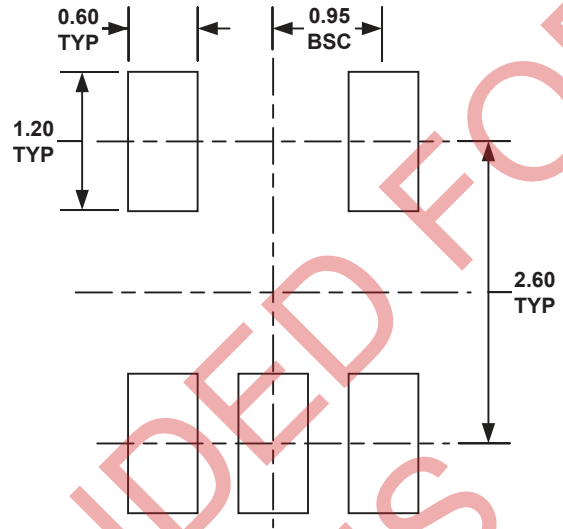
NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
- 4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VCCD-3.
- 5) DRAWING IS NOT TO SCALE.

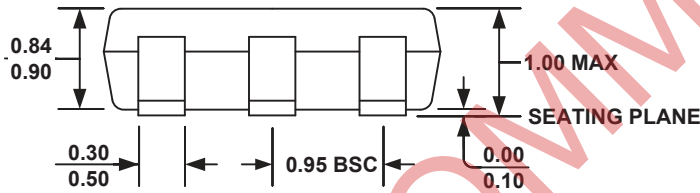
TSOT23-5



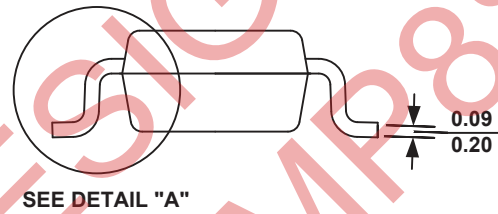
TOP VIEW



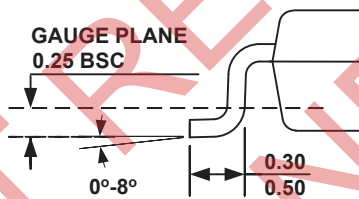
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL A

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
- 5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AA.
- 6) DRAWING IS NOT TO SCALE.

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