

### DESCRIPTION

The MP6420 provides over-charge protection that integrates a protective, open-drain MOSFET for 2- or 3-series cell Li-ion power systems.

The MP6420 provides a  $\pm 25\text{mV}$ , high-accuracy, over-charge threshold to monitor all series' battery pack conditions. With the high-accuracy threshold, the MP6420 can provide different fixed thresholds from 4.2V to 4.8V internally. Any cell over-charge that occurs turns on the internal protective MOSFET to indicate an error after an internally set, fixed delay time.

The MP6420 is available in a small, space-saving TSOT23-8 package.

### FEATURES

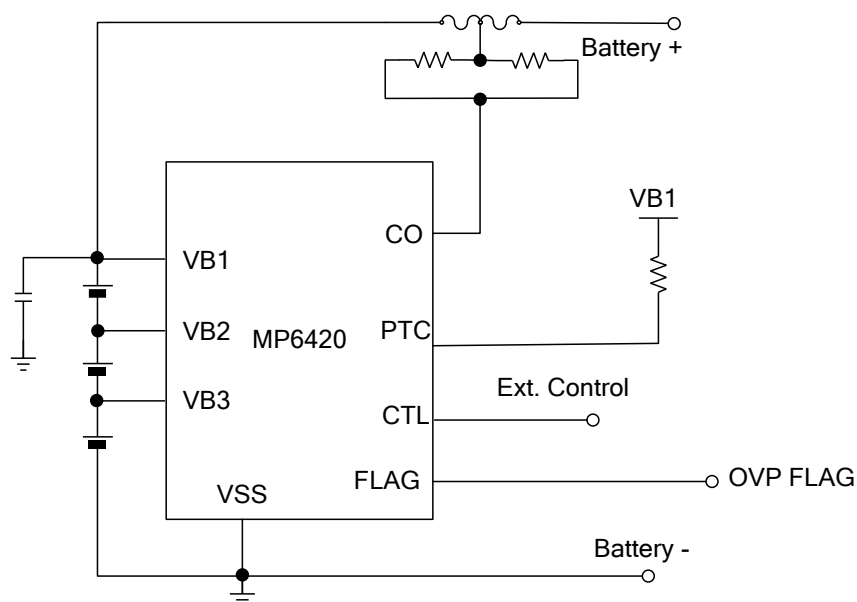
- Wide VB1 Range from 3.6V to 18V
- Fixed Over-Charge Threshold from 4.2V to 4.8V
- High-Accuracy  $\pm 25\text{mV}$  Over-Charge Threshold
- Supports 2- and 3-Series Cells
- Fixed Delay Time from 2s to 8s
- Integrated 24V/100m $\Omega$  Protective MOSFETs
- Low Quiescent Current: 3 $\mu\text{A}$
- Over-Voltage Protection (OVP) Indicator (FLAG) and PTC Interface
- External Control (CTL)
- Available in a TSOT23-8 Package

### APPLICATIONS

- Battery Packs
- Uninterruptible Power Supply (UPS)
- Power Tools

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### TYPICAL APPLICATION



### ORDERING INFORMATION

Part Number*	Package	Top Marking
MP6420GJ	TSOT23-8	See Below

\* For Tape & Reel, add suffix -Z (e.g. MP6420GJ-Z)

### TOP MARKING

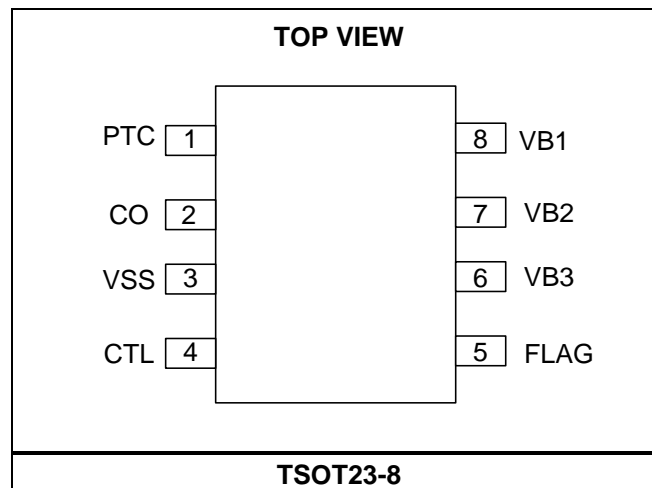
**|AVFY**

AVF: Product code of MP6420GJ  
 Y: Year code

### OVER-VOLTAGE THRESHOLD

Part Number	Over-Voltage Threshold (V <sub>ov</sub> )	Over-Voltage Threshold (V <sub>ov_H</sub> )	Over-Voltage Delay Time
MP6420GJ-445	4.45V ± 25mV	-0.4 ± 0.16V	3.8 ± 0.8s

### PACKAGE REFERENCE



**ABSOLUTE MAXIMUM RATINGS (1)**

VB1, PTC, CO .....	$V_{SS} - 0.3V$ to $V_{SS} + 19.5V$
CTL, FLAG .....	$V_{SS} - 0.3V$ to $6V$
VB1 to VB2, VB2 to VB3 .....	$V_{SS} - 0.3V$ to $6.5V$
VB3 to VSS .....	$V_{SS} - 0.3V$ to $6.5V$
All other pins .....	$V_{SS} - 0.3V$ to $6V$
Junction temperature .....	$150^{\circ}C$
Lead temperature .....	$260^{\circ}C$
Continuous power dissipation (2)	
TSOT23-8 (4) .....	$1.2W$

**Recommended Operating Conditions (3)**

Supply voltage (VB1) .....	$3.6V$ to $18V$
Operating junction temp. ( $T_J$ )...	$-40^{\circ}C$ to $+125^{\circ}C$

<b>Thermal Resistance (4)</b>	$\theta_{JA}$	$\theta_{JC}$
TSOT23-8		
JESD51-7 (4) .....	$100$	$55$ ... $^{\circ}C/W$
EV6420-J-00A (5) .....	$100$	$26$ ... $^{\circ}C/W$

**NOTES:**

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature  $T_J$  (MAX), the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) =  $(T_J$  (MAX) -  $T_A$ ) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, 4-layer PCB.
- 5) Measured on EV6420-J-00A, 2-layer PCB.

## ELECTRICAL CHARACTERISTICS

$V_{B1} = 12V$ ,  $V_{B1}$  to  $V_{B2} = V_{B2}$  to  $V_{B3} = V_{B3}$  to  $V_{SS} = 4V$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , typical value is tested at  $T_J = 25^{\circ}C$ . The limit over temperature is guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
<b>Input and Supply Voltage Range</b>						
Input voltage	$V_{B1}$	$V_{B1}$ voltage	3.6		18	V
$V_{B1}$ under-voltage lockout threshold	$V_{B1\_UVLO}$	Rising edge		3.2	4	V
UVLO hysteresis <sup>(8)</sup>	$V_{B1\_HYS}$			200		mV
Quiescent current	$I_Q$	Normal condition <sup>(6) (7)</sup>		3	5	$\mu A$
Quiescent current during over-discharge		Over-discharge condition, $V_{B1}$ to $V_{B2} = V_{B2}$ to $V_{B3} = V_{B3}$ to $V_{SS} = 3.3V$		2		$\mu A$
Over-discharge cell voltage	$V_{Dis}$	Falling edge, $V_{B1}$ to $V_{B2} = V_{B2}$ to $V_{B3} = V_{B3}$ to $V_{SS}$	3.5	3.8	4.1	V
Over-discharge cell voltage hysteresis				60		mV
Quiescent current during shutdown		Over-discharge condition, $V_{B1}$ to $V_{B2} = V_{B2}$ to $V_{B3} = V_{B3}$ to $V_{SS} = 2.2V$		1		$\mu A$
$V_{BX}$ leakage current	$I_{BX}$	Normal condition <sup>(6) (7)</sup>		0		$\mu A$
<b>Voltage Threshold</b>						
Over-charge threshold	$V_{OV}$	See ordering info		$V_{OV}$		V
Over-charge threshold range		$T_J = 25^{\circ}C$	-25		25	mV
		$T_J = 85^{\circ}C$ <sup>(8)</sup>	-30		45	
		$T_J = -40^{\circ}C$ <sup>(8)</sup>	-50		30	
Over-charge hysteresis	$V_{OV\_H}$	See ordering info		$V_{OV\_H}$		mV
Over-charge hysteresis range		$T_J = 25^{\circ}C$	-160		160	mV
<b>Protective MOSFET</b>						
On resistance	$R_{DS(ON)}$	$V_{B1} = 5.0V$ , single channel		100		m $\Omega$
Current capability		Guaranteed by design	4.5			A
Breakdown voltage			28			V
Resistor between FLAG and CTL				240		k $\Omega$
FLAG low voltage		Sink 1mA			0.5	V
FLAG high voltage		Source 1mA	4		5.5	V
CTL low voltage		$V_{B1}$ to $V_{B2} = V_{B2}$ to $V_{B3} = V_{B3}$ to $V_{SS} = 3.7V$ , sink 1 $\mu A$			0.3	V
CTL high voltage		$V_{B1}$ to $V_{B2} = V_{B2}$ to $V_{B3} = V_{B3}$ to $V_{SS} = 4.5V$ , source 1 $\mu A$ load	4	4.5	5.5	V
CTL rising threshold		Turn on the protective MOSFET		2		V
CTL falling threshold		Turn off the protective MOSFET		1.5		V
<b>PTC Interface</b>						
PTC threshold		Falling edge		$V_{B1} - 1.2$		V
PTC hysteresis		Rising edge		400		mV
PTC deglitch delay		Guaranteed by design		100		$\mu s$

**ELECTRICAL CHARACTERISTICS (continued)**

$V_{B1} = 12V$ ,  $V_{B1}$  to  $V_{B2} = V_{B2}$  to  $V_{B3} = V_{B3}$  to  $V_{SS} = 4V$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , typical value is tested at  $T_J = 25^{\circ}C$ . The limit over temperature is guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
<b>Delay Time</b>						
Over-charge response delay	$T_{OV}$	Any $V_{BX}$ over-charge	3	3.8	4.6	s
Over-charge reset time	$T_{OV\_RES}$			10		ms
Over-charge release delay	$T_{OV\_N}$			60		ms
PTC response delay		Before turning on protective MOSFET		1.8		ms
Over-discharge recovery delay		From over-discharge to normal mode		1		ms
<b>Internal Filter</b>						
Filter resistor <sup>(9)</sup>				3		MΩ
Filter capacitor <sup>(9)</sup>				100		pF

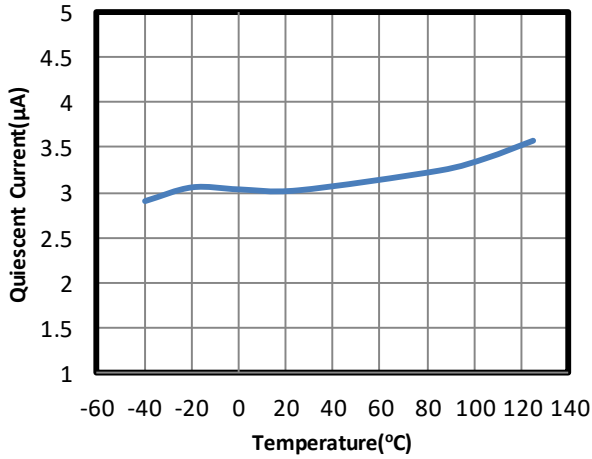
**NOTES:**

- 6) Normal condition means no over-charge condition occurred.  $V_{B1}$  to  $V_{B2} = V_{B2}$  to  $V_{B3} = V_{B3}$  to  $V_{SS} = 4V$ .
- 7) Test schematic excludes FLAG sink current.
- 8) Not tested in production, guaranteed by design specification.
- 9) Guaranteed by design.

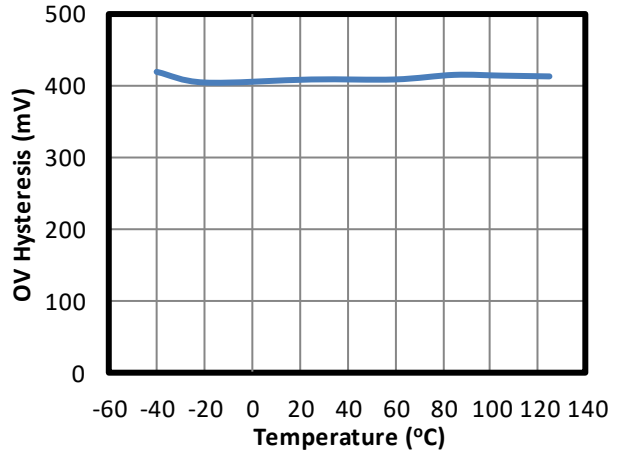
### TYPICAL CHARACTERISTICS

$V_{B1} = 12V$ ,  $V_{B1}$  to  $V_{B2} = V_{B2}$  to  $V_{B3} = V_{B3}$  to  $V_{SS} = 4V$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$ . Test based on MP6420GJ-445, unless otherwise noted.

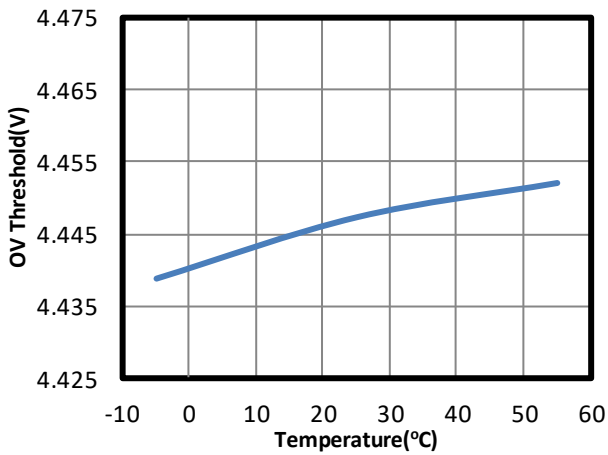
Quiescent Current vs. Temperature



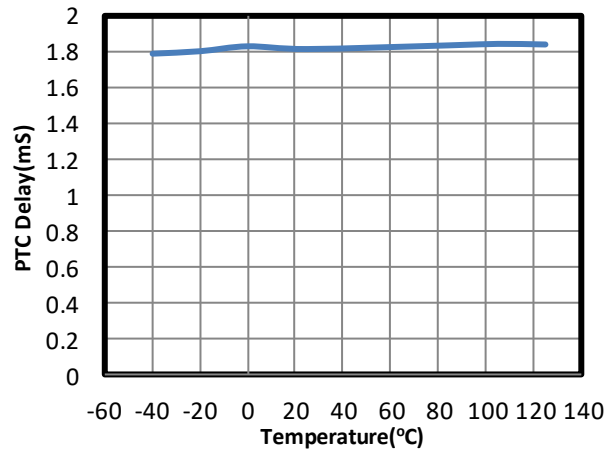
OV Hysteresis vs. Temperature



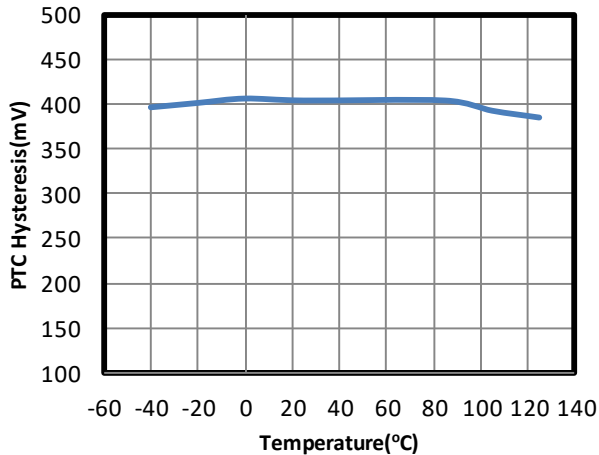
OV Threshold Vs. Temperature



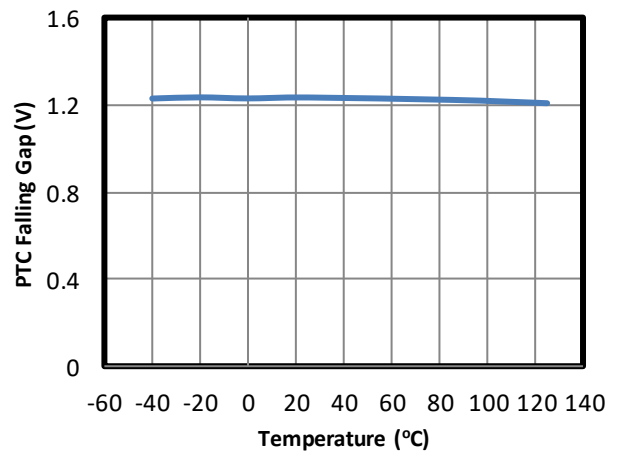
PTC Delay vs. Temperature



PTC Hysteresis vs. Temperature

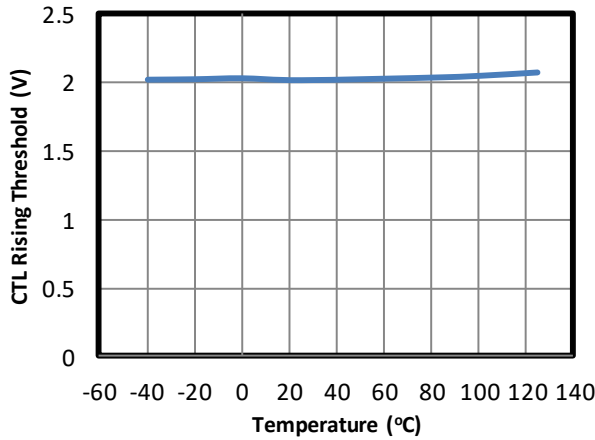
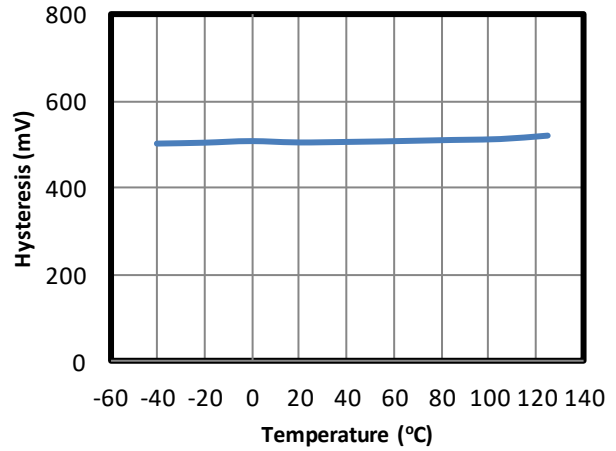


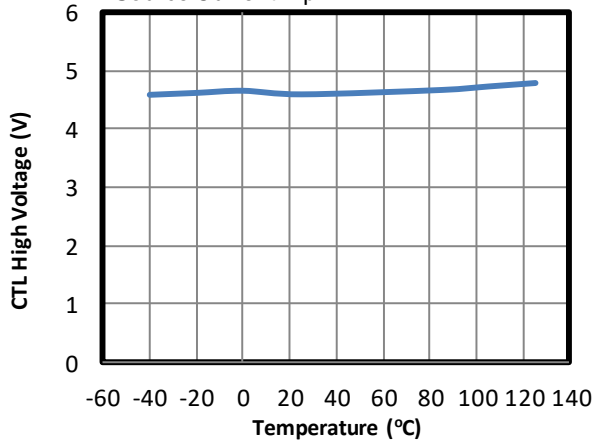
PTC Falling Gap vs. Temperature

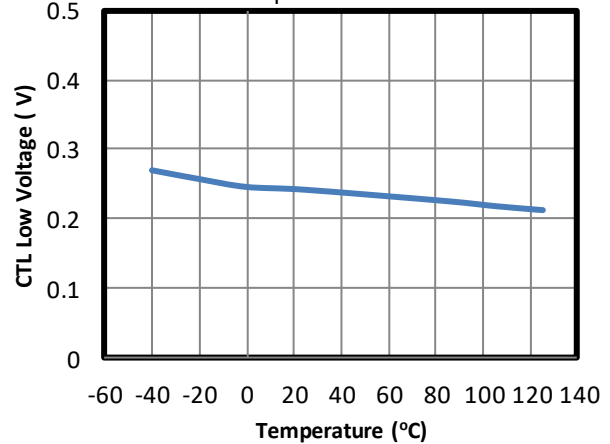


**TYPICAL CHARACTERISTICS (continued)**

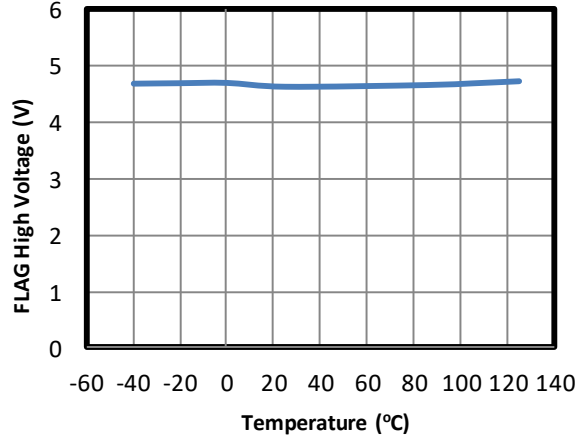
$V_{B1} = 12V$ ,  $V_{B1}$  to  $V_{B2} = V_{B2}$  to  $V_{B3} = V_{B3}$  to  $V_{SS} = 4V$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$ . Test based on MP6420GJ-445, unless otherwise noted.

**CTL Rising Threshold vs. Temperature**

**CTL Hysteresis vs. Temperature**

**CTL High Voltage vs. Temperature**

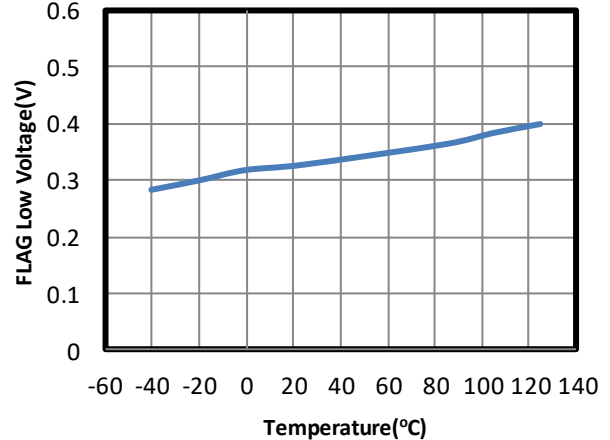
 Source Current=1 $\mu$ A

**CTL Low voltage vs. Temperature**

 Sink Current=1 $\mu$ A

**FLAG High Voltage vs. Temperature**

Source Current=1mA

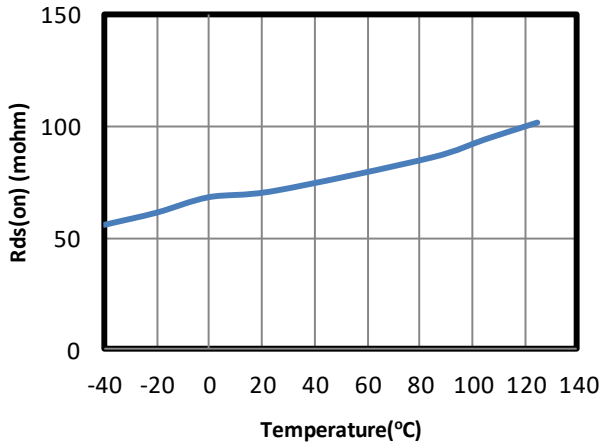
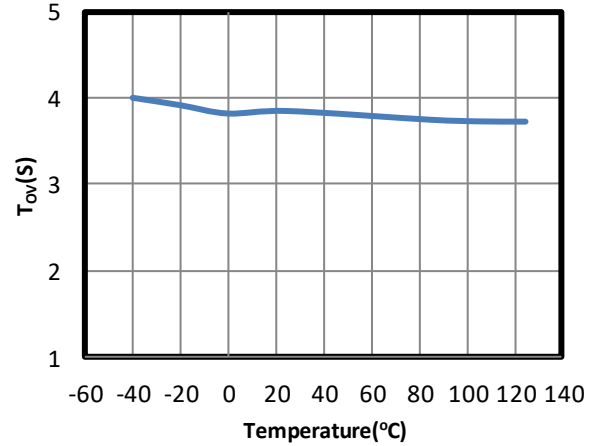
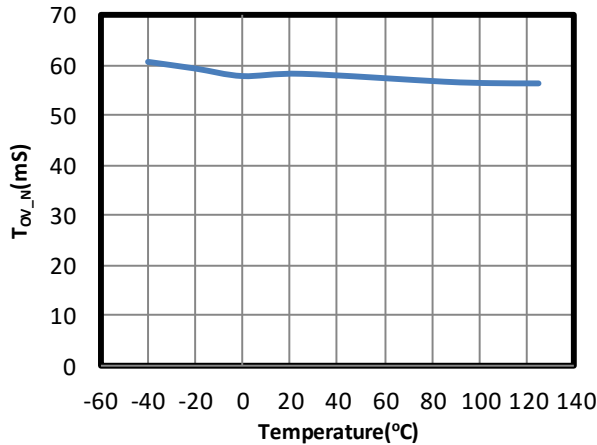
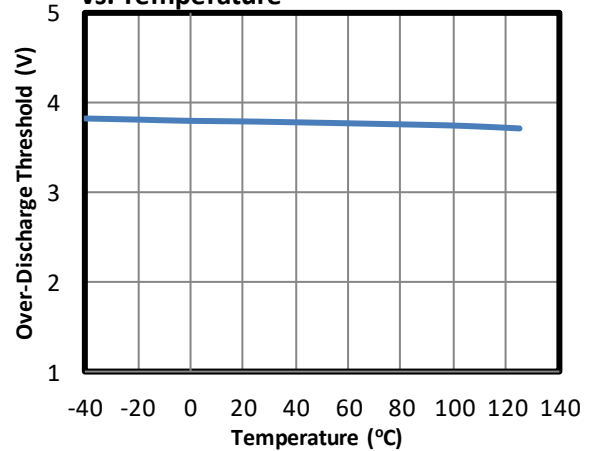
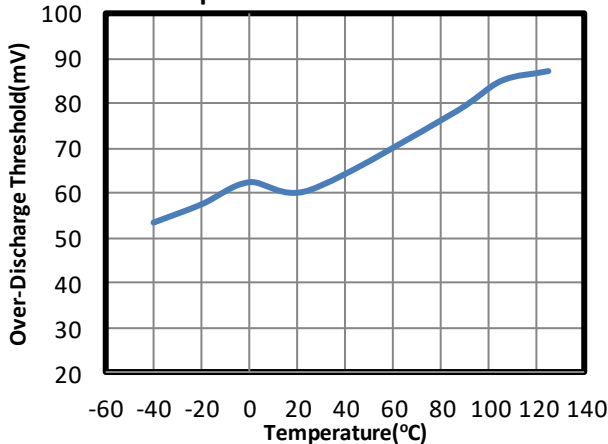

**FLAG Low Voltage vs. Temperature**

Sink Current=1mA



**TYPICAL CHARACTERISTICS (continued)**

$V_{B1} = 12V$ ,  $V_{B1}$  to  $V_{B2} = V_{B2}$  to  $V_{B3} = V_{B3}$  to  $V_{SS} = 4V$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$ . Test based on MP6420GJ-445, unless otherwise noted.

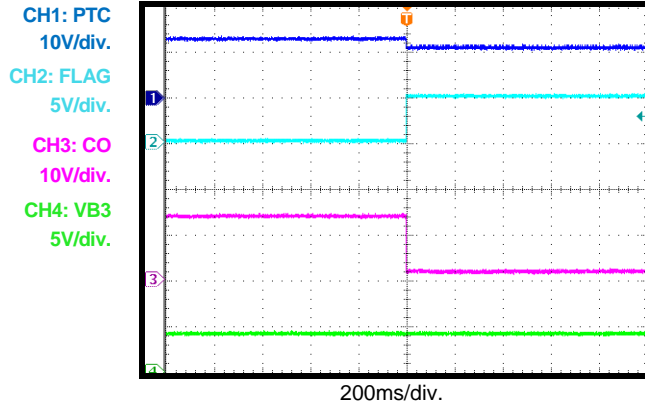
**R<sub>ds(on)</sub> vs. Temperature**

**T<sub>ov</sub> vs. Temperature**

**T<sub>ov\_N</sub> vs. Temperature**

**Over-Discharge Threshold vs. Temperature**

**OV-Discharge Hysteresis vs. Temperature**




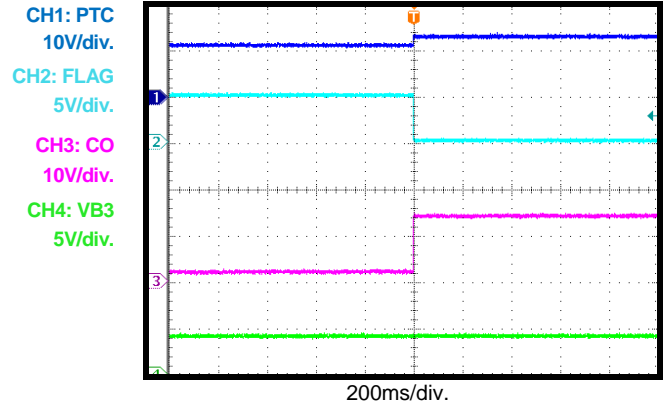
## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{B1}$  to  $V_{B2} = V_{B2}$  to  $V_{B3} = V_{B3}$  to  $V_{SS} = 4V$  with  $10k\Omega$  resistor between  $V_{B1}$  and PTC,  $T_J = 25^\circ C$ . Test based on MP6420GJ-445, unless otherwise noted.

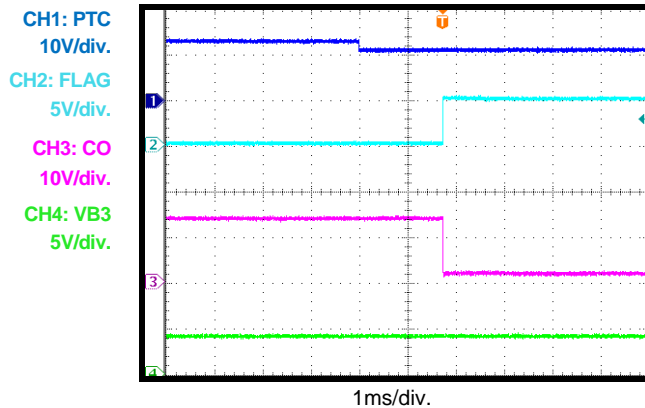
### PTC Response



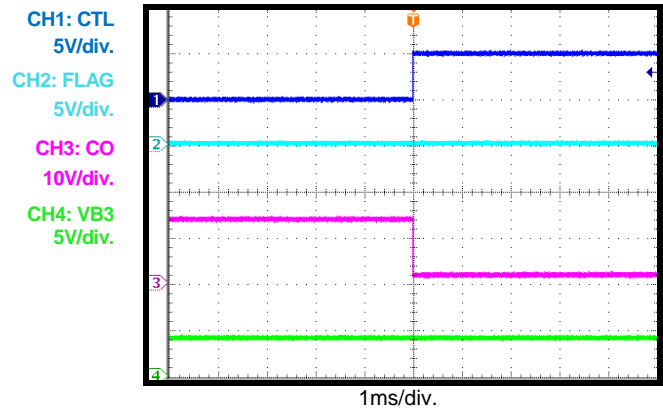
### PTC Response



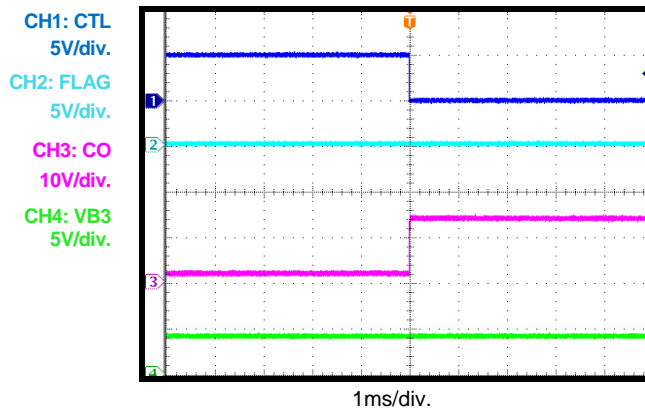
### PTC Delay



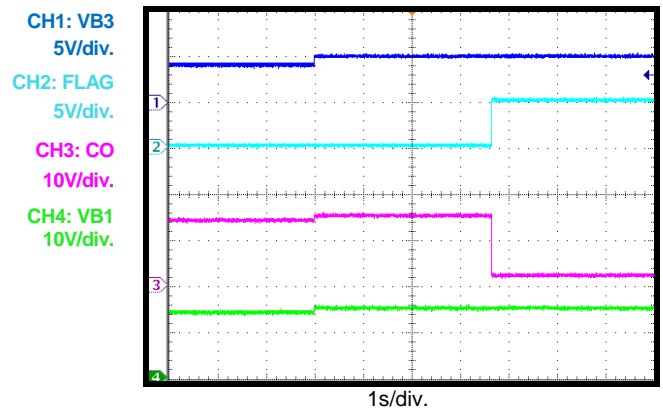
### CTL Response



### CTL Response

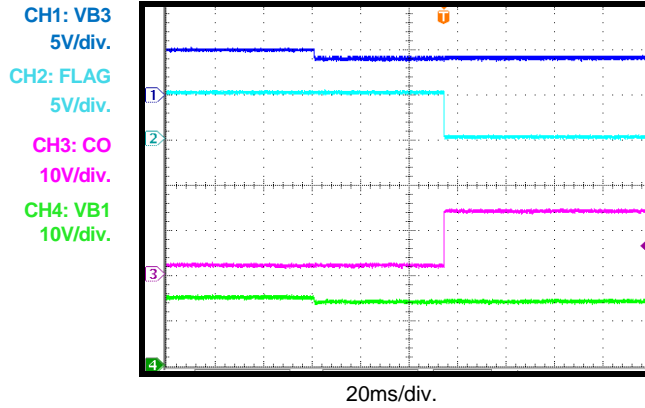


### OVP Response

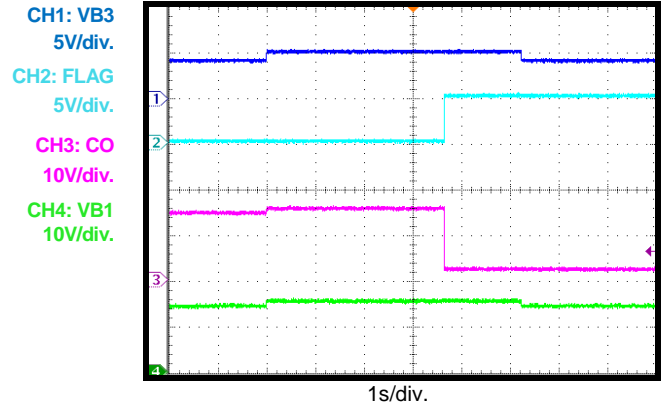


**TYPICAL PERFORMANCE CHARACTERISTICS** *(continued)*

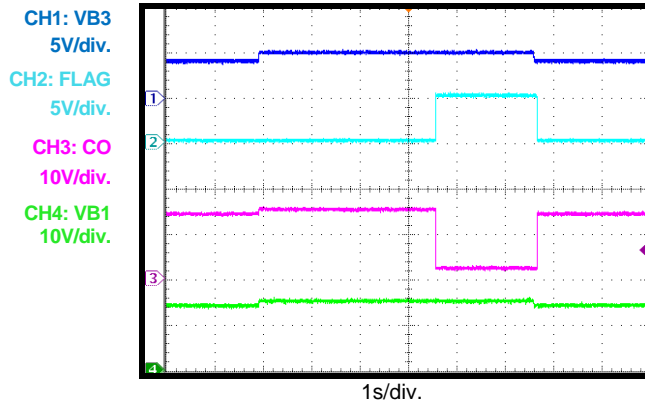
$V_{B1}$  to  $V_{B2} = V_{B2}$  to  $V_{B3} = V_{B3}$  to  $V_{SS} = 4V$  with  $10k\Omega$  resistor between  $VB1$  and PTC,  $T_J = 25^\circ C$ . Test based on MP6420GJ-445, unless otherwise noted.

**OVP Recovery Delay**

**OVP Response**

$V_{B1}$  to  $V_{B2} = V_{B2}$  to  $V_{B3} = 4.1V$


**OVP Recovery**

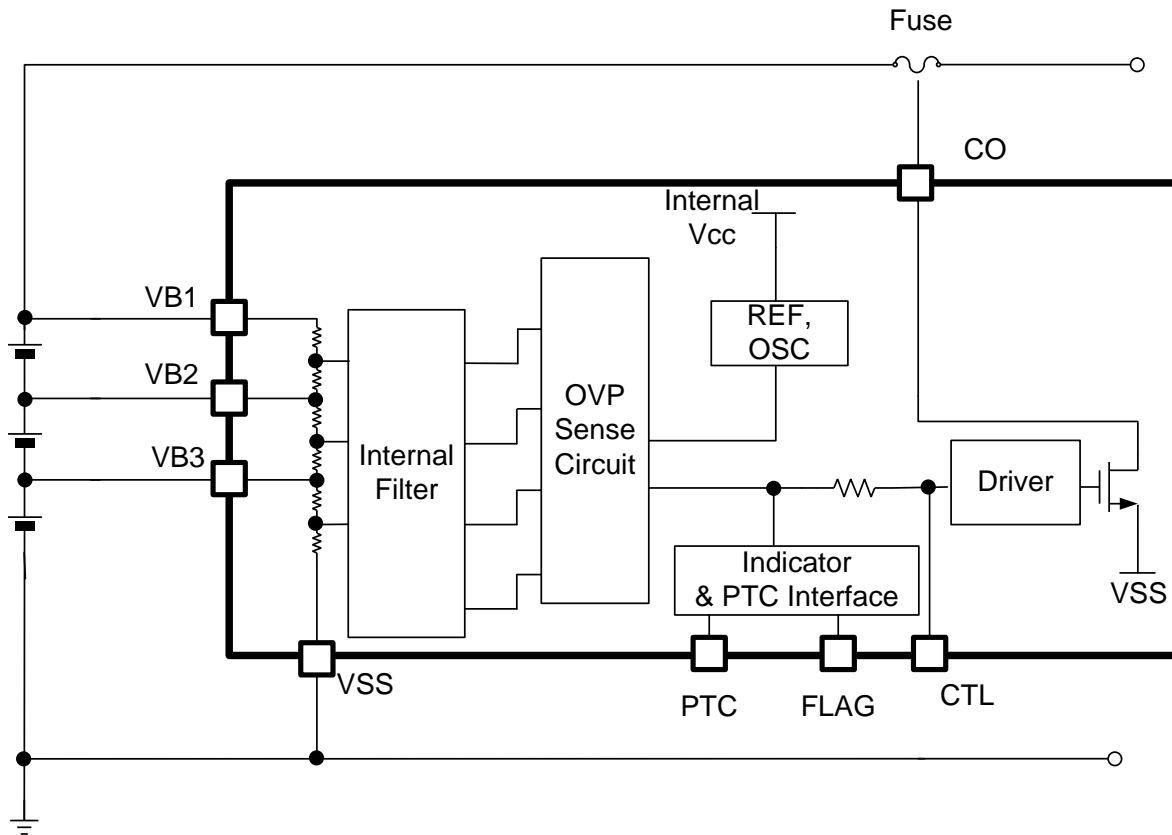
$V_{B1}$  to  $V_{B2} = V_{B2}$  to  $V_{B3} = 3.9V$



**PIN FUNCTIONS**

Package Pin #	Name	Description
1	PTC	<b>Positive thermal coefficient interface.</b>
2	CO	<b>Open-drain output of the protective MOSFET.</b>
3	VSS	<b>Negative power supply.</b>
4	CTL	<b>External control.</b> CTL connects to the gate pin of the internal protective MOSFET.
5	FLAG	<b>Battery OVP indicator.</b> When OVP occurs and the internal protective MOSFET turns on, FLAG is pulled up to at least 4V.
6	VB3	<b>Voltage sense point of battery cell 3.</b> VB3 is connected to the positive voltage of cell 3. Place cell 2 between VB2 and VB3.
7	VB2	<b>Voltage sense point of battery cell 2.</b> VB2 is connected to the positive voltage of cell 2. Place cell 1 between VB1 and VB2.
8	VB1	<b>Voltage sense point of battery cell 1.</b> VB1 is connected to the positive voltage of cell 1.

**BLOCK DIAGRAM**



**Figure 1: Functional Block Diagram**

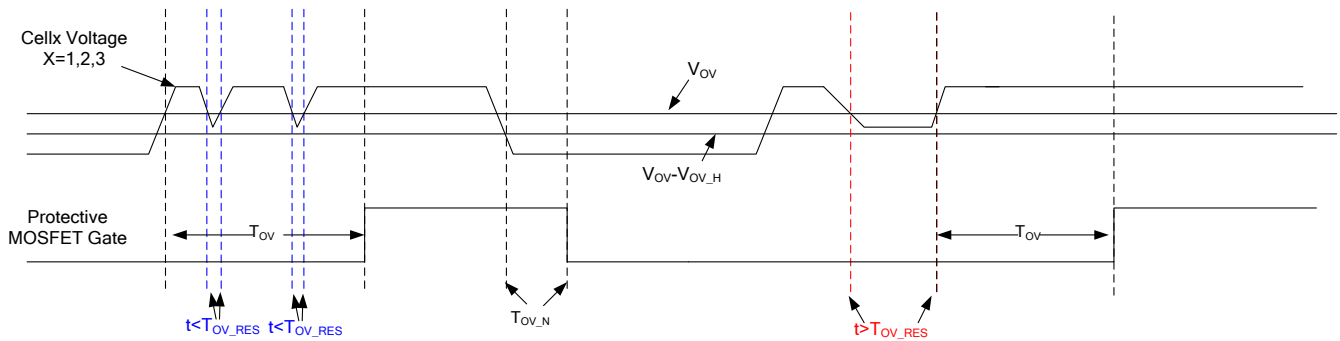
## OPERATION

The MP6420 provides an over-charge protection that integrates a protective, open-drain MOSFET for 2- or 3-series cell Li-ion power systems.

The MP6420 provides a  $\pm 25\text{mV}$ , high-accuracy, over-charge threshold to monitor all series' battery pack conditions. With the high-accuracy threshold, the MP6420 provides different fixed thresholds from 4.2V to 4.8V internally. Any cell over-charge turns on the internal protective MOSFET to indicate an error after a fixed, internally set delay time. FLAG is used to indicate an over-voltage protection (OVP) condition, provide a PTC interface, and can control the protective MOSFET externally with CTL.

## Over-Voltage Detection

All cells are monitored between VB1 and VB2, VB2 and VB3, and VB3 and VSS. If any of the voltages from these cells rise higher than the over-voltage threshold ( $V_{OV}$ ), OVP is triggered. The internal MOSFET turns on and remains on until the cell over-voltage status remains longer than the over-charge response delay ( $T_{OV}$ ). The  $T_{OV}$  timer can be reset if the cell voltage drops below the over-threshold voltage and remains longer than the over-charge reset time ( $T_{OV\_RES}$ ). The OVP status is released if all cell voltages fall below the over-voltage release voltage ( $V_{OV} - V_{OV\_H}$ ), and the internal MOSFET turns off again. There is an over-charge release delay ( $T_{OV\_N}$ ) to deglitch noise (see Figure 2).



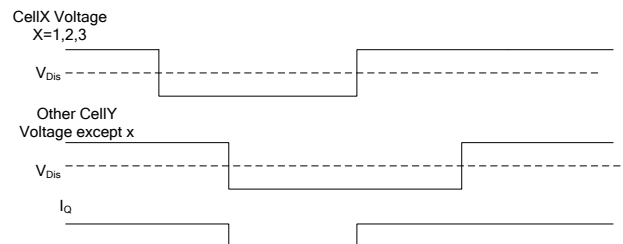
**Figure 2: MP6420 Over-Voltage Response**

## Integrated MOSFET and Filter

Traditionally, secondary battery protection ICs need an external, high-voltage, or large-current MOSFET. Each cell requires an R-C filter to prevent cell voltage noise. The MP6420 provides a fully integrated solution with a protective MOSFET and internal filter. The internal filter has an equivalent  $1\text{k}\Omega/0.1\mu\text{F}$  external R-C filter performance. This helps lower cost and make the layout easier. The internal protective MOSFET is a  $24\text{V}/100\text{m}\Omega$  device. The filter works with an anti-noise over-voltage comparator, which can monitor the battery voltage.

## Over-Discharge Status

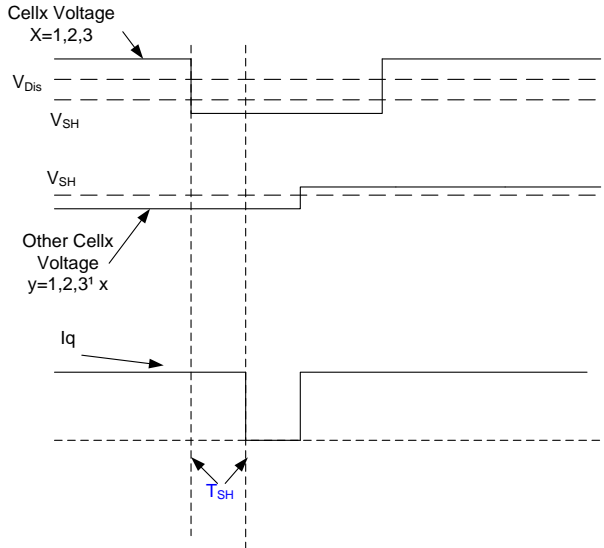
The MP6420 saves quiescent current when the voltage on all cells is over-discharged. If the voltage of all the cells is lower than the over-discharge threshold ( $V_{Dis}$ ), the cell over-voltage monitor block is disabled. The disabled over-charge detection block decreases the quiescent current during an over-discharge status (see Figure 3).



**Figure 3: Over-Discharge Status**

### Shutdown Status

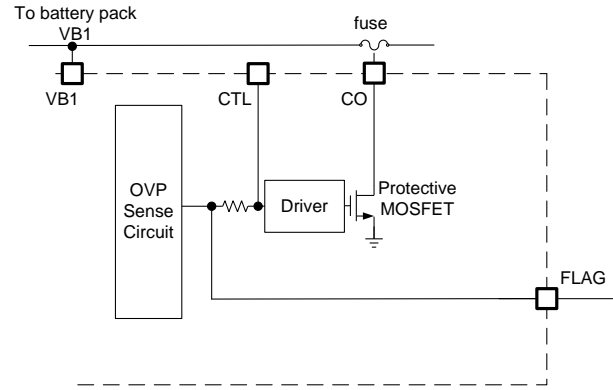
The MP6420 decreases most of the quiescent current during shutdown. When all cell voltages are lower than  $V_{Dis}$  and the shutdown voltage ( $V_{SH}$ ), all over-voltage (OV) monitor blocks are disabled (see Figure 4).



**Figure 4: Shutdown Status**

### FLAG Indicator

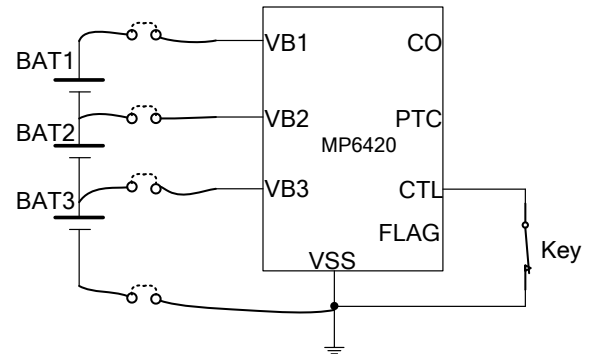
FLAG is an indicator pin. Under normal conditions, FLAG is at logic low. When over-charge occurs or over-temperature is detected by PTC, FLAG is pulled up to an internal 5V supply (see Figure 5). FLAG can be floated.



**Figure 5: FLAG and CTL Structure**

### Cell Connection Power Sequence

Since the MP6420 internal VCC is based on VB3, it is recommended to make VB3 the first connection in the power sequence (see Table 1). CTL provides another way to avoid a malfunction during the assembly process. CTL is pulled down to VSS so that the inner protective MOSFET is not active.



**Figure 6: Recommended Safe Operation during Assembly Process**

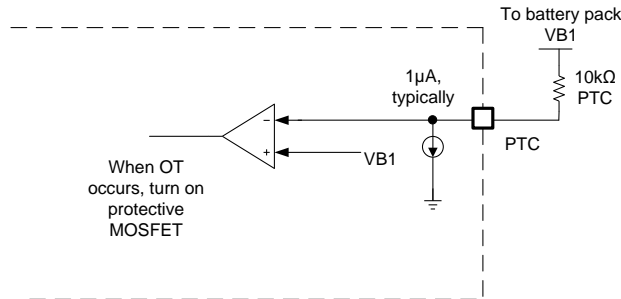
**Table 1: Recommended Connection Sequence**

Connection Sequence	FLAG Pin Signal				CO Pin Signal			
	Int.	1st	2nd	3rd	Int.	1st	2nd	3rd
→VSS→VB3→VB2→VB1	Low	Low	Low	Low	Low	High	High	High
→VSS→VB3→VB1→VB2	Low	Low	Low	Low	Low	High	High	High

## APPLICATION INFORMATION

### PTC Interface

PTC can be used to monitor the ambient temperature and turn on the protective MOSFET. PTC cannot be floated. PTC requires a resistor (typically 10kΩ) pulled to VB1 (see Figure 7). When the PTC interface is required, a 10kΩ PTC resistor is recommended. See Table 2 for a list of recommended resistors and manufacturers.



**Figure 7: MP6420 PTC Interface**

There is an internal sink current source used to pull down the PTC voltage (typically ~1µA). Under normal conditions, the FLAG output is at logic low. With 10kΩ of PTC resistance under room temperature, the PTC voltage is almost equal to VB1. If the sensor PTC resistor monitors high temperatures, the PTC resistance ramps quickly, and the PTC voltage drops. When the PTC voltage is lower than VB1 - 1.2V, the MP6420 triggers PTC protection.

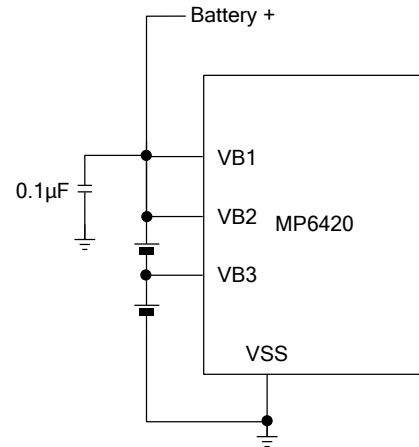
If the PTC function is not needed, a normal 10kΩ resistor is sufficient.

**Table 2: Recommended PTC Resistors**

Part Number	Description	Vendor
PRF15BB103RB6RC	10kΩ, 130°C	Murata
ECPH1608103P130ST	10kΩ, 130°C	Joinset

### 2-/3-Cell Usage

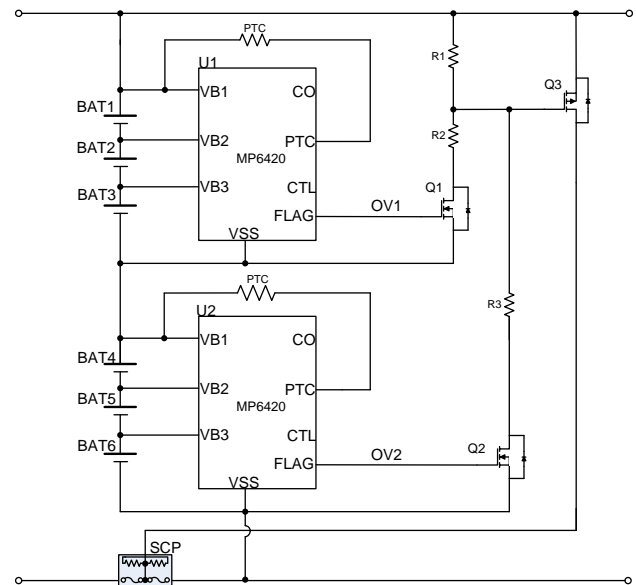
When the MP6420 has more monitor ports than it is using, the unused ports should be shorted. The VB1 - VB3 monitors must be used from the bottom side. For example, if only two cells are used, then VB1 should be shorted to VB2 (see Figure 8).



**Figure 8: 2-Cell Usage**

### More than 3-Cell Usage

For applications using a battery with more than three cells, use a MP6420 series circuit (see Figure 9).



**Figure 9: 3-Cell Battery or More Application Circuit**

Each FLAG is active high when one-cell OVP is triggered. Q3 then turns on to pull down the self-control protector (SCP). The OR logic circuit consists of extra MOSFETs (Q1, Q2, Q3) and pull-up resistors (R1, R2, R3). Choose MOSFETs and resistors based Equation (1):

$$V_{ds\_max\_Q1} = 1.3 \times V_{BAT} \quad (1)$$

Where  $V_{BAT}$  is the voltage of each cell battery.

When OV1 is low (no OV trigger on U1) and considering a 30% margin, calculate  $V_{ds}$  with Equation (2):

$$V_{ds\_max\_Q2} = 1.3 \times 6V_{BAT} \quad (2)$$

The Q2 maximum  $V_{ds} = 3V_{BAT}$ .

When OV2 is low (no OV trigger on U2) and considering a 30% margin, calculate  $V_{ds}$  with Equation (3):

$$V_{ds\_max\_Q3} = 1.3 \times 6V_{BAT} \quad (3)$$

The Q3 maximum  $V_{ds} = 6V_{BAT}$ .

When both OV1 and OV2 are low (no OV trigger on either cell) and considering a 30% margin, calculate  $V_{gs}$  with Equation (4) and Equation (5):

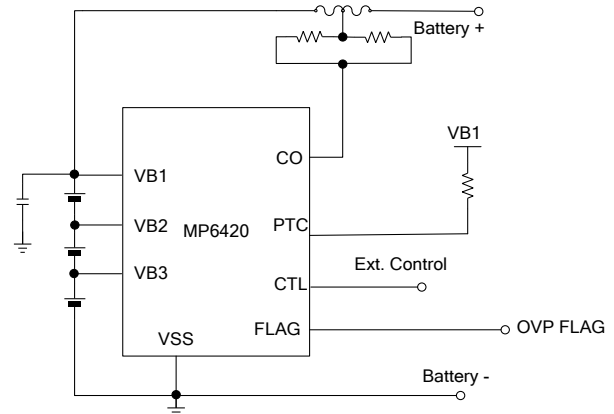
$$V_{gs(th)\_max\_Q3} < 3V_{BAT} \times R1 / (R1 + R2) < V_{gs\_max\_Q3} \quad (4)$$

$$V_{gs(th)\_max\_Q3} < 6V_{BAT} \times R1 / (R1 + R3) < V_{gs\_max\_Q3} \quad (5)$$

Where  $V_{gs(th)\_max\_Q3}$  is the maximum gate-to-source threshold voltage, and  $V_{gs\_max\_Q3}$  is the maximum gate-to-source voltage of Q3.

### Testing Over-Voltage Safely

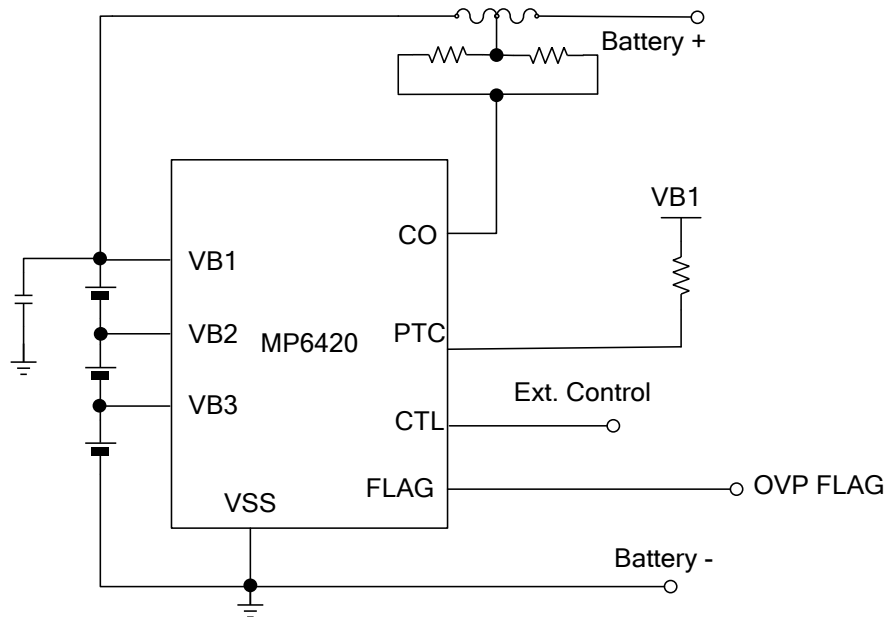
During the production test, OVP can be tested safely without blowing the fuse. Connect CTL to GND externally. With this configuration, the protective MOSFET gate is pulled to GND. With this configuration, the battery status can be indicated with FLAG (see Figure 10).



**Figure 10: Safe OVP Test**



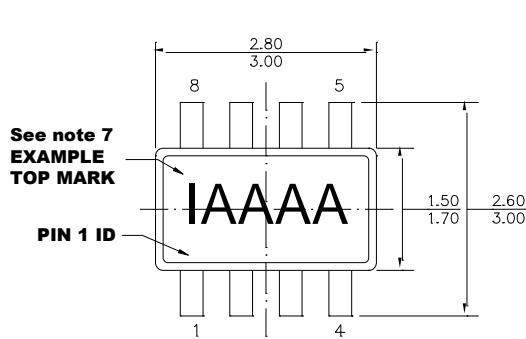
**TYPICAL APPLICATION CIRCUIT**



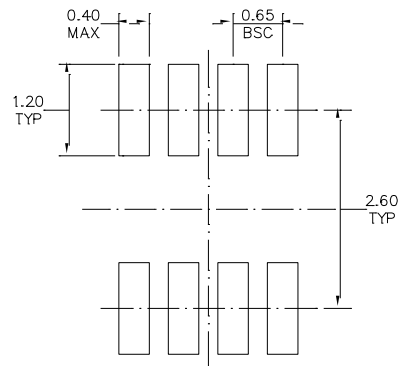
**Figure 11: MP6420 Typical Schematic**

## PACKAGE INFORMATION

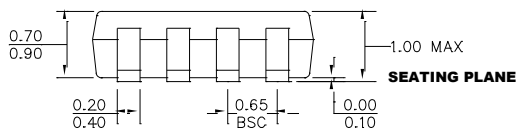
## TSOT23-8



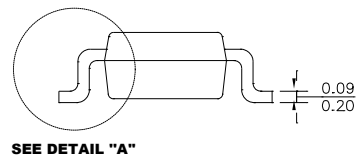
TOP VIEW



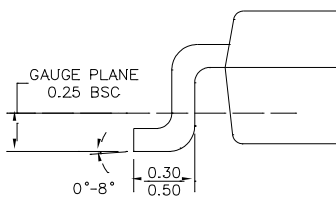
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

**NOTE:**

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
- 5) JEDEC REFERENCE IS MO-193, VARIATION BA.
- 6) DRAWING IS NOT TO SCALE.
- 7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

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