MP6302

Energy Storage and Release Control IC

The Future of Analog IC Technology

DESCRIPTION

The MP6302 is an energy storage and release controller. It charges storage capacitor from input during normal operation. Once the storage capacitor is charged to the selected voltage, the charge is stopped, and the storage capacitor is separated from the input. The charging circuit maintains the storage voltage after the charge is completed.

The MP6302 keeps monitoring the input voltage, and releases the charge from storage capacitor to the input capacitor when the input voltage is lower than a selected release voltage. It regulates the input voltage close to release voltage for as long as possible.

The MP6302 has built-in current limit circuit during the charging of the storage capacitor. The storage and release voltage can be programmed to user desired value by external resistors.

MP6302 comes in a tiny 2mmx3mm QFN10 package and requires a minimum number of readily available standard external components.

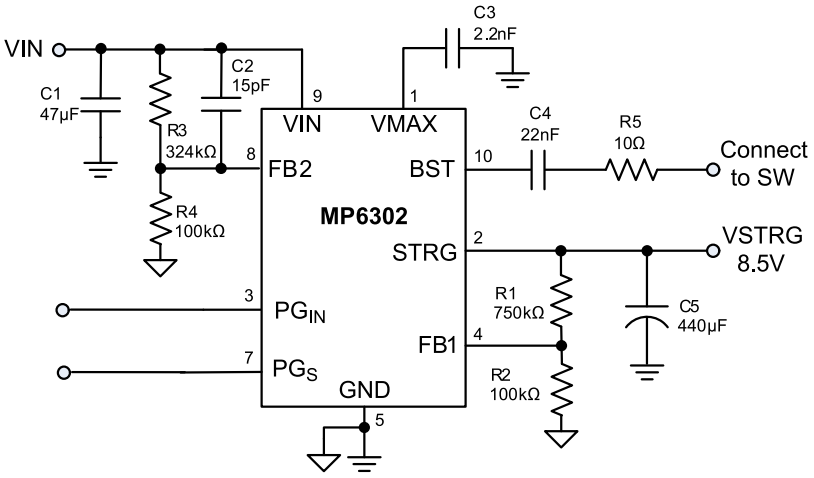
FEATURES

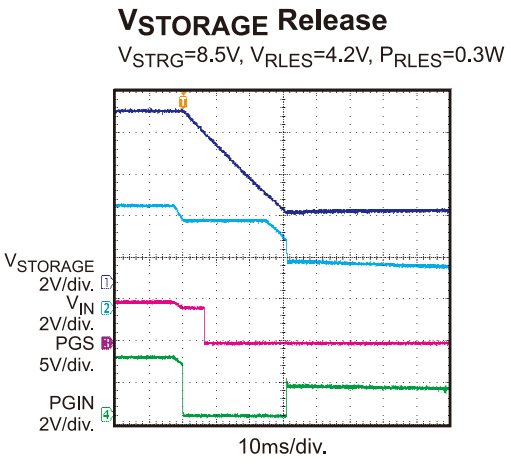
- Wide 4.2V to 18V input operating range
- 2.5A dumping current from storage to Vin
- Built-in 250mA current limit for charging storage capacitor
- User programmable storage and release voltage
- Indicators for storage and input voltage
- Available in a 2mmx3mm QFN10 package

APPLICATIONS

- Hard Disk Drives
- Solid State Drives

TYPICAL APPLICATION



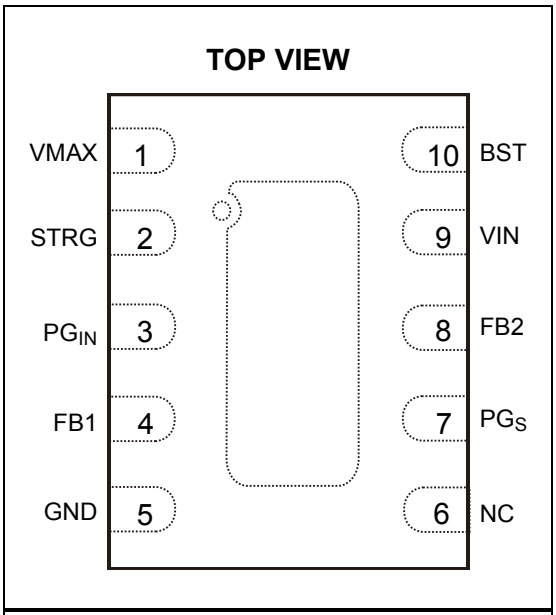


ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
MP6302DD	QFN10 (2x3mm)	ABC	-40°C to +85°C

* For Tape & Reel, add suffix –Z (e.g. MP6302DD–Z);

PACKAGE REFERENCE



QFN10 (2x3mm)

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to 22V
V_{BST} ..... -0.3V to 40V
V_{BST}-V_{IN} ..... -0.3V to 25V
V_{MAX} ..... -0.3V to 42V
V_{MAX}-V_{IN} ..... -0.3V to 25V
V_{STRG} ..... -0.3V to 32V
V_{STRG}-V_{IN} ..... -0.3V to 25V
V_{PG}, V_{GASP} ..... -0.3V to 22V
All Other Pins ..... -0.3V to 6.5V
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Continuous Power Dissipation (T_A = +25°C) (2) 1.2W
Junction Temperature ..... 150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ..... 4.5V to 18V
Storage Voltage V_{STRG} ..... V_{IN} to 2xV_{IN}(32V max)
Maximum Junction Temp (T_J) ..... +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
QFN10 (2x3mm)	70	15	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS (5)

V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply Voltage Range	V_{IN}		4.2		18	V
Supply Current (Shutdown)	I_s	V_{EN} = 0V		1		μA
Supply Current (Quiescent)	I_q	V_{EN} = 2V, V_{FB} = 1.1V		250		μA
VIN Under Voltage Lockout Threshold Rising	$INUV_{Vth}$		3.0	3.5	4.0	V
VIN Under Voltage Lockout Threshold Hysteresis	$INUV_{HYS}$			350		mV
Feedback Voltage	V_{FB1}, V_{FB2}		0.97	1	1.03	V
Vstorage Refresh Threshold-High	V_{FB1_H}			V_{FB}+0.025	V_{FB}+0.05	V
Vstorage Refresh Threshold-Low	V_{FB1_L}		V_{FB}-0.05	V_{FB}-0.025		V
Vstorage Refresh Threshold-Hysteresis	V_{FB1_Hys}			50		mV
Feedback Current	I_{FB}	V_{FB1}= V_{FB2}=1V		10	50	nA
PG_S High Threshold	VTH_{PGS}			0.9		V_{FB1}
PG_S Low Threshold	VTL_{PGS}			0.85		V_{FB1}
PG_S Delay	$PG_{S.Td}$			25		μs
PG_S Sink Current Capability	V_{PGS}	Sink 4mA		0.2		V
PG_S Leakage Current	I_{PGS_LEAK}	V_{PGS}=3.3V		10		nA
PG_{IN} High Threshold	VTH_{PGIN}			1.05		V_{FB2}
PG_{IN} Low Threshold	VTL_{PGIN}			1		V_{FB2}
PG_{IN} Delay	$PG_{IN.Td}$			2		μs
PG_{IN} Sink Current Capability	V_{PGIN}	Sink 4mA		0.2		V
PG_{IN} Leakage Current	I_{PGIN_LEAK}	V_{PGIN}=3.3V		10		nA
Input Inrush Current Limit for Charging Storage Capacitor	$I_{PRECHARGE\_LIMIT}$	V_{IN}=12V, Charging $C_{STORAGE}$ from 0 to V_{IN}		0.25		A
Current limit for Dumping Charge from $C_{STORAGE}$ to V_{IN}	I_{DUMP_LIMIT}			2.5	4	A
Thermal Shutdown	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			30		°C

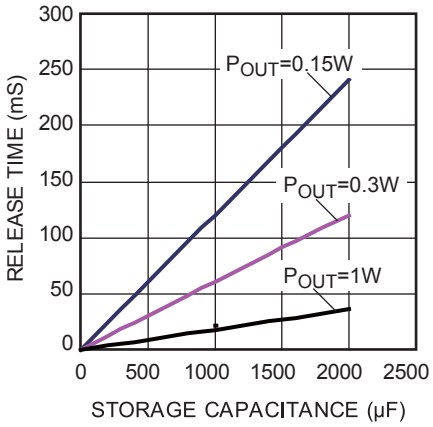
Note:

5) Guaranteed by design.

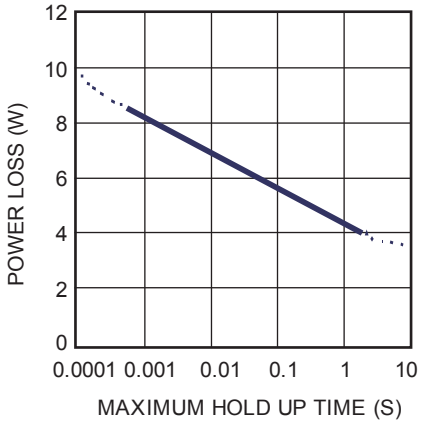
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, $V_{STORAGE}$ = 8.5V, $V_{RELEASE}$=4.2V, For DCDC Converter: P_{OUT}=0.3W, V_{OUT}=1.8V, T_A = +25ºC, unless otherwise noted.

Release Time vs. Storage Capacitance



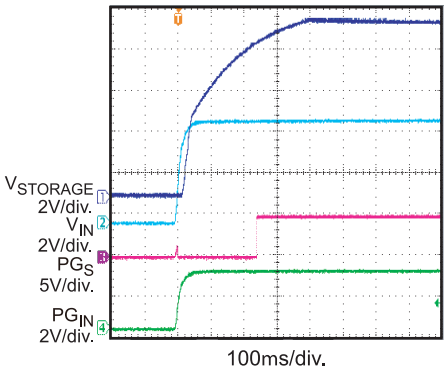
Thermal Performance



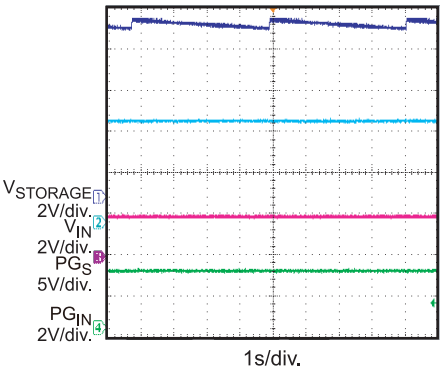
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, $V_{STORAGE}$ = 8.5V, $V_{RELEASE}$=4.2V, For DCDC Converter: P_{OUT}=0.3W, V_{OUT}=1.8V, T_A = +25°C, unless otherwise noted.

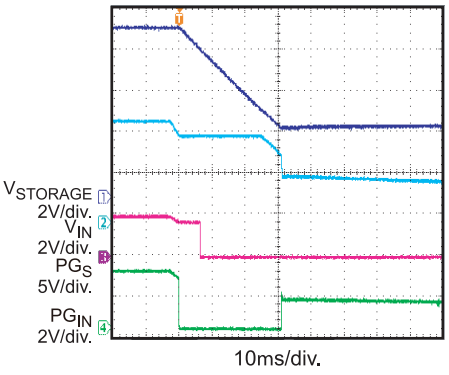
$V_{STORAGE}$ Charge Up



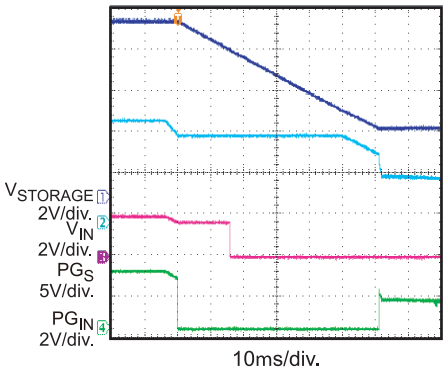
$V_{STORAGE}$ Refresh



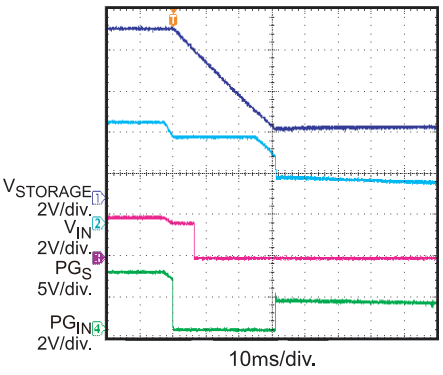
$V_{STORAGE}$ Release



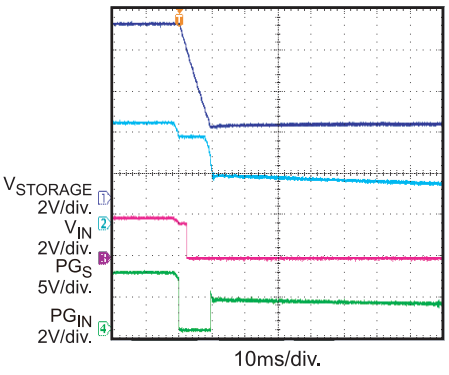
Release Time @ P_{OUT} = 0.15W, $C_{STORAGE}$=440µF



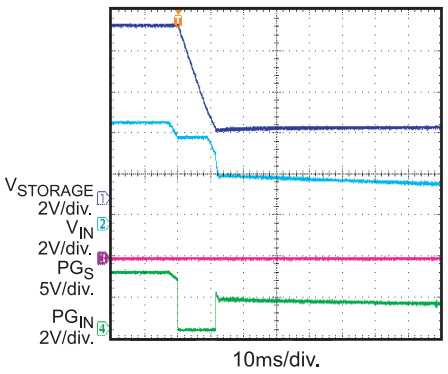
Release Time @ P_{OUT} = 0.3W, $C_{STORAGE}$=440µF



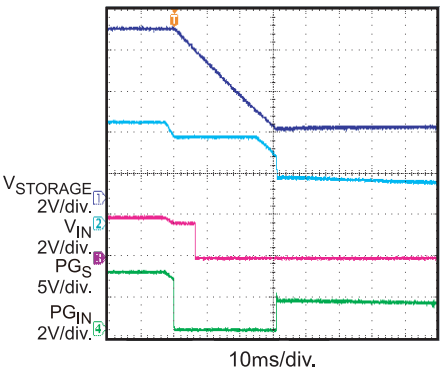
Release Time @ P_{OUT} = 1W, $C_{STORAGE}$=440µF



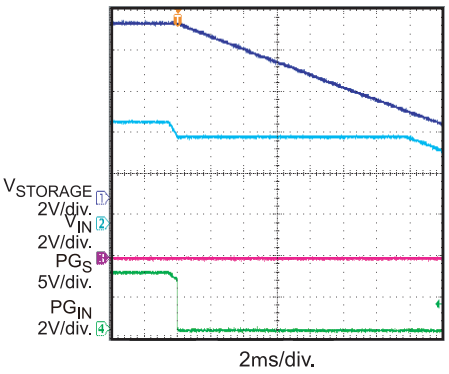
Release Time @ P_{OUT} = 0.3W, $C_{STORAGE}$ =150µF



Release Time @ P_{OUT} = 0.3W, $C_{STORAGE}$ =440µF



Release Time @ P_{OUT} = 0.3W, $C_{STORAGE}$ =1000µF



PIN FUNCTIONS

QFN2x3 Pin #	Name	Description
1	VMAX	Internal Supply. A 2.2nF ceramic capacitor is required for decoupling. Place this capacitor as close to the pin as possible.
2	STRG	Connect to storage capacitor for energy storage and release operation.
3	PG_{IN}	Open drain output to indicate input power availability.
4	FB1	Feedback to set storage voltage.
5	GND	System Ground. This pin is the reference ground of the regulated output voltage. For this reason care must be taken in PCB layout.
6	N/C	The pin should not be connected.
7	PG_s	Open drain output to indicate storage voltage availability.
8	FB2	Feedback to set release voltage.
9	VIN	Supply Voltage. The MP6302 operates from a +4.2V to +18V input rail. Input decoupling capacitor is needed to decouple the input rail.
10	BST	Bootstrap. A capacitor and a resistor in series connected between this pin and DC/DC converter's SW node is required to charge storage capacitor.

OPERATION

The MP6302 is an energy storage and release control IC. It charges the storage capacitors from input supply during power start up and keeps refreshing the storage voltage at a regulated value during normal operation. The MP6302 continuously monitors the input voltage. Once the input voltage is lower than a selected release voltage as in the case of losing input power, it releases the charge from the storage capacitors to input side, and keeps the input voltage regulated to the release voltage for as long as possible. This allows the system to respond to input power failure.

Start-up

During power start-up, there are two periods to charge the storage voltage. In the first period, the MP6302 pre-charges the large storage capacitors from 0 to VIN with built-in inrush current limit. Once the storage voltage is close to the input voltage, an internal boost circuitry will continuously charge and regulate the storage capacitors to the target voltage. The BST pin of MP6302 should connect to the DCDC switch node. Figure1 shows the charging process of MP6302.

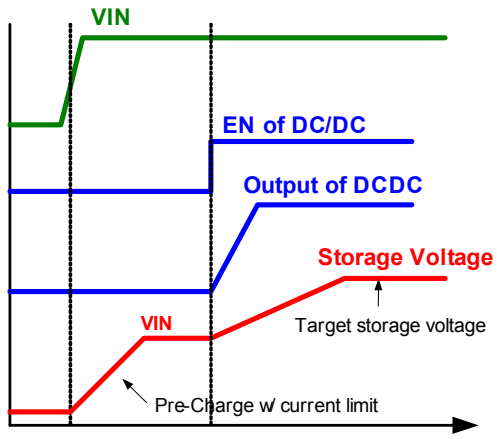


Figure 1—Timing of Charging

Storage Power Good Indicator

When the voltage on FB1 pin is lower than $0.85XV_{FB1}$, the PGs pin will be internally pulled low. When the FB1 is above $0.9XV_{FB1}$, this pin can be driven to the high logic.

Storage Voltage

After the start up period of MP6302, the storage voltage can automatically regulated at a selected output voltage. With the hysteretic mechanism, when the storage voltage is lower than selected voltage, an internal controlled switch is turned on and charges the storage capacitor. Once the storage voltage is charged up, the switch turns off and waits for the next refresh cycle.

Release

The MP6302 keeps monitoring the input voltage. Once the input voltage is lower than the selected release voltage as in the case of losing input power, the MP6302 moves the charge from high voltage storage capacitor to low input voltage capacitor through an internal controlled release path. MP6302 must charge Vs up till PGs rises to high before a release can be executed. The release voltage can be determined by choosing appropriate input resistance divider. The maximum release current can be as high as 2.5A. The release process is shown in Figure2.

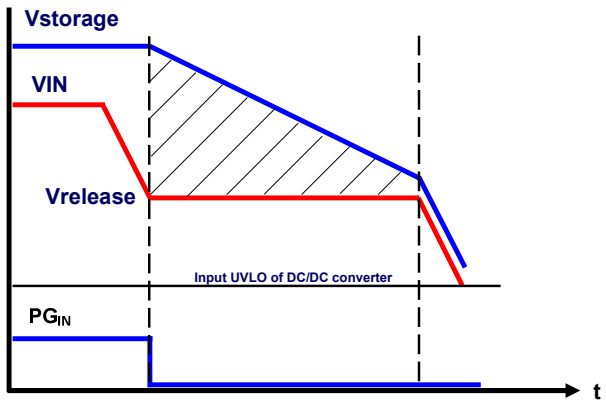


Figure 2—Timing of Releasing

Input Power Good Indicator

When the FB2 voltage, feedback voltage for the input power, is higher than $1.05XV_{FB2}$, the PG_{IN} pin can be pulled up to high logic. Connect a resistor across VIN and PG_{IN} can drive PG_{IN} high. When the FB voltage is lower than $1.00XV_{FB2}$, the PG_{IN} voltage will be internally pulled low.

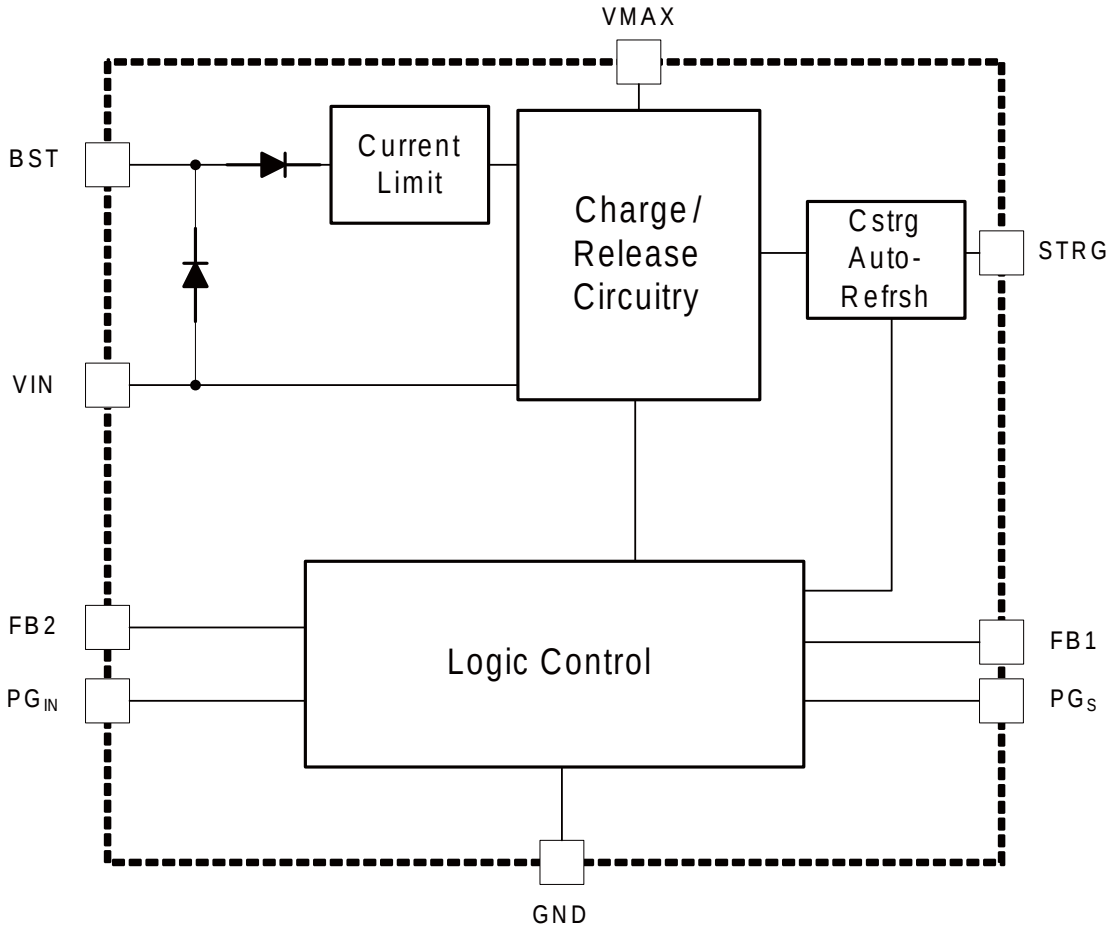


Figure 3—Functional Block Diagram

APPLICATION INFORMATION

Setting the Storage Voltage

The storage voltage can be set by choosing appropriate external feedback resistors R1 and R2 which is shown in Figure 4.

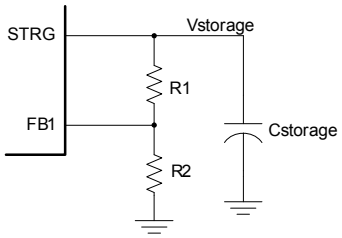


Figure 4—Feedback Circuit for Storage Voltage

The storage voltage can be calculated by:

$$V_{STORAGE} = (1+\frac{R1}{R2}) \times V_{FB1}$$

For example, if the storage voltage is set to be 8.5V, choose R2 to be 100kΩ, R1 will be then given by:

$$R1 = \frac{100k\Omega \times (8.5V - 1V)}{1V} = 750k\Omega$$

Table 1 lists the recommended resistors for different storage voltage settings.

Table 1—Resistor Selection for Different Storage Voltages

$V_{STORAGE}$ (V)	R1 (kΩ)	R2 (kΩ)
8.5	750	100
12	750	68
15	750	53.6

Setting the Release Voltage and Input Capacitors Selection

The release voltage can be set by external feedback resistors R3 and R4 shown in Figure 5.

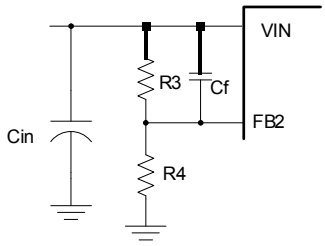


Figure 5—Feedback Circuit for Realease Voltage

The release voltage can be calculatedt by:

$$V_{RELEASE} = (1+\frac{R3}{R4}) \times V_{FB2}$$

The selection of R3 and R4 not only determines the release voltage, but also impacts the stability of the release circuit. The 300kΩ-500kΩ R3 and a 47μF C_{IN} are recommended. Table 2 lists the recommended resistors for different release voltage settings. A 15pF feed-forward capacitor is recommended for good release dynamic performance.

Table 2—Resistor and Capacitors Selection for Different Release Voltages

$V_{RELEASE}$ (V)	R3 (kΩ)	R4 (kΩ)	Cf (pF)	C_{IN} (μF)
11	475	47.5	15	47
10.2	464	49.9	15	47
4.2	324	100	15	47

Storage Capacitor Selection

The storage capacitor is used for energy storage during normal operation and the energy will be released to VIN in case of losing input power. Usually, the small ceramic capacitors or poscap can be used based on different applications.

The voltage rating of storage capacitor needs to be higher than the targeted storage voltage. The voltage rating of storage capacitor can be fully utilized since the voltage of storage capacitor is very stable during normal operation.

The necessary storage capacitance can be estimated by:

$$Cs = \frac{I_{RELEASE} \times T_{HOLD}}{V_{STORAGE} - V_{RELEASE}}$$

Here, $I_{RELEASE}$: release current

$V_{RELEASE}$: release voltage

T_{HOLD} : Hold up time

$V_{STORAGE}$: voltage on $C_{STORAGE}$

For example, if $I_{RELEASE}$=0.5A, T_{HOLD}=20ms, $V_{STORAGE}$=8.5V, $V_{RELEASE}$=4.2V the needed storage capacitance is around 2200μF.

PCB Layout Guide

PCB layout is important to achieve good performance operation for MP6302. Follow guidelines below and use the EVB board layout as a reference.

1) Connect the BST pin as close as possible to the SW node of DCDC converter through a resistor and a small ceramic capacitor. Try to avoid interconnect the feedback path.
2) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
3) Keep the connection of the storage capacitors and STRG pin as short and wide as possible.

TYPICAL APPLICATION CIRCUITS

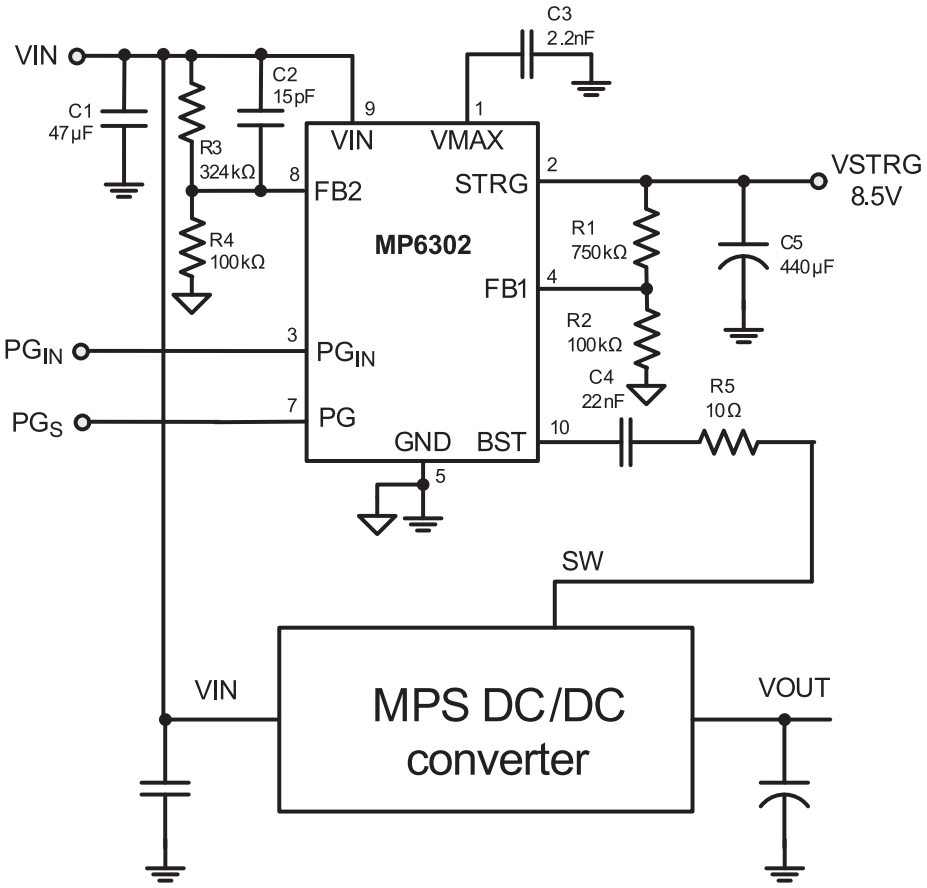
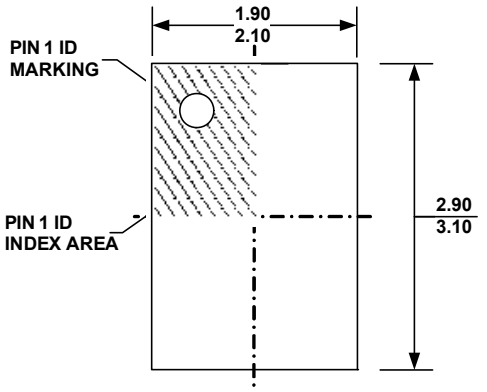


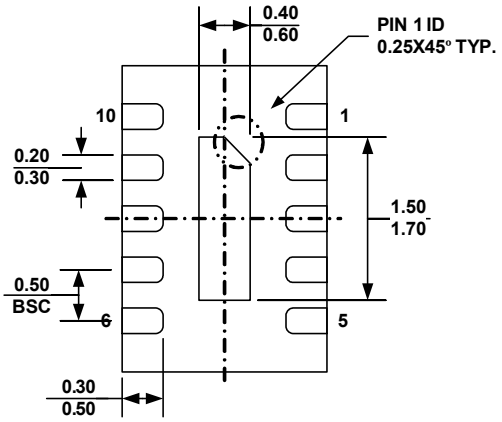
Figure 6—MP6302 Application Circuit

PACKAGE INFORMATION

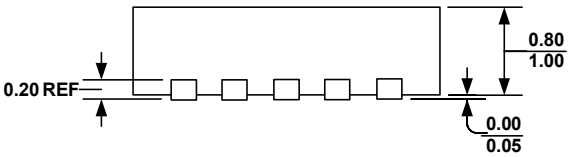
QFN10 (2x3mm)



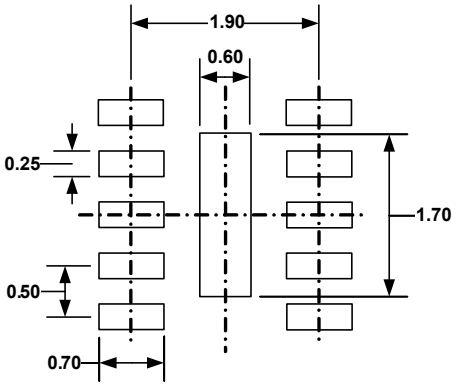
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX
4) JEDEC REFERENCE DRAWING IS JEDEC MO-220
5) DRAWING IS NOT TO SCALE