

## DESCRIPTION

The MP2161 is a monolithic step-down switch mode converter with built-in internal power MOSFETs. It achieves 2A continuous output current from a 2.5V to 6V input voltage with excellent load and line regulation. The output voltage can be regulated as low as 0.6V.

The Constant-On-Time control scheme provides fast transient response and eases loop stabilization. Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown.

The MP2161 is available in the small TSOT23-8 package and requires a minimum number of readily available standard external components.

The MP2161 is ideal for a wide range of applications including High Performance DSPs, FPGAs, PDAs, and portable instruments.

## FEATURES

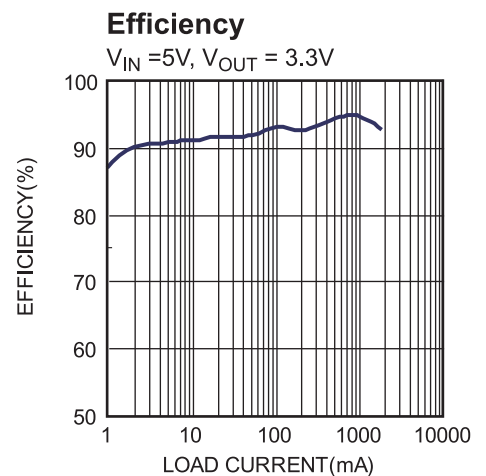
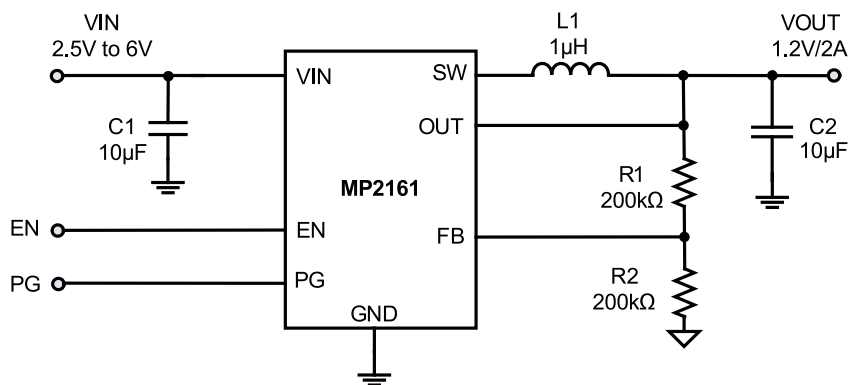
- Very Low I<sub>Q</sub>: 17 $\mu$ A
- Default 1.5MHz Switching Frequency
- EN and Power Good for Power Sequencing
- Wide 2.5V to 6V Operating Input Range Output Adjustable from 0.6V
- Up to 2A Output Current
- 100% Duty Cycle in Dropout
- 100m $\Omega$  and 60m $\Omega$  Internal Power MOSFET Switches
- Cycle-by-Cycle Over Current Protection
- Short Circuit Protect with Hiccup Mode
- Stable with Low ESR Output Ceramic Capacitors
- Available in a TSOT23-8 Package

## APPLICATIONS

- Wireless/Networking Cards
- Portable Instruments
- Battery Powered Devices
- Low Voltage I/O System Power

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## TYPICAL APPLICATION





**ELECTRICAL CHARACTERISTICS <sup>(5)</sup>**
 **$V_{IN} = 5V$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted.**

Parameter	Symbol	Condition	Min	Typ	Max	Units
Feedback Voltage	$V_{FB}$	$2.5V \leq V_{IN} \leq 6V$	-3%	0.600	+3%	V/%
		$T_A = -40^{\circ}C$ to $+85^{\circ}C$ <sup>(6)</sup>	-3.5%		+3.5%	
Feedback Current	$I_{FB}$	$V_{FB} = 0.6V$		10	50	nA
PFET Switch On Resistance	$R_{DSON\ P}$			100		m $\Omega$
NFET Switch On Resistance	$R_{DSON\ N}$			60		m $\Omega$
Switch Leakage		$V_{EN} = 0V$ , $V_{IN} = 6V$ $V_{SW} = 0V$ and $6V$		0	1	$\mu A$
PFET Current Limit			2.7	3.2	4.0	A
ON Time	$T_{ON}$	$V_{IN}=5V$ , $V_{OUT}=1.2V$		185		ns
		$V_{IN}=3.6V$ , $V_{OUT}=1.2V$		245		
Switching frequency	$F_s$	$V_{OUT}=1.2V$	-20%	1500	+20%	kHz/%
		$T_A = -40^{\circ}C$ to $+85^{\circ}C$ <sup>(6)</sup>	-25%	1500	+25%	
Minimum Off Time	$T_{MIN-OFF}$			60		ns
Soft-Start Time	$T_{SS-ON}$			1.5		ms
Power Good Upper Trip Threshold	$PG_H$	FB voltage respect to the regulation		+10		%
Power Good Lower Trip Threshold	$PG_L$			-10		%
Power Good Delay	$PG_D$			50		$\mu s$
Power Good Sink Current Capability	$V_{PG-L}$	Sink 1mA			0.4	V
Power Good Logic High Voltage	$V_{PG-H}$	$V_{IN}=5V$ , $V_{FB}=0.6V$	4.9			V
Power Good Internal Pull Up Resistor	$R_{PG}$			550		k $\Omega$
Under Voltage Lockout Threshold Rising			2.15	2.3	2.45	V
Under Voltage Lockout Threshold Hysteresis				260		mV
EN Input Logic Low Voltage					0.4	V
EN Input Logic High Voltage			1.2			V
EN Input Current		$V_{EN}=2V$		1.5		$\mu A$
		$V_{EN}=0V$		0		$\mu A$
Supply Current (Shutdown)		$V_{EN}=0V$ , $V_{IN}=3V$		20	100	nA
Supply Current (Quiescent)		$V_{EN}=2V$ , $V_{FB}=0.63V$ , $V_{IN}=5V$		17	20	$\mu A$
Thermal Shutdown <sup>(5)</sup>				150		$^{\circ}C$
Thermal Hysteresis <sup>(5)</sup>				30		$^{\circ}C$

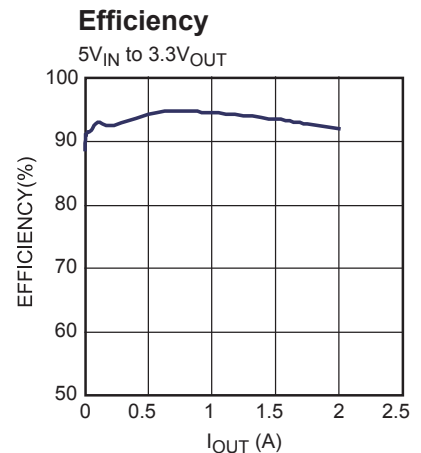
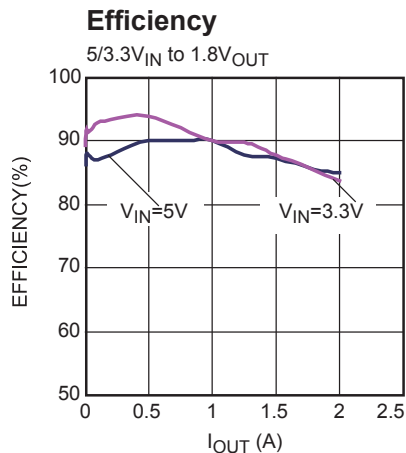
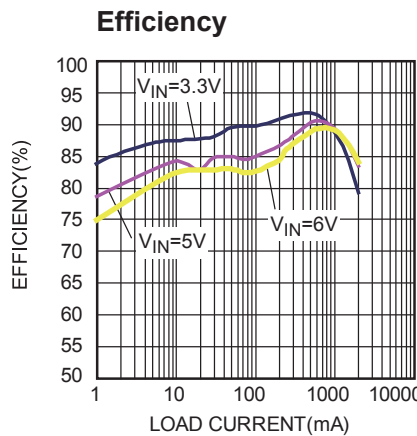
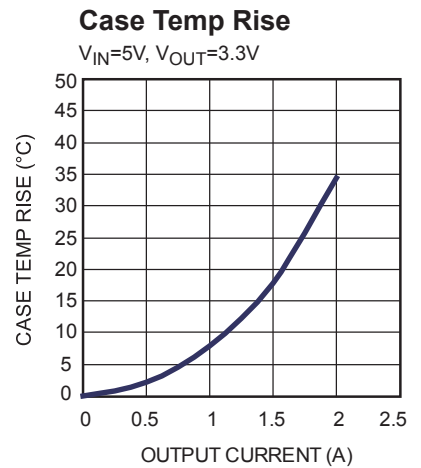
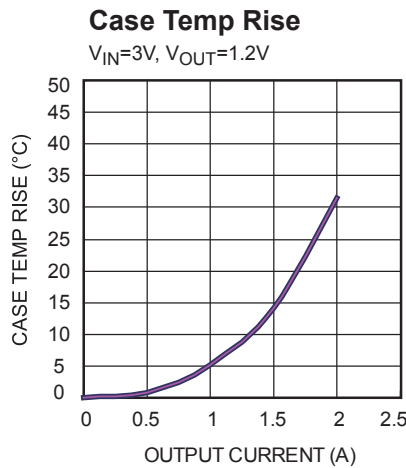
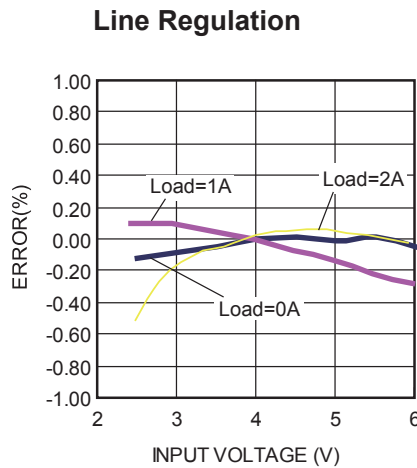
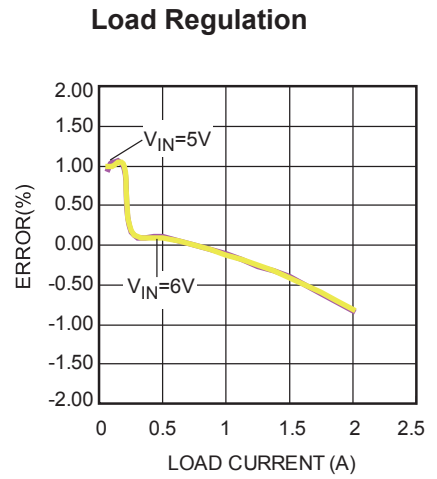
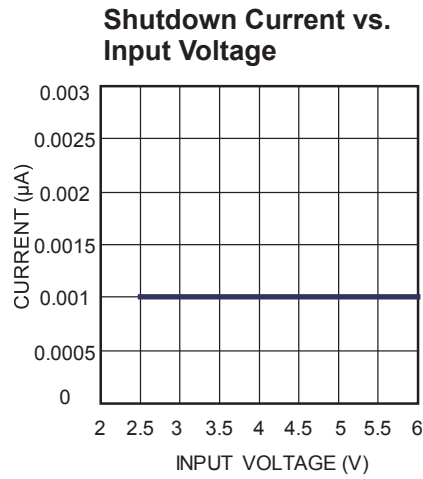
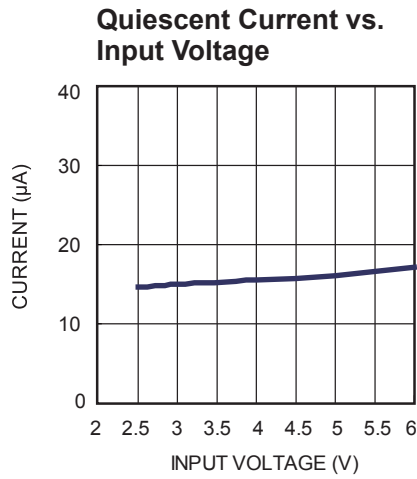
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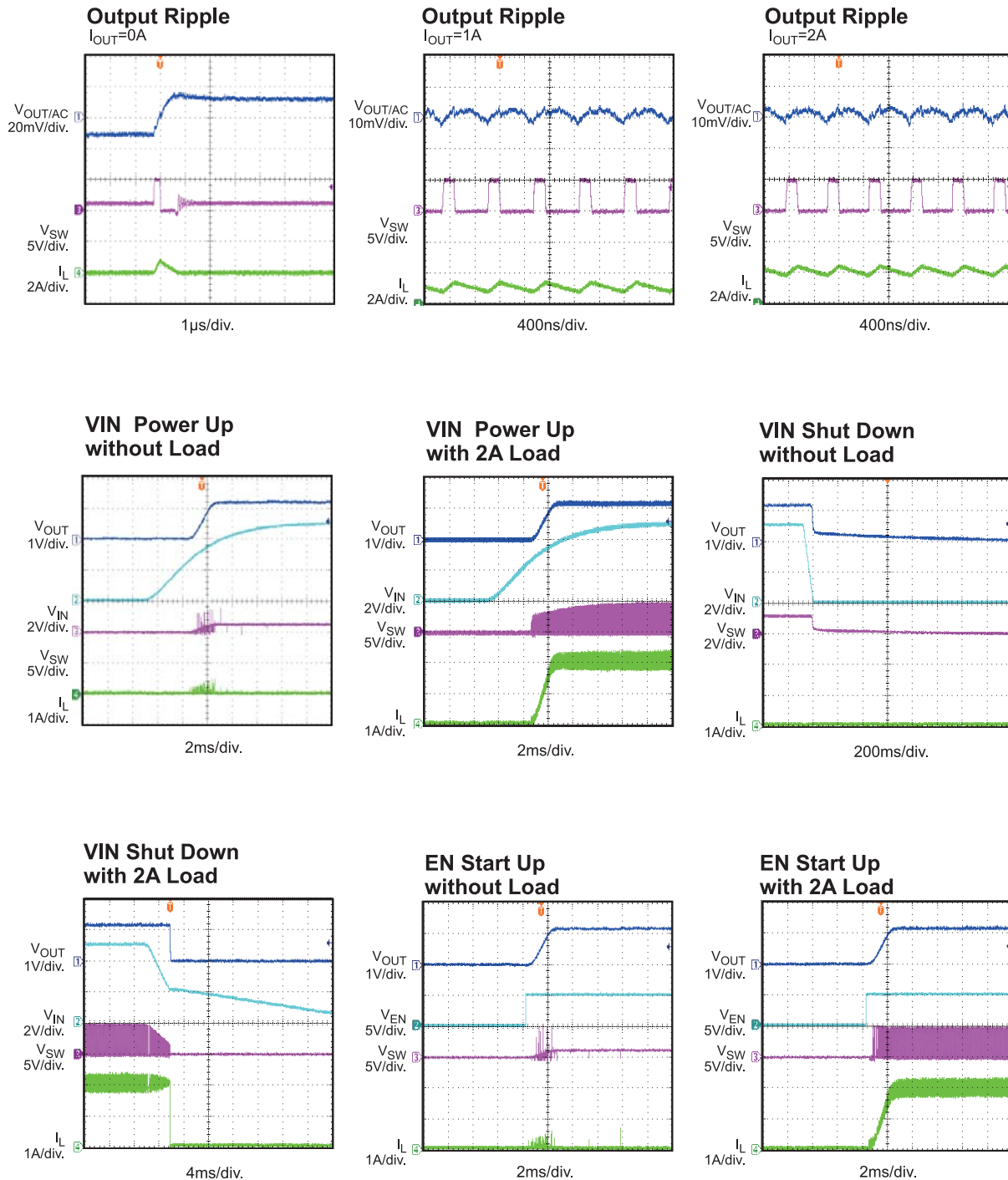
5) Guaranteed by design.

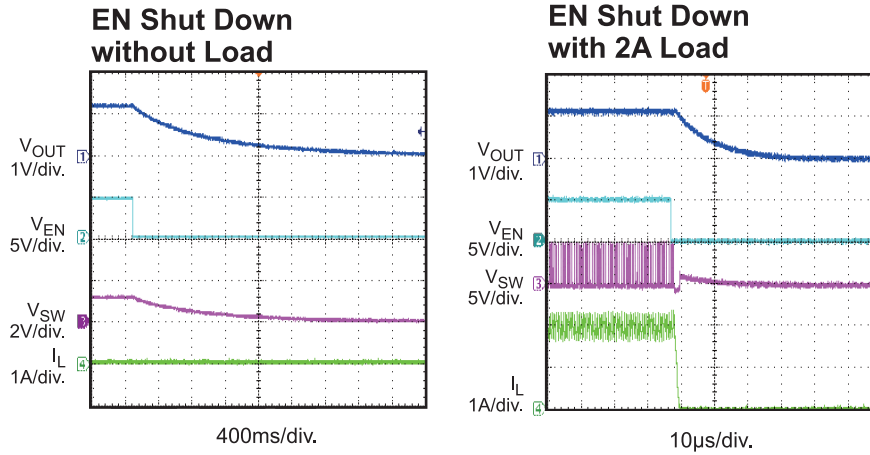
6) Guaranteed by characterization test.

## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 5V$ ,  $V_{OUT} = 1.2V$ ,  $L = 1.0\mu H$ ,  $T_A = +25^\circ C$ , unless otherwise noted.

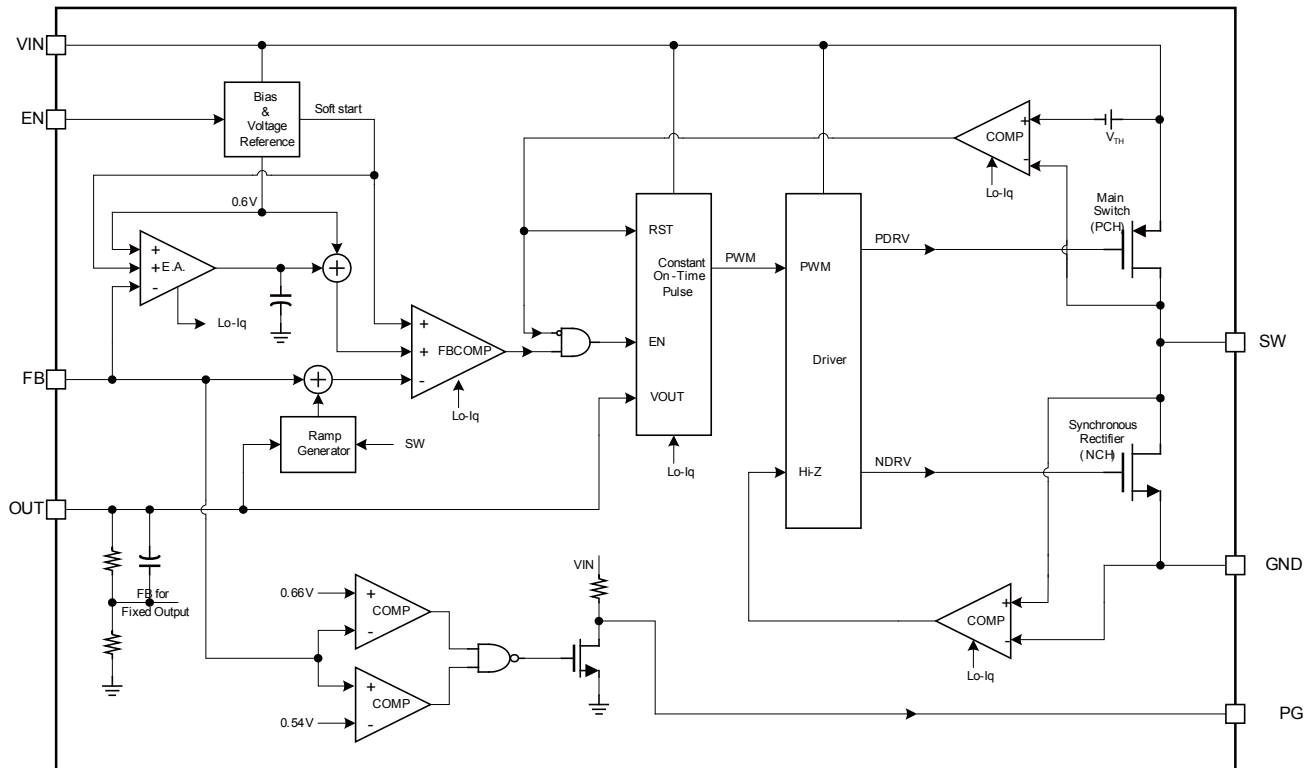


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**
 $V_{IN} = 5V, V_{OUT} = 1.2V, L = 1.0\mu H, T_A = +25^\circ C$ , unless otherwise noted.


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 $V_{IN} = 5V, V_{OUT} = 1.2V, L = 1.0\mu H, T_A = +25^\circ C$ , unless otherwise noted


## PIN FUNCTIONS

Pin #	Name	Description
1	PG	Power Good Indicator. The output of this pin is an open drain with internal pull up resistor to VIN. PGOOD is pulled up to VIN when the FB voltage is within 10% of the regulation level, if FB voltage is out of that regulation range, it is LOW.
2	VIN	Supply Voltage. The MP2161 operates from a +2.5V to +6V unregulated input. C1 is needed to prevent large voltage spikes from appearing at the input.
3	SW	Switch Output
4	PGND	Power ground
5	OUT	Input sense pin for output voltage
6	AGND	Analogy ground for internal control circuit
7	FB	Feedback pin. An external resistor divider from the output to GND, tapped to the FB pin, sets the output voltage.
8	EN	On/Off Control

**BLOCK DIAGRAM**

**Figure 1: MP2161 Block Diagram**



## OPERATION

MP2161 uses constant on-time control with input voltage feed forward to stabilize the switching frequency over full input range. At light load, MP2161 employs a proprietary control of low side switch and inductor current to eliminate ringing on switching node and improve efficiency.

### Constant On-time Control

Compare to fixed frequency PWM control, constant on-time control offers the advantage of simpler control loop and faster transient response. By using input voltage feed forward, MP2161 maintains a nearly constant switching frequency across input and output voltage range. The on-time of the switching pulse can be estimated as:

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 0.667\mu s$$

To prevent inductor current run away during load transient, MP2161 fixes the minimum off time to be 60ns. However, this minimum off time limit will not affect operation of MP2161 in steady state in any way.

### Light Load Operation

In light load condition, MP2161 uses a proprietary control scheme to save power and improve efficiency. The MP2161 will turn off the low side switch when inductor current starts to reverse. Then MP2161 works in discontinuous conduction mode (DCM) operation.

The DCM mode happens only after low side switch turned off by ZCD circuit. Considering the ZCD circuit propagation time, the typical delay is 30ns. It means the inductor current still fall after the ZCD is trigger during this delay. If the inductor current falling slew rate is fast ( $V_o$  voltage is high or close to  $V_{in}$ ), the low side MOSFET is turned off at the moment inductor current may be negative. This phenomena will cause MP2161 can not enter DCM operation. If the DCM mode is required, the off time of low side MOSFET in CCM should be longer than 60ns. It means the maximum duty is 90% to guarantee DCM mode at light load.

For example,  $V_{IN}$  is 3.4V and  $V_{OUT}$  is 3.3V, the off time in CCM is 20ns. It is difficult to enter

DCM at light load. And using smaller inductor can improve it and make it enter DCM easily.

### Enable

When input voltage is greater than the under-voltage lockout threshold (UVLO), typically 2.3V, MP2161 can be enabled by pulling EN pin to higher than 1.2V. Leaving EN pin float or pull down to ground will disable MP2161. There is an internal 1Meg Ohm resistor from EN pin to ground.

### Soft Start

MP2161 has built-in soft start that ramps up the output voltage in a controlled slew rate, avoiding overshoot at startup. The soft start time is about 1.5ms typical.

### Power GOOD Indicator

MP2161 has an open drain with 550kΩ pull-up resistor pin for power good indicator PGOOD. When FB pin is within +/-10% of regulation voltage, i.e. 0.6V, PGOOD pin is pulled up to  $V_{IN}$  by the internal resistor. If FB pin voltage is out of the +/-10% window, PGOOD pin is pulled down to ground by an internal MOS FET. The MOS FET has a maximum  $R_{dson}$  of less than 100 Ohm.

### Current limit

MP2161 has a typical 3.2A current limit for the high side switch. When the high side switch hits current limit, MP2161 will touch the hiccup threshold until the current lower down. This will prevent inductor current from continuing to build up which will result in damage of the components.

### Short Circuit and Recovery

MP2161 enters short circuit protection mode also when the current limit is hit, and tries to recover from short circuit with hiccup mode. In short circuit protection, MP2161 will disable output power stage, discharge soft-start cap and then automatically try to soft-start again. If the short circuit condition still holds after soft-start ends, MP2161 repeats this operation cycle till short circuit disappears and output rises back to regulation level.

## APPLICATION INFORMATION

### COMPONENT SELECTION

#### Setting the Output Voltage

The external resistor divider is used to set the output voltage (see Typical Application on page 1). The feedback resistor R1 can not be too large neither too small considering the trade-off for stability and dynamic. Choose R1 to be around 120kΩ to 200kΩ. R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{out}}{0.6} - 1}$$

The feedback circuit is shown as Figure 2.



**Figure 2: Feedback Network**

Table 1 lists the recommended resistors value for common output voltages.

**Table 1—Resistor Selection for Common Output Voltages**

V <sub>OUT</sub> (V)	R1 (kΩ)	R2 (kΩ)
1.0	200(1%)	300(1%)
1.2	200(1%)	200(1%)
1.8	200(1%)	100(1%)
2.5	200(1%)	63.2(1%)
3.3	200(1%)	44.2(1%)

#### Selecting the Inductor

A 0.68μH to 2.2μH inductor is recommended for most applications. For highest efficiency, the inductor DC resistance should be less than 15mΩ. For most designs, the inductance value can be derived from the following equation.

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI<sub>L</sub> is the inductor ripple current.

Choose inductor current to be approximately 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

#### Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 10μF capacitor is sufficient. For higher output voltage, 47μF may be needed for more stable system.

Since the input capacitor absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worse case condition occurs at V<sub>IN</sub> = 2V<sub>OUT</sub>, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose the input capacitor whose RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small and high quality ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_s \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

### Selecting the Output Capacitor

The output capacitor (C2) is required to maintain the DC output voltage. Ceramic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_s \times C2}\right)$$

Where  $L_1$  is the inductor value and  $R_{ESR}$  is the equivalent series resistance (ESR) value of the output capacitor.

Using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_s^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

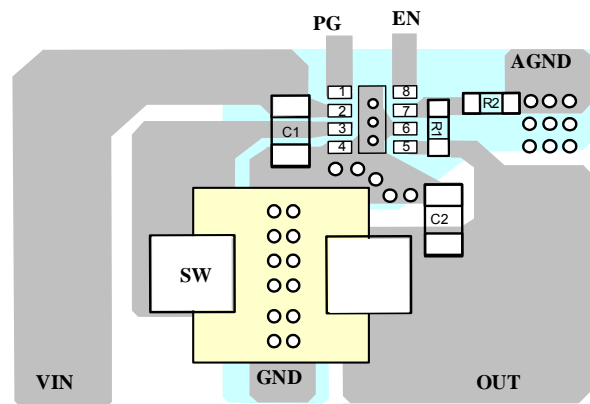
$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system.

### PCB Layout

Proper layout of the switching power supplies is very important, and sometimes critical for proper function. For the high-frequency switching converter, poor layout design can result in poor line or load regulation and stability issues.

The high current paths (GND, IN and SW) should be placed very close to the device with short, direct and wide traces. The input capacitor needs to be as close as possible to the IN and GND pins. The external feedback resistors should be placed next to the FB pin. Keep the switching node SW short and away from the feedback network.



**Figure 3: PCB Layout Recommendation**

### Design Example

Below is a design example following the application guidelines for the specifications:

**Table 2: Design Example**

$V_{IN}$	5V
$V_{OUT}$	1.2V
$f_{sw}$	1500kHz

The detailed application schematic is shown in Figure 4. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more device applications, please refer to the related Evaluation Board Datasheets.

TYPICAL APPLICATION CIRCUITS

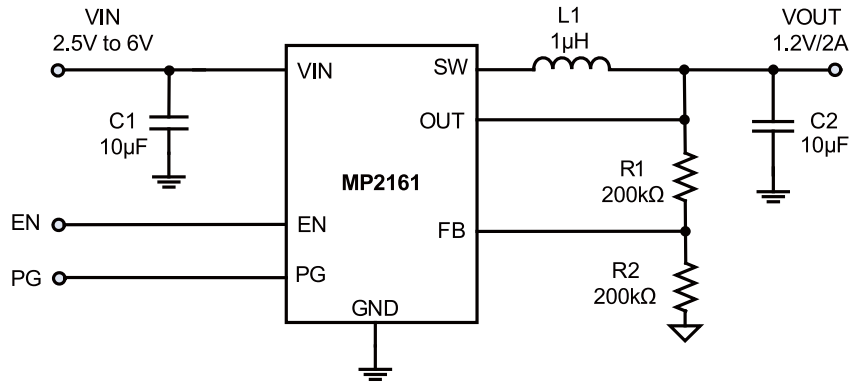
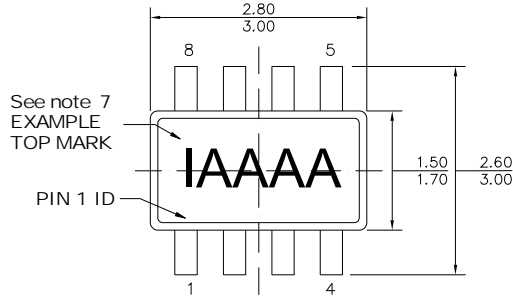
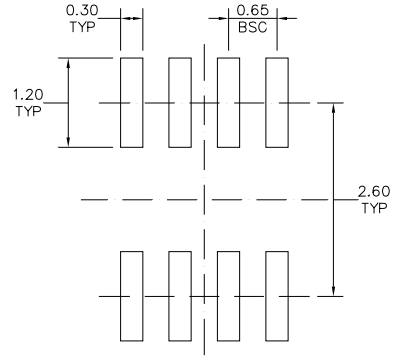
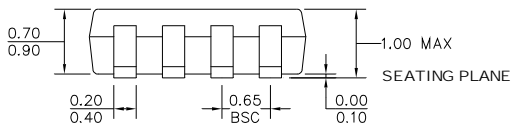
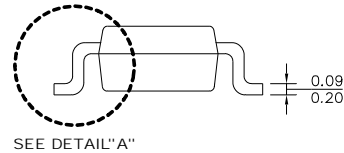
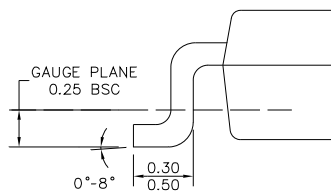


Figure 4: Typical Application Circuit

**PACKAGE INFORMATION**
**TSOT23-8**

**TOP VIEW**

**RECOMMENDED LAND PATTERN**

**FRONT VIEW**

**SIDE VIEW**

**DETAIL "A"**
**NOTE:**

- 1) ALL DIMENSIONS ARE IN MILLIMETERS
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX
- 5) JEDEC REFERENCE IS MQ193, VARIATION BA
- 6) DRAWING IS NOT TO SCALE
- 7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

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