# MP1921B

## 100V, 2.5A, High-Frequency Half-Bridge Gate Driver

## DESCRIPTION

The MP1921B is a high-frequency 100V half-bridge N-channel power MOSFET driver. Its low-side and high-side driver channels are independently controlled and matched, with a time delay of less than 5ns. Under-voltage lockout on both high-side and low-side supplies force their outputs low in case of insufficient supply. The integrated bootstrap diode reduces external component count.

## FEATURES

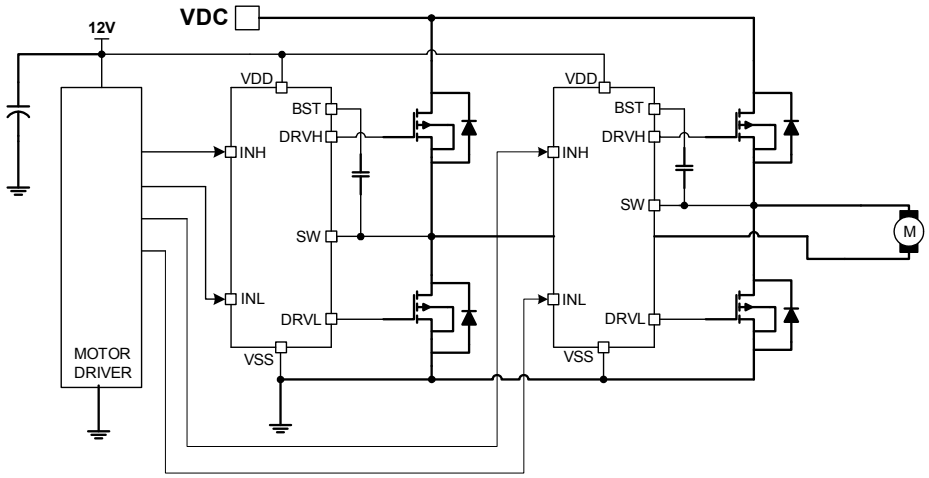
- Drives N-Channel MOSFET Half-Bridge
- 120V $V_{BST}$ Voltage Range
- On-Chip Bootstrap Diode
- Typical 16ns Propagation Delay Time
- Less Than 5ns Gate Drive Matching
- Drives 1nf Load with 12ns/9ns Rise/Fall Times with 12V VDD
- TTL Compatible Input
- Less Than 150μA Quiescent Current
- UVLO for Both High Side and Low Side
- In QFN10 (3mmx3mm) Package

## APPLICATIONS

- Telecom Half-Bridge Power Supplies
- Avionics DC/DC Converters
- Two-Switch Forward Converters
- Active-Clamp Forward Converters
- DC Motor Drivers



## TYPICAL APPLICATION



## ORDERING INFORMATION

| Part Number* | Package | Top Marking |
|---|---|---|
| MP1921GQ-B | QFN10 (3mmx3mm) | *See Below* |

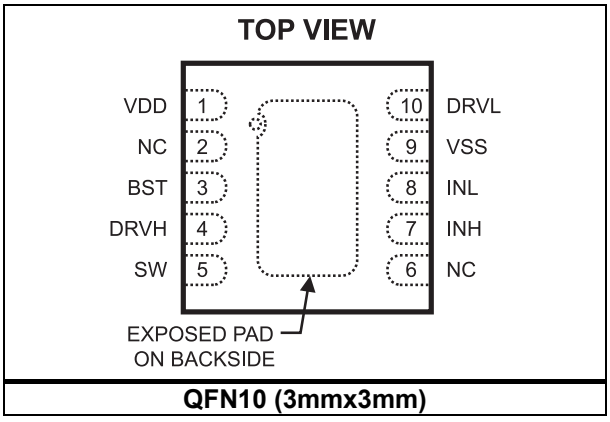
* For Tape & Reel, add suffix –Z (e.g. MP1921GQ-B–Z).

## TOP MARKING

BLDY
LLL

BLD: Product code of MP1921GQ-B
Y: Year code
LLL: Lot number

## PACKAGE REFERENCE




QFN10 (3mmx3mm)

## PIN FUNCTIONS

| QFN10 (3x3mm) | Name | Description |
|---|---|---|
| 1 | VDD | **Supply input.** VDD supplies power to all the internal circuitry. A decoupling capacitor to ground must be placed close to VDD to ensure stable and clean supply. |
| 2,6 | NC | **No connection.** |
| 3 | BST | **Bootstrap.** This is the positive power supply for the internal floating high-side MOSFET driver. Connect a bypass capacitor between BST and SW. |
| 4 | DRVH | **Floating driver output.** |
| 5 | SW | **Switching node.** |
| 7 | INH | **Control signal input for the floating driver.** |
| 8 | INL | **Control signal input for the low-side driver.** |
| 9 | VSS, Exposed Pad | **Chip ground.** Connect exposed pad to VSS for proper thermal operation. |
| 10 | DRVL | **Low-side driver output.** |

## ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage ($V_{DD}$) ..... -0.3V to +20V
SW voltage ($V_{SW}$) ..... -5.0V to +105V
BST voltage ($V_{BST}$) ..... -0.3V to +120V
BST to SW ..... -0.3V to +18V
DRVH to SW..... -0.3V (-5V for <100ns) to (BST-SW) + 0.3V
DRVL to VSS ..... -0.3V to (VDD + 0.3V)
All other pins ..... -0.3V to ($V_{DD}$ + 0.3V)
Continuous power dissipation..... ($T_A$ =25°C) (2)
QFN10 (3mmx3mm) ..... 2.5W
Junction temperature ..... 150°C
Lead temperature..... 260°C
Storage temperature ..... -65°C to +150°C

## *Recommended Operating Conditions* (3)

Supply voltage ($V_{DD}$) ..... 9.0V to 18V
SW voltage ($V_{SW}$) ..... -1.0V to +100V
SW slew rate ..... <50V/ns
Operating junction temp ($T_J$)..... -40°C to +125°C

| *Thermal Resistance* (4) | $\theta_{JA}$ | $\theta_{JC}$ | |
|---|---|---|---|
| QFN10 (3mmx3mm) | 50 | 12 | °C/W |

**Notes:**

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$(MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$(MAX) = ($T_J$(MAX) - $T_A$) / $\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

**$V_{DD}$ = $V_{BST}$-$V_{SW}$ = 12V, $V_{SS}$ = $V_{SW}$ = 0V, no load at DRVH and DRVL, $T_A$ = 25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Supply Currents** | | | | | | |
| VDD quiescent current | $I_{DDQ}$ | INL = INH = 0 | | 100 | 150 | µA |
| VDD operating current | $I_{DDO}$ | $f_{sw}$ = 500kHz | | 2.8 | 3.5 | mA |
| Floating driver quiescent current | $I_{BSTQ}$ | INL = INH = 0 | | 60 | 90 | µA |
| Floating driver operating current | $I_{BSTO}$ | $f_{sw}$ = 500kHz | | 2.1 | 3 | mA |
| Leakage current | $I_{LK}$ | BST = SW = 100V | | 0.05 | 1 | µA |
| **Inputs** | | | | | | |
| INL/INH high | | | | 2 | 2.4 | V |
| INL/INH low | | | 1 | 1.4 | | V |
| INL/INH internal pull-down resistance | $R_{IN}$ | | | 185 | | kΩ |
| **Under-Voltage Protection** | | | | | | |
| VDD rising threshold | $V_{DDR}$ | | 7.7 | 8.1 | 8.5 | V |
| VDD hysteresis | $V_{DDH}$ | | | 0.5 | | V |
| (BST-SW) rising threshold | $V_{BSTR}$ | | 6.7 | 7.1 | 7.5 | V |
| (BST-SW) hysteresis | $V_{BSTH}$ | | | 0.55 | | V |
| **Bootstrap Diode** | | | | | | |
| Bootstrap diode VF @ 100µA | $V_{F1}$ | | | 0.5 | | V |
| Bootstrap diode VF @ 100mA | $V_{F2}$ | | | 0.9 | | V |
| Bootstrap diode dynamic R | $R_D$ | @ 100mA | | 2.5 | | Ω |
| **Low-Side Gate Driver** | | | | | | |
| Low-level output voltage | $V_{OLL}$ | $I_O$ = 100mA | | 0.15 | 0.22 | V |
| High-level output voltage to rail | $V_{OHL}$ | $I_O$ = -100mA | | 0.45 | 0.6 | V |
| Peak pull-up current | $I_{OHL}$ | $V_{DRVL}$ = 0V, $V_{DD}$ = 12V | | 1.5 | | A |
| | | $V_{DRVL}$ = 0V, $V_{DD}$ = 16V | | 2.5 | | A |
| Peak pull-down current | $I_{OLL}$ | $V_{DRVL}$ = $V_{DD}$ = 12V | | 2.5 | | A |
| | | $V_{DRVL}$ = $V_{DD}$ = 16V | | 3.5 | | A |
| **Floating Gate Driver** | | | | | | |
| Low-level output voltage | $V_{OLH}$ | $I_O$ = 100mA | | 0.15 | 0.22 | V |
| High-level output voltage to rail | $V_{OHH}$ | $I_O$ = -100mA | | 0.45 | 0.6 | V |
| Peak pull-up current | $I_{OHH}$ | $V_{DRVH}$ = 0V, $V_{DD}$ = 12V | | 1.5 | | A |
| | | $V_{DRVH}$ = 0V, $V_{DD}$ = 16V | | 2.5 | | A |
| Peak pull-down current | $I_{OLH}$ | $V_{DRVH}$ = $V_{DD}$ = 12V | | 2.5 | | A |
| | | $V_{DRVH}$ = $V_{DD}$ = 16V | | 3.5 | | A |

## ELECTRICAL CHARACTERISTICS *(continued)*

**$V_{DD}$ = $V_{BST}$-$V_{SW}$ = 12V, $V_{SS}$ = $V_{SW}$ = 0V, no load at DRVH and DRVL, $T_A$ = 25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Switching Spec. – Low Side Gate Driver** | | | | | | |
| Turn-off propagation delay INL falling to DRVL falling | $T_{DLFF}$ | | | 16 | | ns |
| Turn-on propagation delay INL rising to DRVL rising | $T_{DLRR}$ | | | 16 | | |
| DRVL rise time | | $C_L$ = 1nF | | 12 | | ns |
| DRVL fall time | | $C_L$ = 1nF | | 9 | | ns |
| **Switching Spec. – Floating Gate Driver** | | | | | | |
| Turn-off propagation delay INL falling to DRVH falling | $T_{DHFF}$ | | | 16 | | ns |
| Turn-on propagation delay INL rising to DRVH rising | $T_{DHRR}$ | | | 16 | | ns |
| DRVH rise time | | $C_L$ = 1nF | | 12 | | ns |
| DRVH fall time | | $C_L$ = 1nF | | 9 | | ns |
| **Switching Spec. – Matching** | | | | | | |
| Floating driver turn-off to low side drive turn-on | $T_{MON}$ | | | 1 | 5 | ns |
| Low side driver turn-off to floating driver turn-on | $T_{MOFF}$ | | | 1 | 5 | ns |
| Minimum input pulse width that changes the output | $T_{PW}$ | | | | 50 (5) | ns |
| Bootstrap diode turn-on or turn-off time | $T_{BS}$ | | | 10 (5) | | ns |

**Note:**
5) Guaranteed by design.

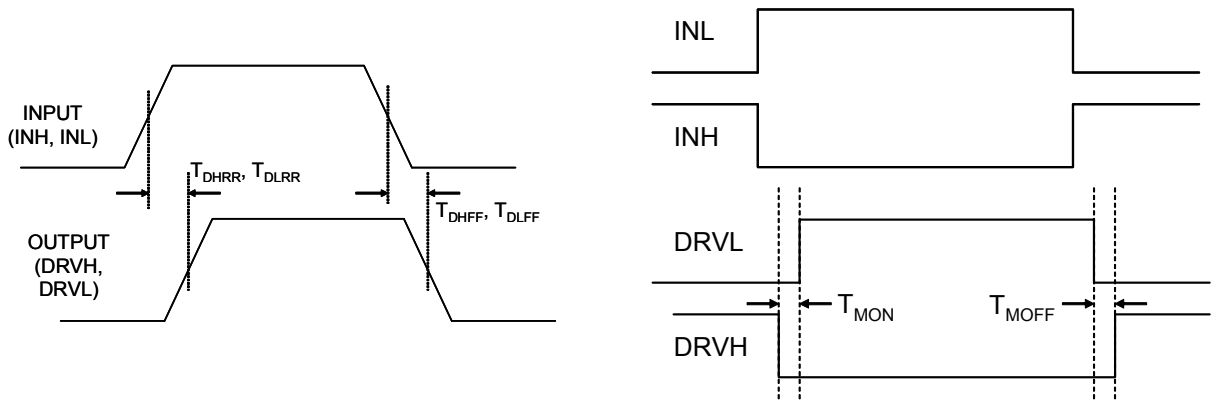
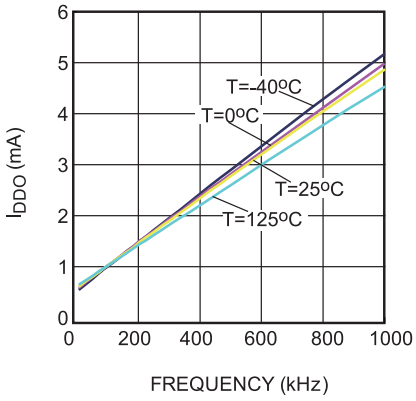



**Figure 1: Timing Diagram**

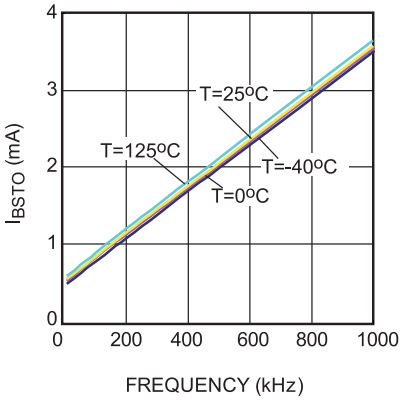
## TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{DD}$ = 12V, $V_{SS}$ = $V_{SW}$ = 0V, $T_A$ = 25°C, unless otherwise noted.**

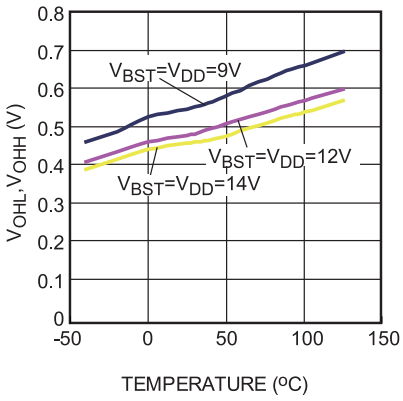
### $I_{DDO}$ Operation Current vs. Frequency



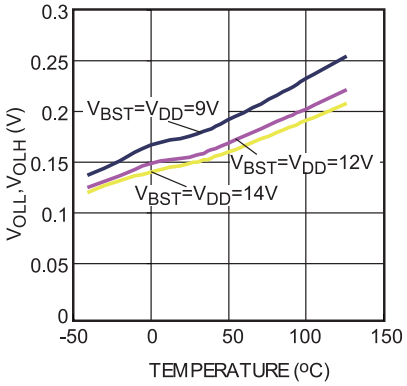

### $I_{BSTO}$ Operation Current vs. Frequency



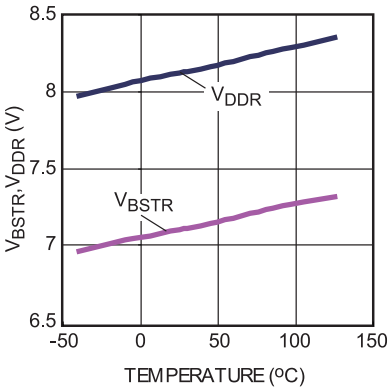

### High Level Output Voltage vs.Temperature



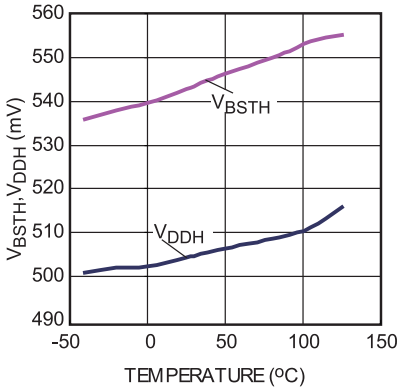

### Low Level Output Voltage vs. Temperature



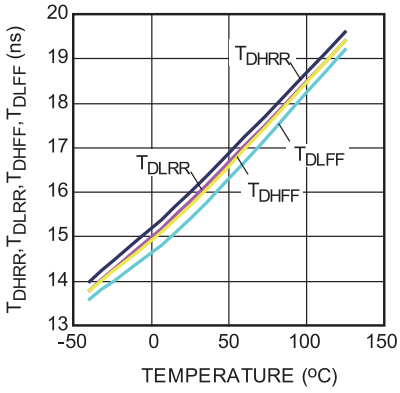

### Undervoltage Lockout Threshold vs.Temperature



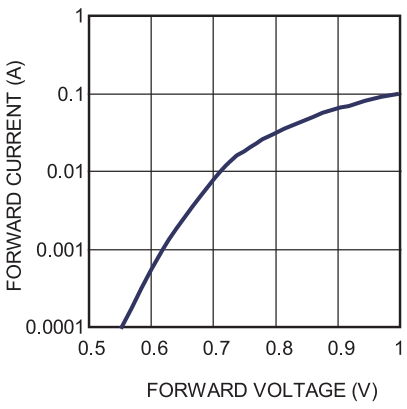

### Undervoltage Lockout Hysteresis vs.Temperature



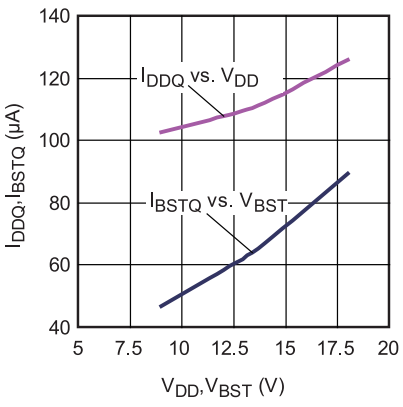

### Propagation Delay vs. Temperature




### Bootstrap Diode I-V Characteristics



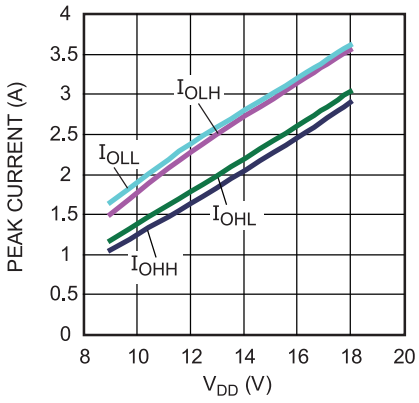

### Quiescent Current vs. Voltage



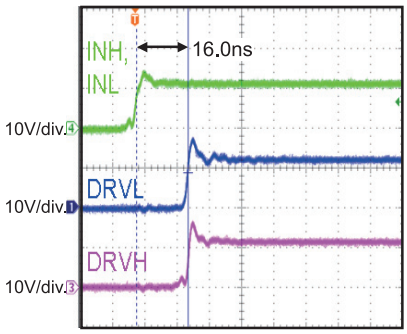
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{DD}$ = 12V, $V_{SS}$ = $V_{SW}$ = 0V, $T_A$ = 25°C, unless otherwise noted.**

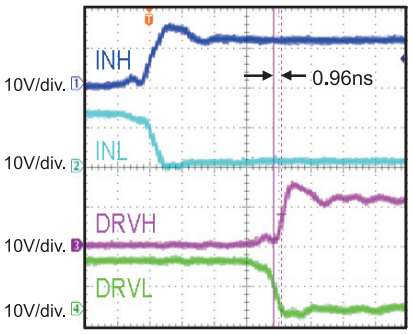
### Peak Current vs. $V_{DD}$ Voltage



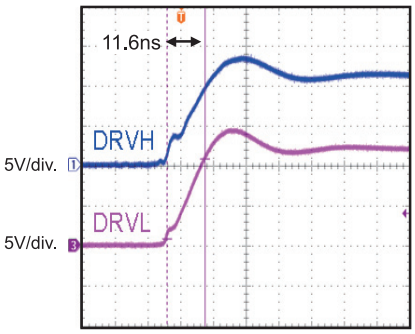

### Turn-On Propagation Delay



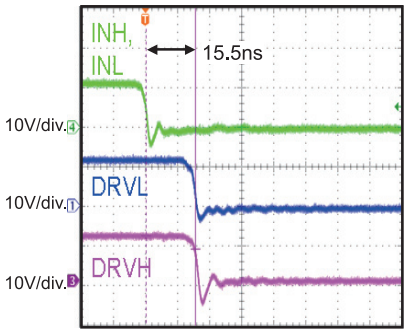

### Gate Drive Matching $T_{MOFF}$



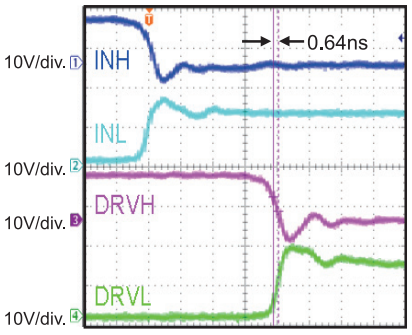

### Drive Rise Time (1nF Load)



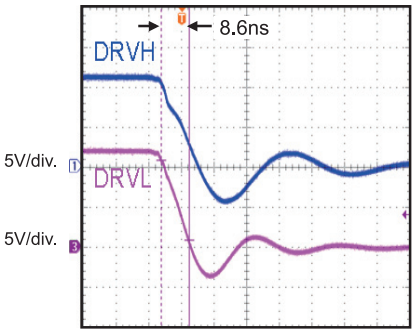

### Turn-Off Propagation Delay




### Gate Drive Matching $T_{MON}$




### Drive Fall Time (1nF Load)



## BLOCK DIAGRAM

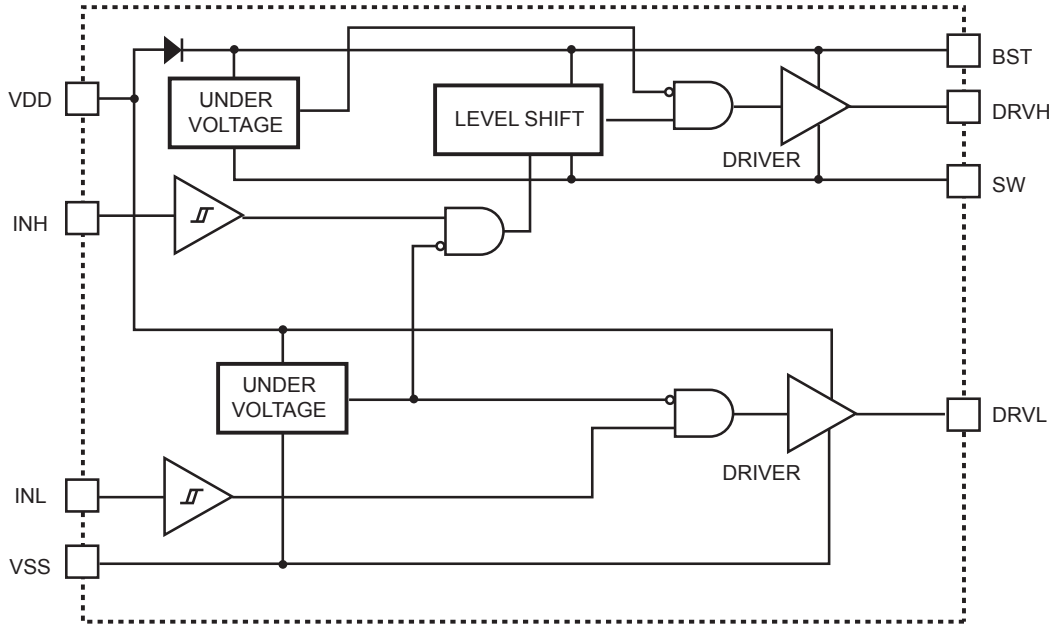



**Figure 2: Function Block Diagram**

## APPLICATION

The INH and INL input signals can be controlled independently. If both INH and INL are controlling the HS-FET and LS-FET of the same bridge, then users must avoid shoot-through by setting a sufficient dead time between INH and INL low, and vice versa (see Figure 3). Dead time is the time interval between INH low and INL low.

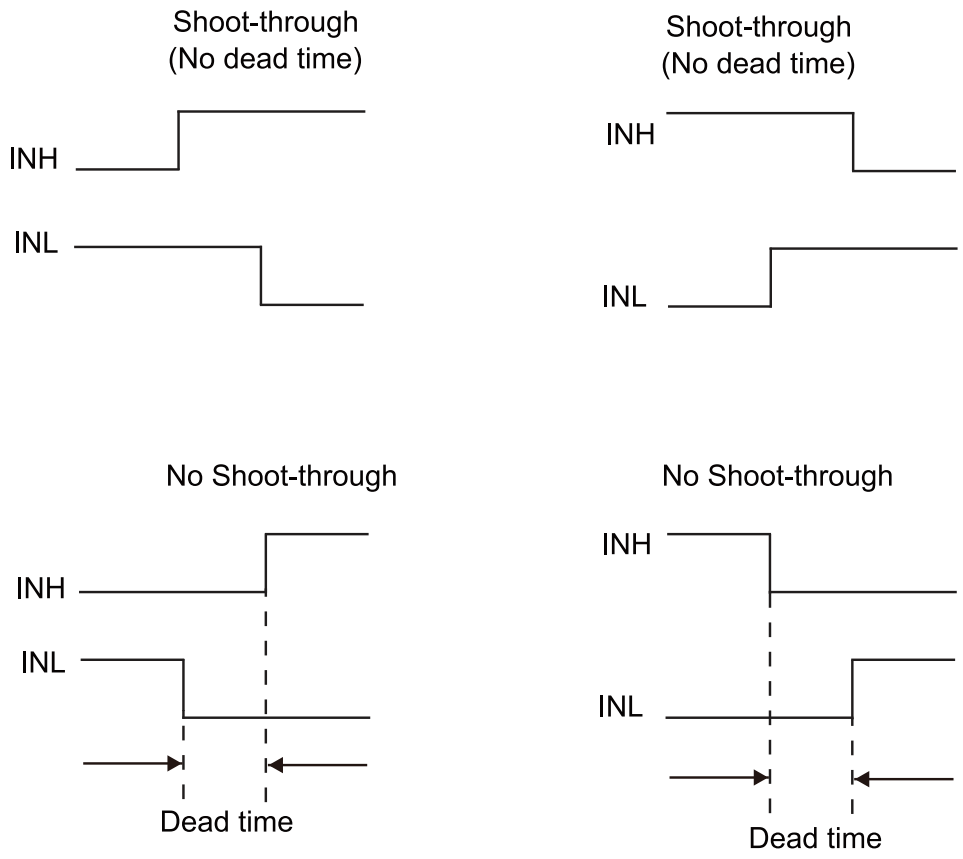



**Figure 3: Short-Through Timing Diagram**

# REFERENCE DESIGN CIRCUITS

### Half-Bridge Converter

In half-bridge converter topology, the MOSFETs are driven alternately with dead time. Therefore, INH and INL are driven with alternating signals from the PWM controller (see Figure 4). Input voltage can be up to 100V in this application.

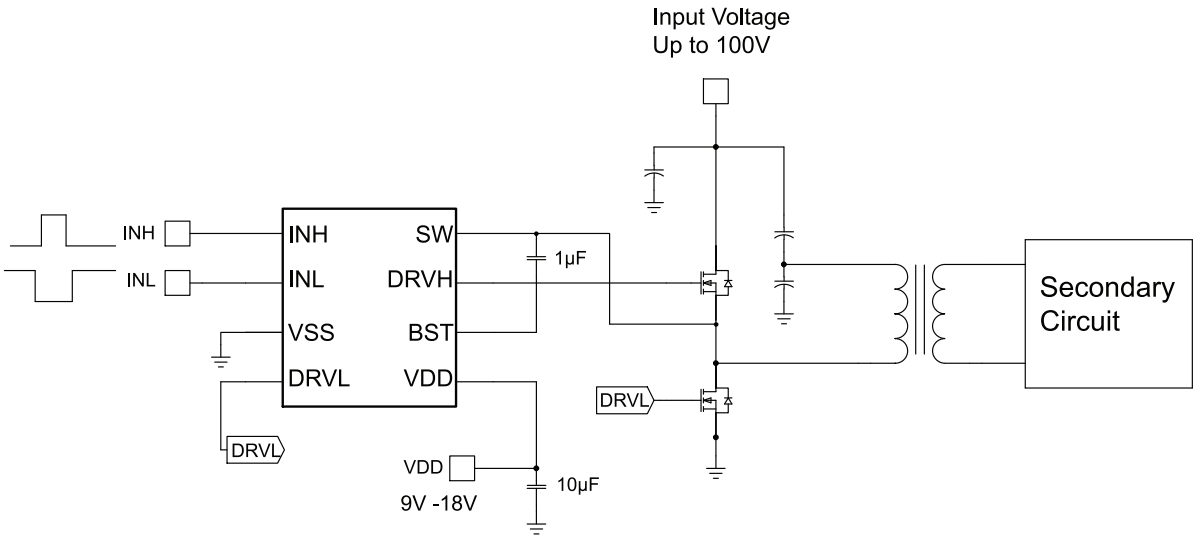



**Figure 4: Half-Bridge Converter**

### Two-Switch Forward Converter

In two-switch forward converter topology, both MOSFETs are turned on and off together. The input signal (INH and INL) comes from the PWM controller, which senses the output voltage and output current if current-mode control is used (see Figure 5). The Schottky diodes clamp the reverse swing of the power transformer, and must be rated at the input voltage. Input voltage can be up to 100V in this circuit.

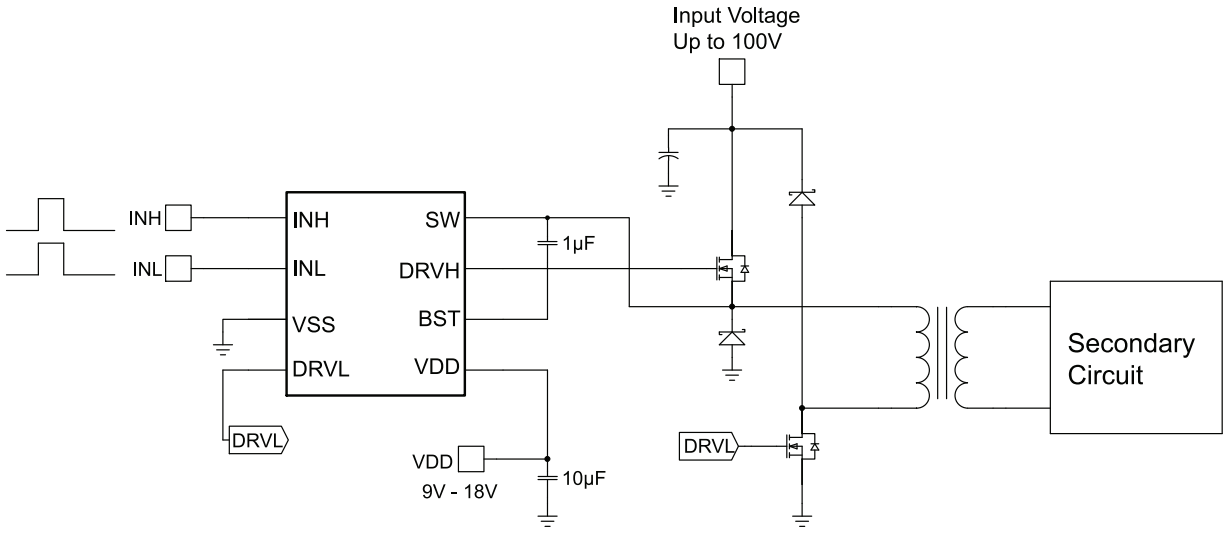



**Figure 5: Two-Switch Forward Converter**

### Active-Clamp Forward Converter

In active-clamp forward converter topology, the MOSFETs are driven alternately. The high-side MOSFET, along with capacitor $C_{reset}$, is used to reset the power transformer in a lossless manner. This topology lends itself well to run at duty cycles exceeding 50%. For these reasons, the input voltage may not be able to run at 100V for this application.

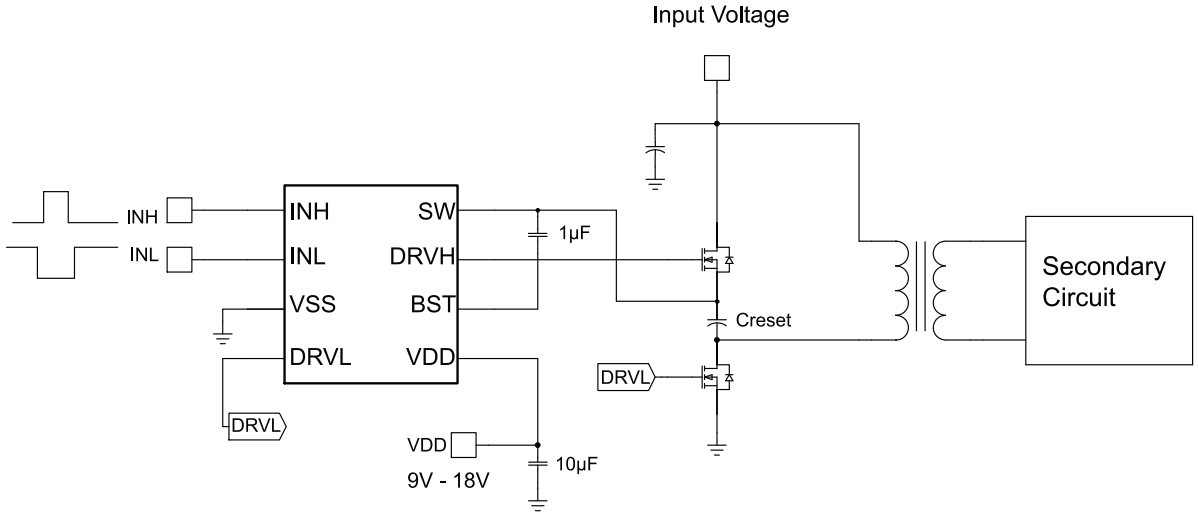
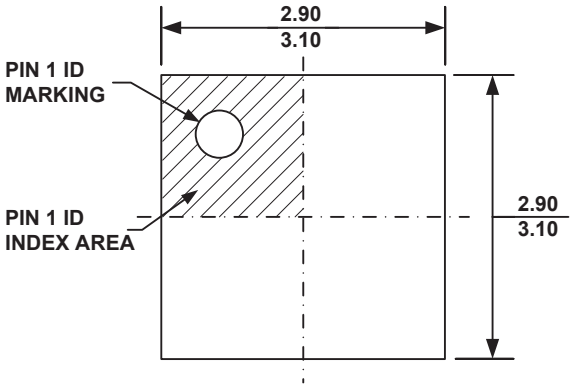


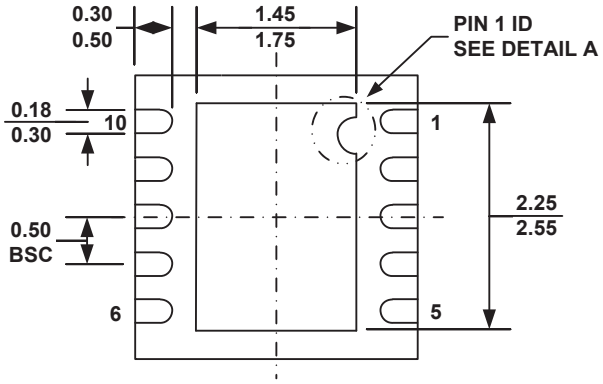

**Figure 6: Active-Clamp Forward Converter**

## PACKAGE INFORMATION

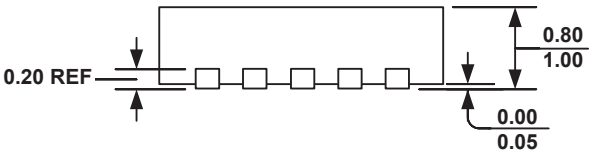
**QFN10 (3mm×3mm)**



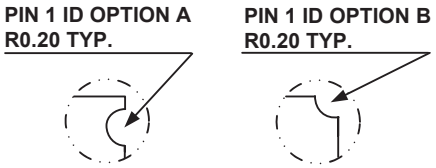

**TOP VIEW**



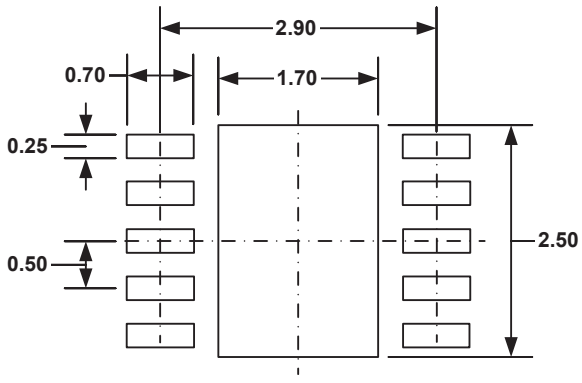

**BOTTOM VIEW**




**SIDE VIEW**




**DETAIL A**




**RECOMMENDED LAND PATTERN**

**NOTE:**

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
5) DRAWING IS NOT TO SCALE.