MP1720

2.7W Mono Class D Low-EMI High-Efficiency Audio Amplifier

The Future of Analog IC Technology

DESCRIPTION

The MP1720 is a high efficiency Class-D audio amplifier. It utilizes a full bridge output structure capable of delivering 2.7W into 4Ω speaker. This device exhibits the high fidelity of a class AB amplifier with an efficiency of 90% which dramatically reduces solution size by integrating the following:

- 250mΩ power MOSFETs (V_{IN} =3.3V)
- Startup / Shutdown pop elimination
- Short circuit /Thermal overload Protection

The MP1720 features a pin-selectable 1MHz or 1.3MHz frequency control or can be synchronized to an external clock source. The flexible switching frequency and internal EMI-reduction scheme eliminates the need for an output LC filter and passes emission standards without filter & with considerable cable.

The MP1720 has five fixed gain options. MP1720-3: 3dB; MP1720-6: 6dB; MP1720-9: 9dB; MP1720-12: 12dB; MP1720-216: 21.6dB.

The MP1720 is available in 10-pin MSOP-EP and 10-pin QFN packages.

FEATURES

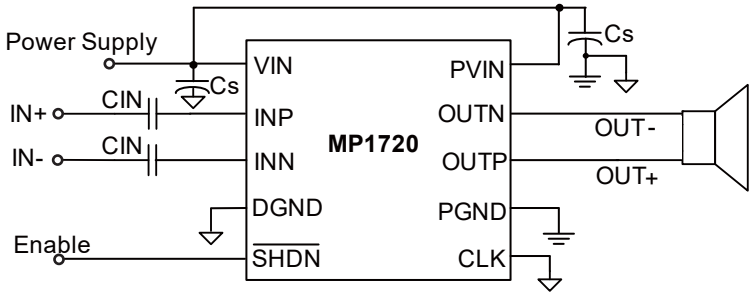
- Passes FCC-Radiated Emissions Standards with 24inch of Cable without output filter
- 2.7W Into 4Ω with 5V VIN @ 10% THD+N
- Up to 90% Efficiency
- Flexible Switching Frequency setting
- Low Noise (53μV Typical) with 3.3V VIN
- 15ms Start-up time Eliminates pop
- Low Quiescent Current (4mA @3.3V)
- Low Shutdown Current (0.1μA)
- Full Bridge Output Drive
- Fully Differential Input
- Short circuit Protection
- Thermal Shutdown

APPLICATIONS

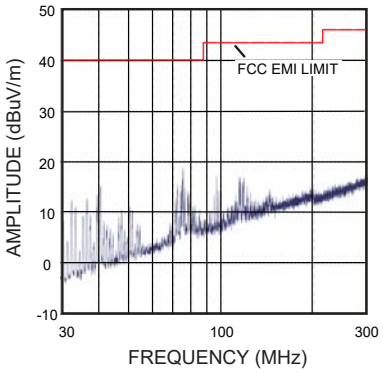
- Cellular Phones
- PDAs
- MP3 Players
- Portable Audio

All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit MPS website under Products, Quality Assurance page.

TYPICAL APPLICATION



EMI Spectrum Diagram
VIN=3.3V, R_{LOAD}=8Ω, no output filter,
CLK=GND, Near field,
6 inch unshielded twisted-pair-speaker cable

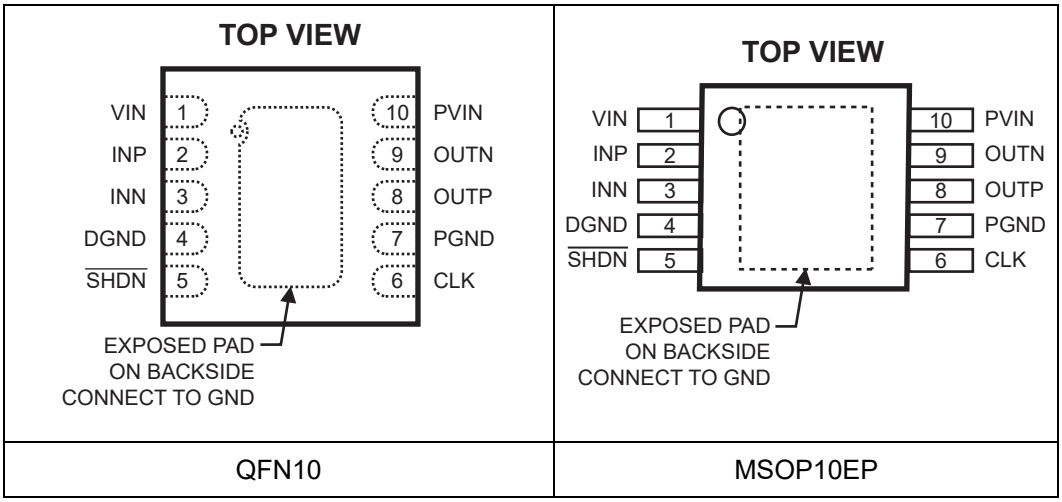


ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
MP1720DQ-3	QFN10 (3mm x 3mm)	6J	-40°C to +85°C
MP1720DQ-6*		7J	
MP1720DQ-9*		8J	
MP1720DQ-12*		9J	
MP1720DQ-216		2K	
MP1720DH-3*	MSOP10EP	1720K	
MP1720DH-6*		1720L	
MP1720DH-9*		1720M	
MP1720DH-12*		1720N	
MP1720DH-216		1720P	

* Contact factory for availability

PACKAGE REFERENCE



QFN10	MSOP10EP

ABSOLUTE MAXIMUM RATINGS (1)

VIN to DGND.....6.0V
PVIN to PGND 6.0V
DGND to PGND .....-0.3V to +0.3V
PVIN to VIN .....-0.3V to +0.3V
All Other Pins to DGND….-0.3V to (VIN + 0.3V)
Continuous Power Dissipation (T_A = +25°C) (2)
QFN10 ..... 2.5W
MSOP10-EP 1.2W
Junction Temperature.....+140°C
Storage Temperature Range ...-65°C to +150°C
Lead Temperature (soldering, 10s) .....+260°C

Recommended Operating Conditions (3)

Supply Voltage VIN.....2.5V to 5.5V
Operating Junct. Temp. (T_J)..... -40°C to +125°C

Thermal Resistance (4)	θ_{JA}	θ_{JC}
3x3 QFN10	50	12 °C/W
MSOP10-EP	105	19 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operation conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

VIN = PVIN = $\overline{SHDN}$=3.3V, DGND = PGND = 0V, CLK = DGND (f_{CLK}=1.0MHz), R_{Load} = ∞, R_{Load} connected between OUT+ and OUT-, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Output Offset Voltage	$\|V_{OS}\|$	Vs=0V, Av=4V/V, V_{IN}=2.5V to 5.5V			± 6	± 80	mV
Power Supply Rejection Ratio	PSRR	V_{IN}=2.5V to 5.5V			-70		dB
Common Mode Rejection Ratio	CMRR	V_{IN}=3.3V, V_{ID}=0.05V, ΔV_{IC}=0.6V			-66		dB
Quiescent Current	I_Q	V_{IN}=5.5V, no load, switching			7		mA
		V_{IN}=3.3V, no load, switching			4	8	
		V_{IN}=2.5V, no load, switching			3.5		
Shut Down Current	I_{ds}	$\overline{SHDN}$ =0, V_{IN}=2.5V to 5.5V			0.1	4	µA
Turn-On Time	t_{ON}				15		ms
Input Equivalent Resistance	R_{INE}			12	21		kΩ
Input Bias Voltage	V_{BIAS}	Either input	MP1720-3	950	995	1035	mV
			MP1720-6	900	940	980	
			MP1720-9	820	860	900	
			MP1720-12	745	784	825	
			MP1720-216	410	465	530	
Voltage Gain	A_V	MP1720-3		1.3	1.4	1.5	V/V
		MP1720-6		1.9	2.0	2.1	
		MP1720-9		2.7	2.85	3.0	
		MP1720-12		3.8	4.0	4.2	
		MP1720-216		11.4	12.0	12.6	
Output Slew Rate	SR	V_{IN}=3.3V			200		V/µs
Rise/Fall Time	t_{RISE},t_{FALL}	10% to 90%			12		ns
Oscillator Frequency	f_{OSC}	CLK = GND			1000		kHz
		CLK = FLOAT			1300		
CLK Frequency Lock Range	F_{CLK}	V_{IN}=2.5V to 5.5V		500		1400	kHz
UVLO					2.25		V
CLK Input Thresholds	V_{CLKH}	V_{IN}=2.5V to 5.5V		2.5			V
	V_{CLKL}					1	
$\overline{SHDN}$ Input Thresholds	V_{SDH}	V_{IN}=2.5V to 5.5V		1.6			V
	V_{SDL}					0.45	
$\overline{SHDN}$ Input Leakage Current	I_{Lkg_SHND}	$\overline{SHDN}$ =6.3V			0.1	±1	µA
CLK Input Current (5)	I_{Lkg_CLK}	Vclk = 0V			-1.25	±10	µA

Notes:

5) CLK has an internal 1MΩ resistor to VREF.

OPERATION CHARACTERISTICS

TEST SET-UP GRAPH, VIN = PVIN = $\overline{SHDN}$=3.3V, DGND = PGND = 0V, CLK = DGND (f_{CLK}=1.0MHz), R_{Load} = 4Ω, Gain=12dB, T_A = +25°C, unless otherwise noted [6].

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Output Power	P_{OUT}	THD+N=1%, R_{Load}=4Ω	V_{IN} =5.0V		2.14		W
			V_{IN} =3.3V		0.87		
			V_{IN} =2.5V		0.48		
		THD+N=10%, R_{Load}=4Ω	V_{IN} =5.0V		2.78		
			V_{IN} =3.3V		1.18		
			V_{IN} =2.5V		0.64		
		THD+N=1%, R_{Load}=8Ω	V_{IN} =5.0V		1.19		W
			V_{IN} =3.3V		0.55		
			V_{IN} =2.5V		0.31		
		THD+N=10%, R_{Load}=8Ω	V_{IN} =5.0V		1.56		
			V_{IN} =3.3V		0.71		
			V_{IN} =2.5V		0.40		
Total Distortion Pulse Noise	THD+N	P_{OUT}=2W,	V_{IN} =5.0V		0.15%		
		P_{OUT}=0.8W	V_{IN}=3.3V		0.13%		
		P_{OUT}=0.4W	V_{IN}=2.5V		0.13%		
Supply Ripple Rejection Ratio[7]	K_{SVR}	f_S=217Hz, V_{Ripple}=300mV_{PP}, input AC-ground	V_{IN}=3.3V		-60		dB
Signal to Noise Ratio	SNR	V_{OUT}=2 V_{RMS} A-weighted	V_{IN}=3.3V		91.3		dB
Output Noise	V_n	V_{IN}=3.3V, f_s=20Hz to 20kHz, input AC-grounded	No weighting		72		μV_{RMS}
			A weighting		53		
Common Mode Rejection Ratio[8]	CMRR	Vic_{RIPPLE}=300mV_{PP}, f_s=1kHz	V_{IN}=3.3V		-62		dB

PIN FUNCTIONS

Pin #	Name	Description
1	VIN	Analog Power Supply
2	INP	Positive differential input
3	INN	Negative differential input
4	DGND	Analog Ground
5	$\overline{\text{SHDN}}$	Shutdown input (drive high to enable the MP1720)
6	CLK	Frequency select and external clock input; CLK=GND: Operate frequency f_{CLK}=1.0MHz CLK=FLOAT: Operate frequency f_{CLK}=1.3MHz CLK=Clocked: Operate frequency f_{CLK}=external clock frequency
7	PGND	Power Ground
8	OUTP	Positive BTL output
9	OUTN	Negative BTL output
10	PVIN	Power Supply
	Thermal Pad	Must be soldered to a ground on PCB

FUNCTIONAL BLOCK DIAGRAM

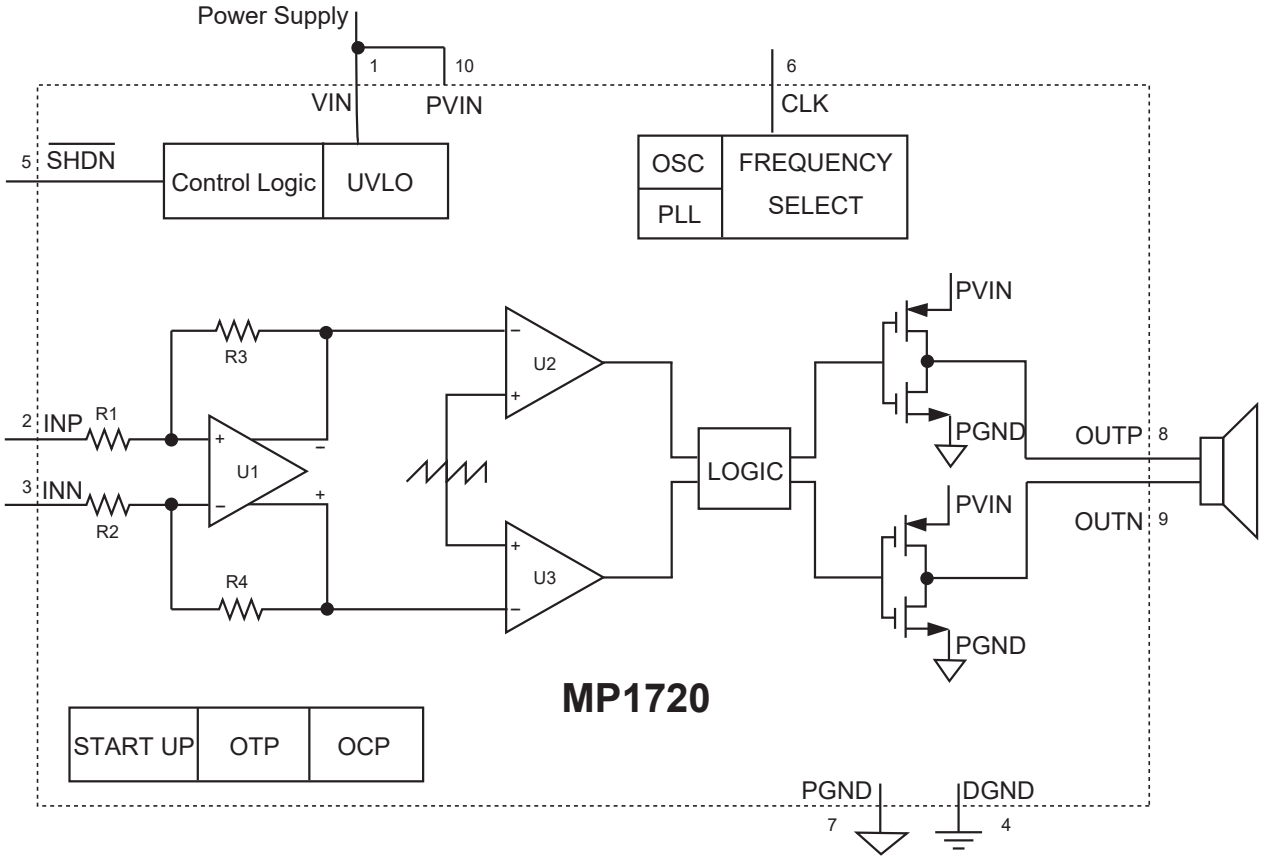
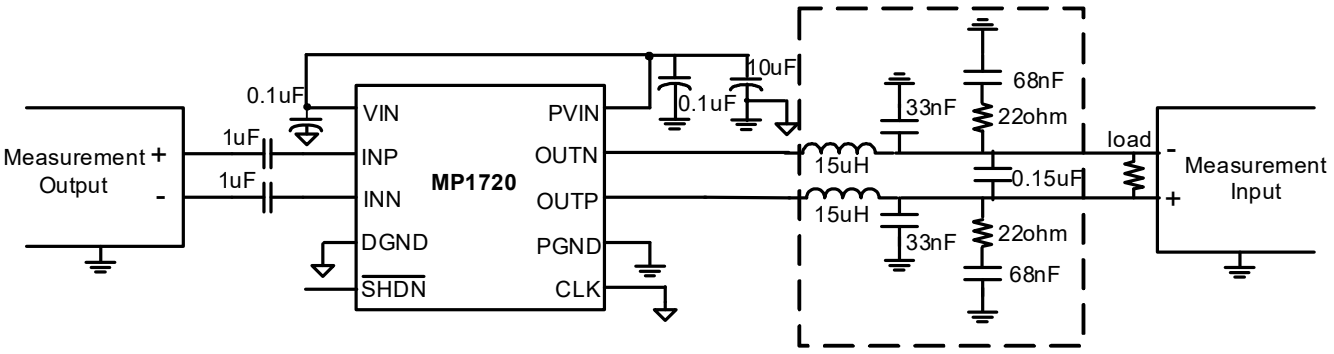


Figure 1—MP1720 Functional Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

TEST SET-UP GRAPH



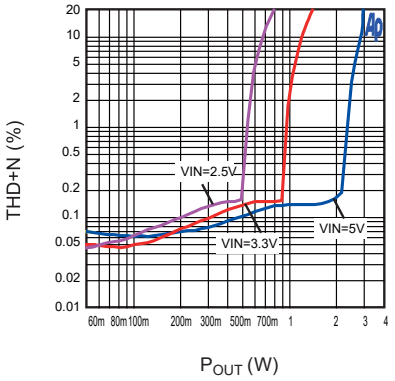
Notes:

6) The 70kHz low-pass filter is required even if the analyzer has a low-pass filter.
7) For PSRR test, Please remove the 10uF decoupling capacitor and just keep the small decoupling capacitors for recovery switching currents.
8) CIN was shorted for any Common-Mode input voltage measurement.

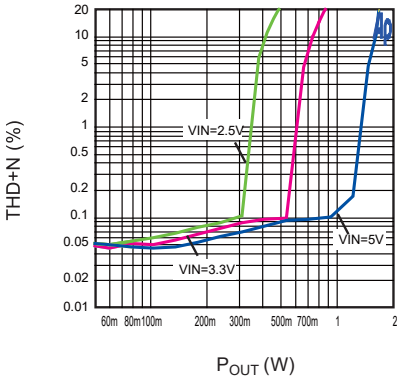
TYPICAL PERFORMANCE CURVES

VIN = PVIN = $\overline{SHDN}$=3.3V, DGND = PGND = 0V, CLK = DGND (f_{CLK}=1.0MHz), signal frequency f_s=1kHz, Gain=12dB, T_A = +25°C, unless otherwise noted (6,7,8).

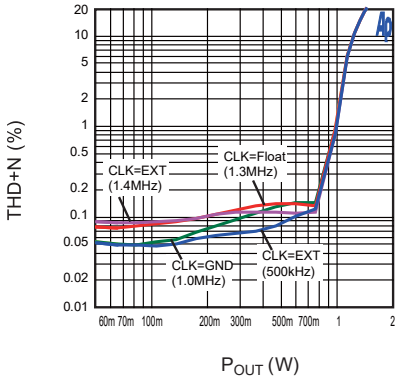
THD+N vs. P_{OUT}
R_{LOAD}=4Ω



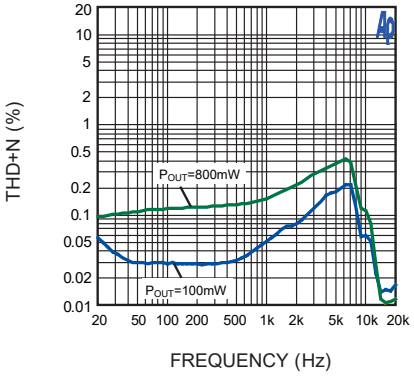
THD+N vs. P_{OUT}
R_{LOAD}=8Ω



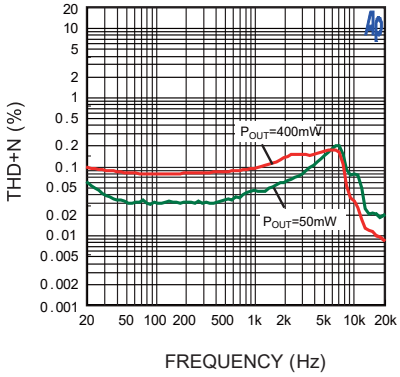
THD+N vs. P_{OUT}
R_{LOAD}=4Ω, VIN=3.3V



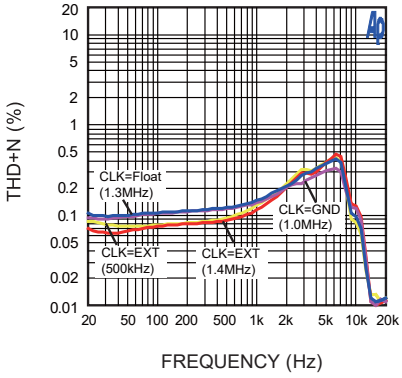
THD+N vs. Frequency
R_{LOAD}=4Ω, VIN=3.3V



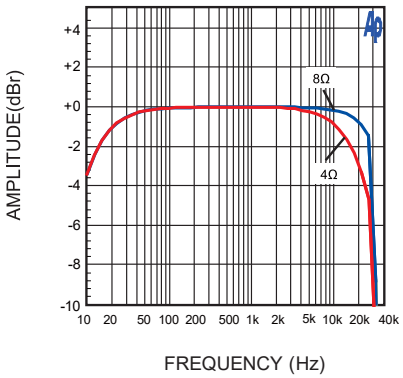
THD+N vs. Frequency
R_{LOAD}=8Ω, VIN=3.3V



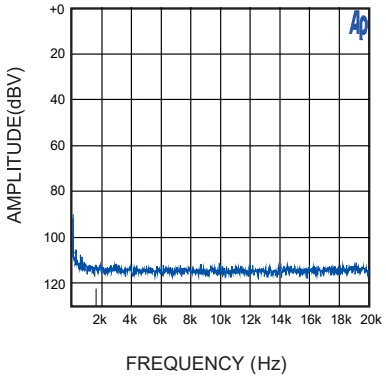
THD+N vs. Frequency
R_{LOAD}=4Ω, P_{OUT}=800mW, VIN=3.3V



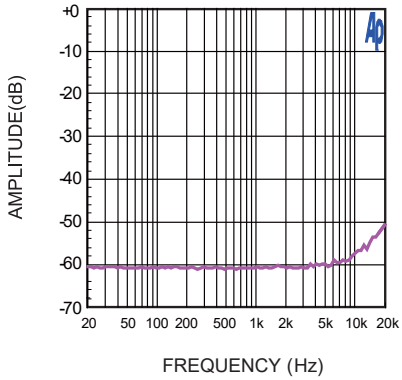
Frequency Response
VIN=3.3V, P_{OUT}=100mW



Noise Floor
VIN=3.3V, R_{LOAD}=4Ω,
No Input Signal



PSRR vs. Frequency
VIN=3.3V, R_{LOAD}=4Ω,
Vripple=300mVpp, Input ac-grounded

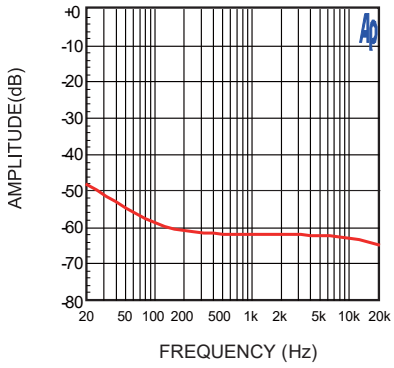


TYPICAL PERFORMANCE CURVES *(continued)*

VIN = PVIN = $\overline{SHDN}$=3.3V, DGND = PGND = 0V, CLK = DGND (f_{CLK}=1.0MHz), signal frequency f_s=1kHz, Gain=12dB, T_A = +25°C, unless otherwise noted (6,7,8).

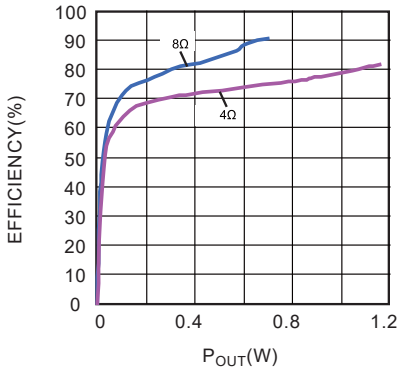
CMRR vs. Frequency

VIN=3.3V, R_{LOAD}=4Ω,
V_{ic_ripple}=300mVpp



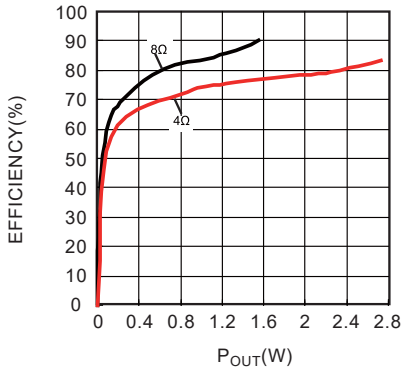
Efficiency vs. P_{OUT}

VIN=3.3V



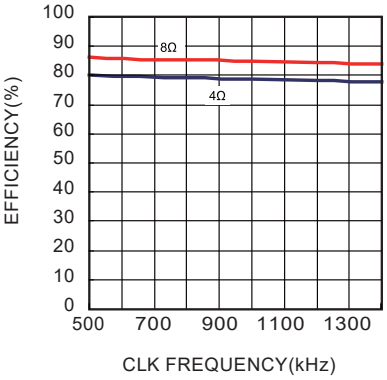
Efficiency vs. P_{OUT}

VIN=5V



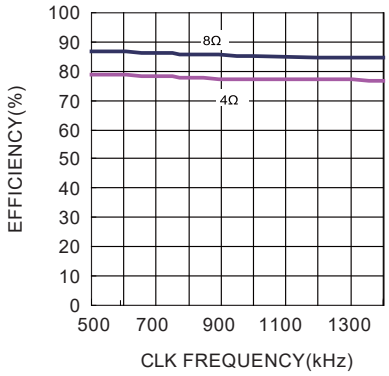
Efficiency vs. CLK Frequency

VIN=5V, THD+N=1%



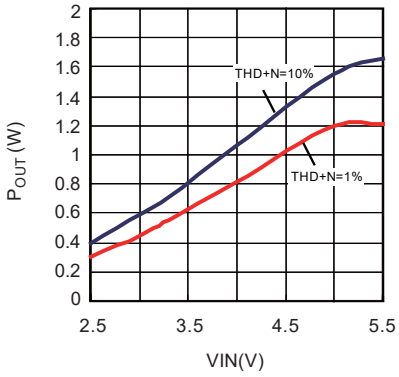
Efficiency vs. CLK Frequency

VIN=3.3V, THD+N=1%



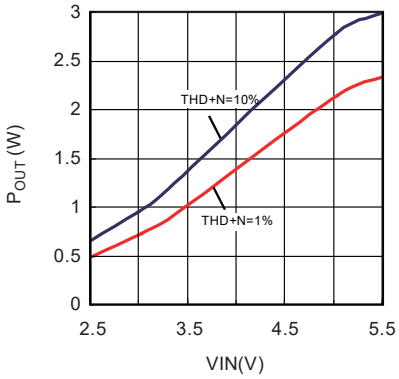
P_{OUT} vs. VIN

R_{LOAD}=8Ω



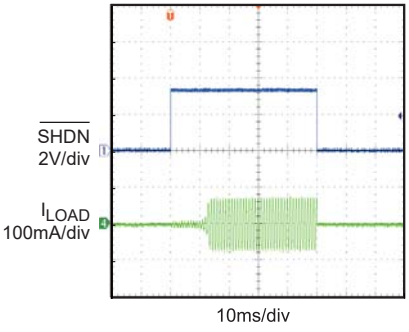
P_{OUT} vs. VIN

R_{LOAD}=4Ω



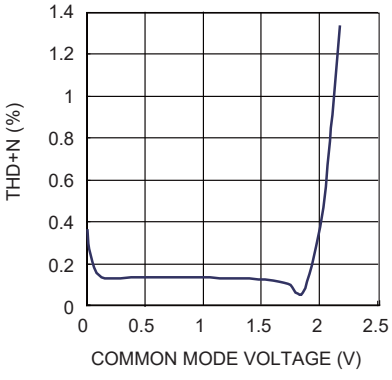
Turn on/Turn off response

R_{LOAD}=8Ω, VIN=3.3V, P_{OUT}=25mW



THD+N Vs. Common Mode Voltage

R_{LOAD}=4Ω, VIN=3.3V~5V, P_{OUT}=500mW



OPERATION

The MP1720 is a high efficiency Class D audio power amplifier, low cost which can operate well without output LC filter, low EMI which can pass FCC-Radiated Emissions Standards with 24inch unshielded twisted-pair-speaker Cable without output filter. It has fully differential input and output. And this device can still be used with a single-ended input; but for some noisy environment the MP1720 should be used with differential inputs to ensure maximum noise rejection.

MP1720 Functional Block Diagram is shown as Figure 1. The amplifier detects the input signal and gets the input differential voltage, which would be combined with the DC bias voltage to generate the complementary voltage. The complementary voltage is compared with the sawtooth waveform. The output of the comparators (U2, U3) would trip when the input magnitude of the sawtooth exceeds the complementary voltage. When no signal is inputted, the output of both comparators are the pulse with a fixed turn on time, and zero output is got from the difference of two channel output (V_{OUTP}-V_{OUTN}). As the larger positive signal is inputted, the output duty of one comparator would be larger while another remains the fixed turn on time or less time, so larger output is got from the difference of two channel output (V_{OUTP}-V_{OUTN}). And there is opposite duty adjustment when the larger negative signal is inputted.

CLK Operating Modes

The MP1720 offers two kinds of operate frequency solution: internal fixed clock setting or be synchronized to an external clock. Allowing the switching frequency to be flexibly adjusted can avoid the frequency or harmonics fall in sensitive frequency bands.

1) Internal clock Mode

The MP1720 have two kinds of internal clock selection. Setting CLK = DGND, the switching frequency is 1.0MHz. Setting CLK = FLOAT, the switching frequency is 1.3MHz.

2) External Clock Mode

The MP1720 CLK input allows the amplifier to be synchronized to an external TTL clock, which can push the spectral components of the switching harmonics off sensitive frequency bands. This external TTL clock frequency range is very wide and frequency from 0.5MHz to 1.4MHz is recommended.

Table 1—CLK Operating Modes

CLK=GND	f_{CLK}=1.0MHz
CLK=FLOAT	f_{CLK}=1.3MHz
CLK=Clocked	f_{CLK}=external clock frequency

Input configuration

The MP1720 is a mono BTL Class-D amplifier with differential inputs and outputs, and this device can still be used with a single-ended input

1) Differential Input

For some noisy environment, the MP1720 should be used with differential inputs. The fully differential amplifier allows the inputs to be biased at voltage other than mid-supply. The input coupling capacitors are not required if the design uses a differential source that is biased from 0.2 V to 1.9V (please see TPC: THD+N vs. Common mode voltage). Although the input coupling capacitor is saved, the low frequency noise would be amplified to the speaker.

If the input signal is not biased within the recommended common-mode input range, the input coupling capacitors are needed to pass only the AC audio signal to the input of the amplifier as a high pass filter.

2) Single-Ended Input

The MP1720 also can be configured as a single-ended input amplifier. Input coupling capacitor is needed to create a high-pass filter with the input resistor and get the low frequency rejection.

Note: The voltage at each input pin (INP or INN) should be not lower than -0.5V, so the input signal voltage and the maximum output power would be limited, especially for the low gain part. For the high output power applications, the higher gain versions or the differential input is recommended.

The peak-to-peak range of limited input voltage on each input pin $V_{LIMIT(PP)}$ can be calculated by the DC bias voltage V_{BIAS} as the following formula.

$$V_{LIMIT\ (PP)} = 2^* (V_{BIAS}+0.5) \qquad (1)$$

Take the application with input coupling capacitor as an example, the input DC bias voltage V_{BIAS} on each input pin is set internally (detailed value please see Input Bias Voltage in the EC table). For different gain options, the calculated maximum input signal and the tested maximum output power, with SE input or differential input, are shown in the Table 2.

Table 2—Maximum Input voltage and Maximum Output Power

Test condition:VIN=PVIN=5V; 4Ω load.

Part	SE input		Differential input	
	V_{IN_max} (V_{PP})	P_{OUT}_max (W)	V_{IN_max} (V_{PP})	P_{OUT}_max (W)
MP1720-3	2.99	0.52	5.98	1.9
MP1720-6	2.88	0.93	5.76	2.7 @ 10% THD+N
MP1720-9	2.72	1.74	5.44	2.7 @ 10% THD+N
MP1720-12	2.568	2.62	5.136	2.7 @ 10% THD+N
MP1720-216	1.93	2.7 @ 10% THD+N	3.86	2.7 @ 10% THD+N

Shutdown Function

The MP1720 $\overline{SHDN}$ input is a low-active control. To shutdown MP1720, drive $\overline{SHDN}$ low-level voltage. To enable MP1720, drive $\overline{SHDN}$ high-level voltage. Shutdown function can place the MP1720 in a low-power (0.1μA) shutdown mode and reduce power consumption and extend battery life.

Thermal Shutdown/ Short Circuit Protection

The MP1720 provides internal over thermal protection and short-circuit protection. The amplifier would be disabled to prevent damage to the IC if the junction temperature surpasses +125°C. The junction temperature must fall below +112°C before normal operation resumes. The currents of both the high-side and low-side MOSFETs are measured. If the current exceeds an internally preset value, all MOSFETs will be turned off. After the over thermal or short circuit fault is monitored, the MP1720 remains disabled status for a minimum of 50μs until normal operation resumes.

Pop Suppression

After driving $\overline{SHDN}$ pin high, there is a 15ms Start-up time to eliminate the startup pop. During this period, an internal circuitry would charges the bias voltages of the device to a certain level to prevent the startup click or pop. And after driving $\overline{SHDN}$ pin low, the all outputs will be set to high impedance immediately

APPLICATION INFORMATION

COMPONENT SELECTION

The MP1720 uses a minimum number of external components to complete a fully bridged Class D audio amplifier. Use the following sections to customize the amplifier for your particular application.

1) Input Coupling Capacitors (C_{IN})

The MP1720 is a mono BTL Class-D amplifier with differential outputs and inputs. If the input signal is not biased within the recommended common-mode input range or if using a single-ended source, the input coupling capacitors are used to pass only the AC audio signal to the input of the amplifier as a high pass filter. Choose an input coupling capacitor such that the corner frequency f_{IN} is less than the desired pass-band frequency. The formula for the corner frequency is:

$$f_{IN} = \frac{1}{2\pi R_{IN} C_{IN}} \quad (2)$$

R_{IN} is 15kΩ for MP1720. Speakers in wireless handsets usually can't respond well to low frequencies, so for this application the corner frequency can be set to block the low frequencies.

The input coupling capacitance is calculated as:

$$C_{IN} = \frac{1}{2\pi R_{IN} f_{IN}} \quad (3)$$

If the corner frequency is within the audible band, the capacitors should have a tolerance of ±10% or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.

Tantalum or aluminum electrolytic capacitor with low-voltage coefficients is recommended, or the largest package ceramics capacitor to minimize voltage coefficient effects, for example X7R dielectrics is better than Y5V or Z5U.

2) Power Supply Decoupling Capacitor (C_S)

The class-D audio amplifier requires adequate power supply decoupling to ensure the efficiency is high and total harmonic distortion (THD+N) is low. To carry the higher frequency transient current, spikes, or digital hash on the line, a good low

ESR ceramic capacitor is necessary. Place a 1μF decoupling capacitor as close as possible to the device VCC lead. It is very important for the efficiency of the class-D amplifier, because any resistance or inductance in the trace between the capacitor and the device may cause a loss. A 10μF or greater capacitor placed near the audio power amplifier would also help for filtering lower-frequency noise

TYPICAL APPLICATION CIRCUIT

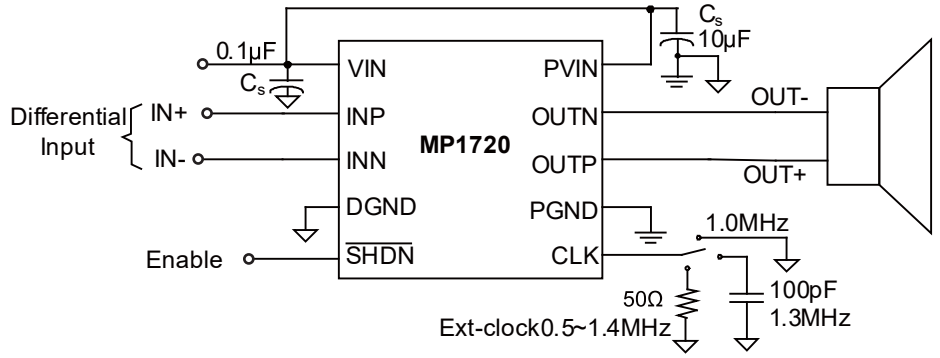


Figure 2—MP1720 Application Schematic with Differential Input

(Input DC-biased voltage is within the recommended common-mode voltage range)

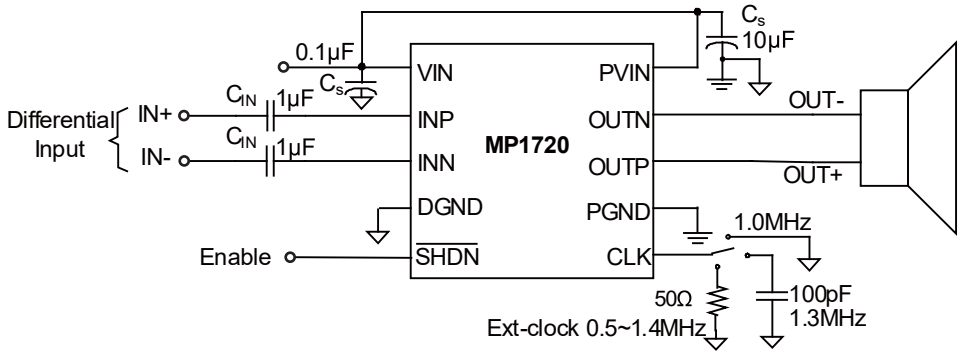


Figure 3—MP1720 Application Schematic with Differential Input

(Input DC-biased voltage is out of the recommended common-mode voltage range)

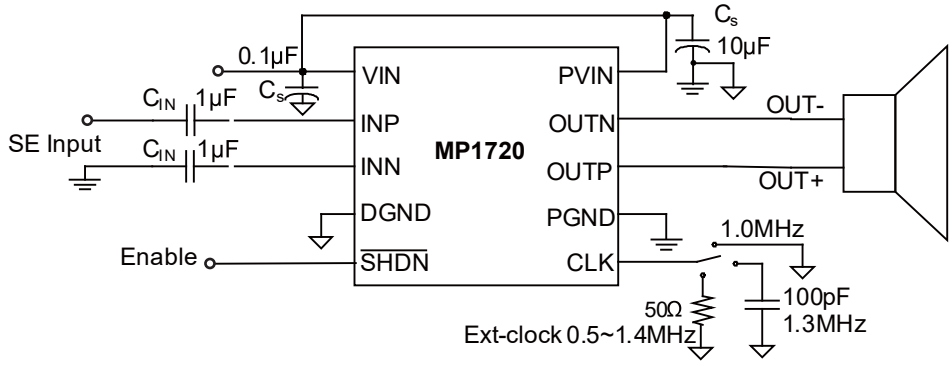
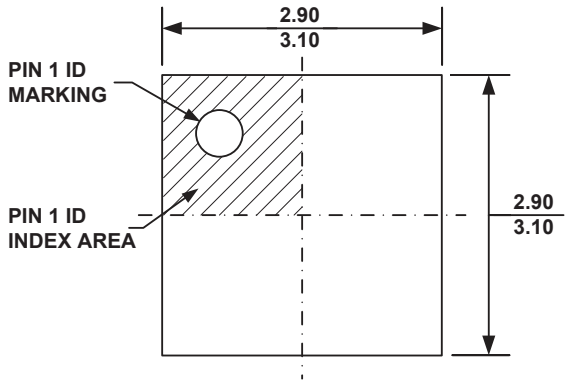


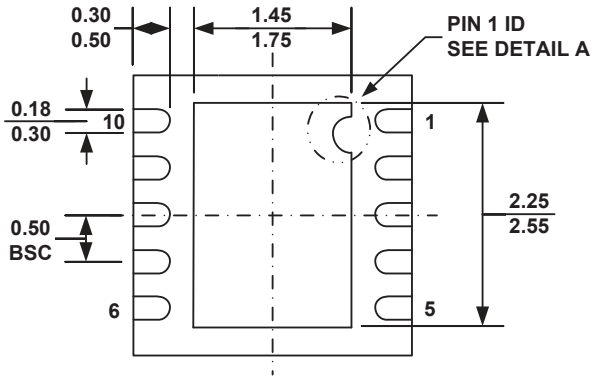
Figure 4—MP1720 Application Schematic with Single Ended Input

PACKAGE INFORMATION

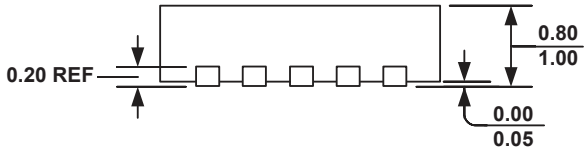
3mm x 3mm QFN10



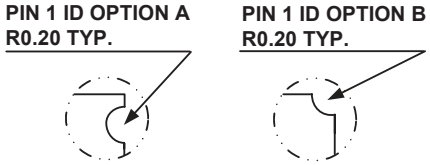
TOP VIEW



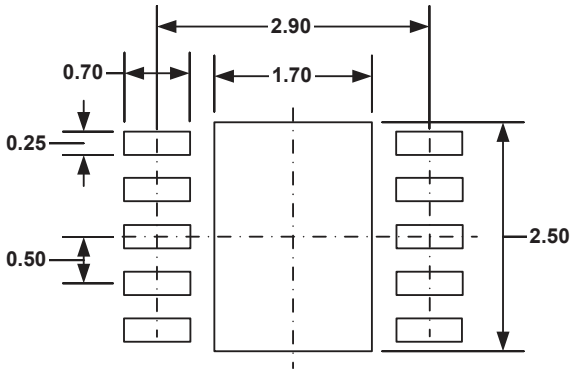
BOTTOM VIEW



SIDE VIEW



DETAIL A

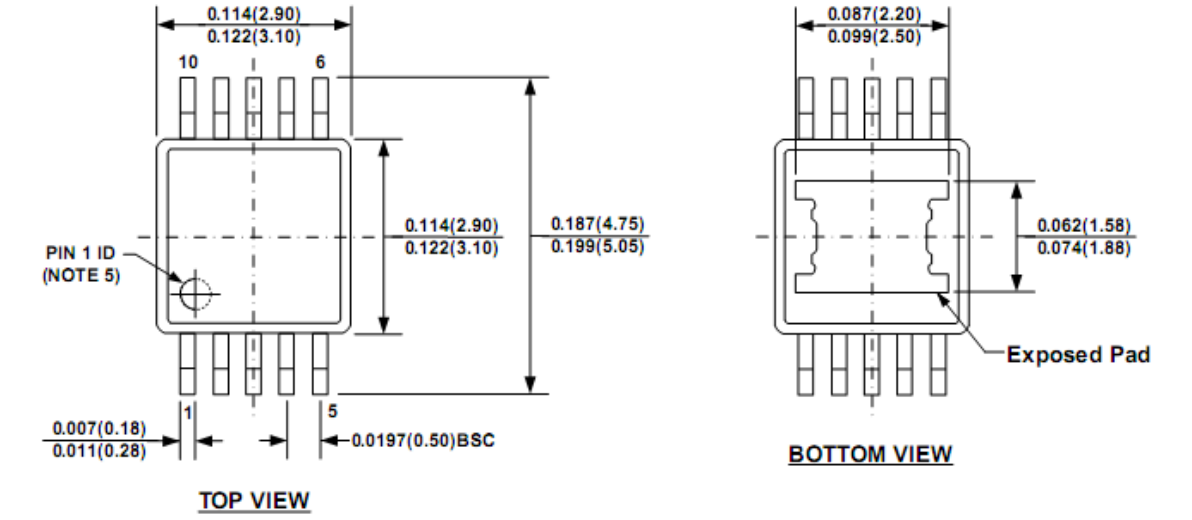


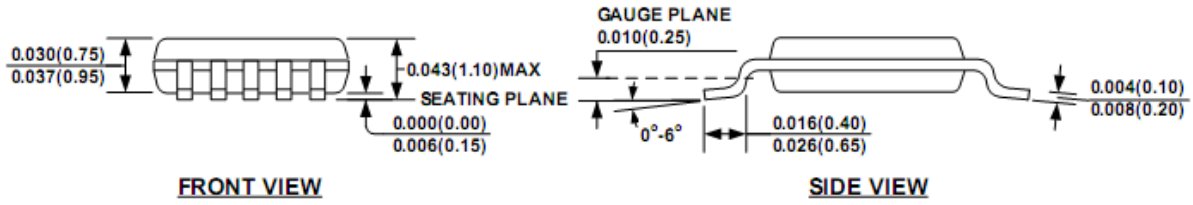
RECOMMENDED LAND PATTERN

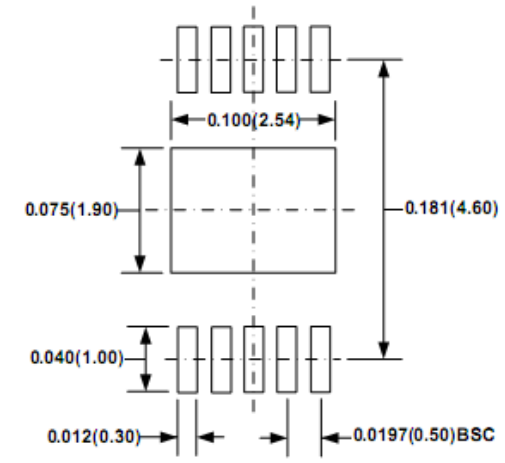
NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
5) DRAWING IS NOT TO SCALE.

MSOP-EP







NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) PIN 1 IDENTIFICATION HAS THE HALF OR FULL CIRCLE OPTION.
6) DRAWING MEETS JEDEC MO-187, VARIATION BA-T.
7) DRAWING IS NOT TO SCALE.