HFG610-45

High-Frequency Quasi-Resonant Flyback Regulator with Integrated 270mΩ GaN FET

DESCRIPTION

The HFG610-45 is a quasi-resonant (QR) flyback regulator with an integrated GaN FET, which is suitable for high-performance and high-frequency designs. Unlike conventional QR flyback regulators, the HFG610-45's frequency foldback guarantees high efficiency across the entire load range.

The HFG610-45 is a secondary-side regulation (SSR)-based primary regulator, and must work with secondary-side feedback circuitry. The higher frequency shrinks the passive component size and achieves higher power density. The HFG610-45 integrates a high-voltage start-up circuit and an X-capacitor discharger circuit, in addition to an ultra-low quiescent current (I_Q) in burst mode. The no-load power consumption can be less than 30mW.

The HFG610-45 adopts MPS's patented valley lock technique to restrain jumping from one valley to another valley during steady state operation, which can avoid audible noise completely. The wide supply voltage (V_{CC}) range makes the device suitable for applications with a wide output voltage (V_{OUT}) range without adding auxiliary winding.

Advanced protections include primary-sense output over-voltage protection (ZCD OVP), primary-sense output under-voltage protection (ZCD UVP), V_{CC} over-voltage protection (V_{CC} OVP), output overload protection (OLP), internal brown-in/brownout (BI/BO), short-circuit protection (SCP), current-sense short protection (SSP), internal thermal shutdown (OTP), and under-voltage lockout (UVLO).

The HFG610-45 is available in QFN-21 (5mmx6mm) and QFN-25 (7mmx7mm) packages.

	Recommended Output Power (3)			
	90V_{AC} to 265V_{AC}		230V_{AC} ±15%	
	Adapter (1)	Open Frame (2)	Adapter	Open Frame
P_{OUT1} (W) (4)	45	50	50	55
P_{OUT2} (W) (4)	50	55	55	60

FEATURES

- Integrated 700V/270mΩ GaN FET
- Novel Patented Quasi-Resonant (QR) Control to Eliminate Audible Noise
- Frequency Foldback and Burst Mode for Low Light-Load Power Consumption
- Ultra-Wide Supply Voltage (V_{CC}) Range to Support USB Power Delivery (PD) Applications
- Built-In X-Capacitor Discharger
- Built-In, High-Voltage Start-Up Circuit
- Ultra-Low Standby Power Consumption with PD Protocol IC (<30mW)
- Peak Current Mode Control and Leading-Edge Blanking (LEB)
- Under-Voltage Lockout (UVLO), V_{CC} Over-Voltage Protection (OVP), Primary-Sense Output Over-Voltage Protection (ZCD OVP), Primary-Sense Output Under-Voltage Protection (ZCD UVP), Overload Protection (OLP), Internal Brown-In (BI) and Brownout (BO), Short-Circuit Protection (SCP), Current-Sense Short Protection (SSP), and Over-Temperature Protection (OTP)
- Available in QFN-21 (5mmx6mm) and QFN-25 (7mmx7mm) Packages

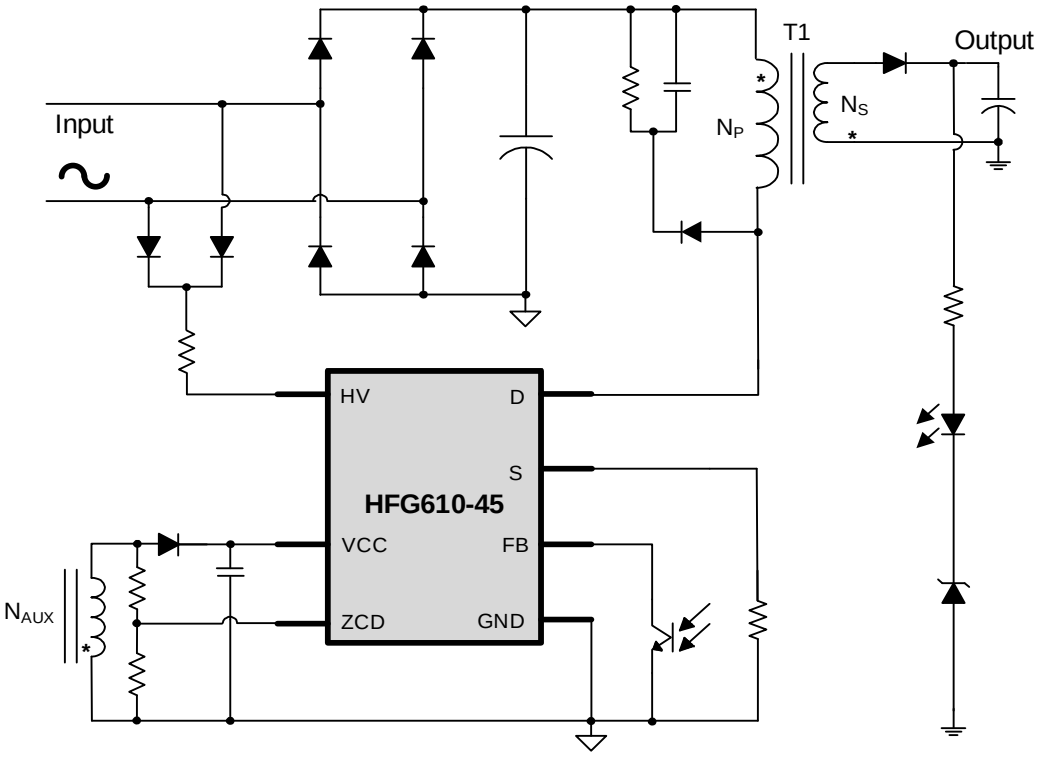
APPLICATIONS

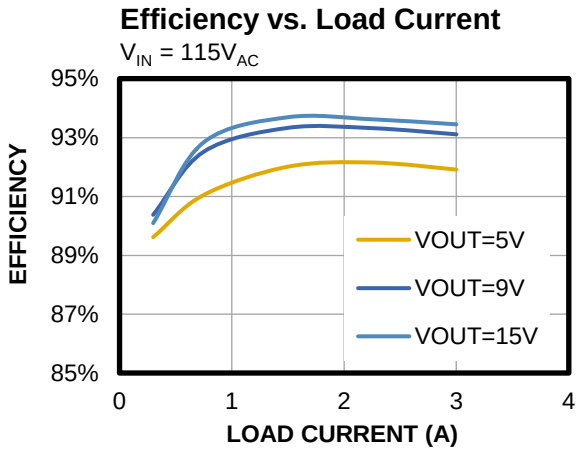
- High-Density AC/DC Adapters
- Offline Battery Chargers
- High-Efficiency, High-Current Power Supplies

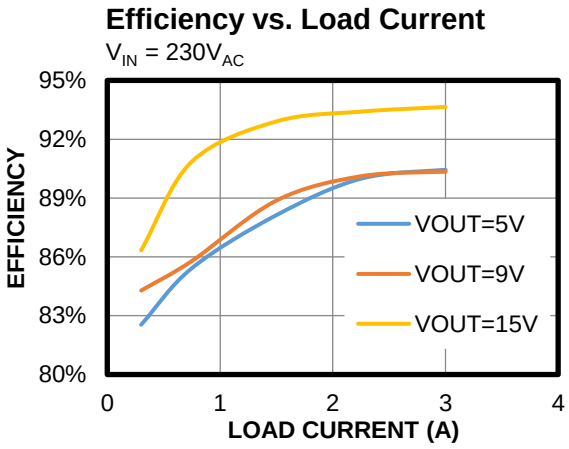
Notes:

1) The maximum continuous power in a non-ventilated enclosed adapter is measured at an ambient temperature (T_A) of 40°C.
2) The maximum continuous power is in an open frame design at T_A = 40°C.
3) The junction temperature (T_J) can limit the maximum P_{OUT}.
4) P_{OUT1} refers to the P_{OUT} for the QFN (5mmx6mm) package, and P_{OUT2} refers to the P_{OUT} for the QFN (7mmx7mm) package.

TYPICAL APPLICATION







ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
HFG610GQJ-45	QFN-21 (5mmx6mm)	*See Below*	2
HFG610GQN-45	QFN-25 (7mmx7mm)	*See Below*	3

* For Tape & Reel, add suffix -Z (e.g. HFG610GQJ-45-Z).

* For Tape & Reel, add suffix -Z (e.g. HFG610GQN-45-Z).

TOP MARKING (QFN (5mmx6mm))

MPSYYWW
HFG610
LLLLLLL
45

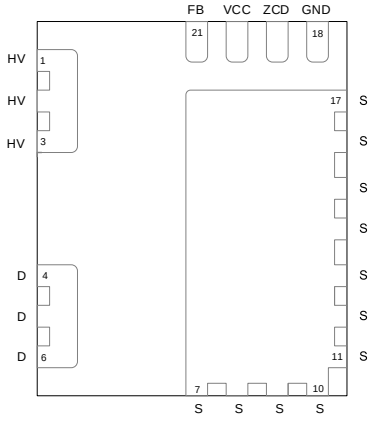
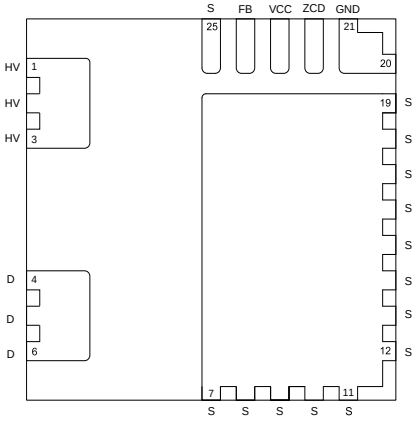
MPS: MPS prefix
YY: Year code
WW: week code
HFG610-45: Part number
LLLLLLL: Lot number

TOP MARKING (QFN (7mmx7mm))

MPS YYWW
HFG610-45
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: week code
HFG610-45: Part number
LLLLLLLLL: Lot number

PACKAGE REFERENCE

TOP VIEW	TOP VIEW
	
QFN-21 (5mmx6mm)	**QFN-25 (7mmx7mm)**

PIN FUNCTIONS

Pin #		Name	Description
QFN-21	QFN-25		
1, 2, 3	1, 2, 3	HV	**Input for the start-up high-voltage current source.** The HV pin also provides line voltage sensing, brown-in and brownout, line removal detection circuit, and X-capacitor discharge functions.
4, 5, 6	4, 5, 6	D	**GaN FET drain.**
7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17	7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 25	S	**GaN FET source.** The S pin also functions as the current-sense (CS) node. A CS resistor is connected between the S and GND pin to sense the primary current for current mode.
18	20, 21	GND	**Ground.**
19	22	ZCD	**Integrated over-voltage protection (OVP) and under-voltage protection (UVP).** A resistor divider placed between the auxiliary winding and the ZCD pin provides the input to the demagnetization detection comparator and output voltage (V_{OUT}) information to achieve protection.
20	23	VCC	**IC power supply.**
21	24	FB	**Feedback.** A pull-down optocoupler controls output regulation.

ABSOLUTE MAXIMUM RATINGS (5)

HV to GND .....-0.3V to +650V
D to GND (9) .....-0.3V to +700V
D to GND, pulse (10).....-0.3V to +750V
D to GND, transient (11) .....-0.3V to +800V
Pulsed DS current (12)..... 8.5A
Continuous DS current (13) 2.8A
VCC to GND .....-0.3V to +57V
ZCD to GND .....-0.7V to +15V
FB to GND .....-0.3V to +6.5V
S to GND, gate on .....-0.3V to +6.5V
S to GND, gate off (9).....-0.3V to +1.4V
Continuous power dissipation (T_A = 25°C) (6)
QFN (5mmx6mm) 4.2W
QFN (7mmx7mm) 5.3W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature..... -60°C to +150°C

ESD Ratings

Human body model..... 1.2kV
Charged-device model (CDM) 2kV

Recommended Operating Conditions (7)

Supply voltage (V_{CC}) .....9V to 49V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (8) θ_{JA} θ_{JC}

QFN-21 (5mmx6mm)……29.2 ... 5.4.. °C/W
QFN-25 (7mmx7mm)……23.5 ..... 2 ... °C/W

Notes:

5) The device is not guaranteed to function outside of its operating conditions.
6) Exceeding these ratings may damage the device.
7) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can generate excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
8) Measured on a JESD51-7, 4-layer PCB.
9) Guaranteed by characterization.
10) Repetitive pulse, t_{PULSE} < 100ns. T_J = 25°C, total time < 10h. T_J = 125°C, total time < 1h. Guaranteed by characterization.
11) Non-repetitive pulse, t_{PULSE} < 200µs. Guaranteed by characterization.
12) T_J = 25°C, t_{PULSE} = 10µs. Guaranteed by characterization.
13) T_J = 125°C. Guaranteed by characterization.

ELECTRICAL CHARACTERISTICS

T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Breakdown voltage	V_{HV_BD}	T_J = 25°C	700			V
HV leakage current	I_{HV_LK}	V_{HV} = 500V			15	μA
HV supply current	I_{HV_SP}	V_{CC} = 12V, V_{HV} = 80V	4.5			mA
		V_{CC} = V_{CC_IOFF} - 0.1V, V_{HV} = 80V	2.7			
	$I_{HV\_SP\_SC}$	V_{CC} = 0V, V_{HV} = 80V		1		
Drain (D Pin)						
Drain breakdown voltage	V_{D_BD}	I_{DSS} < 12μA, T_J = 25°C	700			V
Drain-to-source leakage current	I_{DSS}	V_{DS} = 400V, V_{GS} = 0V, T_J = 25°C		0.8	10	μA
Drain-to-source on resistance	$R_{DS(ON)}$	V_{GS} = 5.5V, T_J = 25°C, I_{DS} = 0.1A		270	350	mΩ
		V_{GS} = 5.5V, T_J = 125°C, I_{DS} = 0.1A		500		
Brownout (BO) Detection and X-Capacitor Discharger (HV Pin)						
Brown-in (BI) threshold	V_{HV_ON}		92	105	118	V
BO threshold	V_{HV_OFF}		82	95	108	V
BI and BO hysteresis	V_{HV_HYS}			10		V
BO detection blanking time	t_{BO}		42	62	82	ms
Line voltage removal detection timer	t_{LINE_RDET}			96		ms
Discharge time duration	t_{LINE_DIS}			144		ms
Line voltage detection duration	t_{LINE_DET}			48		ms
Discharge current	I_{DIS_HV}		4.2			mA
HV high-line threshold	V_{HV_HL}		210	240	270	V
HV high-line voltage detection hysteresis	$V_{HV\_HL\_HYS}$			10		V
HV low-line to high-line blanking time transition (14)	t_{LH}			150		μs
HV high-line to low-line blanking time transition (14)	t_{HL}			16		ms
Supply Voltage Management (VCC Pin)						
HV supply current turn-off voltage	V_{CC_IOFF}	V_{CC} increasing	16.5	17.5	19	V
Minimum operating voltage	V_{CC_MIN}	V_{CC} decreasing	7.4	8.0	8.6	V
Operating voltage hysteresis	V_{CC_HYS}		8			V
V_{CC} release level after auto-recovery protection	V_{CC_PRO}	V_{CC} decreasing	5.5	6.3	7	V

ELECTRICAL CHARACTERISTICS *(continued)*

T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
V_{CC} release level after latch-off protection	V_{CC_LATCH}	V_{CC} decreasing		2.9		V
Transition from $I_{HV\_SP\_SC}$ to I_{HV_SP}	V_{CC_LC}	V_{CC} increasing		0.8		V
V_{CC} over-voltage protection (OVP) threshold	V_{CC_OVP}		50	53	57	V
V_{CC} OVP delay time	t_{VCC_OVP}			23		µs
Operating current	I_{OP}	V_{CC} = 15V		2	3	mA
Operating current during protection	I_{OP_PRO}	V_{CC} = 8V, except BO			200	µA
		V_{CC} = 8V, BO	1.2			mA
Quiescent current	I_Q	V_{CC} = 15V, V_{FB} = 0V			470	µA
Current Sense (S Pin)						
Current-sense (CS) voltage	V_{CS_MAX}		0.388	0.4	0.408	V
	V_{CS_MIN}			0.15		V
Maximum soft-start (SS) time	t_{SS}			6.2		ms
Jittering amplitude	ΔV_{CS}	V_{CS} = 0.4V	±4%	±5%	±6%	V_{CS}
Jittering period	t_{JITTER}			32		cycles
Leading-edge blanking (LEB) for current limitation	t_{LEB_L}			200		ns
LEB for short-circuit protection (SCP)	t_{LEB_S}			150		ns
Detection time for S short	t_{SSP}		2.5	3.5	5	µs
Current-sense voltage (V_{CS}) threshold for S short	V_{SHORT}			45	65	mV
SCP threshold	V_{SCP}		0.6	0.65	0.7	V
Second SCP blanking time	t_{SCP}			130		µs
Number of consecutive pulses to detect the second SCP				8		pulses
Maximum On Time	t_{ON_MAX}			14.5		µs
Feedback (FB Pin)						
Maximum FB voltage	V_{FB_MAX}		3.6	3.7	3.9	V
Delta V_{FB_MAX} - V_{OLP}	$V_{FB\_MAX\_VOLP}$			0.3		V
Time duration before overload protection (OLP) (14)	t_{OLP}			50		ms
Internal pull-up resistor	R_{FB}			18		kΩ
FB voltage (V_{FB}) high threshold to fix current limit	$V_{FB\_CS\_MAX}$			3.2		V
V_{FB} low threshold to fix current limit	$V_{FB\_CS\_MIN}$			1.54		V
Burst mode entry	V_{BUR_IN}	V_{FB} decreasing		0.7		V

ELECTRICAL CHARACTERISTICS *(continued)*

T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

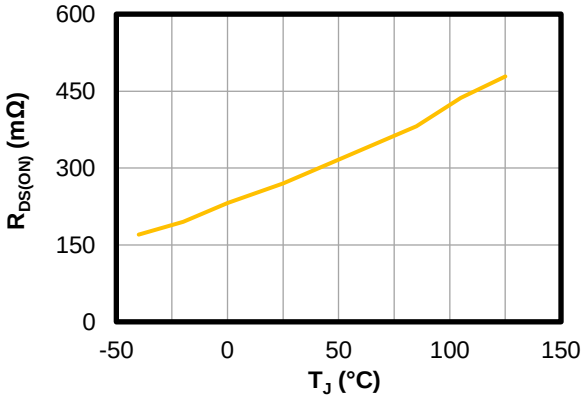
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Burst mode exit	V_{BUR_OUT}	V_{FB} increasing		0.8		V
Burst mode exit hysteresis	V_{BUR_HYS}			0.1		V
Quasi-Resonant (QR) Demagnetization Detection (ZCD Pin)						
ZCD threshold	V_{ZCD_TH}	V_{ZCD} decreasing	36	62	88	mV
ZCD hysteresis threshold	V_{ZCD_HYS}	V_{ZCD} increasing		30		mV
ZCD sample blanking time after turn-off	t_{ZCD_BLANK1}	V_{CS} = 0.4V		820	1170	ns
	t_{ZCD_BLANK2}	V_{CS} = 0.15V		510	720	
Timeout after last demagnetization detection (watchdog)	t_{OUT1}			200		µs
	t_{OUT}		2	2.7	3.6	
ZCD OVP threshold	V_{ZCD_OVP}		11.7	12.2	12.8	V
ZCD OVP blanking time	t_{ZCD_OVP}			3		cycles
ZCD under-voltage protection (UVP) threshold	V_{ZCD_UVP}	After soft start	0.29	0.4	0.48	V
ZCD UVP blanking time (10)	t_{ZCD_UVP}	After soft start		250		µs
ZCD pin negative clamp voltage	V_{ZCD_MIN}	I_{ZCD} = -2mA	-0.4	-0.13	0	V
Internal Over-Temperature Protection (OTP)						
OTP threshold (14)	T_{OTP}			150		°C
Hysteresis to release OTP (14)	ΔT_{OTP}			40		°C

Note:

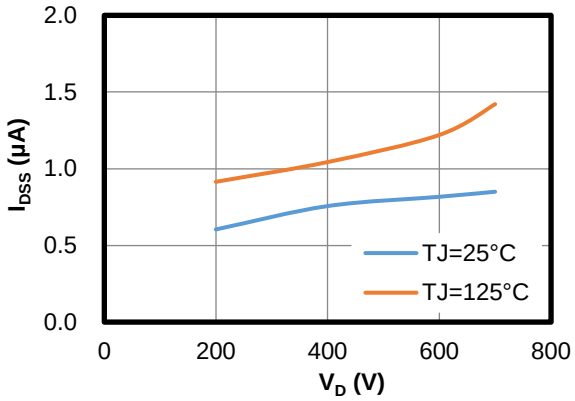
14) Guaranteed by design.

TYPICAL CHARACTERISTICS

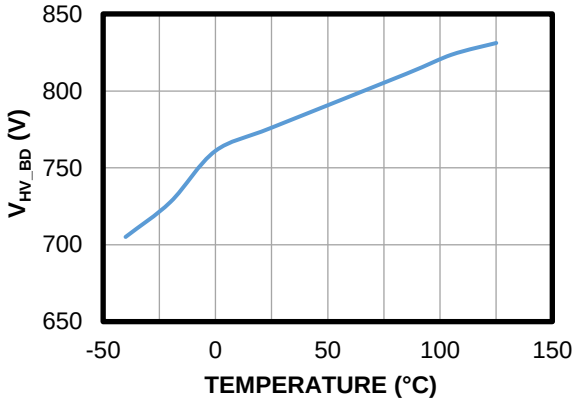
Drain-to-Source On Resistance vs. Junction Temperature



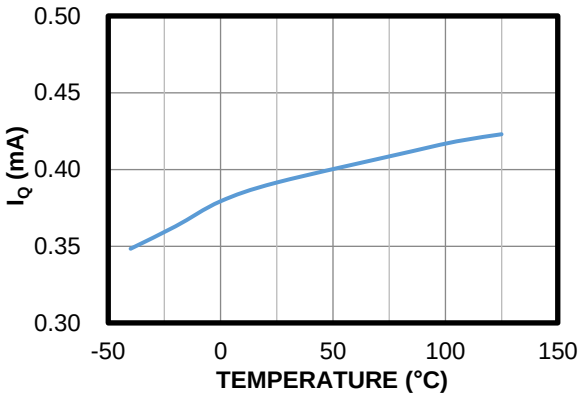
Drain-to-Source Leakage Current vs. Drain Voltage



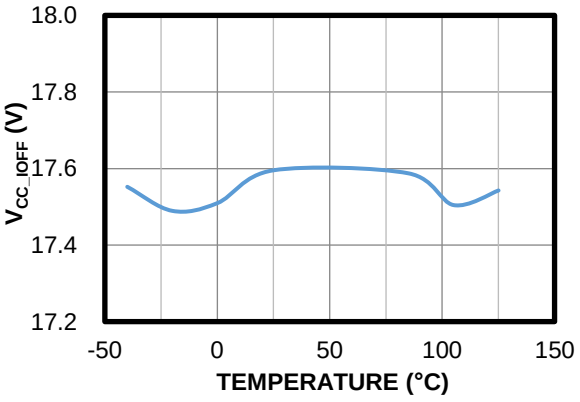
Breakdown Voltage vs. Temperature



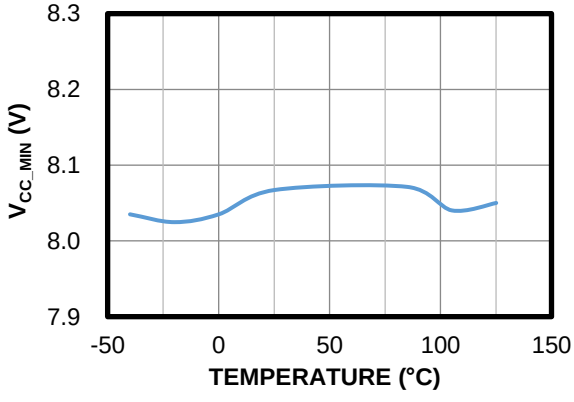
Quiescent Current vs. Temperature



HV Supply Current Turn-Off Voltage vs. Temperature

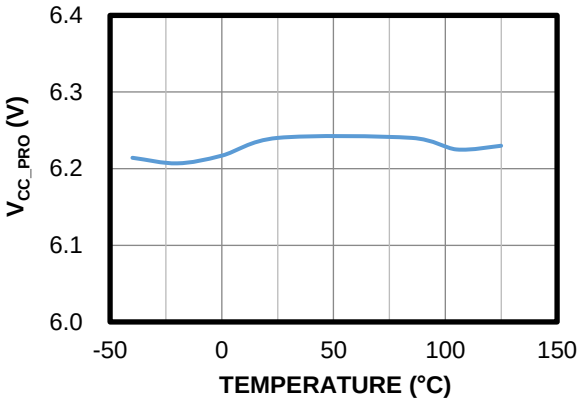


VCC Minimum Operating Voltage vs. Temperature

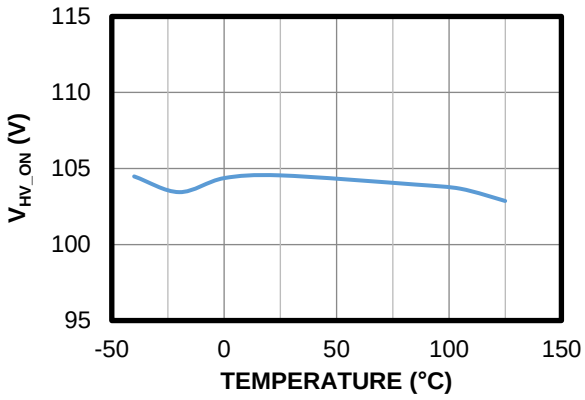


TYPICAL CHARACTERISTICS *(continued)*

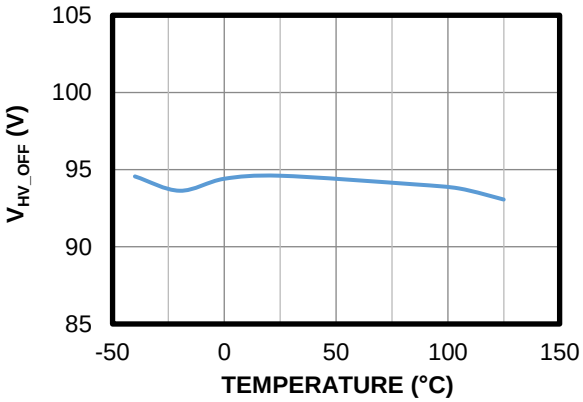
V_{CC} Release Level after Auto-Recovery vs. Temperature



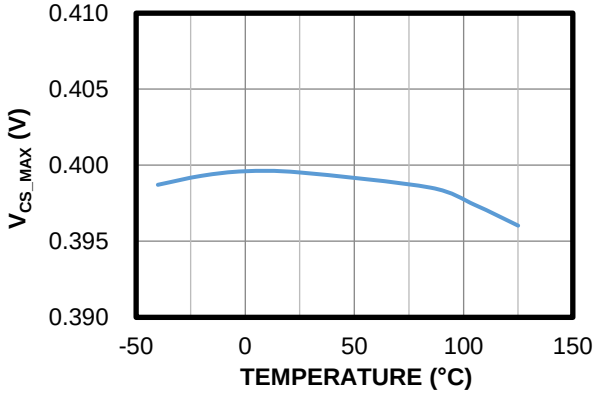
Brown-In Threshold vs. Temperature



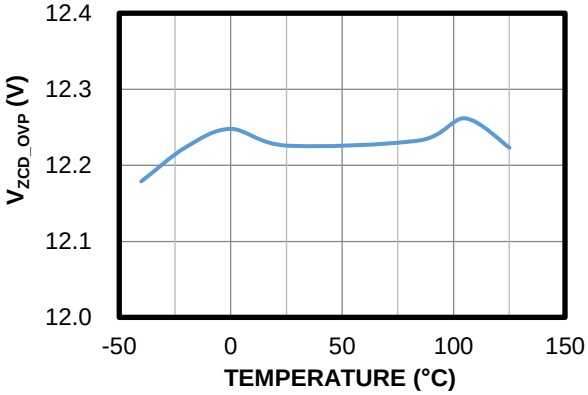
Brownout Threshold vs. Temperature



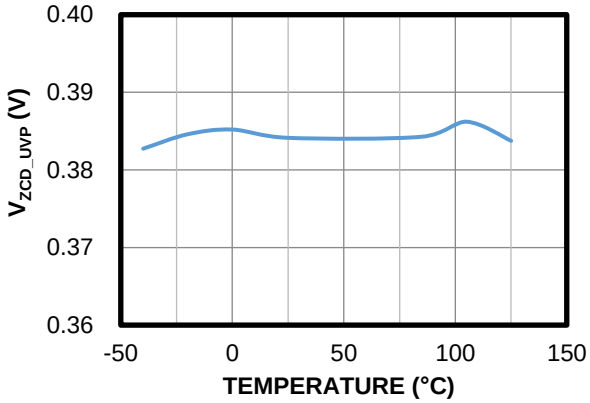
Current-Sense Maximum Voltage vs. Temperature



ZCD OVP Threshold vs. Temperature



ZCD UVP Threshold vs. Temperature

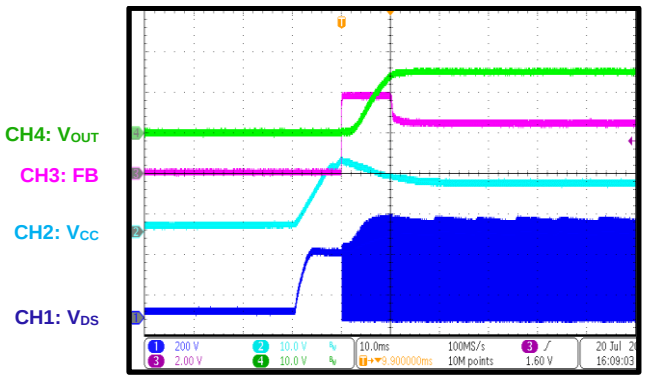


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 90V_{AC} to 265V_{AC}; V_{OUT} = 5V, 9V, or 15V; I_{OUT} = 0A to 3A, unless otherwise noted.

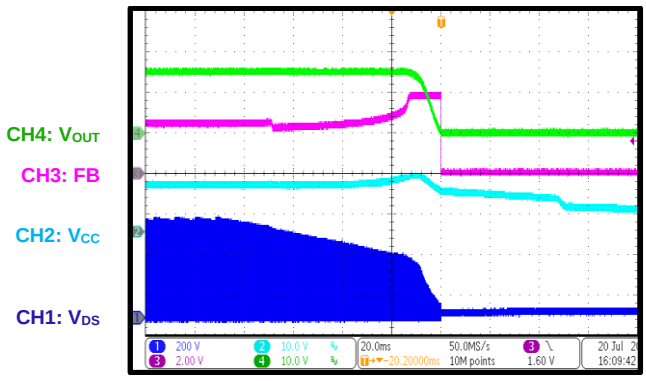
Start-Up

V_{IN} = 230V_{AC}, V_{OUT} = 15V, I_{OUT} = 3A



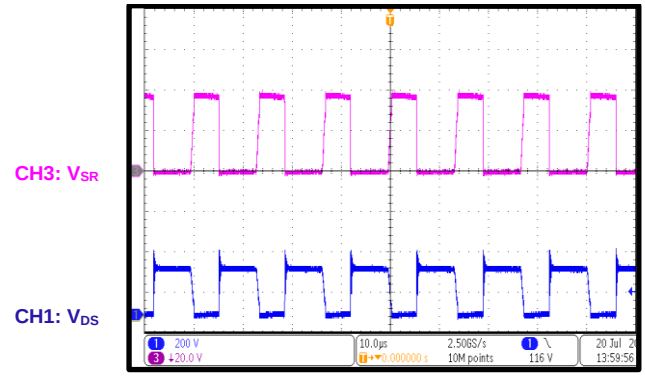
Shutdown

V_{IN} = 230V_{AC}, V_{OUT} = 15V, I_{OUT} = 3A



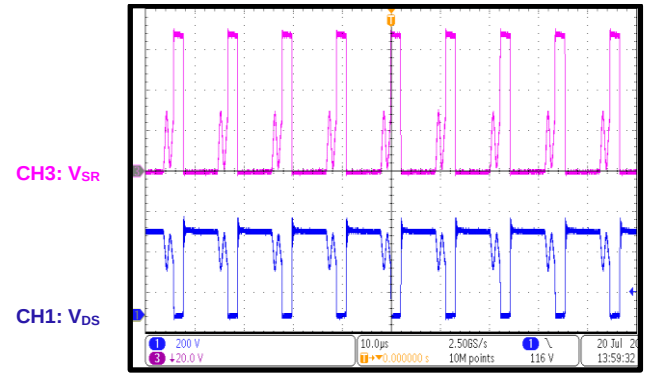
Steady State

V_{IN} = 115V_{AC}, V_{OUT} = 15V, I_{OUT} = 3A



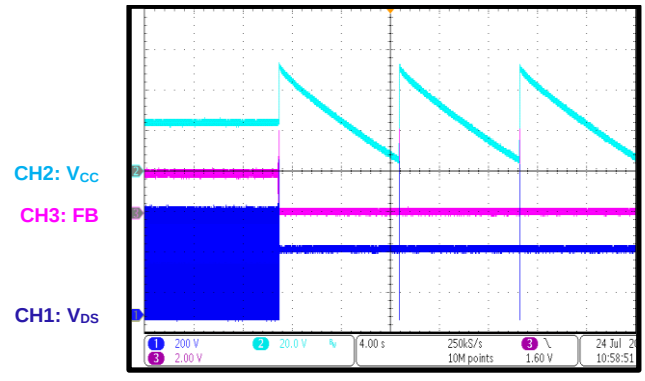
Steady State

V_{IN} = 230V_{AC}, V_{OUT} = 15V, I_{OUT} = 3A



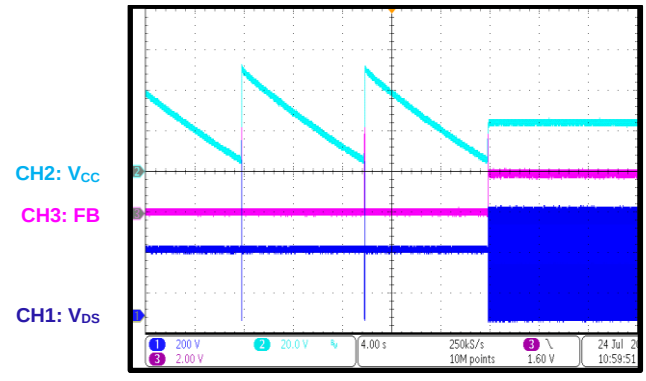
Over-Voltage Protection

V_{IN} = 230V_{AC}, V_{OUT} = 15V



OVP Recovery

V_{IN} = 230V_{AC}, V_{OUT} = 15V

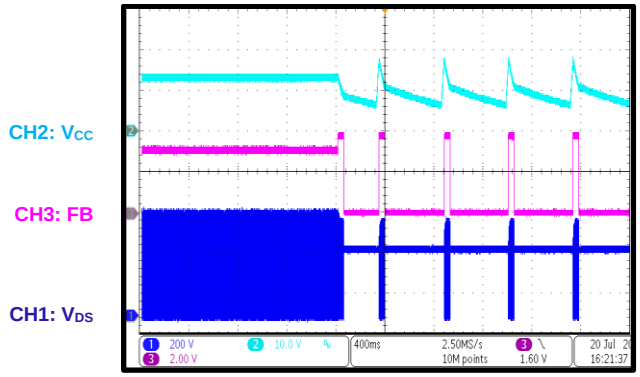


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 90V_{AC} to 265V_{AC}; V_{OUT} = 5V, 9V, or 15V; I_{OUT} = 0A to 3A, unless otherwise noted.

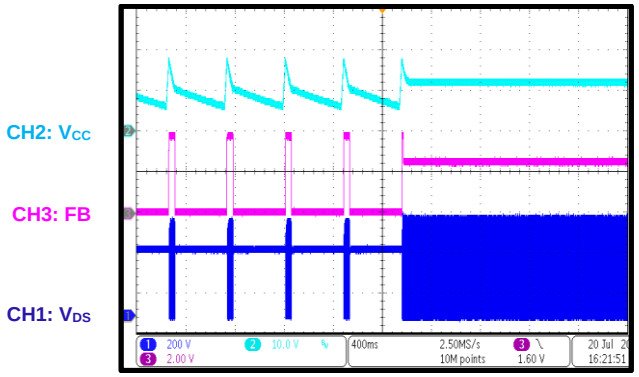
Overload Protection

V_{IN} = 230V_{AC}



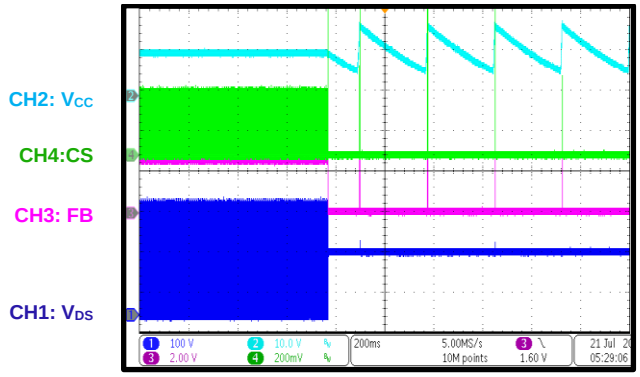
OLP Recovery

V_{IN} = 230V_{AC}



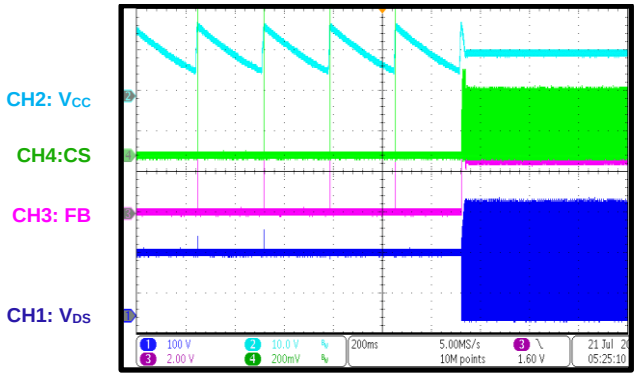
Short-Circuit Protection

V_{IN} = 115V_{AC}



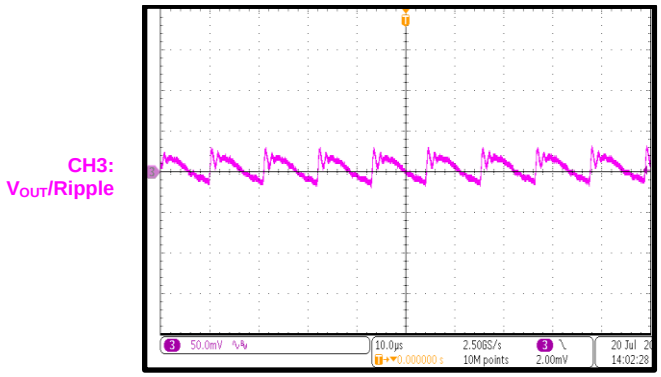
SCP Recovery

V_{IN} = 115V_{AC}



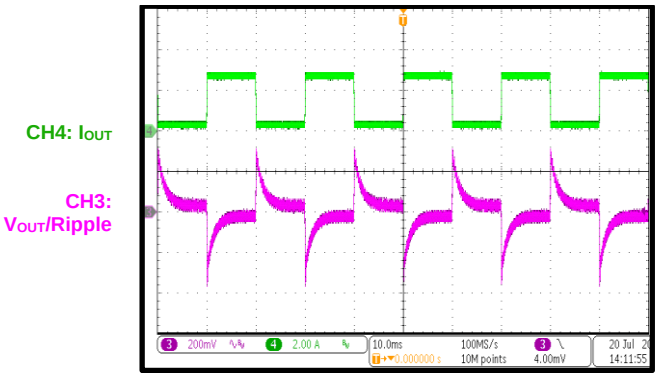
Output Voltage Ripple

V_{IN} = 230V_{AC}, V_{OUT} = 15V, I_{OUT} = 3A



Output Voltage Transient Response

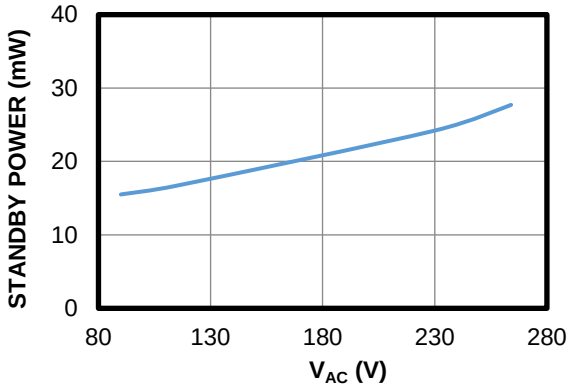
V_{IN} = 230V_{AC}, V_{OUT} = 15V



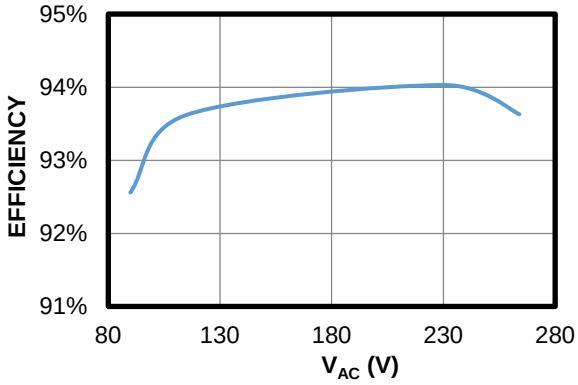
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 90V_{AC} to 265V_{AC}; V_{OUT} = 5V, 9V, or 15V; I_{OUT} = 0A to 3A, unless otherwise noted.

Standby Power vs. Input Voltage



Full Load Efficiency vs. Input Voltage

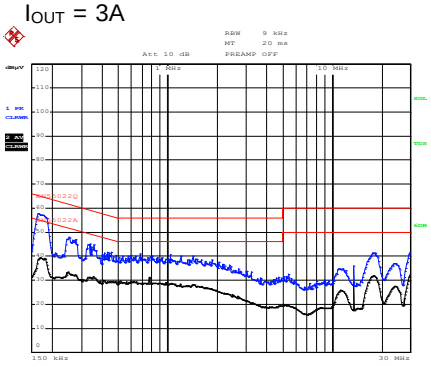


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 115V_{AC} or 230V_{AC}; V_{OUT} = 5V, 9V, or 15V; I_{OUT} = 0A to 3A, unless otherwise noted.

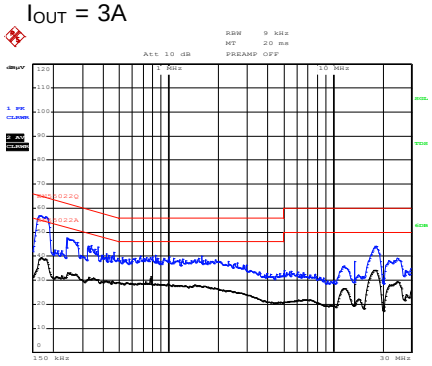
EMI

V_{IN} = 115V_{AC}, L line, V_{OUT} = 15V, I_{OUT} = 3A



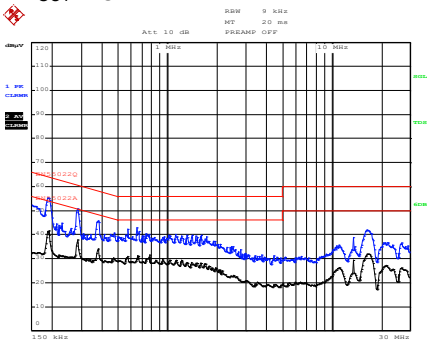
EMI

V_{IN} = 115V_{AC}, N line, V_{OUT} = 15V, I_{OUT} = 3A



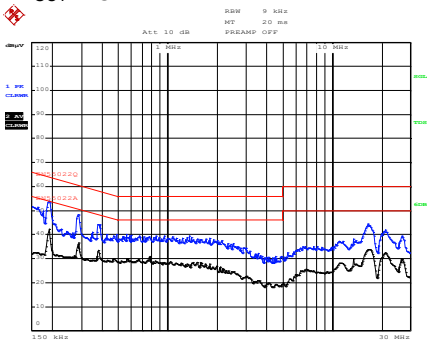
EMI

V_{IN} = 230V_{AC}, L line, V_{OUT} = 15V, I_{OUT} = 3A



EMI

V_{IN} = 230V_{AC}, N line, V_{OUT} = 15V, I_{OUT} = 3A



FUNCTIONAL BLOCK DIAGRAM

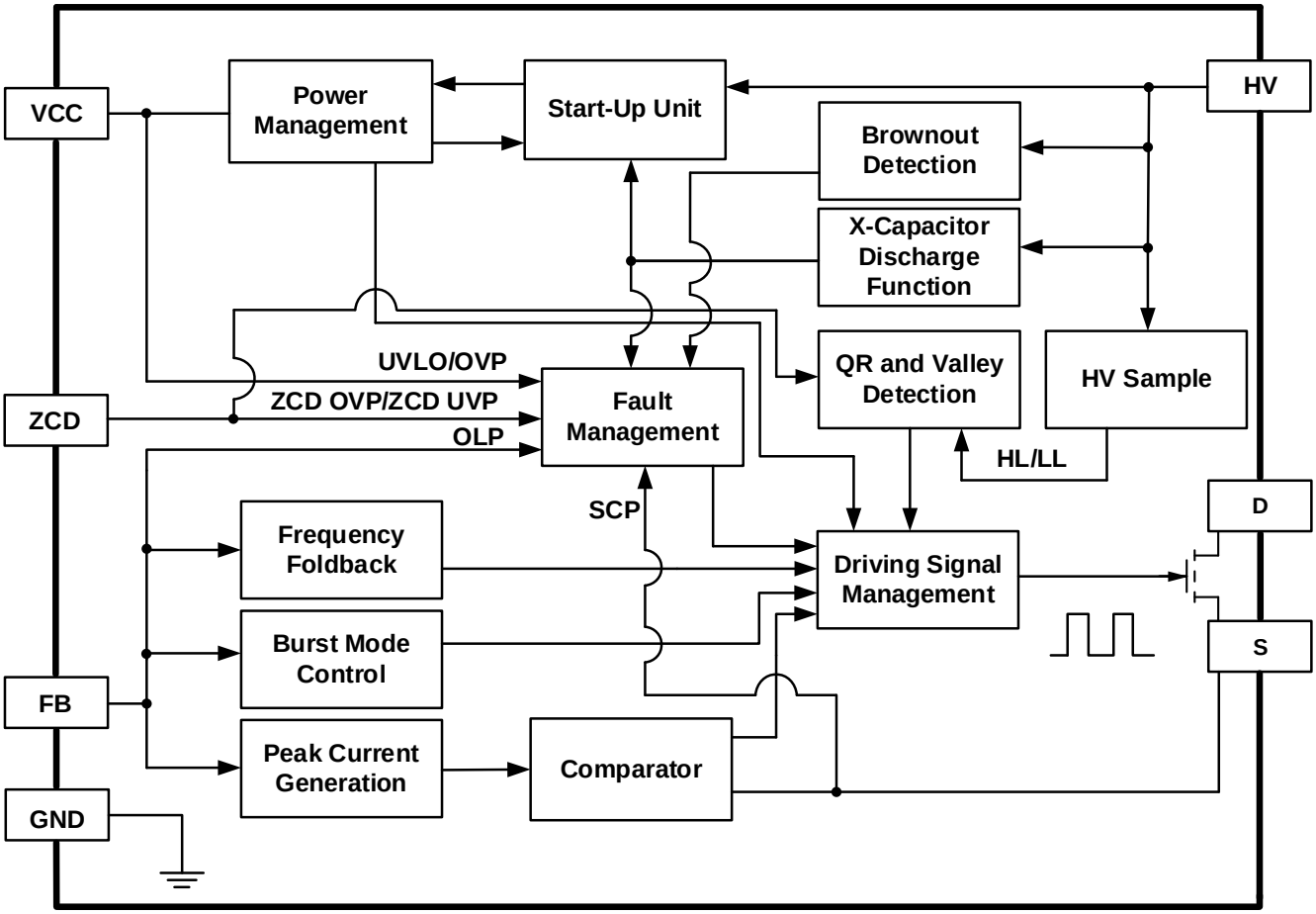


Figure 1: Functional Block Diagram

OPERATION

The HFG610-45 is a high-frequency, quasi-resonant (QR) flyback regulator with an integrated GaN FET and based on peak current mode control. The device runs in QR mode at heavy loads and the valley transfers back and forth smoothly by decreasing the load. Under light loads, the HFG610-45 operates in frequency foldback mode and enters burst mode when the load is extremely light.

For conventional QR control, the switching frequency (f_{SW}) is inverse and proportionate to the system load, leading to a higher f_{SW} at lighter loads and severely deteriorating the light-load efficiency. To improve light-load performance and limit the maximum f_{SW}, the HFG610-45 operates in discontinuous conduction mode (DCM) with frequency foldback, while the minimum f_{SW} is about 30kHz.

The HFG610-45 implements a patented, valley-locked circuit with proper hysteresis to prevent jumping back and forth between two adjacent valleys. Based on the proposed control scheme, the operation always stays in the selected valley until there is a significant change in the output power (P_{OUT}).

Internal High-Voltage Start-Up Circuit with Brown-In (BI) and Brownout (BO) Detection (HV Pin)

Initially, the IC is self-supplied by the internal high-voltage current source via the HV pin. The charge current is divided into two segments. If the VCC voltage (V_{CC}) is below the transition between the HV supply currents (V_{CC_LC}), then the charging current is limited by the HV supply current ($I_{HV\_SP\_SC}$, typically 1mA) to protect the IC from breaking in certain fault conditions, such as if V_{CC} is shorted to GND. When V_{CC} exceeds V_{CC_LC}, the charging current increases to its normal level (I_{HV_SP}, minimum 4.5mA) to ensure V_{CC} charges up as quickly as possible.

As soon as V_{CC} reaches the HV supply current (I_{HV_SP}) turn-off voltage (V_{CC_IOFF}, typically 17.5V), the IC turns off the current source. Then it begins detecting the voltage on the HV pin. Once the HV voltage (V_{HV}) exceeds the brown-in voltage threshold (V_{HV_ON}, typically 105V), V_{CC} charges up again via the HV current source. When V_{CC} reaches V_{CC_IOFF} again, the HFG610-45 begins switching. The recharge before V_{CC} drops to the minimum operating voltage (V_{CC_MIN}, typically 8V), which guarantees the maximum start-up period. When the IC starts switching and V_{OUT} reaches a sufficient level, the transformer's auxiliary winding takes over the IC supply. If V_{CC} falls back to V_{CC_MIN}, the switching pulse stops and the HV current source turns on again. Figure 2 shows the typical waveforms for the HV charge and V_{CC} under-voltage lockout (UVLO).

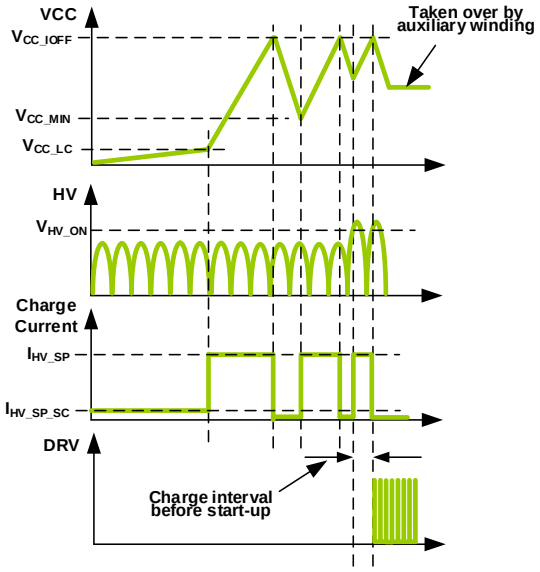


Figure 2: Start-Up with Brown-In and Brownout Detection

Soft Start (SS)

To reduce the stress on power components and smoothly establish V_{OUT}, the HFG610-45 employs soft start (SS). Figure 3 shows the peak current limit gradually increasing from the minimum current-sense voltage (V_{CS_MIN}) to the maximum current-sense voltage (V_{CS_MAX}) during start-up, unless feedback takes over.

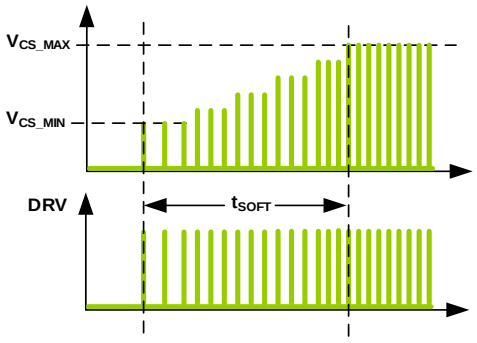


Figure 3: Soft Start

Frequency Modulation and Peak Current Mode Control

When the load becomes lighter for conventional QR control, f_{SW} rises and decreases light-load efficiency. The HFG610-45 adopts a novel form of QR control, in which the pulse-frequency modulation (PFM) signal is generated to control f_{SW} and the valley detection signal. This novel QR control method achieves frequency foldback to prevent an undesirably high f_{SW} at light loads and boost efficiency.

Figure 4 shows the f_{SW} vs. feedback voltage (V_{FB}) curve with patented QR control.

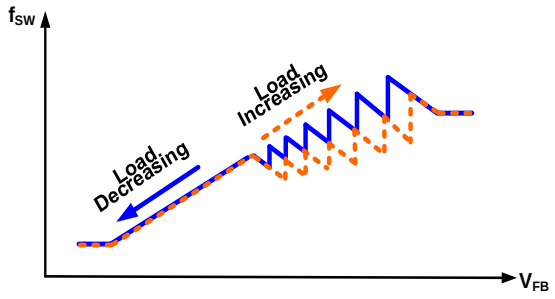


Figure 4: f_{SW} vs. V_{FB}

The HFG610-45 adopts peak current mode for on-time control via the S pin. The CS reference voltage (V_{REF}) is also regulated by V_{FB}, along with the V_{CS_MAX} maximum amplitude and the V_{CS_MIN} minimum value. Figure 5 shows the V_{REF} amplitude reducing as the frequency decreases.

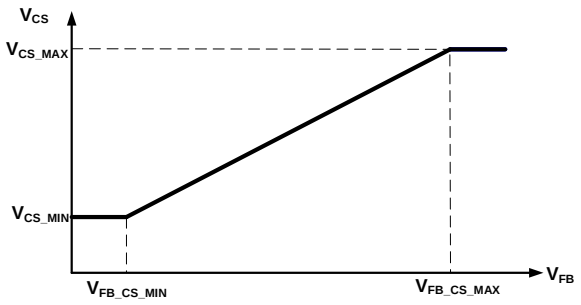


Figure 5: Current Limit Modulation vs. V_{FB}

Valley-Lock Quasi-Resonant (QR) Control

Unlike conventional QR control, the turn-on valley jumps between adjacent valleys many times in one line cycle. The HFG610-45 locks the turn-on valley under certain load condition to avoid the audible noise by valley jumping.

The valley signal generates a time window by detecting the zero-current detection (ZCD) voltage (V_{ZCD}) and comparing it with the internal ZCD threshold (V_{ZCD_TH}). When V_{ZCD} is below V_{ZCD_TH}, the main switch's drain-to-source voltage has reached its valley. Figure 6 shows the valley signal generation.

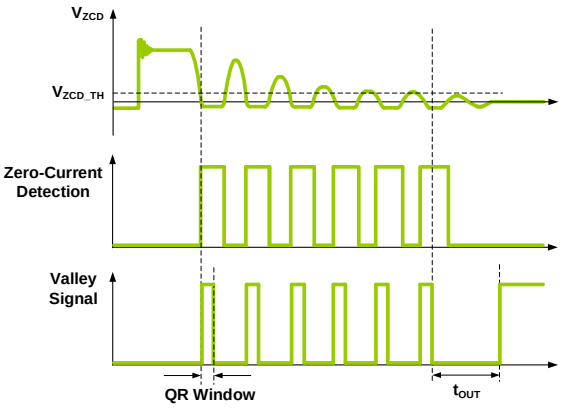


Figure 6: QR Signal Generation

The HFG610-45 monitors the PFM signal by recording the previous turn-on valley and inserting a hysteresis surrounding the PFM signal. If the PFM signal goes high within the hysteresis, the device keeps turning on the driver at the same valley. If the PFM signal goes high ahead of the hysteresis, the device turns on the driver at the valley following the PFM signal. If the PFM signal goes high after the hysteresis, the turn-on valley moves backwards. The turn-on valley can be locked using this method.

Forced Burst Mode

Since both peak current and a minimum frequency are limited, a burst mode is required to keep the power continuously down to zero. The HFG610-45 enters burst mode with switching off when V_{FB} drops below the V_{BUR_IN} (typical 0.7V), and recovers switching when V_{FB} exceeds V_{BUR_OUT} (typical 0.8V).

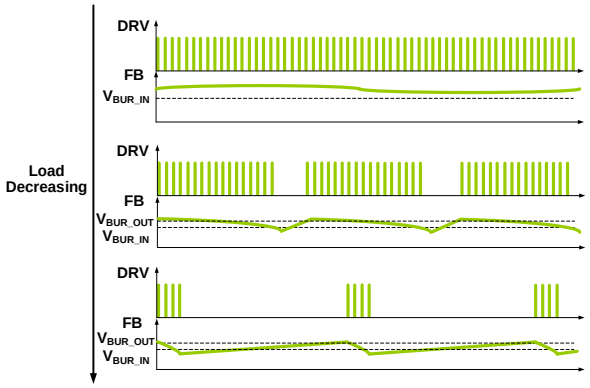


Figure 7: Forced Burst Mode

X-Capacitor Discharger

X-capacitors are typically positioned across a power supply's input terminals to filter differential mode EMI noise. These components alone might present a safety hazard because they can store unsafe levels of high-voltage energy for long periods of time after the AC supply is disconnected. To be compliant with safety standards, use resistors in parallel with the X-capacitor across the AC line to provide a discharge path.

However, these discharge resistors produce a constant power loss while the AC is connected, and contribute significantly to no-load and standby input power consumption. When the AC voltage is applied, the internal high-voltage current source turns off to block the HV current, and the HFG610-45 monitors V_{HV}. If it detects there is no AC voltage supplied during the line voltage removal detection time (t_{LINE_RDET}, typically 96ms), then the HFG610-45 starts discharging for the discharge time (t_{LINE_DIS}, typically 144ms) with the discharge current (I_{DIS_HV}, minimum 4.2mA). Then it resumes normal operation. After the first discharge, the I_{DIS_HV} source turns off for the line voltage detection time (t_{LINE_DET}, typically 48ms) and detects whether the input is plugged back into the AC line. If the AC input remains disconnected, the HFG610-45 continues discharging for t_{LINE_DIS}, then turns off for t_{LINE_DET} to continue detecting until V_{HV} is below V_{CC}. Figure 8 shows the X-capacitor discharge behavior.

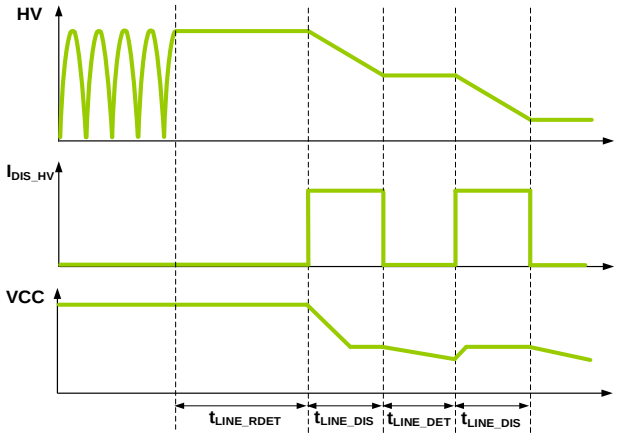


Figure 8: X-Capacitor Discharger

This approach provides an intelligent discharge path for the X-capacitor, eliminating the power loss from external discharge resistors.

Frequency Jittering

Frequency jittering reduces EMI by spreading energy across the frequency jitter range. A low-frequency ramp is added onto the peak current reference. Figure 9 shows the jittering amplitude (ΔV_{CS}) remaining proportional between the peak current as it is regulating and the jittering period (t_{JITTER}, typically 32 switching cycles).

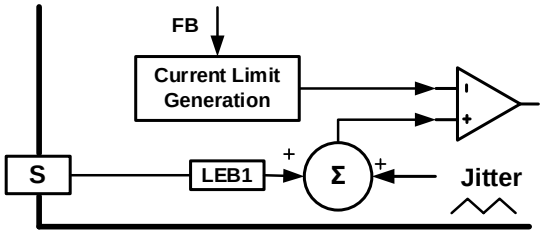


Figure 9: Frequency Jittering

The jitter is removed once the IC enters burst mode.

Leading-Edge Blanking (LEB)

To avoid the parasitic capacitance prematurely terminating the switching pulse, an internal leading-edge blanking (LEB) unit is employed between the S pin and the current comparator input. During the blanking time, the current comparator is disabled and cannot turn off the GaN FET. LEB is divided as LEB for a normal current limit (t_{LEB_L}, typically 200ns) and LEB for the current limit during fault conditions (t_{LEB_S}, typically 150ns).

Protections

The HFG610-45 provides full protection features to guarantee reliability and robustness. There are two protection modes integrated in the HFG610-45 for different features. In auto-recovery mode, if a protection is triggered, switching stops immediately and V_{CC} drops. Once V_{CC} drops to the V_{CC} release level after auto-recovery (V_{CC_PRO}), the protection flag resets and the HV current source begins charging the VCC capacitor (C_{VCC}). Then the HFG610-45 resumes normal operation. In latch-off mode, the switching stops, and the protection flag can only be reset once V_{CC} drops to the V_{CC} release level after latch-off mode (V_{CC_LATCH}) by unplugging the input terminal.

Under-Voltage Lockout (UVLO)

If V_{CC} falls below V_{CC_MIN} (typically 8V), UVLO immediately stops the regulator from switching, and recharges V_{CC} via the HV current source. If this protection occurs, it resets once V_{CC} falls below V_{CC_PRO} (typically 6.3V). In this case, the HV current source is enabled once V_{CC} is below V_{CC_PRO}.

Short-Circuit Protection (SCP)

The current flowing through the CS resistor can increase sharply. It can greatly exceed V_{CS_MAX} (typically 0.4V) after t_{LEB_L} (typically 200ns) under some fault conditions, such as the transformer winding short. Such a high current may cause system damage. To avoid system damage, t_{LEB_S} (typically 150ns) is recommended to prevent the current from being too high.

The HFG610-45 does not enter short-circuit protection (SCP) immediately when V_{CS} exceeds the SCP threshold (V_{SCP}, typically 0.65V) after t_{LEB_S}. The device stops switching for the second SCP blanking time (t_{SCP}, typically 130µs), then starts switching again. If the HFG610-45 detects 8 consecutive pulses where V_{CS} exceeds V_{SCP}, SCP is triggered. Otherwise, the HFG610-45 resumes normal operation. SCP can be immune to the surge test.

Over-Temperature Protection (OTP)

To prevent lethal thermal damage, the HFG610-45 shuts down the switching cycle if the internal temperature exceeds 150° C. Once the internal temperature drops below 110°C, the power supply resumes operation.

V_{CC} Over-Voltage Protection (OVP)

V_{CC} over-voltage protection (OVP) protects system operation. If V_{CC} exceeds the OVP level (V_{CC_OVP}, typically 53V) for the V_{CC} OVP delay time (t_{VCC_OVP}, typically 23µs), then V_{CC} OVP is triggered.

Current-Sense Short Protection (SSP)

During start-up, if V_{CS} cannot reach the V_{CS} threshold for CS short circuit (V_{SHORT}, typically 45mV) after the CS short detection time (t_{SSP}, typically 3.5µs), a short-circuit condition is detected and the device latches off.

ZCD Over-Voltage Protection (ZCD OVP) and Under-Voltage Protection (ZCD UVP)

The positive plateau of the auxiliary winding voltage is proportional to the output voltage (V_{OUT}). ZCD over-voltage protection (ZCD OVP) and ZCD under-voltage protection (ZCD UVP) use the auxiliary winding voltage instead of monitoring V_{OUT} directly. Figure 10 shows the ZCD OVP and ZCD UVP block.

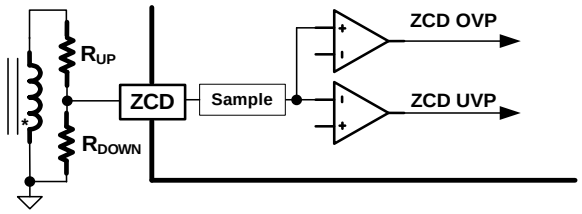


Figure 10: ZCD OVP and ZCD UVP Circuit

The plateau voltage (V_{ZCD}) can be calculated with Equation (1):

$$V_{ZCD} = \frac{V_{OUT} \times N_{AUX}}{N_S} \times \frac{R_{DOWN}}{R_{DOWN} + R_{UP}} \quad (1)$$

Where N_{AUX} is the transformer's auxiliary winding turns, and N_S is the transformer's secondary winding turns.

When V_{ZCD} reaches the ZCD OVP threshold (V_{ZCD_OVP}, typically 12.2V) for three consecutive cycles, ZCD OVP is triggered (see Figure 11).

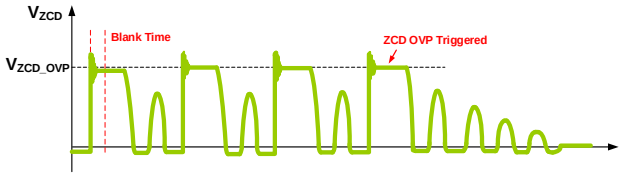


Figure 11: ZCD OVP Voltage Sampling

If the voltage sampled on the ZCD pin is below the ZCD UVP threshold (V_{ZCD_UVP}, typically 0.4V) for t_{ZCD_UVP}, except during the SS period, then ZCD UVP is triggered (see Figure 12).

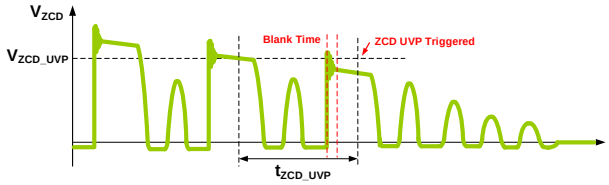


Figure 12: ZCD UVP Voltage Sampling

To avoid mistriggers due to the oscillation of the leakage inductance and the parasitic capacitance, both ZCD OVP and ZCD UVP sampling have a blanking time.

Overload Protection (OLP)

If f_{SW} is fixed in the flyback converter, the maximum P_{OUT} is limited by the peak current. If P_{OUT} exceeds the power limit, V_{OUT} drops below the set value. This reduces the current through the optocoupler, and V_{FB} is pulled high. If V_{FB} exceeds the overload protection (OLP) voltage (V_{OLP}), it is considered an error flag and the internal timer begins counting. If the timer reaches the time duration before OLP (t_{OLP}, typically 50ms), OLP is triggered and the HFG610-45 stops switching. If the error flag is removed during the count period, the timer resets. This timer duration excludes the SS time (t_{SS}). The OLP timer can avoid protection mistriggers during normal load transients.

APPLICATION INFORMATION

Selecting the VCC Capacitor (C_{VCC})

Figure 13 shows the start-up circuit.

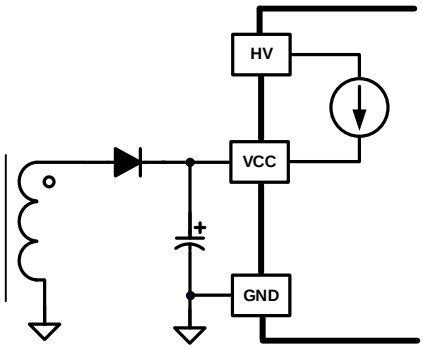


Figure 13: Start-Up Circuit

The HV pin initially charges the supply voltage (V_{CC}). When V_{CC} reaches the HV supply current turn-off voltage (V_{CC_IOFF}), the HV pin stops charging V_{CC} and the IC starts to operate. To guarantee successful start-up, V_{OUT} should be set up before V_{CC} drops to the minimum operating voltage (V_{CC_MIN}). For most applications, choose a VCC capacitance (C_{VCC}) to be about 22μF. To ensure safe operation across the entire input and output range, especially under no-load conditions, V_{CC} should have some margin. It is recommended to have a minimum V_{CC} that is about 1V greater than V_{CC_MIN}. The recommended C_{VCC} can be calculated with Equation (2):

$$C_{VCC} > \frac{I_{OP} \times t_{START\_UP}}{V_{CC\_IOFF} - (V_{CC\_MIN} + 1)} \quad (2)$$

Designing the Transformer

Table 1 shows the calculation procedure for a typical 45W application inductance.

Table 1: Calculation for Typical 45W Application

Parameter	Symbol	Value
Input AC RMS voltage	V_{AC}	90V_{AC} to 265V_{AC}
Output voltage	V_{OUT}	15
Output current	I_{OUT}	3A
Efficiency	η	92%
Maximum switching frequency	f_{SW}	130kHz

The input power (P_{IN}) can be estimated with Equation (3):

$$P_{IN} = \frac{V_{OUT} \times I_{OUT}}{\eta} \quad (3)$$

According to the power device's voltage rating and selecting turns ratio, a proper N_{PS} should satisfy Equation (4) and Equation (5):

$$\sqrt{2}V_{AC\_MAX} + N_{PS} \times V_{OUT} + V_{SPIKE\_PRI} \le 0.9V_{BV\_PRI} \quad (4)$$

$$\frac{\sqrt{2}V_{AC\_MAX}}{N_{PS}} + V_{OUT} + V_{SPIKE\_SEC} \le 0.9V_{BV\_SEC} \quad (5)$$

In this application N_{PS} is selected as 6.

The converter's duty cycle can be calculated with Equation (6):

$$D = \frac{N_{PS} \times V_{OUT}}{\sqrt{2}V_{AC} + N_{PS} \times V_{OUT}} \quad (6)$$

According to the HFG610-45's mode, the switching frequency (f_{SW}) increases as the input voltage (V_{IN}) increases, but a higher frequency means more switching loss and EMI. The HFG610-45 cannot turn on at the first valley in high line (see Figure 14).

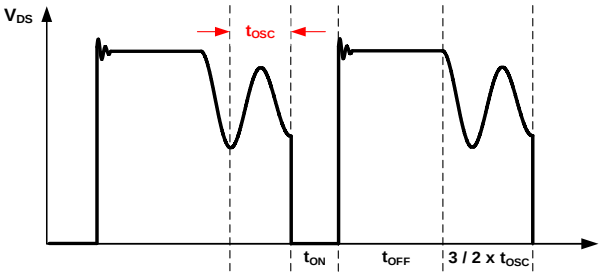


Figure 14: Switching Period in High Line

Where t_{OSC} is the discontinuous conduction mode (DCM) oscillation period, and is related to the inductance (L) and parasitic parameters. The maximum switching frequency (f_{SW}) is 130kHz, and the oscillation period can be estimated to be 1.2μs. The switching period can be calculated with Equation (7):

$$\frac{1}{f_{SW}} = t_{ON} + t_{OFF} + \frac{3}{2}t_{OSC} \quad (7)$$

The on time (t_{ON}) and off time (t_{OFF}) for the duty cycle also satisfy Equation (8):

$$\frac{t_{ON}}{t_{OFF}} = \frac{D_{MIN}}{1-D_{MIN}} \quad (8)$$

In DCM flyback topology, Equation (9) and Equation (10) can be derived as follows:

$$P_{IN} = \frac{1}{2} L \times f_{SW} \times I_{PK}^2 \quad (9)$$

$$I_{PK} = \frac{\sqrt{2} V_{AC\_MAX}}{L} \times t_{ON} \quad (10)$$

For Equation (3), Equation (4), Equation (5), Equation (6), Equation (7), Equation (8), Equation (9), and Equation (10), L can be calculated with Equation (11):

$$L = \frac{f_{SW} \times (\sqrt{2} V_{AC\_MAX})^2 \times D_{MIN}^2}{2 \times P_{IN}} \left(\frac{1}{f_{SW}} - \frac{3}{2} t_{OSC} \right)^2 \quad (11)$$

Where L is 300μH.

After calculating L, it is necessary to calculate the maximum inductor current (I_{PK_MAX}) before calculating the turns. According to the HFG610-45's mode, the inductor current (I_L) reaches its maximum when the input capacitor voltage drops to its lowest point (V_{DC_MIN}). At low line, the device locks the first valley (see Figure 15).

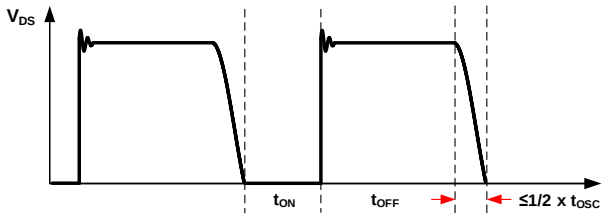


Figure 15: Switching Period in Low Line

Similarly, for Equation (3), Equation (4), Equation (5), Equation (6), Equation (7), Equation (8), Equation (9), and Equation (10), I_{PK_MAX} can be calculated with Equation (12):

$$I_{PK\_MAX} = \frac{V_{DC\_MIN} \times D_{MAX}}{L} \left(\frac{L \times I_{PK\_MAX}^2}{2 \times P_{IN}} - \frac{t_{OSC}}{2} \right) \quad (12)$$

Since 1/2 x t_{OSC} is a small value, it can be ignored; Equation (12) can be simplified with Equation (13):

$$I_{PK\_MAX} = \frac{2 \times P_{IN}}{V_{DC\_MIN} \times D_{MAX}} \quad (13)$$

I_{PK_MAX} should be below the continuous DS current (typically 2.8A at 125°C). After calculating L and I_{PK_MAX} according to the magnetic core parameter, N_P and N_S can be calculated.

Selecting the Current-Sense Resistor

The HFG610-45's maximum current-sense voltage (V_{CS_MAX}) is 0.4V, meaning the current-sense resistor (R_{SENSE}) can be calculated with Equation (14):

$$R_{SENSE} = \frac{V_{CS\_MAX}}{I_{PK\_MAX}} \times 0.9 \quad (14)$$

The selected R_{SENSE} should ensure that I_{PK_MAX} is below the continuous DS current (typically 2.8A at 125°C).

Selecting the ZCD Divider Resistor

The ZCD pin integrates ZCD over-voltage protection (ZCD OVP). Suitable divider resistors should guarantee that ZCD OVP and ZCD UVP do not mistrigger and the ZCD OVP voltage is not too high. It is recommended for V_{ZCD} to be below 0.8 x V_{ZCD_OVP}, and V_{ZCD} to exceed V_{ZCD_UVP}. V_{ZCD} can be calculated with Equation (15):

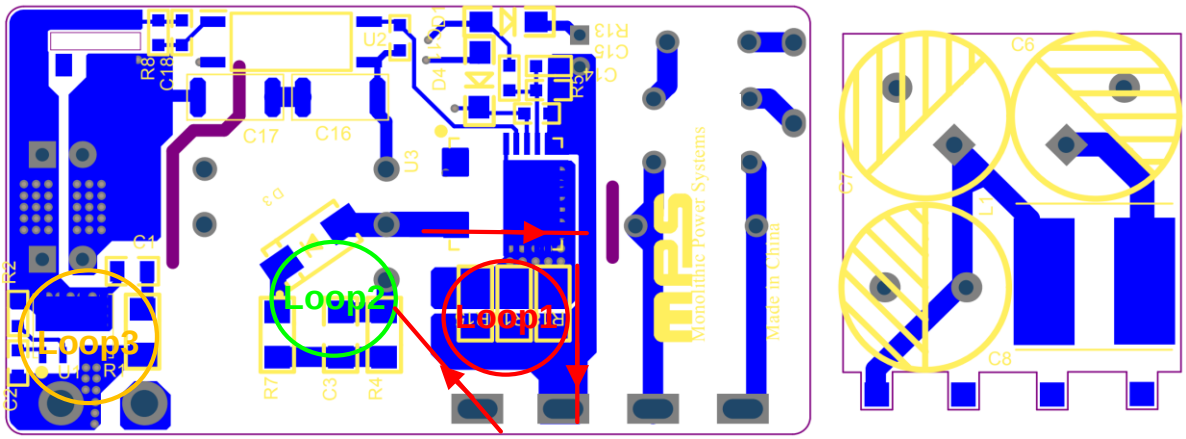
$$V_{ZCD} = \frac{V_{OUT} \times N_{AUX}}{N_S} \times \frac{R_{DOWN}}{R_{DOWN} + R_{UP}} \quad (15)$$

Where N_{AUX} is the transformer's auxiliary winding turns, and N_S is the transformer's secondary winding turns.

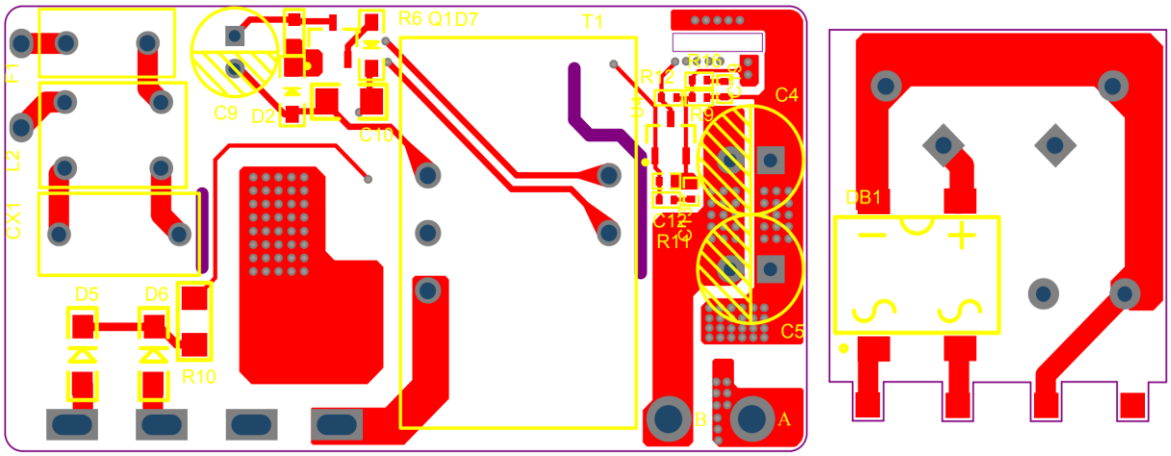
PCB Layout Guidelines

Efficient PCB layout is critical for achieving reliable operation and excellent EMI performance. For the best results, refer to Figure 16 and follow the guidelines below:

1. Minimize the power stage loop area, including the primary power loop (Loop 1), the snubber loop (Loop 2), and the secondary power loop (Loop 3).
2. Separate the IC GND and power GND.
3. Place the decoupling capacitors for VCC, FB, and ZCD close to the IC.
4. Route the EMI filter far away from the hopping point.



Bottom Layer



Top Layer

Figure 16: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

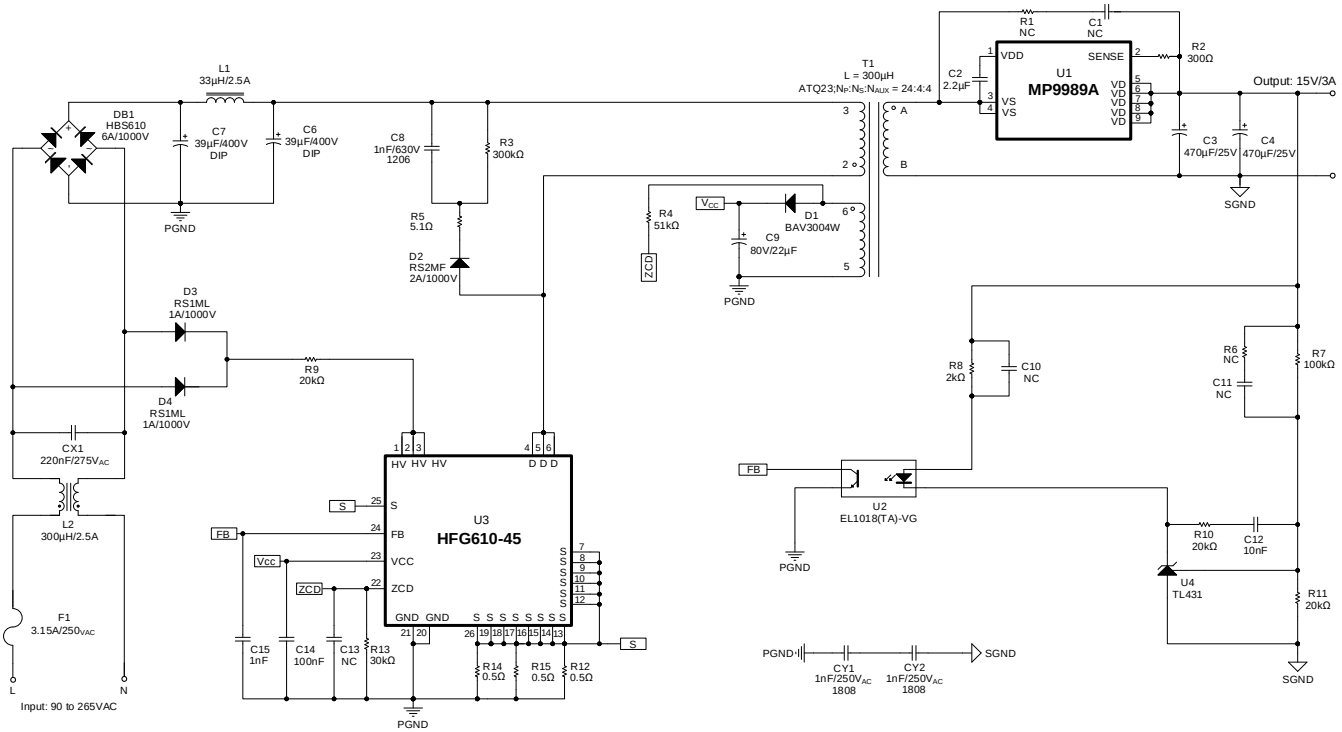
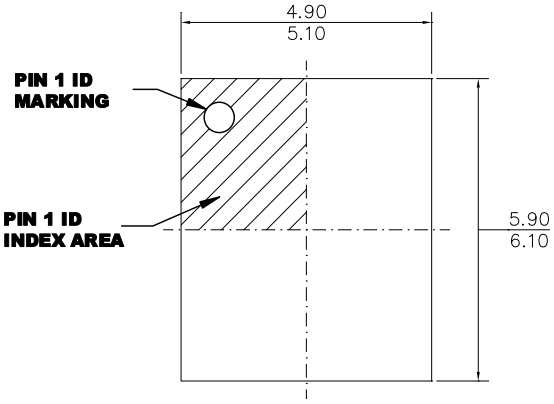


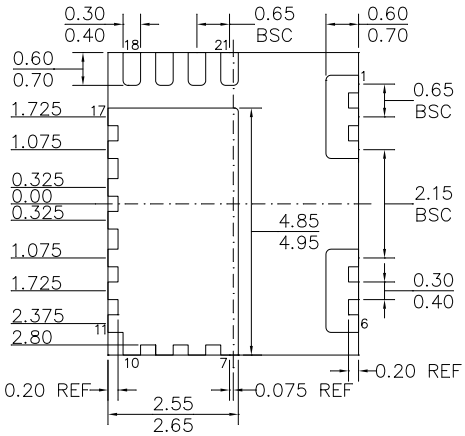
Figure 17: Typical Application Circuit (45W Output and Universal Input)

PACKAGE INFORMATION

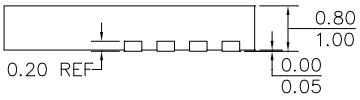
QFN-21 (5mmx6mm)



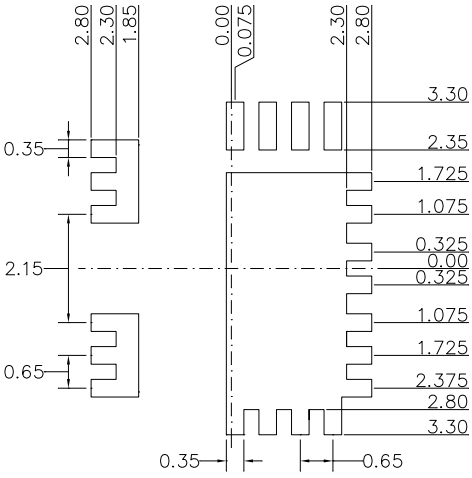
TOP VIEW



BOTTOM VIEW



SIDE VIEW



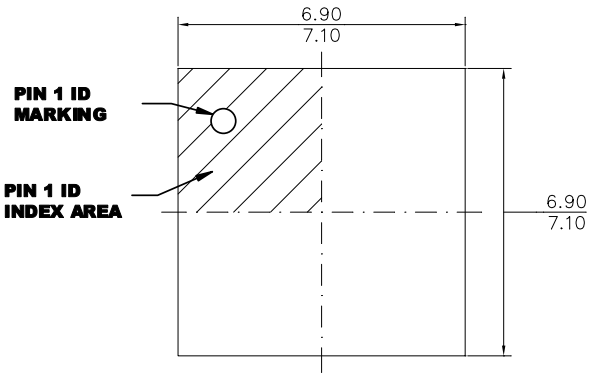
RECOMMENDED LAND PATTERN

NOTE:

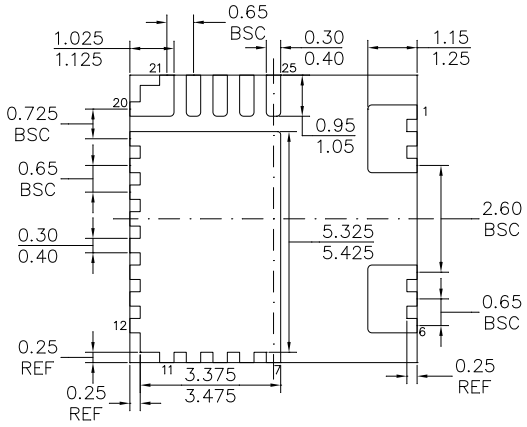
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION *(continued)*

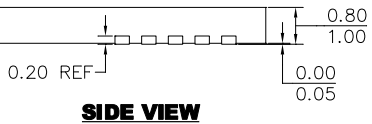
QFN-25 (7mmx7mm)



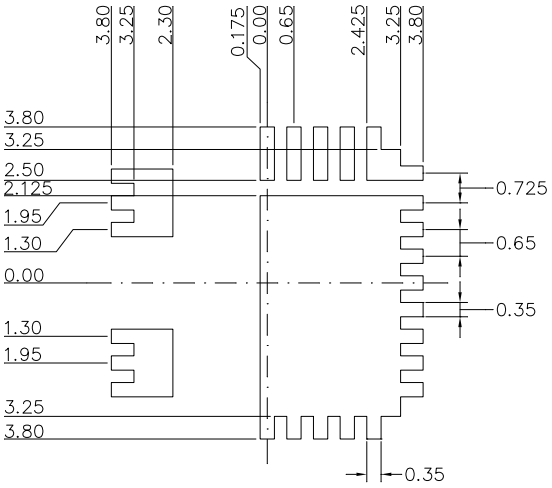
TOP VIEW



BOTTOM VIEW



SIDE VIEW



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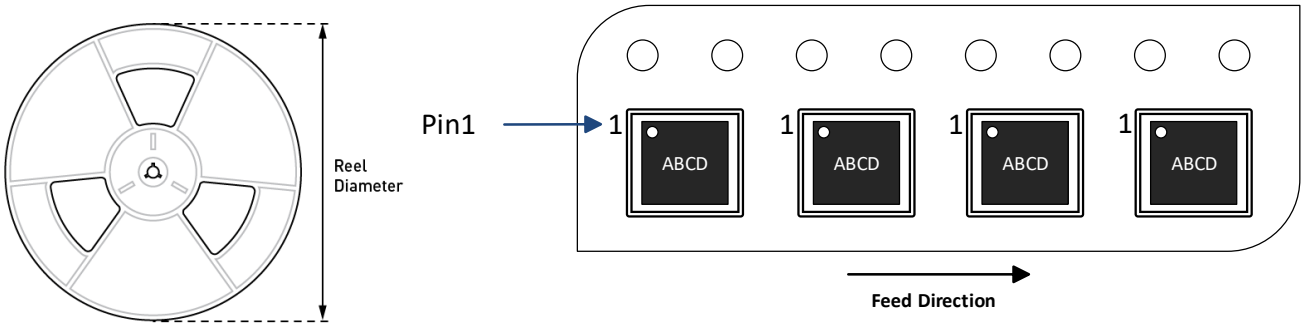
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
HFG610GQJ-45-Z	QFN-21 (5mmx6mm)	5000	N/A	N/A	13in	12mm	8mm
HFG610GQN-45-Z	QFN-25 (7mmx7mm)	2500	N/A	N/A	13in	16mm	12mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	12/6/2024	Initial Release	-