EVQ8785-MJ-2PHASE-01A

16V, 40A, 2-Phase, Scalable, Digital, Synchronous Step-Down Converter with PMBus Evaluation Board

DESCRIPTION

The EVQ8785-MJ-2PHASE-01A is an evaluation board designed to demonstrate the capabilities of the MPQ8785, a fully integrated, PMBus-compatible, high-frequency, synchronous buck converter. The MPQ8785 offers a very compact solution that achieves up to 40A of output current (I_{OUT}) per phase, with excellent load and line regulation across a wide input supply range.

The MPQ8785 achieves high efficiency across a wide I_{OUT} load range. The PMBus interface provides the converter configurations and monitors key parameters.

The MPQ8785 adopts MPS's proprietary, digital, multi-phase constant-on-time (MCOT) control to provide fast transient response and eases loop stabilization. The MCOT scheme also allows multiple MPQ8785 devices to be connected in parallel, with excellent current sharing and phase interleaving for high-current applications.

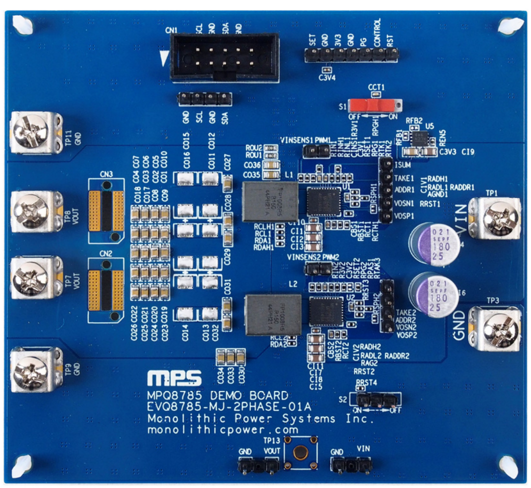
Fully integrated protection features include over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), and over-temperature protection (OTP).

The MPQ8785 requires a minimal number of readily available, standard external components, and is available in a TLGA (5mmx6mm) package.

PERFORMANCE SUMMARY

Parameters	Conditions	Value
Input voltage (V_{IN}) range		3.1V to 16V
Output voltage (V_{OUT})		0.35V to 5.5V
Maximum output current (I_{OUT})		80A
Switching frequency (f_{SW})		300kHz to 2MHz

EVQ8785-MJ-2PHASE-01A EVALUATION BOARD



LxW (101.6mmx92.7mm)

Board Number	MPS IC Number
EVQ8785-MJ-2PHASE-01A	MPQ8785

QUICK START GUIDE

The EVQ8785-MJ-2PHASE-01A evaluation board has an input voltage (V_{IN}) between 3.1V and 16V. The MP2015AGQ-33 provides a 3.3V VCC bias supply (V_{CC}). Due to the MP2015AGQ-33's characteristics, the device only works when V_{IN} exceeds 4.3V and does not require an external 3.3V power supply. When V_{IN} is between 3.1V and 4.3V, an external 3.3V power supply is required.

The MPQ8785's internal registers can be configured via a PMBus interface using MPS's graphic user interface (GUI). This evaluation board can be connected to the interface with a 10-pin connection. For more information, refer to the MPQ8785's GUI user guide.

To start up the EVQ8785-MJ-2PHASE-01A, follow the steps below:

1. Connect the PMBus communication interface to the evaluation board and computer.
2. Connect the load terminals to:
   a. Positive (+): VOUT
   b. Negative (-): GND
3. Preset the power supply output voltage (V_{OUT}) between 3.1V and 16V, then turn the power supply off.
4. Connect the power supply output terminals to:
   a. Positive (+): VIN
   b. Negative (-): GND
5. Ensure that the power supply's current limit is sufficiently high to supply the required power.
6. If V_{IN} on the evaluation board is between 3.1V and 4.3V, connect an external 3.3V power supply to the 3V3 test pin.
7. Turn the power supply on after making the connections.
8. Turn on the EN switch (S1) to enable the CTRL signal. The board should automatically start up.
9. Configure the IC register with the GUI.

EVALUATION BOARD SCHEMATIC

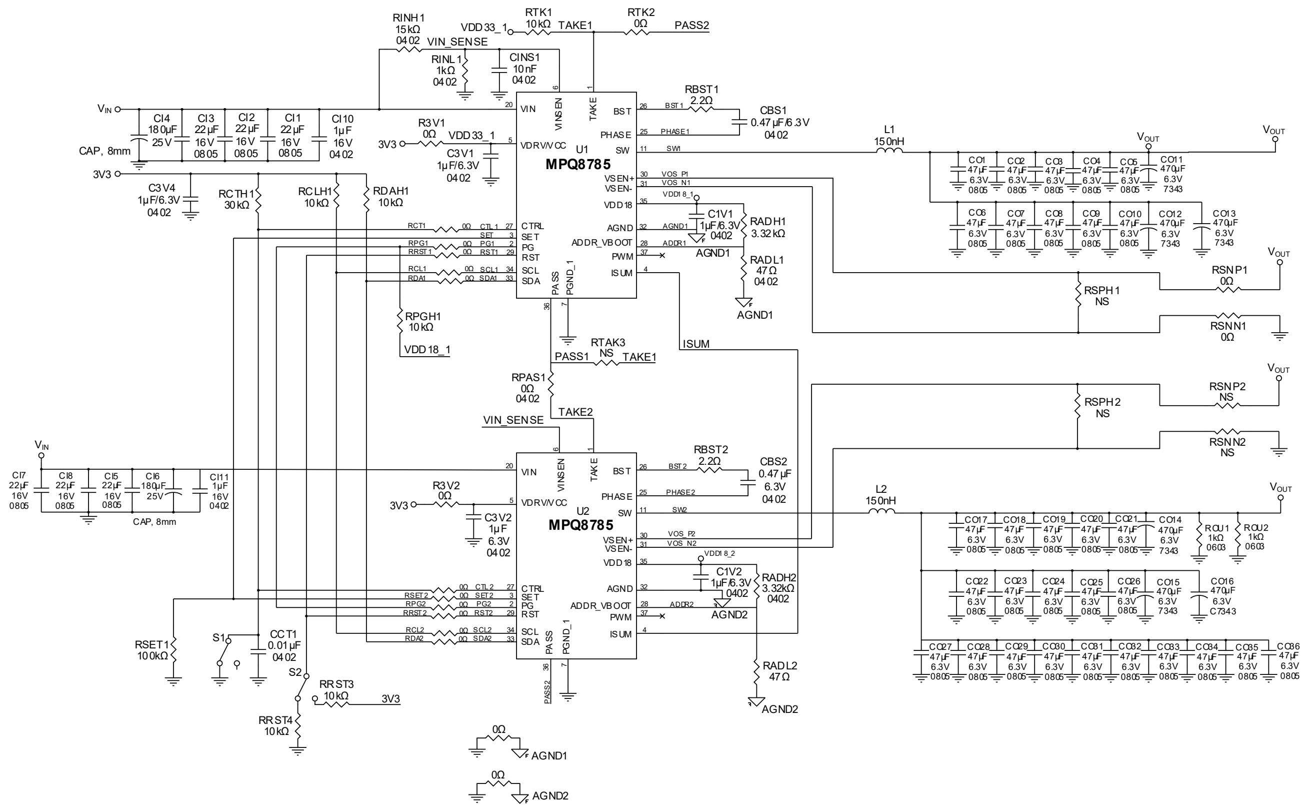


Figure 1: Evaluation Board Schematic

EVQ8785-MJ-2PHASE-01A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
2	CBS1, CBS2	0.22µF	Ceramic capacitor, 16V, X7R, 20%	0402	Murata	GRM155R71C224KA12D
1	COTP1	1nF	Ceramic capacitor, 50V, X7R, 10%	0402	Any	Any
5	C1V1, C1V2, C3V1, C3V2, C3V4	1µF	Ceramic capacitor, 6.3V, X7R, 10%	0402	Any	Any
2	CCT1, CINS1	10nF	Ceramic capacitor, 50V, X7R, 10%	0402	Any	Any
6	CI1, CI2, CI3, CI5, CI7, CI8	22µF	Ceramic capacitor, 25V, X6S, 10%	0805	Murata	GRM21BR61E226ME44L
2	CI10, CI11	1µF	Ceramic capacitor, 16V, X6S, 10%	0402	Murata	GRM155C81C105KE11D
2	CI4, CI6	180µF	Aluminum solid capacitor, 25V	DIP	Panasonic	25SEPF180M
30	CO1, CO2, CO3, CO4, CO5, CO6, CO7, CO8, CO9, CO10, CO17, CO18, CO19, CO20, CO21, CO22, CO23, CO24, CO25, CO26, CO27, CO28, CO29, CO30, CO31, CO32, CO33, CO34, CO35, CO36	47µF	Ceramic capacitor, 6.3V, X6S, ±10%	0805	Murata	GRM21BR60J476ME15L
6	CO11, CO12, CO13, CO14, CO15, CO16	NS				
1	CI9	10µF	Ceramic capacitor, 16V, X5R, 20%	0805	Murata	GRM21BC71C106KE11L
1	C3V3	22µF	Ceramic capacitor, 6.3V, X5R, 20%	0805	Murata	GRM21BR60J226ME39L
2	L1, L2	150nH	Power inductor, 10%	SMD	Eaton	FP1008R5-R150-R
3	PA1L1, PA1L2, PA1L3	NS				
2	RADH1, RADH2	3.32kΩ	Thick film resistor, 1%, 1/16W	0402	Any	Any
7	RTK1, RPGH1, RDAH1, RCLH1, RRST3, RRST4, REN5	10kΩ	Thick film resistor, 1%, 1/16W	0402	Any	Any
1	RCTH1	30kΩ	Thick film resistor, 1%, 1/16W	0402	Any	Any

EVQ8785-MJ-2PHASE-01A BILL OF MATERIALS *(continued)*

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
25	RSNP1, RSNN1, RRST1, RPG1, RPAS1, RIN1, RDA1, RCT1, RCL1, RBST1, RADDR1, AGND1, RTK2, RSET2, RRST2, RPG2, RIN2, RDA2, RCT2, RCL2, RBST2, RAG2, RADDR2, R3V1, R3V2	0Ω	Thick film resistor, 5%, 1/16W	0402	Any	Any
2	ROU1, ROU2,	1kΩ	Thick film resistor, 1%	0603	Any	Any
1	RINL1	1kΩ	Thick film resistor, 1%	0402	Any	Any
1	RINH1	15kΩ	Thick film resistor, 1%, 1/16W	0402	Any	Any
2	RADL1, RADL2	47Ω	Thick film resistor, 1%, 1/16W	0402	Any	Any
7	RFB1, RFB2, RTAK3, RSPH1, RSPH2, RSNP2, RSNN2	NS				
1	RSET1	100kΩ	Thick film resistor, 1%, 1/16W	0402	Any	Any
1	U5	MP2015AGQ-33	24V, 150mA, low quiescent current linear regulator	QFN-8 (3mmx 3mm)	MPS	MP2015AGQ-33
2	U1, U2	MPQ8785	16V, 40A, synchronous step-down converter with PMBus	TLGA-37 (5mmx 6mm)	MPS	MPQ8785GMJT-xxxx

DEFAULT SETTING TABLE

Part and Code Number	MPQ8785GMJT-0000	
Output	V_{BOOT}	0.9V
	V_{OUT_MIN}	0.35V
	V_{OUT_MAX}	5.5V
	DVID slew rate	10.4167mV/μs
	f_{SW}	800kHz
Input Voltage (V_{IN})	V_{IN_ON}	2.6V
	V_{IN_OFF}	2V
Soft Start (SS)	Rising on time (t_{ON})	2ms
Soft Shutdown	Falling off time (t_{OFF})	2ms
Output Current (I_{OUT}) Protection	Mode	Hiccup
	OCP_TDC	90A
	OCP_PHASE valley	45A
	NOCP	-20A
Output Voltage (V_{OUT}) Protection	Mode	Hiccup
	V_{OUT_UV}	60% of VID
	V_{OUT_OV}	135% of VID
Temperature Protection	Mode	Hiccup
	OT_FAULT_LIMIT	160°C

PCB LAYOUT

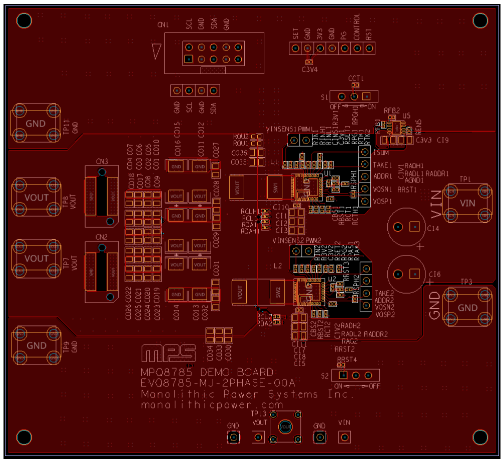


Figure 2: Top Layer

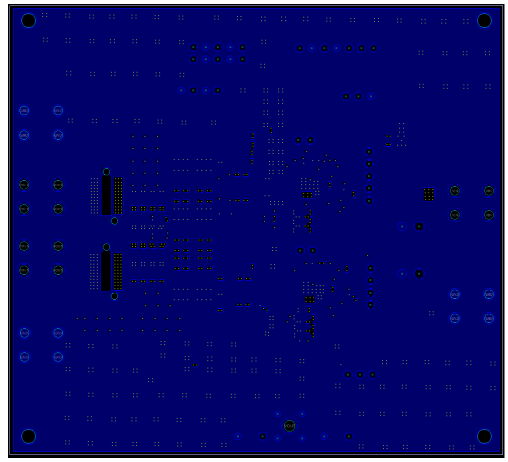


Figure 3: Mid-Layer 1

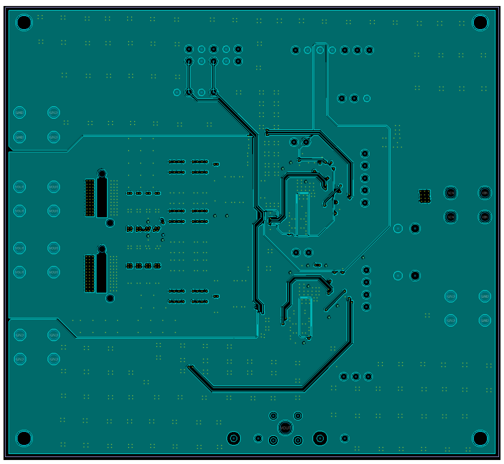


Figure 4: Mid-Layer 2

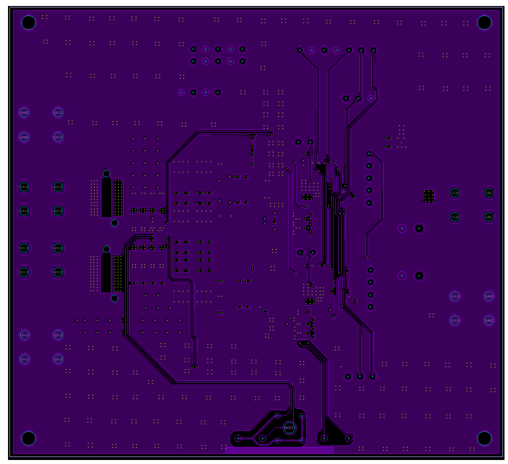


Figure 5: Mid-Layer 3

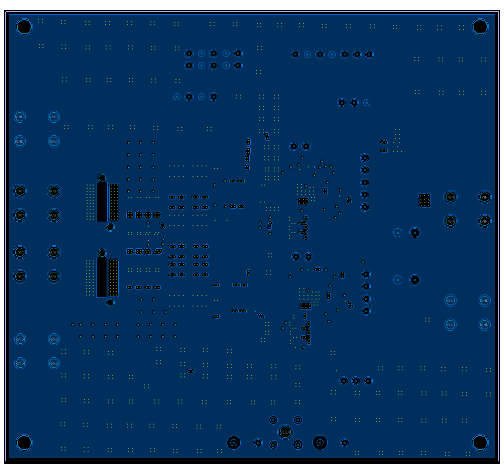


Figure 6: Mid-Layer 4

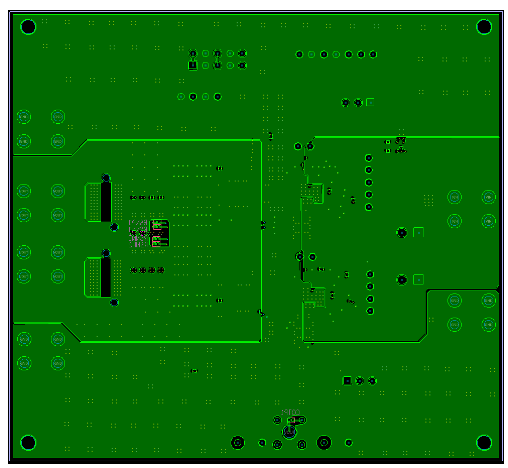


Figure 7: Bottom Layer

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/15/2023	Initial Release	-