EVQ4436-R-00A

45V, 6A, Low I_Q, Synchronous, Step-Down Converter Evaluation Board

DESCRIPTION

The EVQ4436-R-00A evaluation board is designed to demonstrate the capabilities of MPS's MP/MPQ4436.

The MP/MPQ4436 is a frequency-configurable, synchronous, step-down, switching regulator with integrated internal high-side and low-side power MOSFETs. It provides up to 6A of highly efficient output, with current mode control for fast loop response.

The wide 3.3V to 45V input range accommodates a variety of step-down applications in an automotive input environment. A 1.7µA shutdown mode quiescent current allows the part to be used in battery-powered applications.

High power conversion efficiency over a wide load range is achieved by scaling down the switching frequency in light-load conditions to reduce the switching and gate-driving losses.

Frequency foldback prevents inductor current runaway during start-up. Thermal shutdown provides reliable, fault-tolerant operation.

High duty cycle and low dropout mode are provided for automotive cold crank condition.

ELECTRICAL SPECIFICATION

Parameter	Symbol	Value	Units
Input voltage	V_{IN}	3.3 to 45	V
Output voltage	V_{OUT}	3.3	V
Output current	I_{OUT}	6	A

FEATURES

- Wide 3.3V to 45V Operating Voltage Range
- 6A Continuous Output Current
- 1.7µA Low Shutdown Supply Current
- 18µA Sleep Mode Quiescent Current
- Internal 48mΩ High-Side and 20mΩ Low-Side MOSFET
- 350kHz to 530kHz Programmable Switching Frequency for Car Battery Applications
- Synchronize to External Clock
- Multi-Phase Capability
- Out-of-Phase Synchronized Clock Output
- Symmetric V_{IN} for Low EMI
- Power Good Output
- External Soft Start
- 100ns Minimum On Time
- Selectable AAM (Advanced Asynchronous Mode) or FCCM (Continuous Conduction Mode)
- Low Dropout Mode
- Hiccup Over-Current Protection
- Available in a QFN-20 (4mmx4mm) Wettable Flank Package
- AEC-Q100 Grade-1

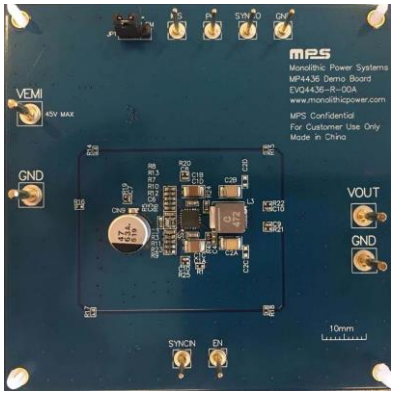
APPLICATIONS

- Infotainment
- Clusters
- Advanced Driver Assistance Systems
- Industrial Power Systems

QUICK START GUIDE

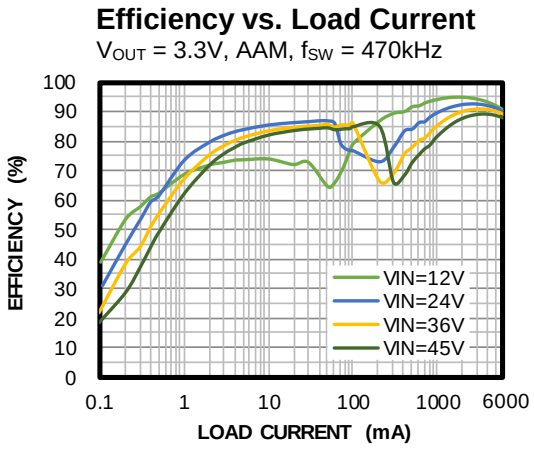
1. Connect the positive and negative terminals of the load to the VOUT and GND pins, respectively. Set the load current between 0A and 6A. Electronic loads represent a negative impedance to the regulator. If they are set to an exceedingly high current, it will trigger over-current or short current protection.
2. Preset the power supply output between 3.3V and 45V, then turn it off. If longer cables are used between the source and the EVB (>0.5m total), install a damping capacitor at the input terminals. This is highly recommended when VEMI ≥ 24V.
3. Connect the positive and negative terminals of the power supply output to the VEMI and GND pins, respectively.
4. Turn the power supply on. The board will automatically start up. The default V_{OUT} is 3.3V.
5. To use the enable function, apply a digital input to the EN pin. Drive EN above 1V to turn on the regulator; drive EN below 0.85V to turn it off.
6. To use the sync function, apply a 350kHz to 530kHz external clock to the SYNCIN pin to synchronize the internal clock's rising edge.
7. JP1 selects forced CCM mode or AAM mode. Connecting pin 2 (mode) to pin 3 (VCC) of JP1 forces the MPQ4436 into forced CCM mode. Connecting pin 1 (GND) to pin 2 (mode) of JP1 forces the MPQ4436 into AAM mode.

EVQ4436-R-00A EVALUATION BOARD

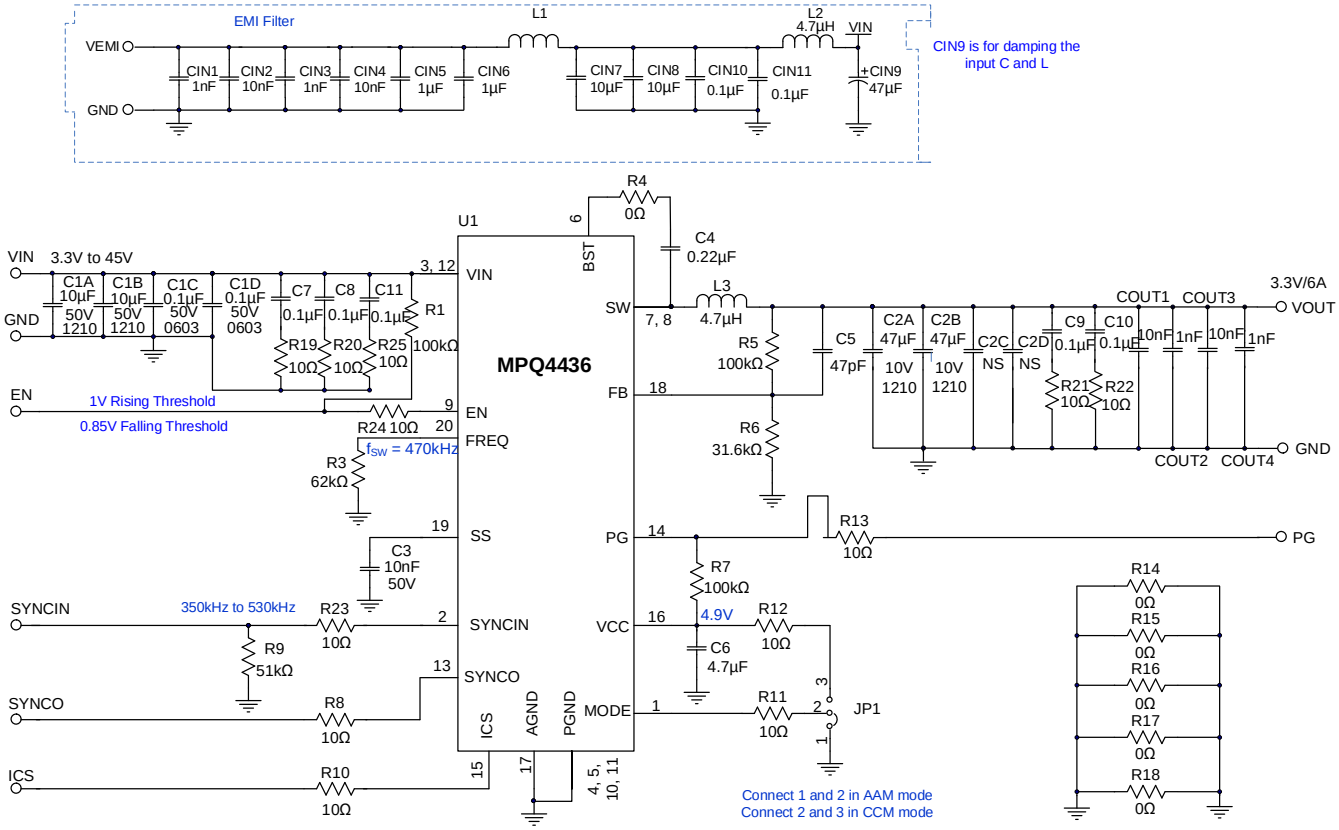


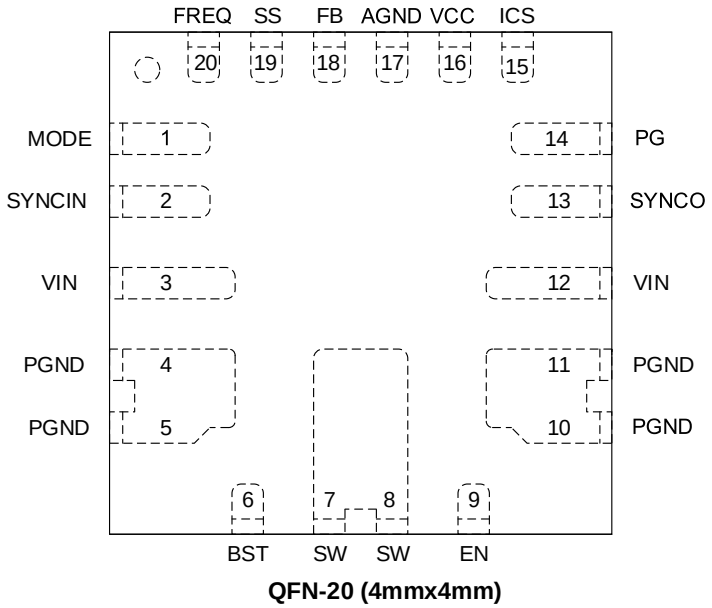
(LxWxH) 9cmx9cmx1.3cm

Board Number	MPS IC Number
EVQ4436-R-00A	MP/MPQ4436GR



EVALUATION BOARD SCHEMATIC





QFN-20 (4mmx4mm)

EVQ4436-R-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufactuer P/N
4	CIN1, CIN3, COUT2, COUT4	1nF	Ceramic capacitor, 50V, X7R	0603	muRata	GRM216R71H102KA01
5	CIN2, CIN4, C3, COUT1, COUT3	10nF	Ceramic capacitor, 50V, X7R	0603	muRata	GRM188R71H103KA01D
2	CIN5, CIN6	1μF	Ceramic capacitor, 50V, X7R	0805	muRata	GRM21BR71H105KA12L
2	CIN7, CIN8	10μF	Ceramic capacitor, 50V, X5R	1206	muRata	GRM31CR61H106KA12L
1	CIN9	47μF	Aluminum capacitor, 63V	SMD	Panasonic	EEE-1JA470UP
2	C1A, C1B	10μF	Ceramic capacitor, 50V, X5R	1210	muRata	GRM32ER61H106KA12L
4	CIN10, CIN11, C1C, C1D	0.1μF	Ceramic capacitor, 50V, X7R	0603	muRata	GCJ188R71H104KA12D
2	C2A, C2B	47μF	Ceramic capacitor, 10V, X5R	1210	muRata	GRM32ER61A476KE20L
1	C4	0.22μF	Ceramic capacitor, 16V, X7R	0603	muRata	GRM188R71C122KA01D
1	C5	47pF	Ceramic capacitor, 50V, COG	0603	TDK	C1608C0G1H470J
1	C6	4.7μF	Ceramic capacitor, 10V, X5R	0603	muRata	GRM188R61A475KE15D
5	C7, C8, C9, C10, C11	0.1μF	Ceramic capacitor, 50V, X7R	0402	muRata	GRM155R71H104KE14D
2	C2C, C2D	NS				
1	L1		Magnetic bead, 6A	1806	muRata	BLM41PG600SN1L
1	L2	4.7μH	Inductor, 4.7μH, 31.5m, 6A	SMD	Cyntec	VCMT063T-4R7MN5T
1	L3	4.7μH	Inductor, 4.7μH, 14.4m, 11A	SMD	Coilcraft	XAL6060-472ME
1	R1	100kΩ	Film resistor, 1%	0402	Yageo	RC0402FR-07100KL
1	R3	62k	Film resistor, 1%	0603	Yageo	RC0603FR-062KL
5	R14, R15, R16, R17, R18	0	Film resistor, 1%	0402	Yageo	RC0402FR-070RL
1	R4	0	Film resistor, 5%	0603	Yageo	RC0603JR-070RL
1	R5	100kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-07100KL
1	R6	31.6kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0731K6L
1	R7	100kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-07100KL
1	R9	51kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0751KL

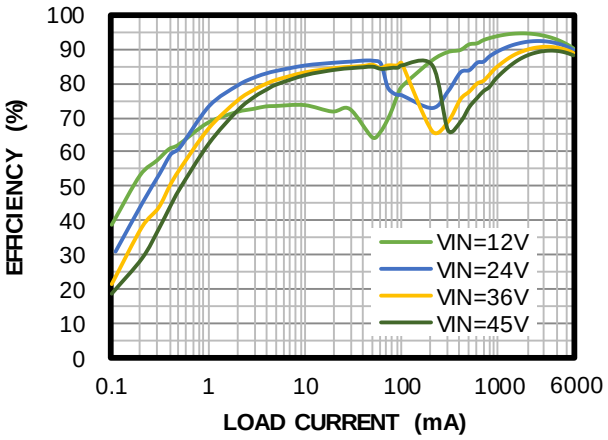
EVQ4436-R-00A BILL OF MATERIALS *(continued)*

Qty	Ref	Value	Description	Package	Manufacturer	Manufactuer_P/N
5	R19, R20, R21, R22, R25	10	Film resistor, 5%	0402	Yageo	RC0402FR-0710RL
7	R8, R10, R11, R12, R13, R23, R24	10	Film resistor, 1%	0603	Yageo	RC0603FR-0710RL
1	U1		Step-down converter	FC-QFN	MPS	MPQ4436GR
1	JP1		Connector, 2x20, 2.54mm, right angle		Any	
5	VIN,VEMI GND, VOUT, GND	Test point	2.0 golden pin		HZ	
8	SS, SYNCIN, FB, ICS, PG, SYNCO, EN, GND	Test point	1.0 golden pin		HZ	

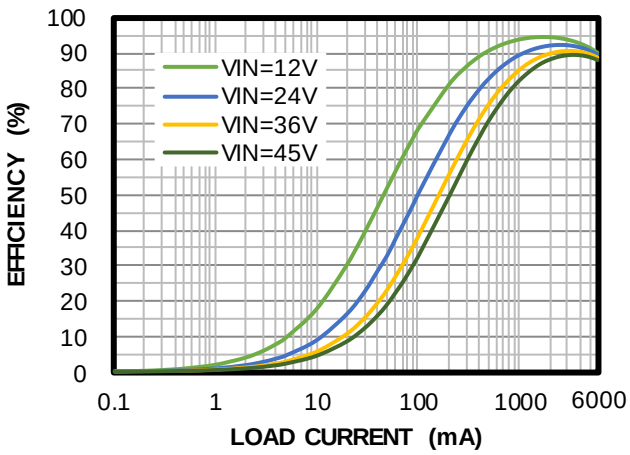
EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, T_A = 25°C, unless otherwise noted.

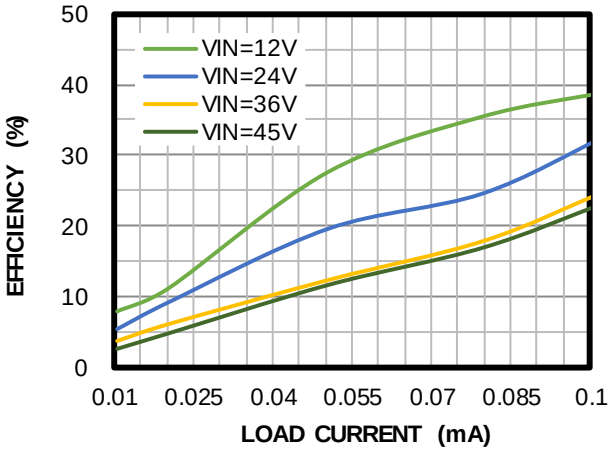
Efficiency vs. Load Current
AAM



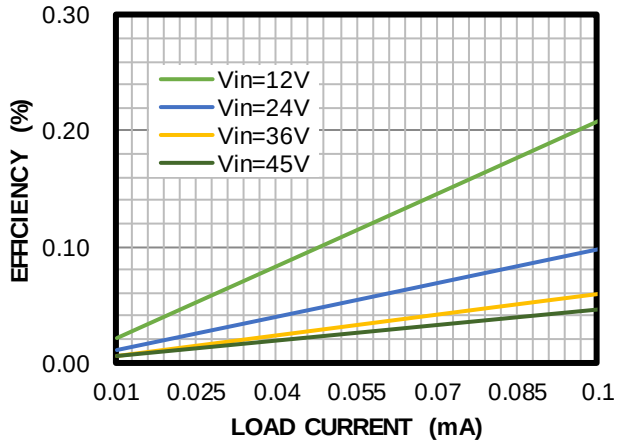
Efficiency vs. Load Current
CCM



Efficiency vs. Load Current
(Extreme light load) AAM



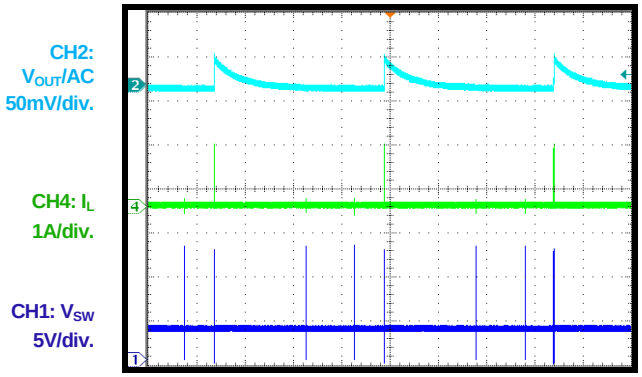
Efficiency vs. Load Current
(Extreme light load) CCM



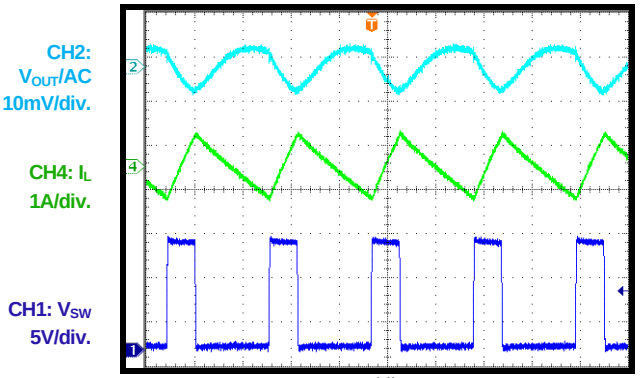
EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

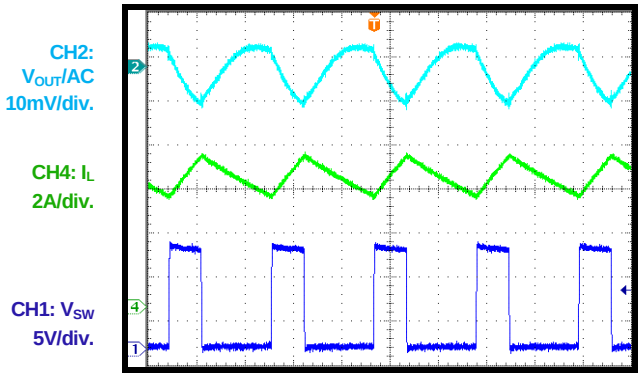
Steady State
I_{OUT} = 0A, AAM



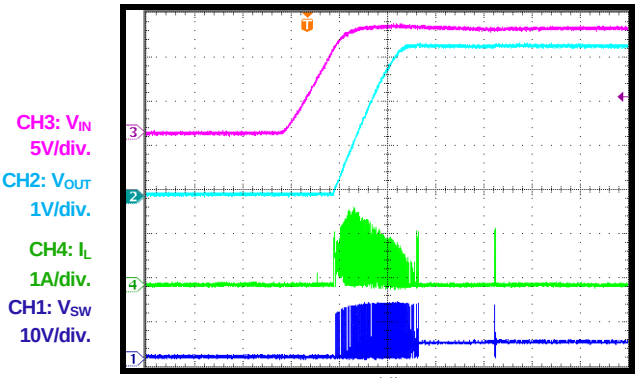
Steady State
I_{OUT} = 0A, FCCM



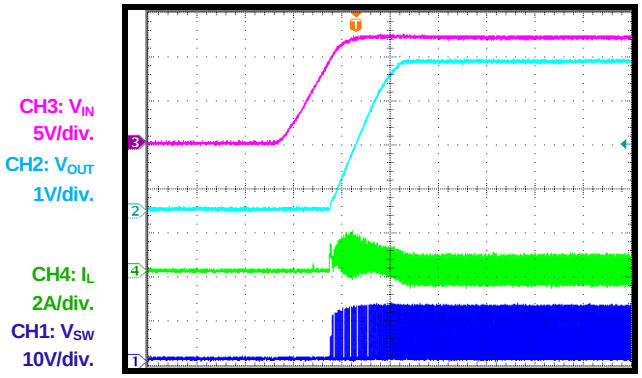
Steady State
I_{OUT} = 6A



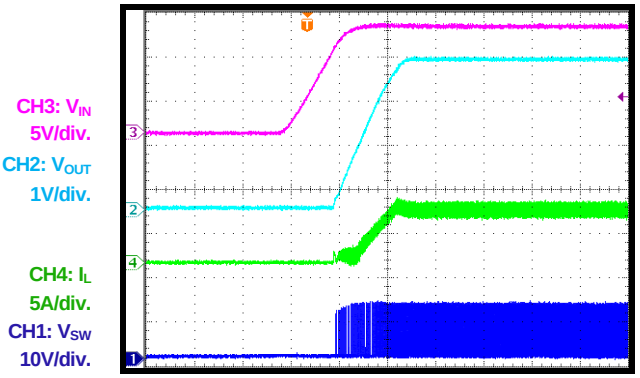
Start-Up through V_{IN}
I_{OUT} = 0A, AAM



Start-Up through V_{IN}
I_{OUT} = 0A, FCCM



Start-Up through V_{IN}
I_{OUT} = 6A

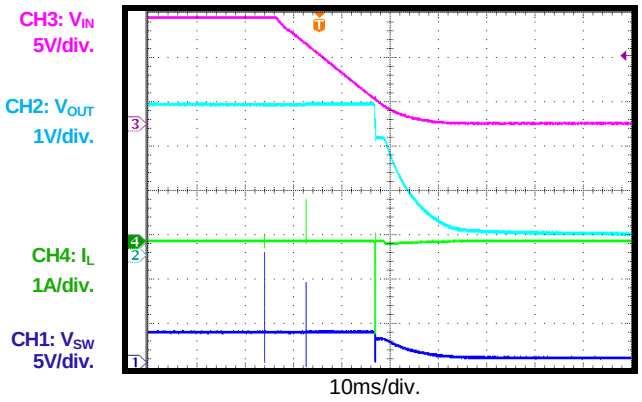


EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

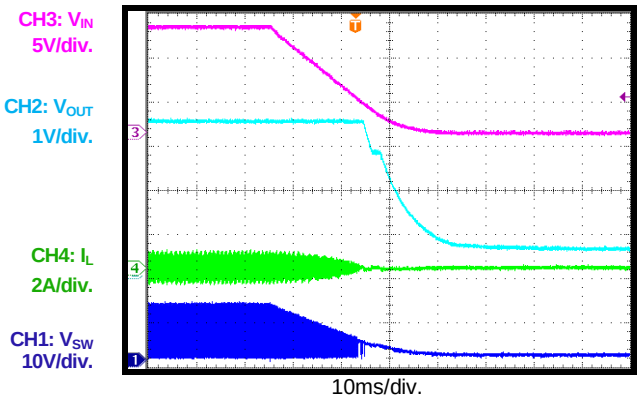
Shutdown through V_{IN}

I_{OUT} = 0A, AAM



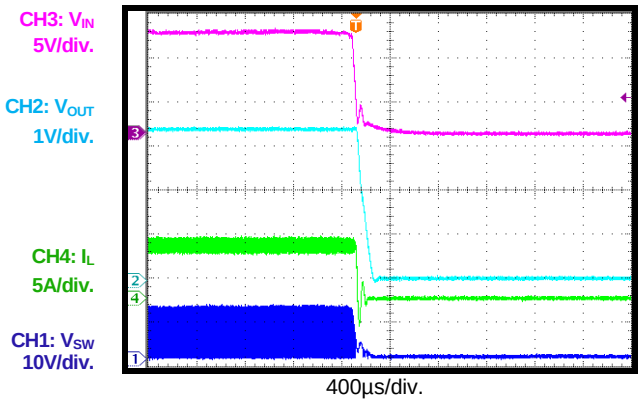
Shutdown through V_{IN}

I_{OUT} = 0A, FCCM



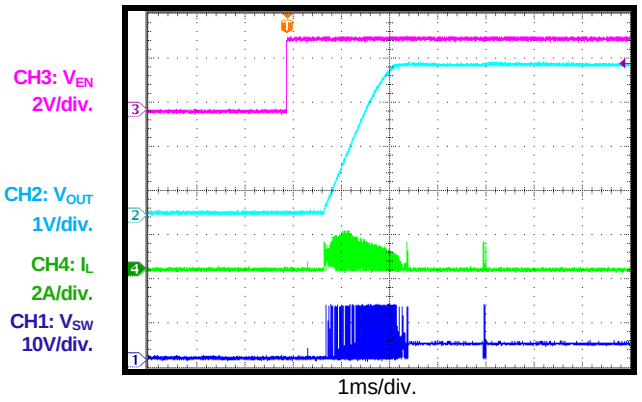
Shutdown through V_{IN}

I_{OUT} = 6A



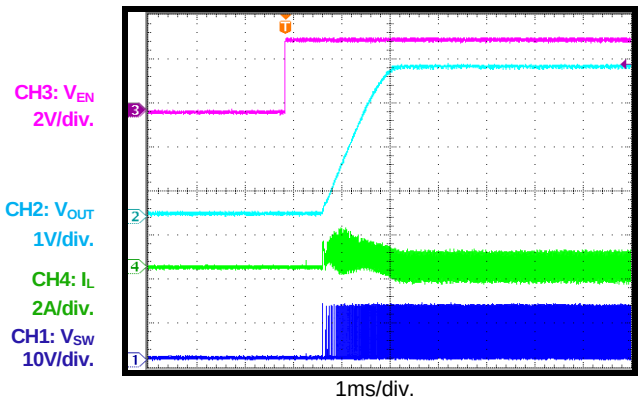
Start-Up through EN

I_{OUT} = 0A, AAM



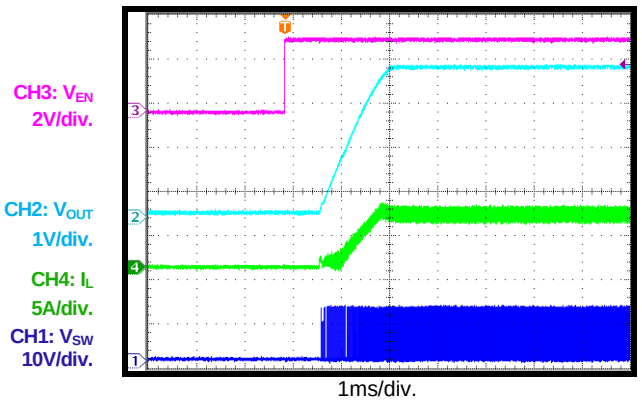
Start-Up through EN

I_{OUT} = 0A, FCCM



Start-Up through EN

I_{OUT} = 6A

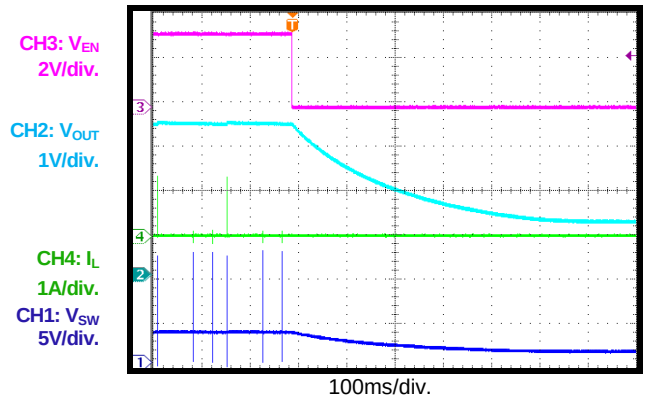


EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

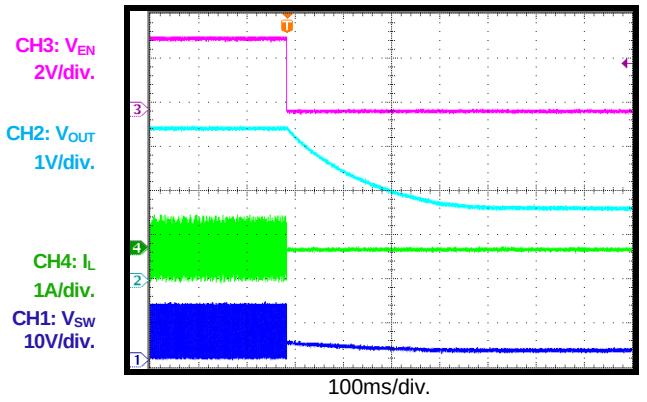
Shutdown through EN

I_{OUT} = 0A, AAM



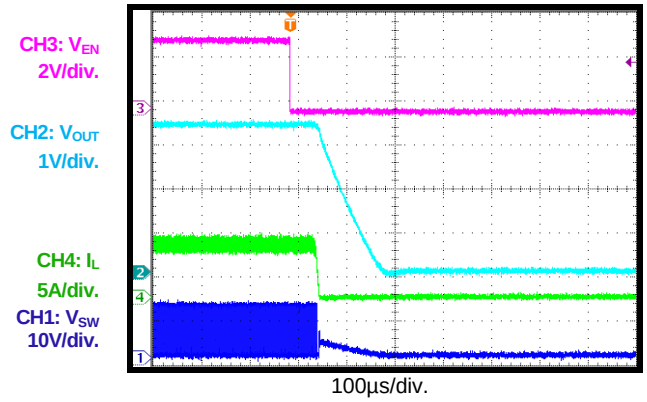
Shutdown through EN

I_{OUT} = 0A, FCCM



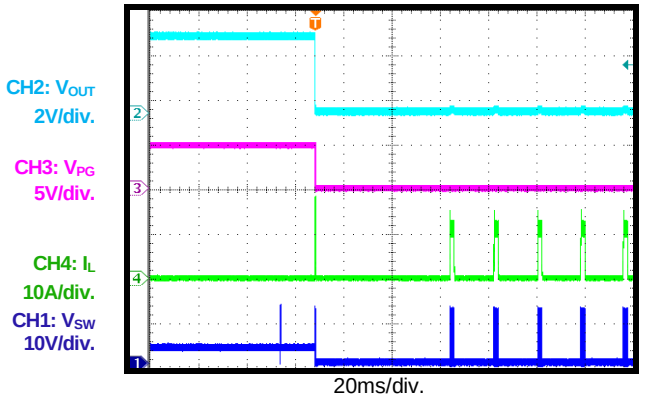
Shutdown through EN

I_{OUT} = 6A



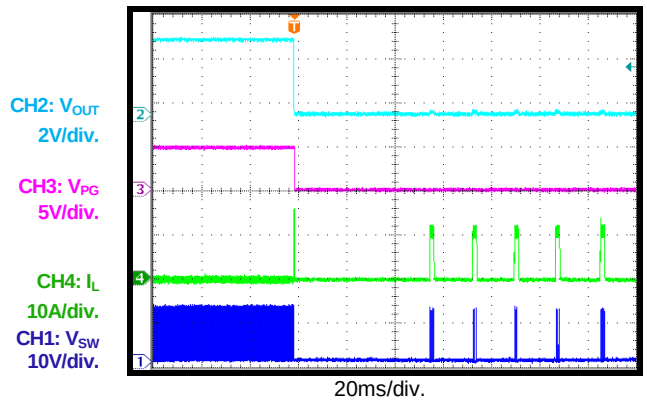
SCP Entry

I_{OUT} = 0A, AAM



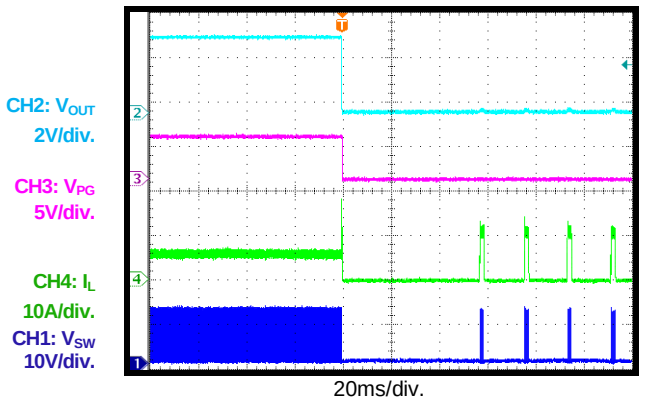
SCP Entry

I_{OUT} = 0A, FCCM



SCP Entry

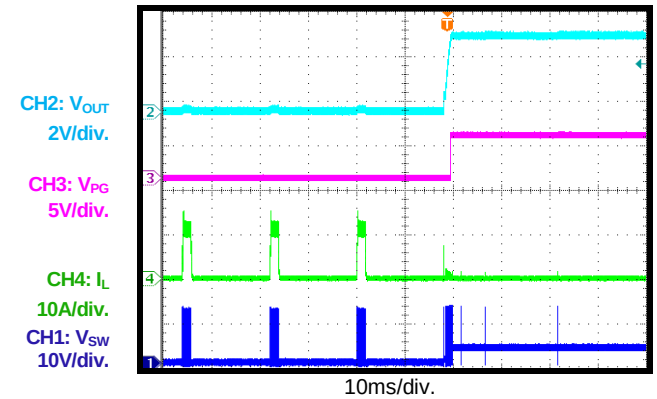
I_{OUT} = 6A



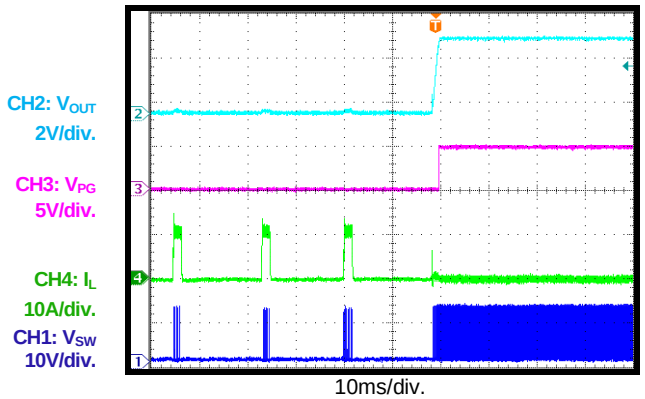
EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

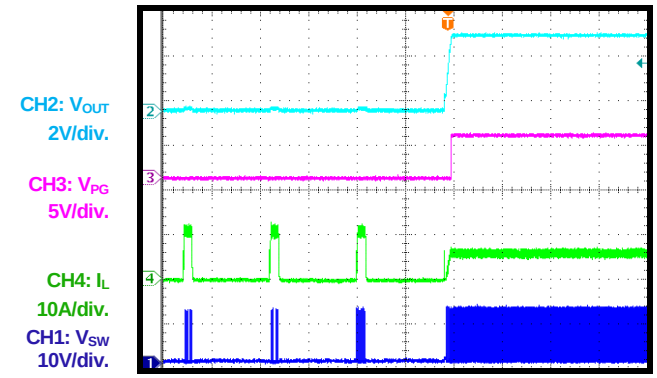
SCP Recovery
I_{OUT} = 0A, AAM



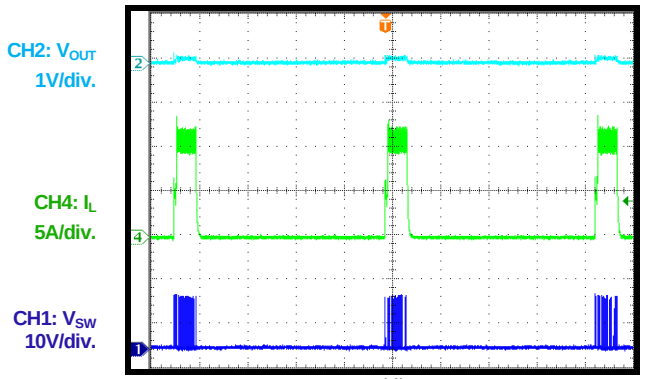
SCP Recovery
I_{OUT} = 0A, FCCM



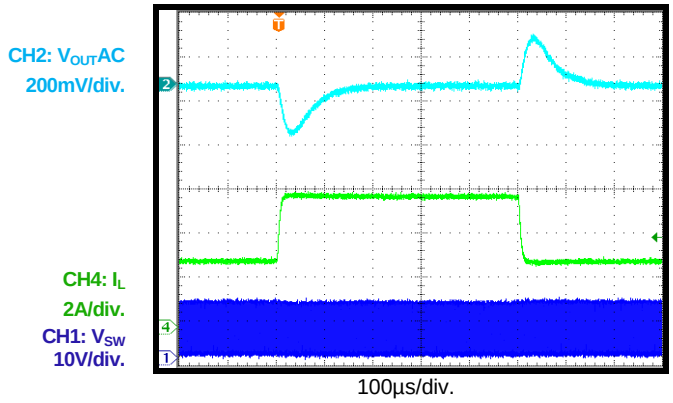
SCP Recovery
I_{OUT} = 6A



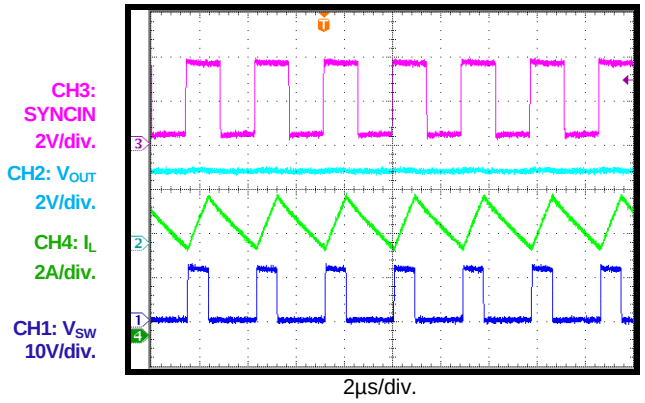
SCP Steady State



Load Transient
I_{OUT} = 3A to 6A, 1.6A/µs



SYNC Operation
I_{OUT} = 6A, SYNC frequency = 350kHz

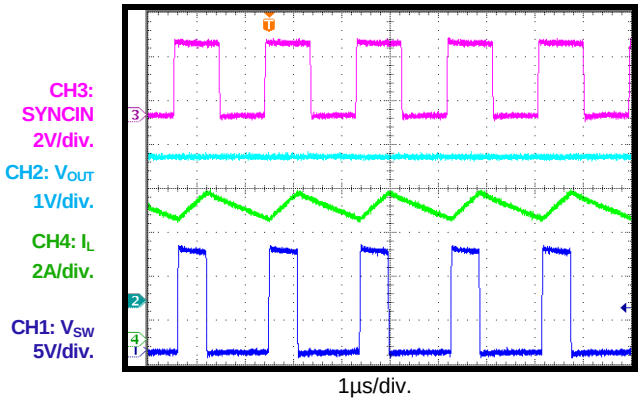


EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

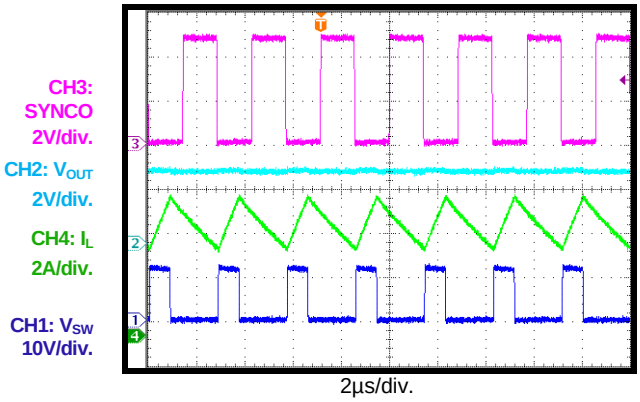
SYNC Operation

I_{OUT} = 6A, SYNC frequency = 530kHz



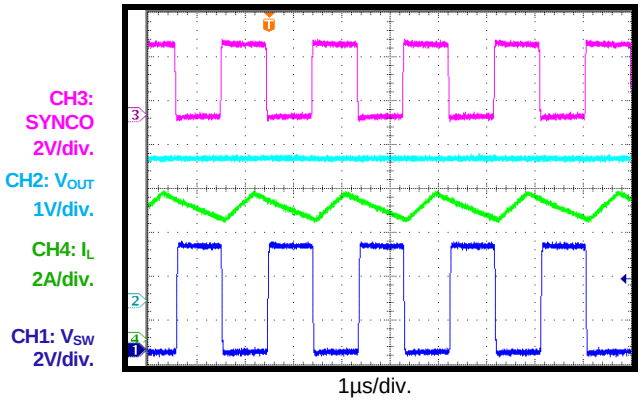
SYNCO Operation

I_{OUT} = 6A, SYNC frequency = 350kHz



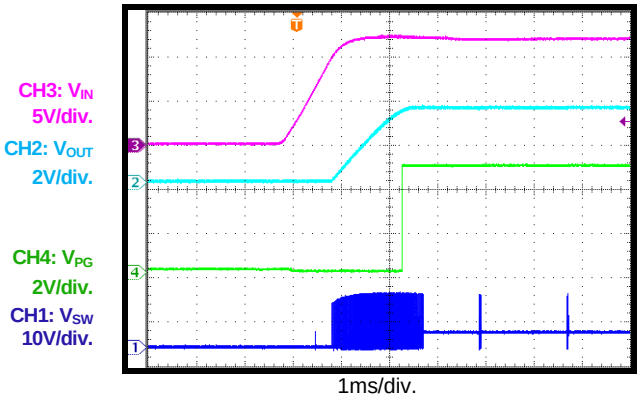
SYNCO Operation

I_{OUT} = 6A, SYNC frequency = 530kHz



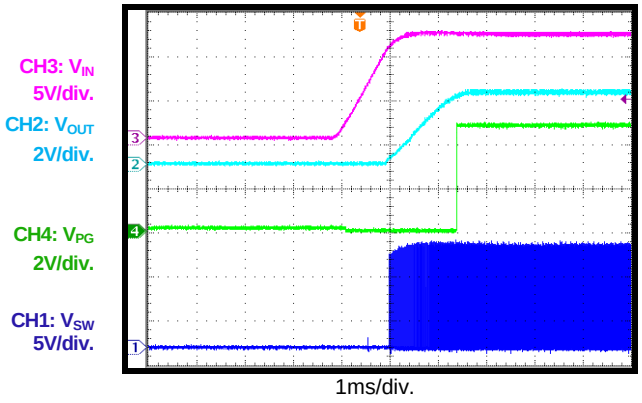
PG Start-Up through V_{IN}

I_{OUT} = 0A



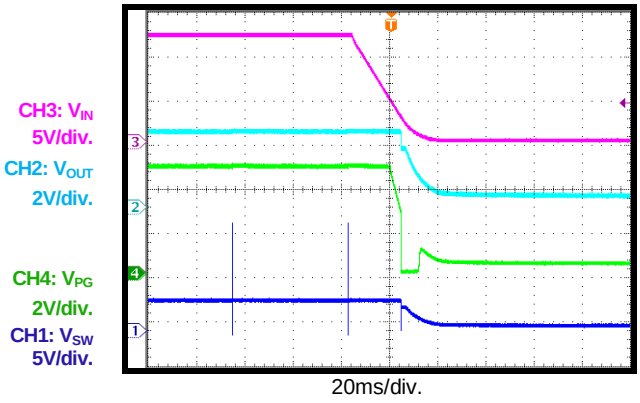
PG Start-Up through V_{IN}

I_{OUT} = 6A



PG Shutdown through V_{IN}

I_{OUT} = 0A

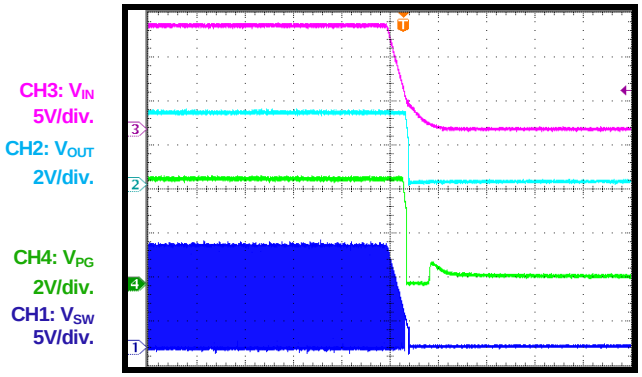


EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

PG Shutdown through V_{IN}

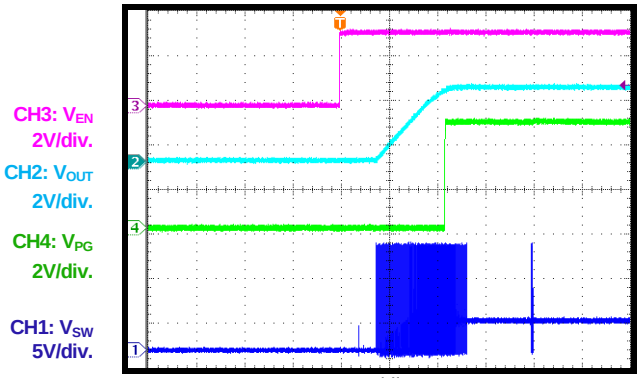
I_{OUT} = 6A



20ms/div.

PG Start-Up through EN

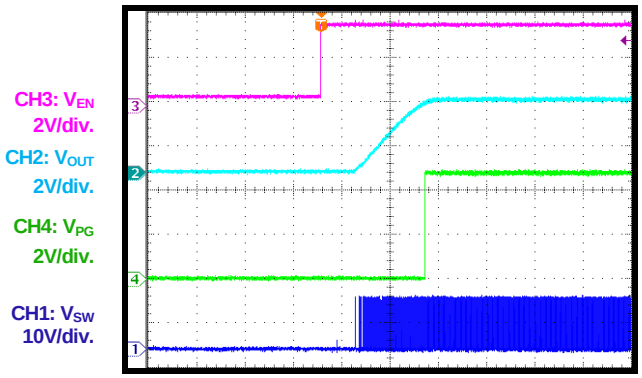
I_{OUT} = 0A



1ms/div.

PG Start-Up through EN

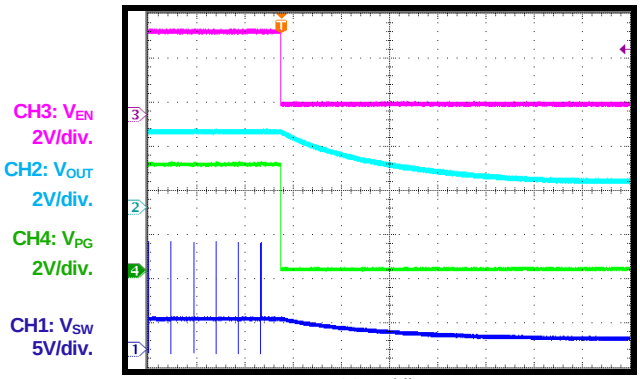
I_{OUT} = 6A



1ms/div.

PG Shutdown through EN

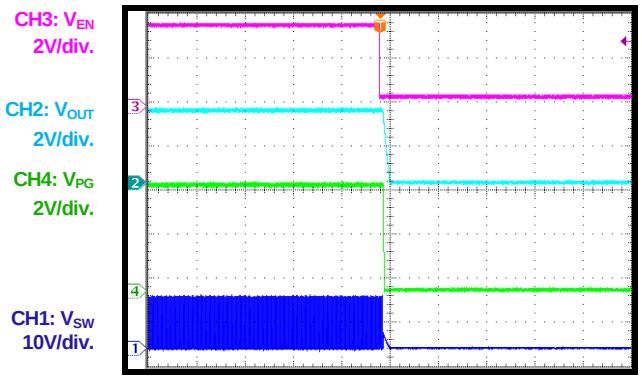
I_{OUT} = 0A



100ms/div.

PG Shutdown through EN

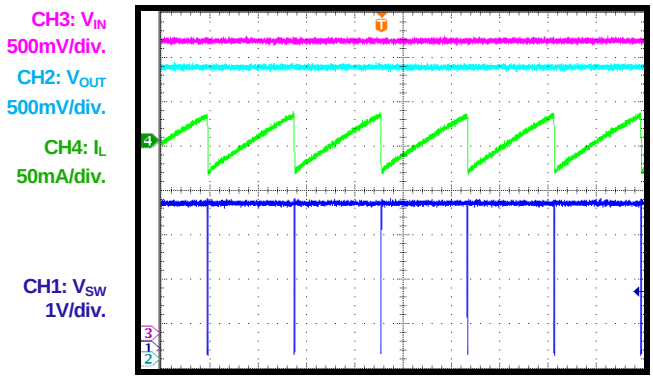
I_{OUT} = 6A



1ms/div.

Dropout Operation

V_{IN} = 3.3V, V_{OUT} set to 3.3V, I_{OUT} = 0A



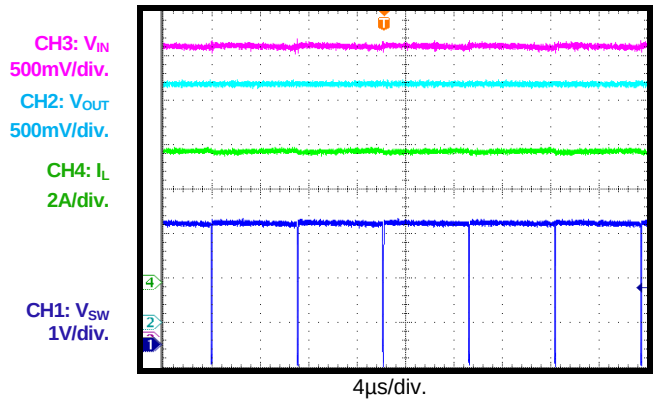
4µs/div.

EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

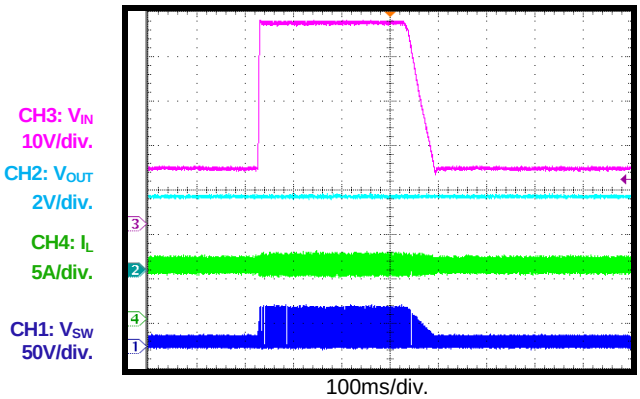
Dropout Operation

V_{IN} = 3.3V, V_{OUT} set to 3.3V, I_{OUT} = 6A



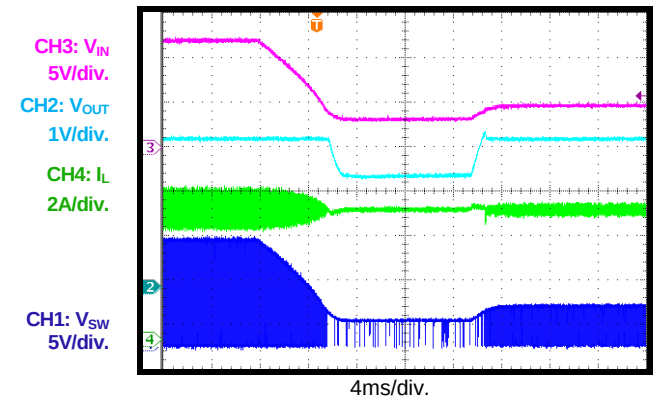
Load Dump

V_{IN} = 12V to 36V, I_{OUT} = 6A



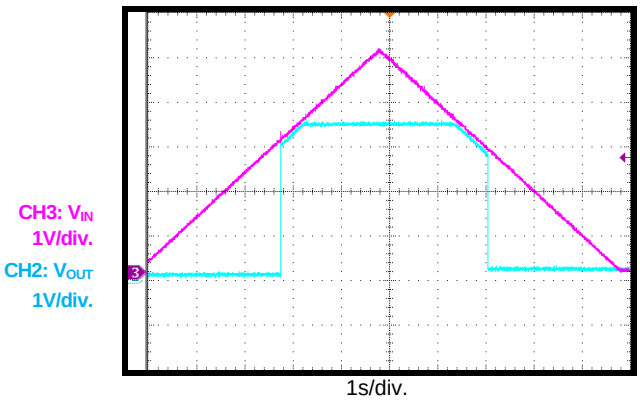
Cold Crank

V_{IN} = 12V to 3.3V to 5V, I_{OUT} = 6A



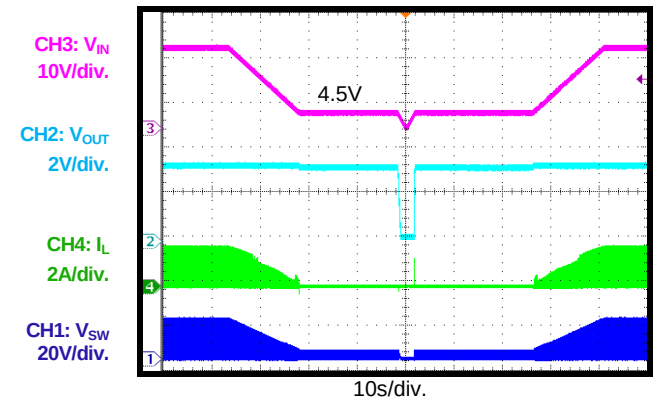
V_{IN} Ramp Up and Down

I_{OUT} = 0.1A



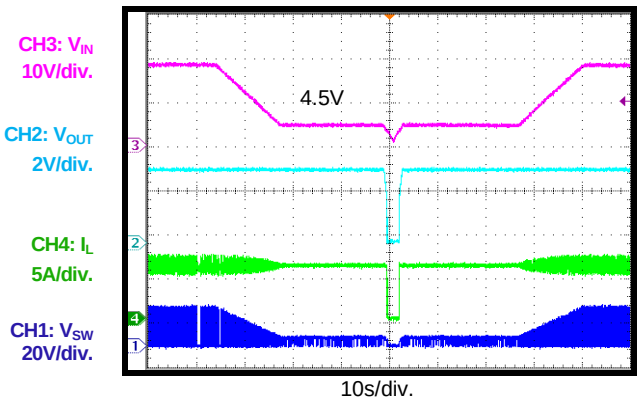
V_{IN} Ramp Down and Up

I_{OUT} = 1mA



V_{IN} Ramp Down and Up

I_{OUT} = 6A



PCB LAYOUT

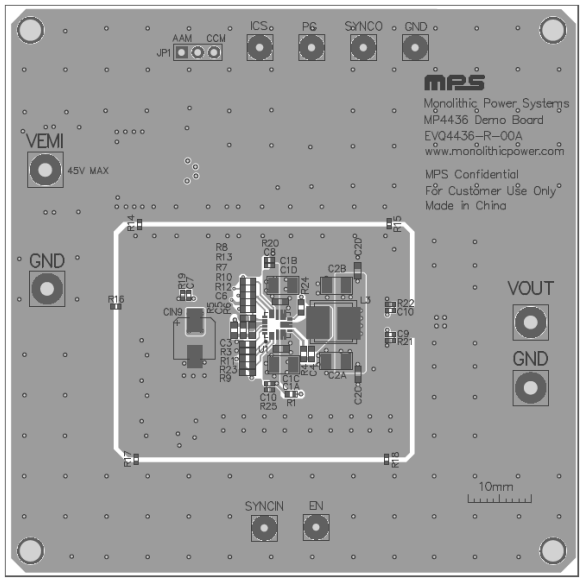


Figure 1: Top Silk Layer and Top Layer

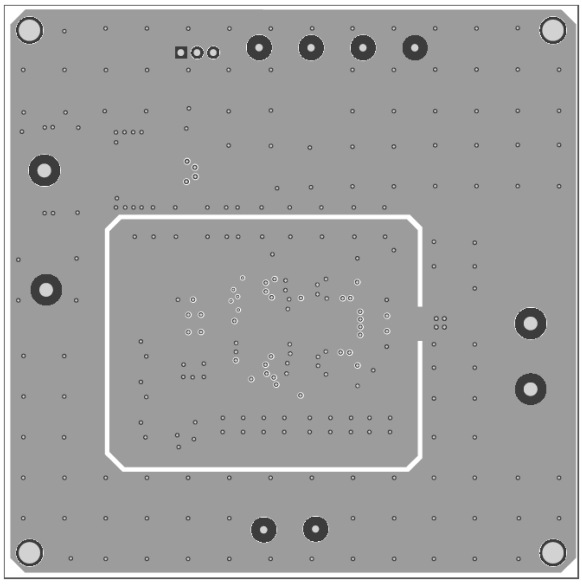


Figure 3: Inner Layer 1

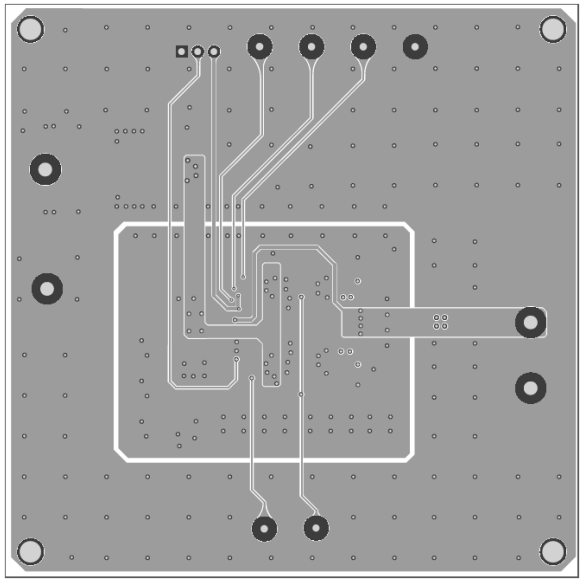


Figure 2: Inner Layer 2

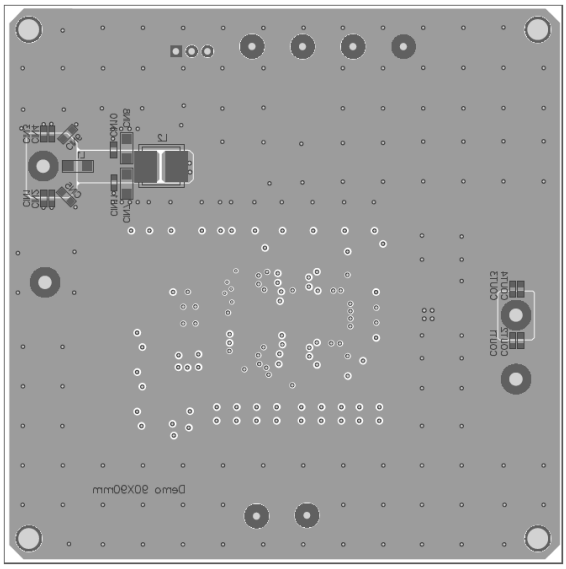


Figure 2: Bottom Silk Layer and Bottom Layer