EVM81204-BC-00A

Dual 12A and Dual 5A Output Step-Down Module Evalution Board

DESCRIPTION

The EVM81204-BC-00A is designed to demonstrate the capabilities of the MPM81204, a quad-output step-down module with dual 12A and dual 5A outputs. It operates at a high efficiency across a wide output current load range. The operation frequency is configurable to 600kHz, 800kHz, or 1000kHz with a single resistor, allowing the frequency to remain constant regardless of the input and output voltages. Four open-drain power good signals indicate whether the outputs are within their normal range. Fully integrated protection features include over-current protection (OCP), over-voltage protection (OVP), and over-temperature protection (OTP).

The MPM81204 requires a minimal number of readily available, standard external components and is available in a BGA (9.5mmx16mmx4.98mm) package.

ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Value	Units
Input voltage	V_{IN}	6.5 to 16	V
Output voltage	V_{OUT0} - V_{OUT3}	1.8, 3.3, 5, 1.2	V
Output current (max)	I_{OUT0} - I_{OUT3}	12, 5, 5, 12	A

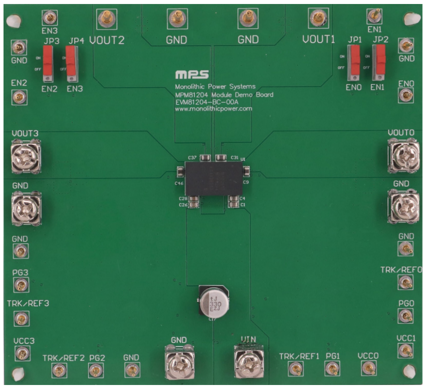
FEATURES

- Wide 4V to 16V Input Voltage Range for the MPM81204
- CH0, CH3: Dual, 12A, 0.6V to 3.3V DC Output
- CH1, CH2: Dual, 5A, 0.6V to 5.5V DC Output
- Adaptive COT for Ultra-Fast Transient Response
- Forced Continuous Conduction Mode (FCCM)
- Output Voltage Tracking
- Programmable Soft-Start Time
- Selectable Switching Frequency: 600kHz, 800kHz, or 1000kHz
- Non-Latch OCP, OVP, UVLO, and Thermal Shutdown
- Available in a BGA (9.5mmx16mmx4.98mm) Package

APPLICATIONS

- Telecom and Networking Systems
- Servers
- Base Stations

EVM81204-BC-00A EVALUATION BOARD

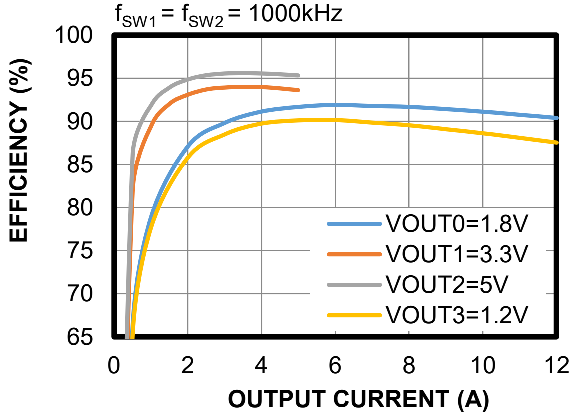


(LxWxH) 12cmx11cmx1.6mm

Board Number	MPS IC Number
EVM81204-BC-00A	MPM81204GBC

Efficiency vs. Output Current

V_{IN} = 12V, f_{SW0} = f_{SW3} = 600kHz
f_{SW1} = f_{SW2} = 1000kHz



QUICK START GUIDE

1. Preset the power supply to 6.5V ≤ V_{IN} ≤ 16V, then turn off the power supply.
2. Connect the power supply terminals to:
    a. Positive (+): VIN
    b. Negative (-):GND
3. Connect the load terminals to:
    a. Positive (+): VOUT0, VOUT1, VOUT2, VOUT3
    b. Negative (-): GND
4. After making the connections, turn on the power supply.

EVALUATION BOARD SCHEMATIC

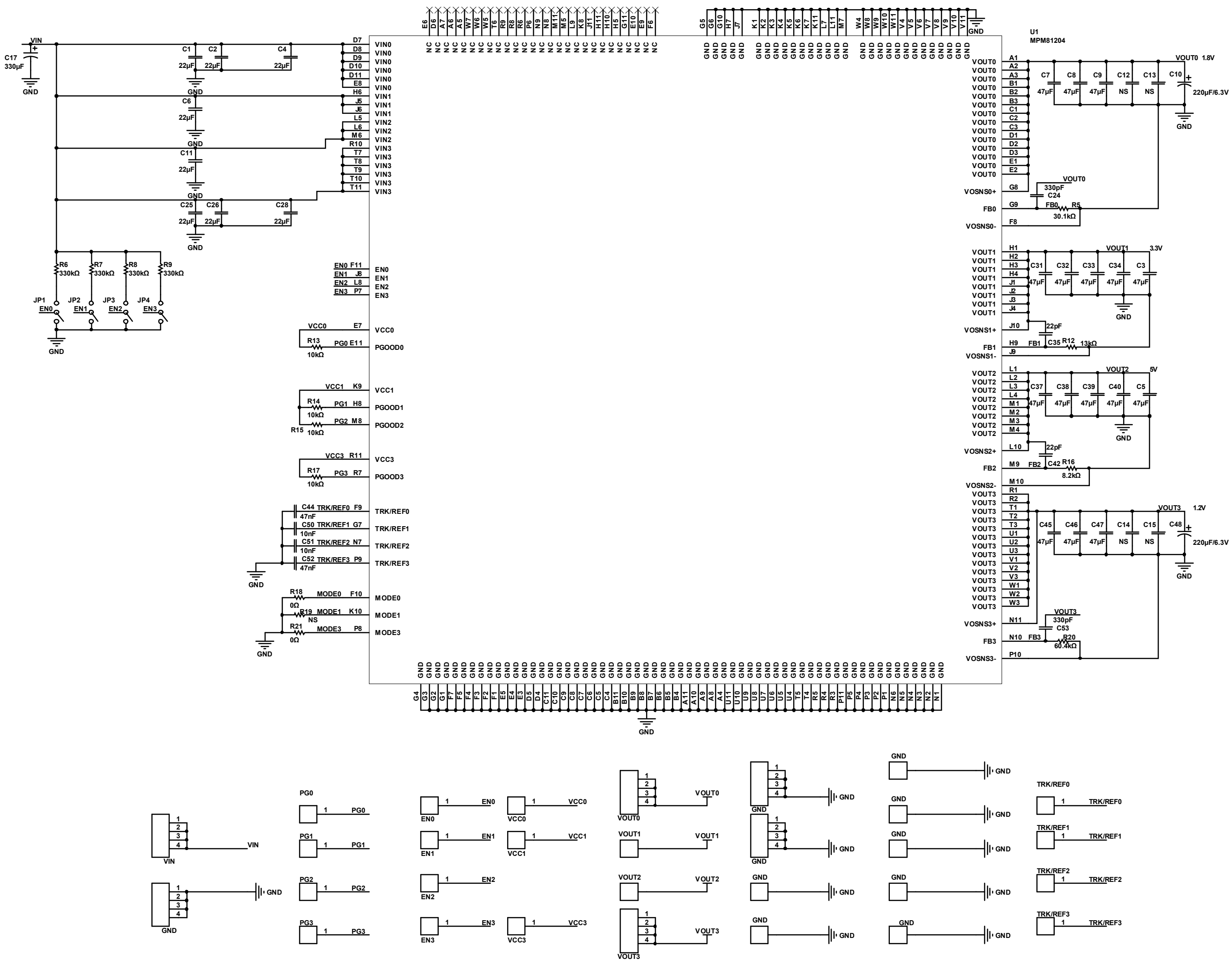


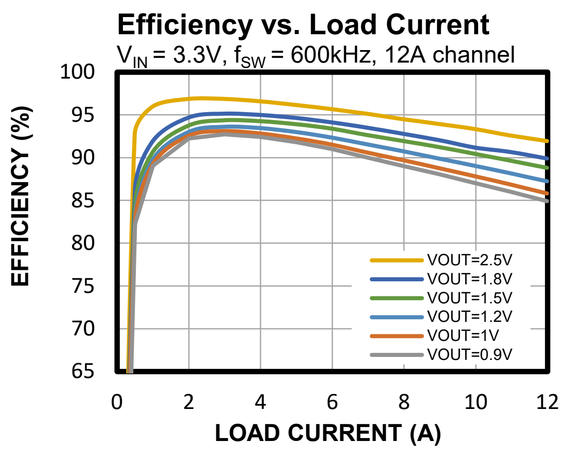
Figure 1: Evaluation Board Schematic

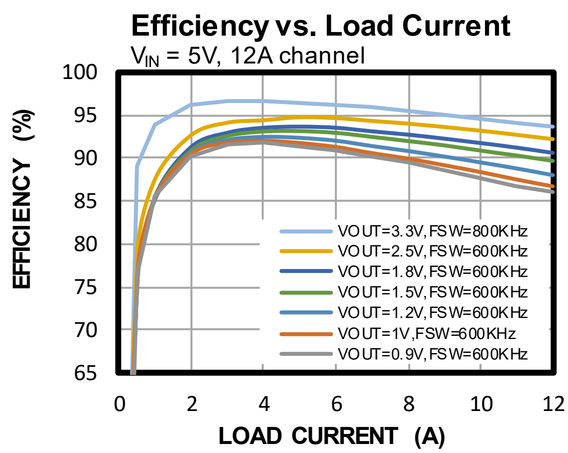
EVM81204-BC-00A BILL OF MATERIALS

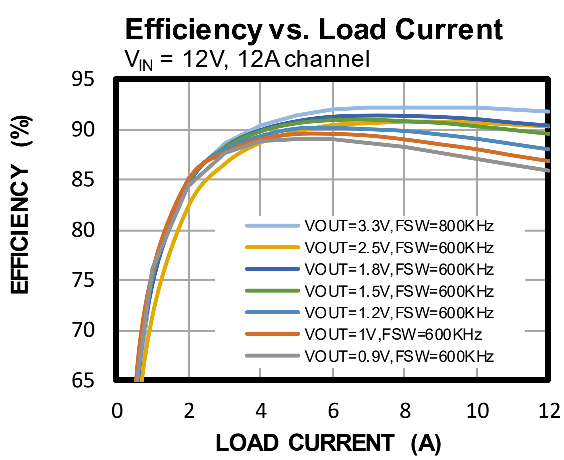
Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
8	C1, C2, C4, C6, C11, C25, C26, C28	22µF	Ceramic capacitor, 25V, X5R	0805	TDK	C2012X5R1E226 MT000E
0	C12, C13, C14, C15	NS				
2	C44, C52	47nF	Ceramic capacitor, 50V, X7R	0603	Wurth	885012206093
2	C50, C51	10nF	Ceramic capacitor, 50V, X7R	0603	Wurth	885012206089
16	C3, C5, C7, C8, C9, C31, C32, C33, C34, C37, C38, C39, C40, C45, C46, C47	47µF	Ceramic capacitor, 10V, X5R	0805	Murata	GRM21BR61A476 ME15L
2	C10, C48	220µF	Tantalum capacitor, 6.3V, 15mΩ	SMD	Panasonic	EEFCX0J221R
1	C17	330µF	330µF, 25V, ±20% ESR, 80mΩ	SMD	Nippon Chemi-Con	EMZJ250ADA331 MHA0G
2	C35, C42	22pF	Ceramic capacitor, 50V, C0G	0402	Murata	GRM1555C1H220 JA01D
2	C24, C53	330pF	Ceramic capacitor, 50V, C0G	0402	TDK	CGA2B2C0G1H33 1JT0Y0F
4	R6, R7, R8, R9	330kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-07330KL
4	R13, R14, R15, R17	10kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710KL
1	R20	60.4kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0760K4L
1	R12	13kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0713KL
1	R16	8.2kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-078K2L
1	R5	30.1kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0730K1L
2	R18, R21	0Ω	Film resistor, 1%	0603	Yageo	RC0603FR-070RL
4	JP1, JP2, JP3, JP4	Switch	SPDT switch	DIP	Wurth	450301014042
0	R19	NS				
4	VOUT1, VOUT2, GND, GND	φ2.0	φ2.0 copper pin	DIP	Custom	
20	TRK/REF0-3, GND, PG0-3, EN0-3, GND, VCC0, VCC1, VCC3, SW	φ1.0	φ1.0 copper pin	DIP	Custom	
6	VOUT0, VOUT3, GND, GND, GND, VIN	7.87mmx 7.87mmx 11.18mm	Screw terminal	DIP	Keystone	KEYSTONE-7697-75
1	U1	MPM 81204	4V to 16V, dual 12A and dual 5A output power module	BGA	MPS	MPM81204GBC

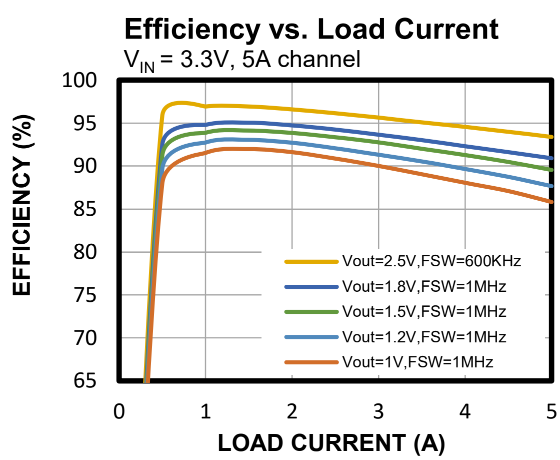
TYPICAL PERFORMANCE CHARACTERISTICS

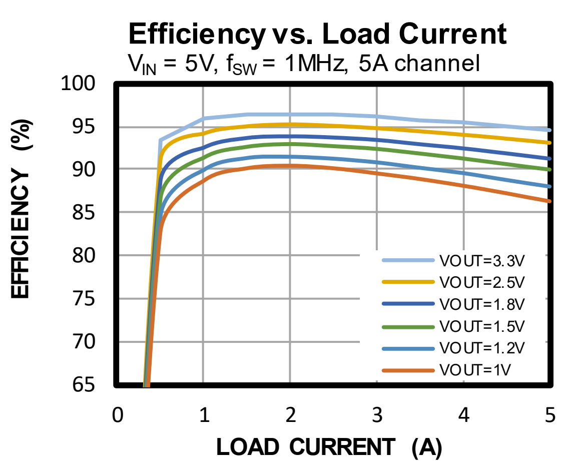
V_{IN} = 12V, V_{OUT0} = 1.8V, V_{OUT1} = 3.3V, V_{OUT2} = 5V, V_{OUT3} = 1.2V, f_{SW0} = f_{SW3} = 600kHz, f_{SW1} = f_{SW2} = 1MHz, CCM, T_A = 25°C, unless otherwise noted.

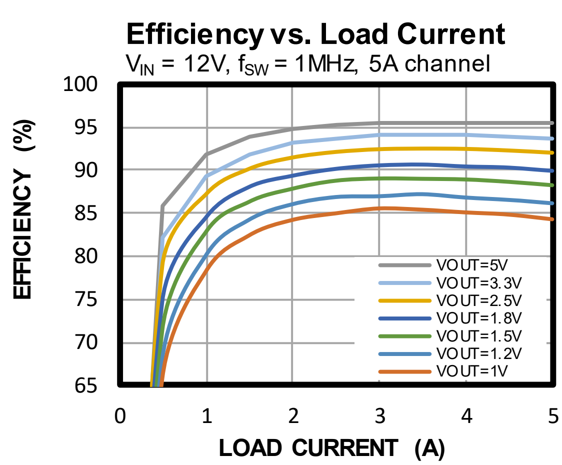










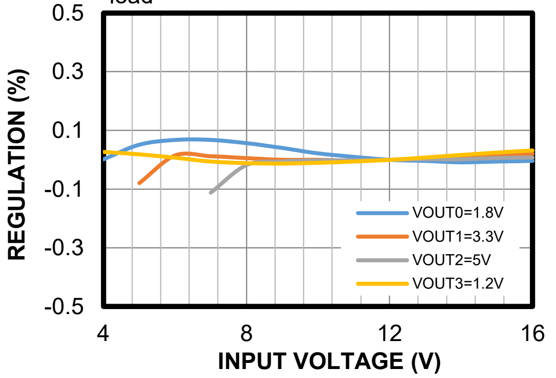


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT0} = 1.8V, V_{OUT1} = 3.3V, V_{OUT2} = 5V, V_{OUT3} = 1.2V, f_{SW0} = f_{SW3} = 600kHz, f_{SW1} = f_{SW2} = 1MHz, CCM, T_A = 25°C, unless otherwise noted.

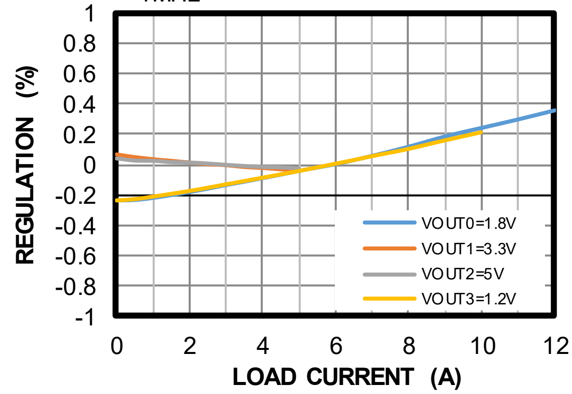
Line Regulation

f_{SW0} = f_{SW3} = 600kHz, f_{SW1} = f_{SW2} = 1MHz, full load

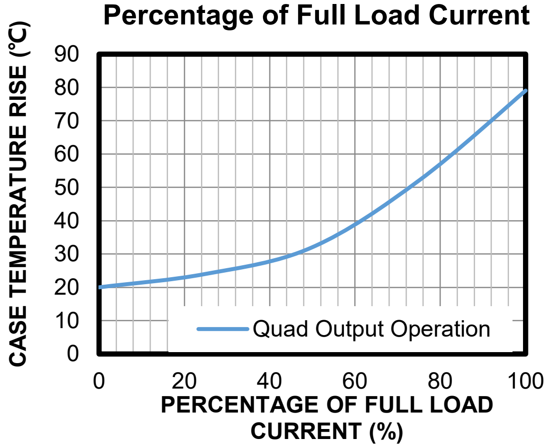


Load Regulation

V_{IN} = 12V, f_{SW} = f_{SW3} = 600kHz, f_{SW1} = f_{SW2} = 1MHz

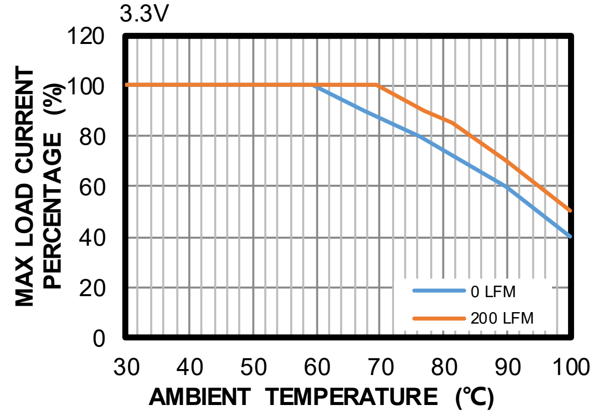


Case Temperature Rise vs. Percentage of Full Load Current



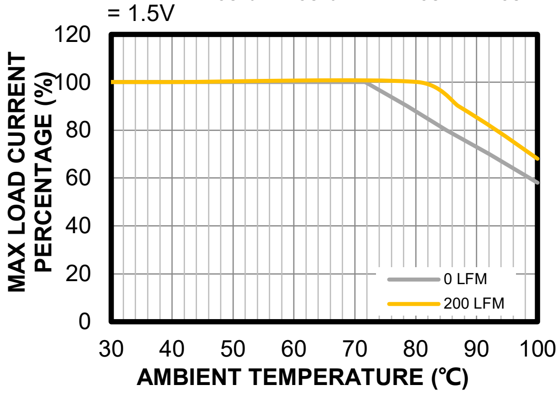
Thermal Derating

V_{IN} = 12V, f_{SW0} = f_{SW3} = 600kHz, f_{SW1} = f_{SW2} = 1MHz, V_{OUT0} = V_{OUT3} = 1.8V, V_{OUT1} = V_{OUT2} = 3.3V



Thermal Derating

V_{IN} = 12V, f_{SW0} = f_{SW3} = 600kHz, f_{SW1} = f_{SW2} = 1MHz, V_{OUT0} = V_{OUT3} = 1V, V_{OUT1} = V_{OUT2} = 1.5V

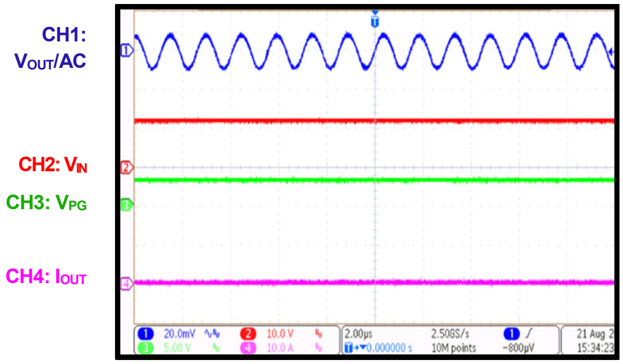


TYPICAL PERFORMANCE CHARACTERISTICS

12A channel, V_{IN} = 12V, V_{OUT} = 1.8V, f_{SW} = 600kHz, C_{OUT} = 3 x 47μF ceramic capacitor + 220μF tantalum capacitor, T_A = 25°C, unless otherwise noted.

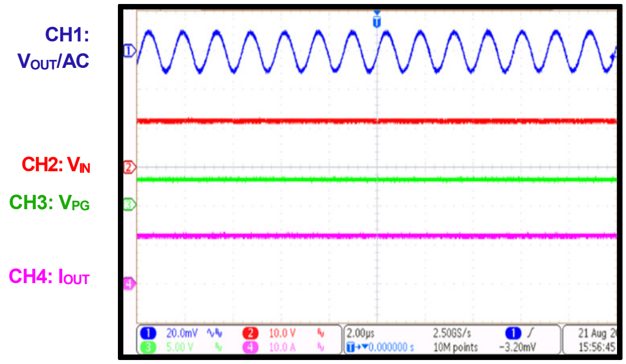
Steady State

I_{OUT} = 0A



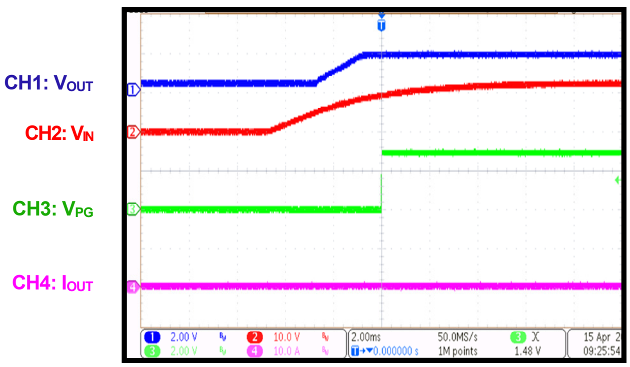
Steady State

I_{OUT} = 12A



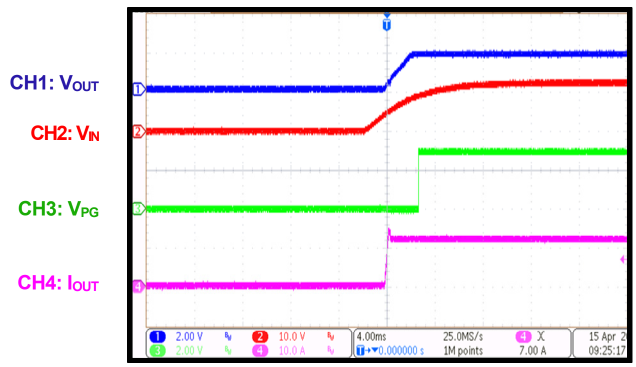
Start-Up through VIN

I_{OUT} = 0A



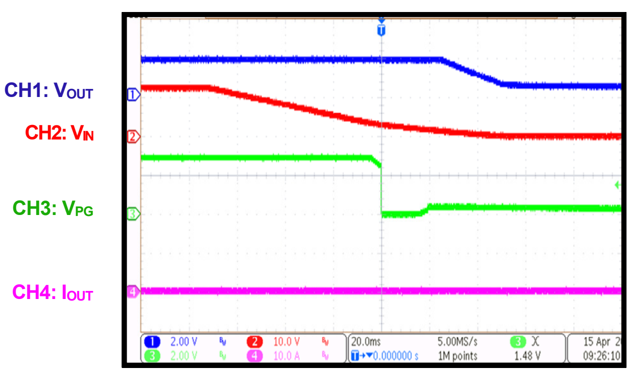
Start-Up through VIN

I_{OUT} = 12A



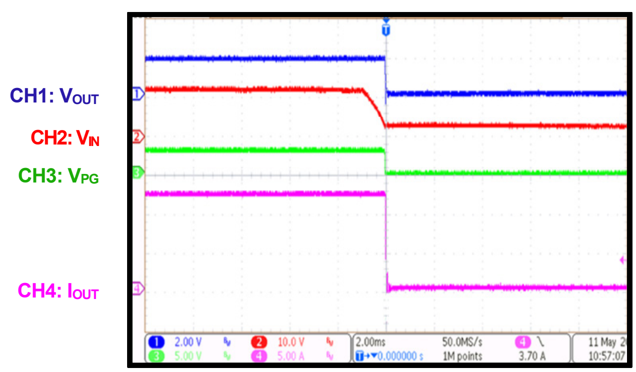
Shutdown through VIN

I_{OUT} = 0A



Shutdown through VIN

I_{OUT} = 12A

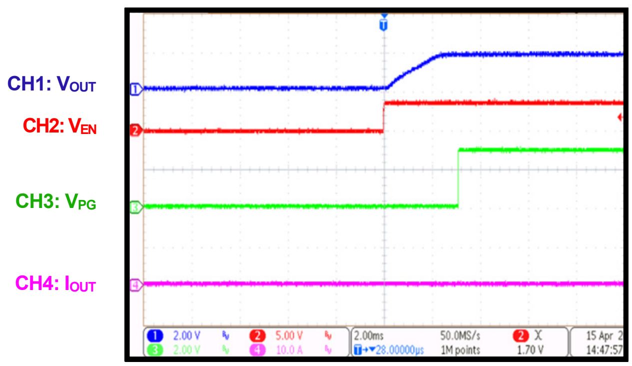


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

12A channel, V_{IN} = 12V, V_{OUT} = 1.8V, f_{SW} = 600kHz, C_{OUT} = 3 x 47µF ceramic capacitor + 220µF tantalum capacitor , T_A = 25°C, unless otherwise noted.

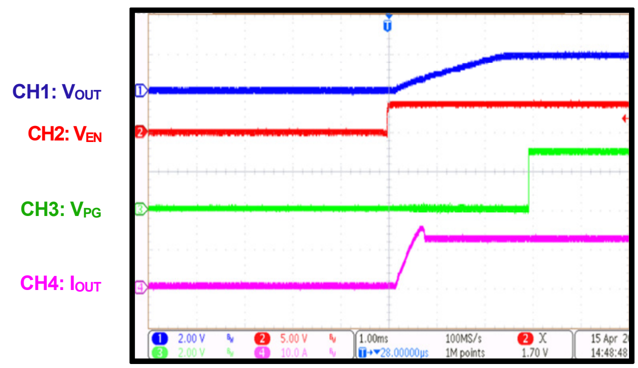
Start-Up through EN

I_{OUT} = 0A



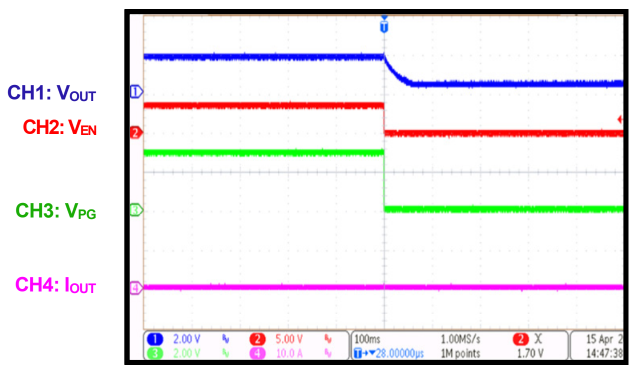
Start-Up through EN

I_{OUT} = 12A



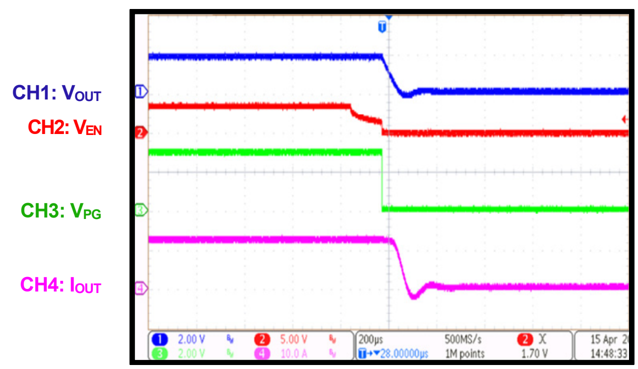
Shutdown through EN

I_{OUT} = 0A



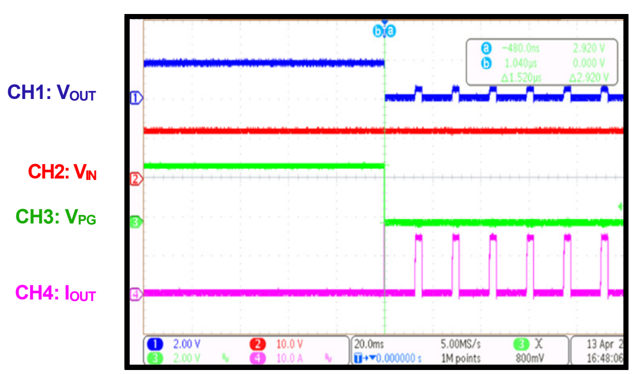
Shutdown through EN

I_{OUT} = 12A



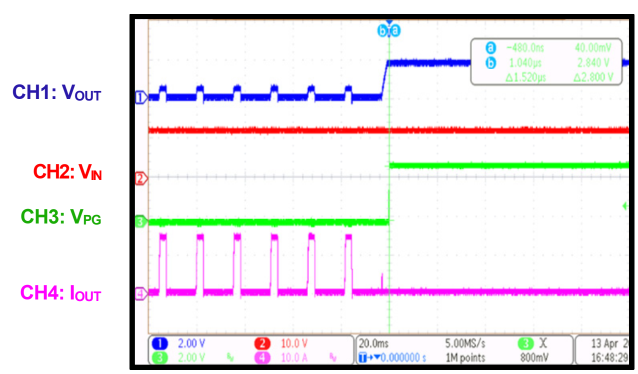
SCP Entry

I_{OUT} = 0A



SCP Recovery

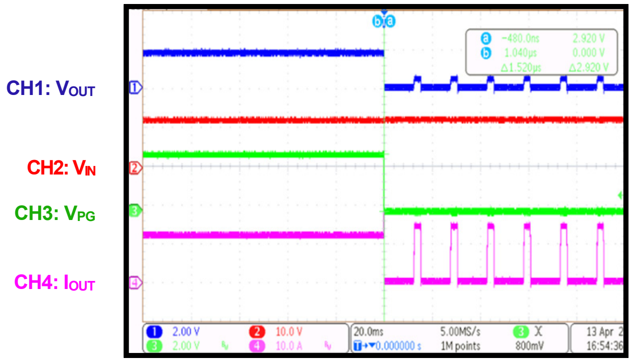
I_{OUT} = 0A



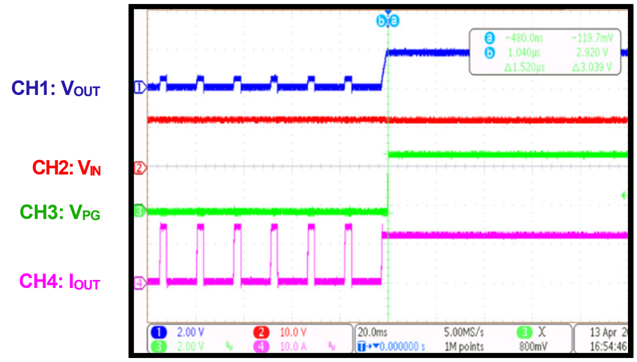
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

12A channel, V_{IN} = 12V, V_{OUT} = 1.8V, f_{SW} = 600kHz, C_{OUT} = 3 x 47μF ceramic capacitor + 220μF tantalum capacitor, T_A = 25°C, unless otherwise noted.

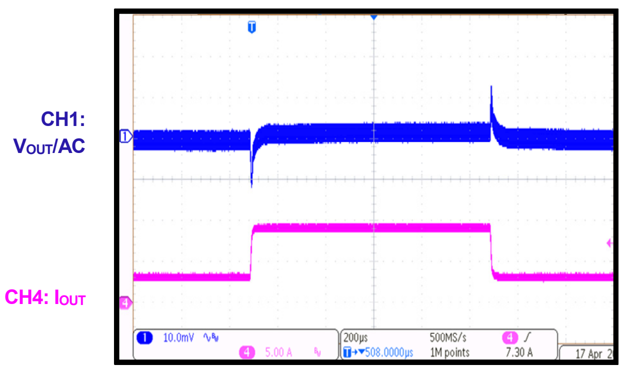
SCP Entry
I_{OUT} = 12A



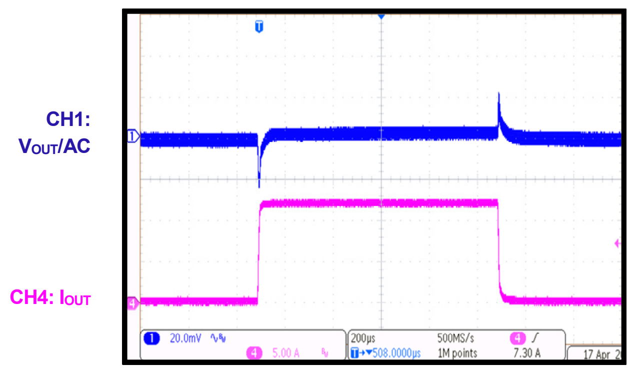
SCP Recovery
I_{OUT} = 12A



Load Transient Response
3A to 9A load step, 2.5A/μs



Load Transient Response
0A to 12A load step, 2.5A/μs

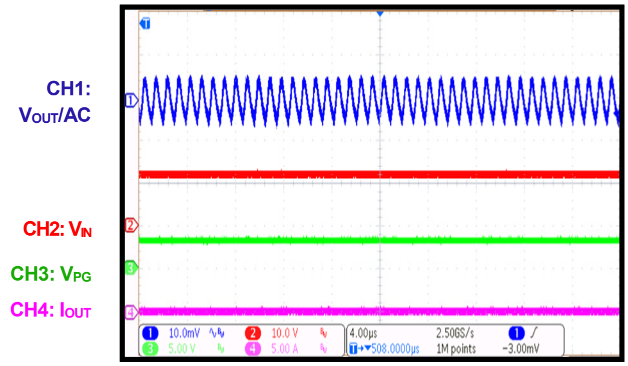


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

5A channel, V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 1MHz, C_{OUT} = 5 x 47µF ceramic capacitor, T_A = 25°C, unless otherwise noted.

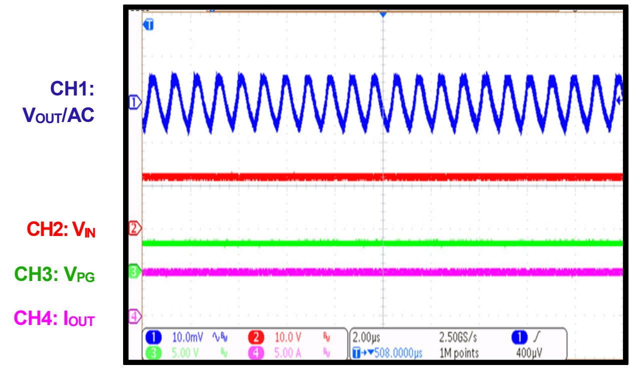
Steady State

I_{OUT} = 0A



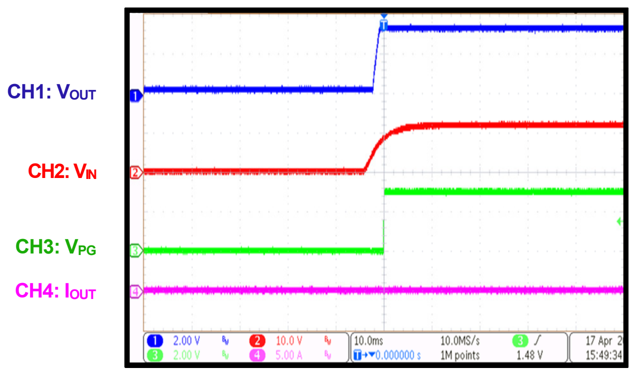
Steady State

I_{OUT} = 5A



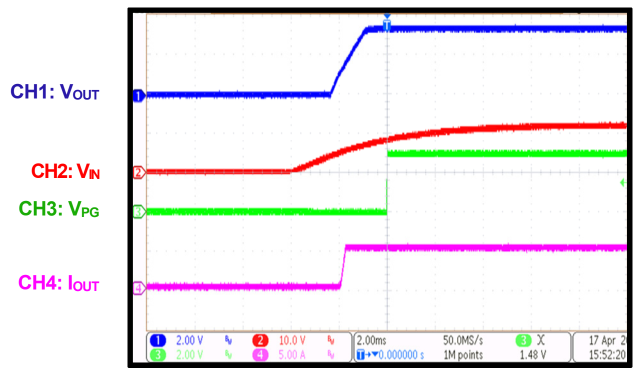
Start-Up through VIN

I_{OUT} = 0A



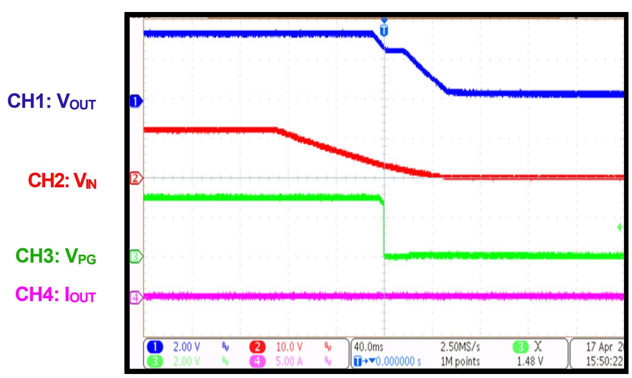
Start-Up through VIN

I_{OUT} = 5A



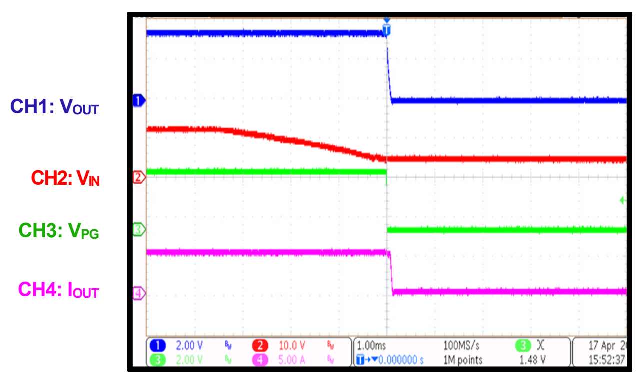
Shutdown through VIN

I_{OUT} = 0A



Shutdown through VIN

I_{OUT} = 5A

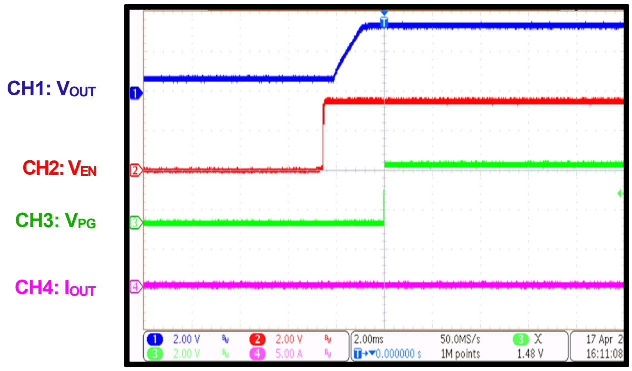


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

5A channel, V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 1MHz, C_{OUT} = 5 x 47µF ceramic capacitor, T_A = 25°C, unless otherwise noted.

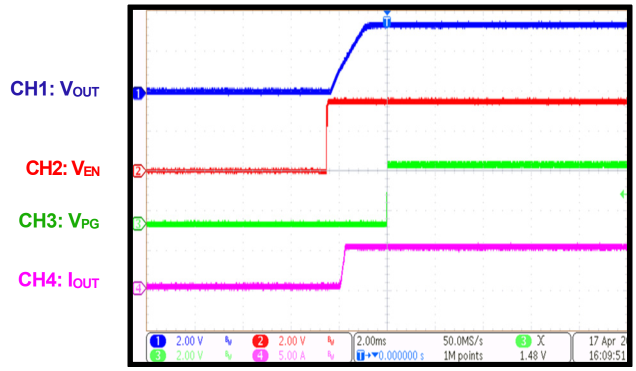
Start-Up through EN

I_{OUT} = 0A



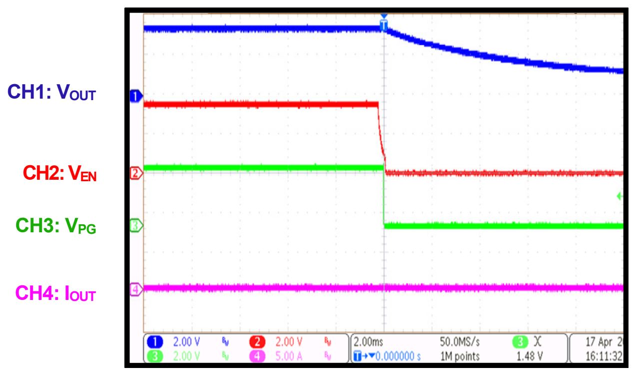
Start-Up through EN

I_{OUT} = 5A



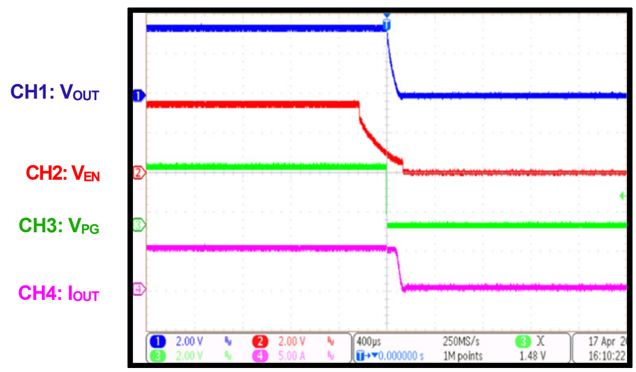
Shutdown through EN

I_{OUT} = 0A



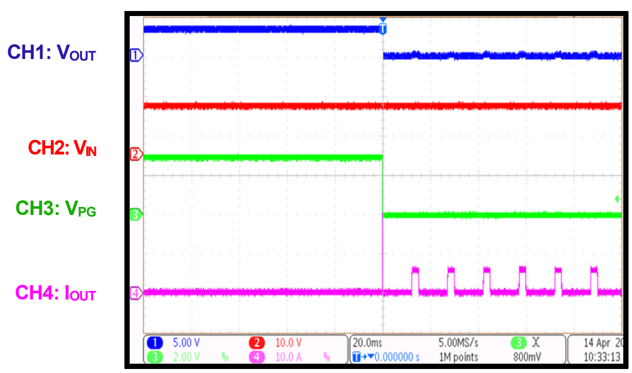
Shutdown through EN

I_{OUT} = 5A



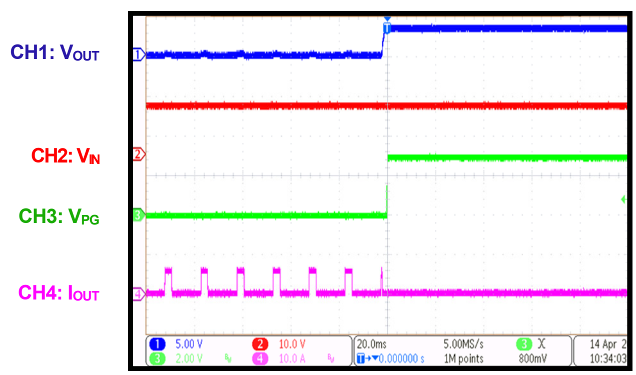
SCP Entry

I_{OUT} = 0A



SCP Recovery

I_{OUT} = 0A

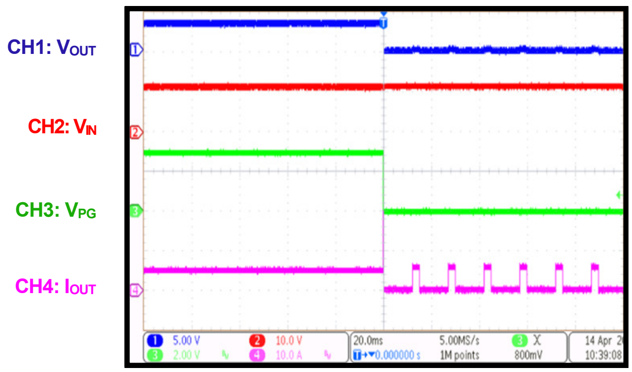


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

5A channel, V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 1MHz, C_{OUT} = 5 x 47µF ceramic capacitor, T_A = 25°C, unless otherwise noted.

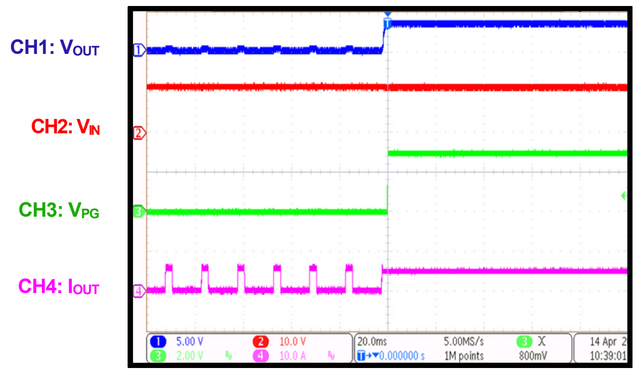
SCP Entry

I_{OUT} = 5A



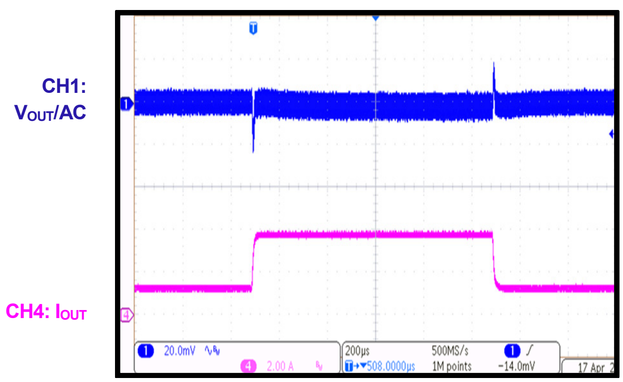
SCP Recovery

I_{OUT} = 5A



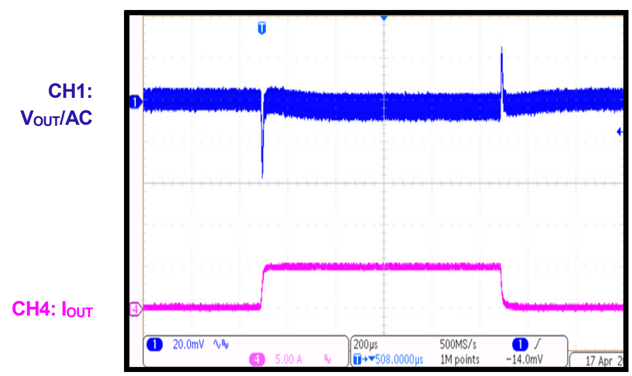
Load Transient

1.25A to 3.75A load step, 2.5A/µs



Load Transient

0A to 5A load step, 2.5A/µs



PCB LAYOUT

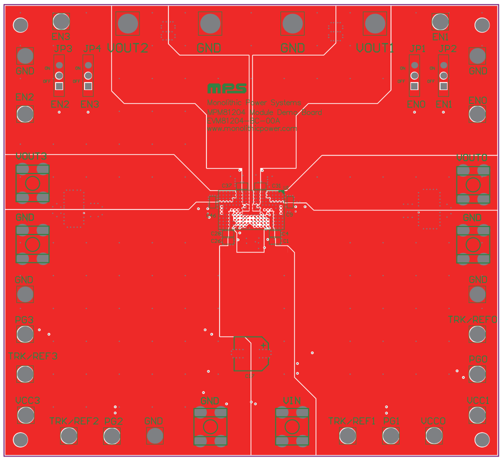


Figure 2: Top Layer

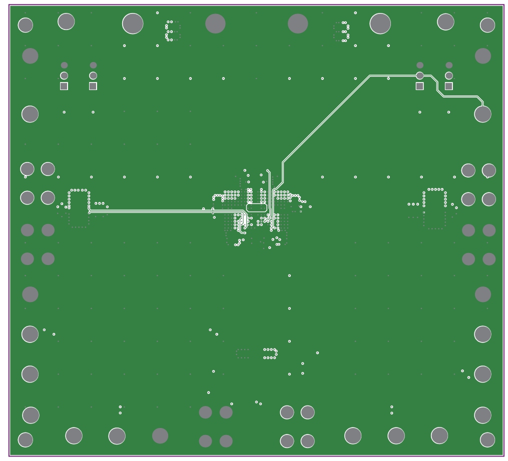


Figure 3: Mid-Layer 1

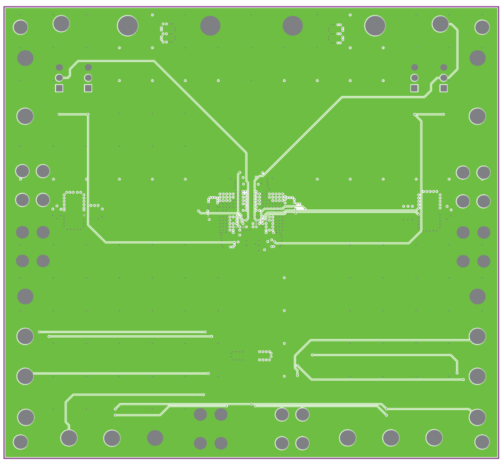


Figure 4: Mid-Layer 2

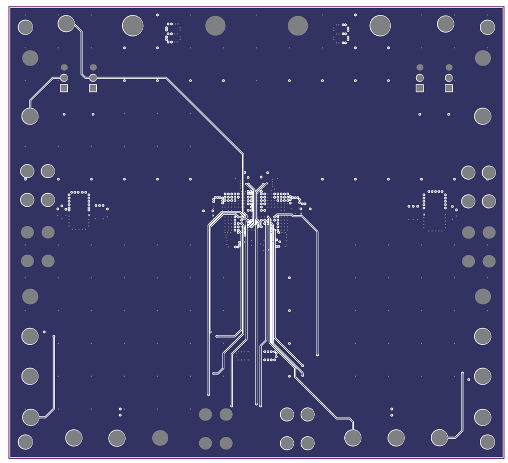


Figure 5: Mid-Layer 3

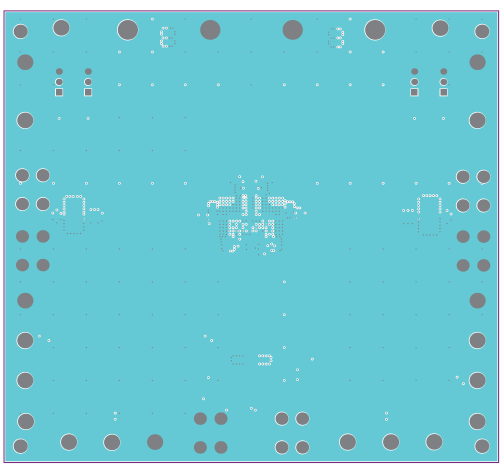


Figure 6: Mid-Layer 4

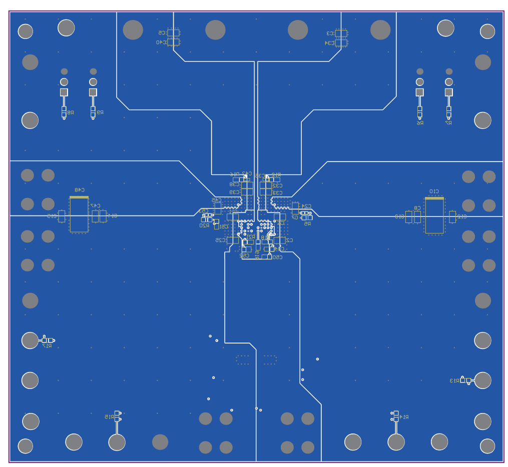


Figure 7: Bottom Layer

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/12/2021	Initial Release	-