EVL5520-QJ-00A

2.7V to 16V, Power-Outage Protection Management IC with Dual E-Fuses and Power-Sharing Function Evaluation Board

DESCRIPTION

The EVL5520-QJ-00A is an evaluation board designed to demonstrate the capabilities of the MP5520, a high-efficiency, monolithic converter used for power management in enterprise and datacenter solid-state drive (SSD) applications. The MP5520 integrates dual input current-limit switches (e-fuses), a bidirectional buck-boost converter, and a bidirectional power-sharing converter.

The dual e-fuses feature low on resistance ($R_{DS(ON)}$) and are designed for input voltages (V_{IN1} and V_{IN2}) up to 16V and 6V, respectively. Both e-fuses provide input current limiting and reverse-current blocking. Soft start (SS) prevents inrush current during system start-up.

The bidirectional buck-boost converter provides energy management. Backup energy is stored in high-voltage capacitors, where the configurable charging current controls the rate at which the storage voltage (V_{STRG}) ramps up. Paired with the reverse-current blocking function of the e-fuses, the backup energy is fully utilized to support the load during power outages.

When the bidirectional converter releases the energy from the storage capacitors, constant-on-time (COT) control minimizes the voltage drop during the transition from charge mode to backup mode. Only one inductor is required, which minimizes the total solution size.

The bidirectional power-sharing converter provides power sharing between the e-fuses. It can be configured to two modes: boost-sharing mode or buck-sharing mode. In buck-sharing mode, the MP5520 can work in either standalone mode or power-sharing mode.

The internal analog-to-digital converter (ADC) accurately monitors the input voltages (V_{INx}), input currents (I_{INx}), and input powers (P_{INx}). To guarantee long-term system reliability, the MP5520 provides storage capacitor health monitoring.

The MP5520 requires a minimal number of readily available, standard external components, and is available in a QFN-37 (5mmx6mm) package.

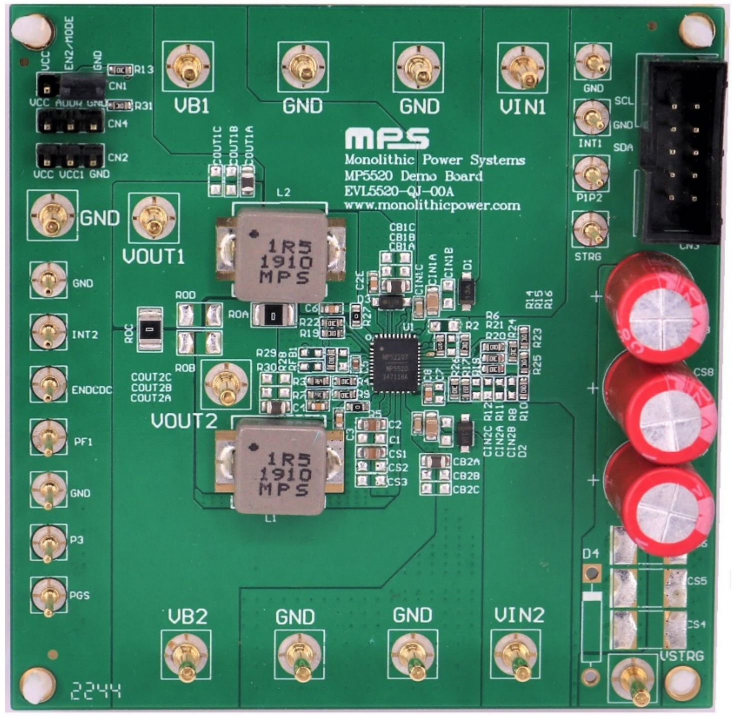
PERFORMANCE SUMMARY

Specifications are at T_A = 25°C, unless otherwise noted.

Parameters	Conditions	Value
E-fuse 1 input voltage (V_{IN1}) range		8.75V to 16V
E-fuse 2 input voltage (V_{IN2}) range		2.75V to 5.7V
Release output voltage (V_{BUS_RLS})	Configured by the FBR resistor divider	
DET trigger voltage (V_{DET})	Configured by the DET resistor divider	
Boost storage voltage (V_{STRG})	Configured by the FBS resistor divider	
PLP buck valley current limit	Digital interface-configurable	1A/3A/5A/7A
Switching frequency (f_{SW})	Digital interface-configurable	0.5MHz/1MHz/ 1.5MHz/2MHz

MPL Optimized Performance with MPS Inductor MPL-AY1050 Series

EVL5520-QJ-00A EVALUATION BOARD



LxWxH (8cmx8cmx3cm)

Board Number	MPS IC Number
EVL5520-QJ-00A	MP5520GQJ

QUICK START GUIDE

1. Connect the EN2/MODE pin to VCC via the jumper on CN1 to select SAS mode; connect EN2/MODE to GND to select PCI-E mode.
2. Connect VCC to VCC1 via the jumper on CN4 to pull up the open-drain indicators (PGS, PFI, INT1, INT2, and ENDCDC) to VCC via a 10kΩ pull-up resistor. Float VCC1 or connect the pin to GND to disable the indicator function.
3. Connect the load terminals to:
   a. Positive (+): VB1 or VB2 (1)
   b. Negative (-): GND
4. Preset the power supply output to 12V or 5V. (2)
5. Turn off the power supply.
6. Connect the power supply terminals to:
   a. Positive (+): VIN1 or VIN2 (2)
   b. Negative (-): GND
7. After making the connections, turn on the power supply. The MP5520 charges the storage capacitor to the target voltage.
8. To observe the power release performance, turn off the power supply.
9. To use the enable (EN) function, apply a digital input to the EN pin. Pull EN high to turn on the MP5520. Pull EN low to force the MP5520 into buck mode until the storage voltage (V_{STRG}) is fully discharged.
10. Connect the ADDR pin to VCC (logic high), to GND (logic low), or float ADDR. The ADDR pin status sets the digital interface slave address (see Table 1).

Table 1: Digital Interface Address Setting

ADDR Pin	Digital Interface Address
Logic low	33h
Logic high	35h
Floating	37h

11. Use R3 and R4 to set V_{STRG}, which can be calculated with Equation (1):

$$V_{STRG} = \left(1 + \frac{R3}{R4}\right) \times V_{FBS\_REF} \tag{1}$$

    Where the FBS reference voltage (V_{FBS_REF}) is typically 0.8V.

12. Select R3 and R4 based on application requirements. Larger R3 and R4 resistances typically have low leakage current, which is recommended for most designs. Table 2 lists the recommended FBS pin resistances for different V_{STRG} values.

Table 2: FBS Resistances for Storage Voltages

V_{STRG} (V)	R3 (kΩ)	R4 (kΩ)
12	140	10
20	240	10
30	365	10

13. The VB1 threshold voltage used to trigger buck release mode is set by R14 and R16, which are connected to the DET1 pin. Use R14 and R16 to set the power failure indicator voltage 1 (V_{B1_PFI}), which can be calculated with Equation (2):

$$V_{B1\_PFI} = \left(1 + \frac{R14}{R16}\right) \times V_{DET1\_REF} \tag{2}$$

    Where the DET1 reference voltage (V_{DET1_REF}) is typically 0.8V.

    The sum of R14 and R16 is recommended to be between 10kΩ and 200kΩ.

14. The VB2 threshold voltage used to trigger buck release mode is set by R17 and R26, which are connected to the DET2 pin. Use R17 and R26 to set the power failure indicator voltage 2 (V_{B2_PFI}), which can be calculated with Equation (3):

$$V_{B2\_PFI} = \left(1 + \frac{R17}{R26}\right) \times V_{DET2\_REF} \tag{3}$$

    Where the DET2 reference voltage (V_{DET2_REF}) is typically 0.8V.

    The sum of R17 and R26 is recommended to be between 10kΩ and 200kΩ.

15. After a power failure occurs, the bus voltage (V_{B1} or V_{B2}) regulation can be set via R7 and R9. (1) The bus output voltage when the IC is operating in backup mode (V_{BUS_RLS}) can be calculated with Equation (4):

$$V_{BUS\_RLS} = \left(1 + \frac{R7}{R9}\right) \times V_{FBR\_REF} \tag{4}$$

    Where the FBR reference voltage (V_{FBR_REF}) is typically 0.8V.

    The sum of R7 and R9 is recommended to be between 10kΩ and 200kΩ.

16. If the power-sharing buck operates in standalone mode, its output voltage (V_{PS}) is regulated by the resistor divider connected to the FB1 pin. Use R29 and R_{FB1} to set V_{PS}, which can be calculated with Equation (5):

$$V_{PS} = \left(1 + \frac{R29}{R_{FB1}}\right) \times V_{FB1\_REF} \tag{5}$$

    Where the FB1 reference voltage (V_{FB1_REF}) is 0.6V by default, and its value can be configured between 400mV and 1.27V via the digital interface.

    The sum of R29 and R_{FB1} is recommended to be between 10kΩ and 200kΩ.

17. If the power-sharing buck operates in power-sharing mode, it is recommended to connect FB1 to VCC, where R28 is set to 0Ω on the evaluation board.

18. The e-fuse current limits can be set via the digital interface. For more details, refer to the ILIM1 and ILIM2 register descriptions in the MP5520 datasheet.

Notes:

1) Use VB1 or VB2, depending on the application. For example, for PLP regulation at V_{BUS} = 12V during buck release, use VB1 as the charge source; for PLP regulation at V_{BUS} = 5V during buck release, use VB2 as the charge source.
2) Use 12V only, or both 12V and 5V, depending on the mode selection. For example, for SAS mode, use both 12V and 5V; for PCI-E mode, use 12V only.

19. Connect a capacitor to the DVDT1 and DVDT2 pins to control the slew rate when VB1 or VB2 rises during start-up, respectively. The DVDT1 rise time (t_{DVDT1}) is the soft-start time of VB1 rising from 0V to V_{IN1}, and can be calculated with Equation (6):

$$t_{DVDT1}(ms) = 0.34 \times C_{DVDT1}(nF) \tag{6}$$

The DVDT2 rise time (t_{DVDT2}) is the soft-start time of VB2 rising from 0V to V_{IN2}, and can be calculated with Equation (7):

$$t_{DVDT2}(ms) = 0.28 \times C_{DVDT2}(nF) \tag{7}$$

Where the recommended DVDT capacitances (C_{DVDTx}) is 10nF.

20. The storage capacitor stores energy during normal operation and releases this energy to VB during an input power loss. General-purpose electrolytic capacitors or low-profile polymer electrolytic (POS) capacitors are used for most applications. The capacitor voltage rating is recommended to be 20% above the target V_{STRG}.

The capacitance reduction and DC voltage offset should also be considered when selecting a storage capacitor. Different types of capacitors have varying capacitance derating performances. Choose a capacitor with a sufficient voltage rating to guarantee the capacitance.

The required capacitance depends on the length of the dying gasp for the application. The required storage capacitance (C_{STRG}) can be calculated with Equation (8):

$$C_{STRG} = \frac{2 \times V_{BUS\_RLS} \times I_{RLS} \times t_{DASP}}{\left[(V_{STRG})^2 - (V_{BUS\_RLS})^2\right] \times Eff.} \tag{8}$$

Where I_{RLS} is the bus release current when the bus voltage (V_{BUS}) is regulated at V_{BUS_RLS} in buck release mode, t_{DSAP} is the required dying gasp time, and Eff. is the energy release efficiency in buck release mode.

When choosing C_{STRG}, consider the desired efficiency during buck release mode. For example, if I_{RLS} is 3A, t_{DASP} is 20ms, V_{STRG} is 28V, V_{BUS_RLS} is 7.5V, and the efficiency is 90%, then the required C_{STRG} is 1374μF.

21. The BST capacitor (C_{BST}) supplies power to the buck converter's high-side MOSFET (HS-FET). It is recommended to use a 0.1μF to 1μF ceramic capacitor to decouple BST. Connect a 0.1μF or greater ceramic capacitor between CT1 and GND to achieve stable operation in boost sharing mode. In buck-sharing mode, CT1 and VB1 can be connected directly. The CT2 capacitor stabilizes the PLP converter's pre-charge loop. It is recommended to connect a 2.2μF or greater capacitor between CT2 and GND.

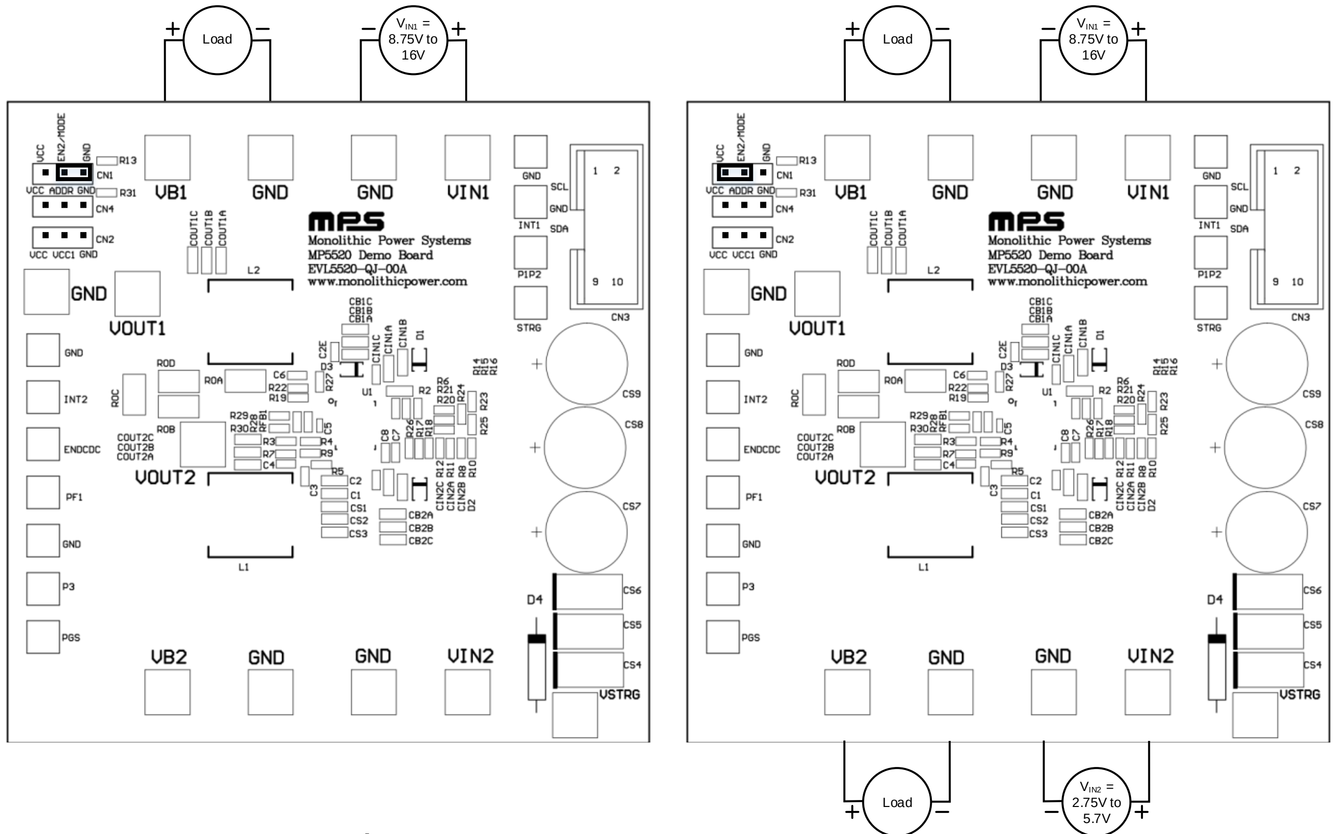
22. During the capacitor test, the MP5520 discharges C_{STRG} via an external resistor connected to the RT pin and the internal discharge MOSFET. The internal discharge MOSFET is connected from RT to GND with a resistance of about 1Ω. The discharge peak current should be limited below 500mA by the external resistor. A 1kΩ to 15kΩ discharge resistor is typically recommended.

23. A voltage spike may occur on the input switches during start-up or a fast shutdown. Adding an input capacitor can effectively reduce the voltage spike. The application determines the required capacitance. A larger-value capacitor typically reduces voltage spikes more effectively. However, a larger input capacitance also results in higher input inrush current, especially during hot-plug conditions.

A minimum 0.1μF capacitor is recommended since a higher capacitance can cause inrush current issues. To mitigate issues caused by the voltage spike, an efficient method is to add a TVS diode at the input, which also helps limit the inrush current during hot-plug conditions.

24. If necessary, the MP5520's register settings can be modified by connecting the MP5520 to the EVKT-USBI2C-02 kit. Use the MP5520's graphic user interface (GUI) to read and write the digital interface registers.

25. Figure 1 shows the proper measurement equipment set-up.



PCIe Mode **SAS Mode**

Figure 1: Measurement Equipment Set-Up

EVALUATION BOARD SCHEMATIC

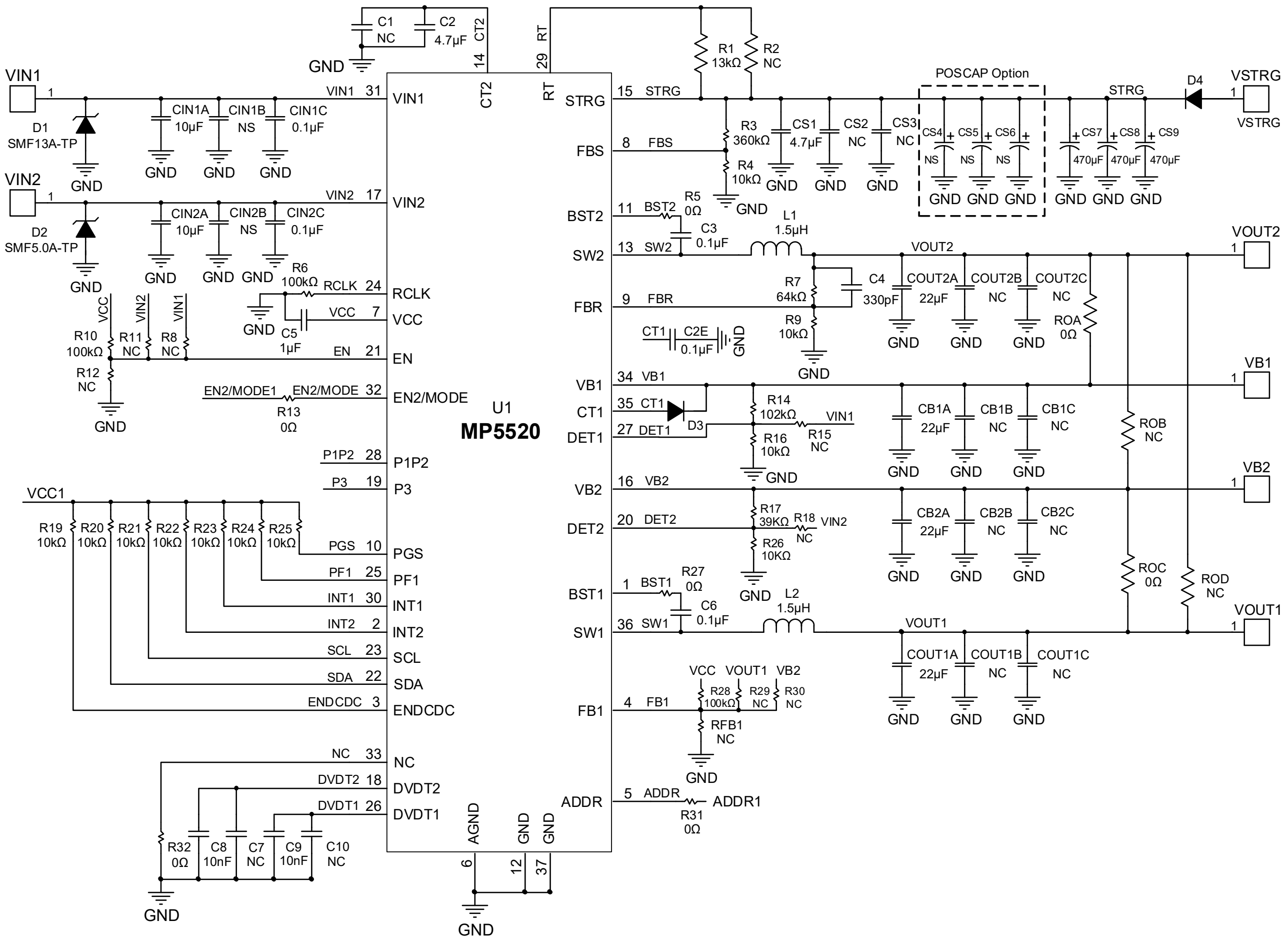


Figure 2: Evaluation Board Schematic

EVL5520-QJ-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
2	L1, L2 (Optional)	1.5µH	Inductor, RDC = 4.2mΩ, I_{SAT} = 29A	11.5mmx 10mmx 4mm	Sumida	104CDMCCDS-1R5MC
1	C4	330pF	Ceramic capacitor, 50V, X7R	0603	Wurth	885012206080
2	C8, C9	10nF	Ceramic capacitor, 50V, X7R	0603	Wurth	GRM188R71H103KA01D
2	CIN1C, CIN2C	0.1µF	Ceramic capacitor, 50V, X7R	0603	Wurth	885012206095
2	C6, C3, C2E	0.1µF	Ceramic capacitor, 25V, X7R	0603	Wurth	885012206071
1	C5	1µF	Ceramic capacitor, 25V, X6S	0402	Murata	GRM155C81E105KE11D
2	C2, CS1	4.7µF	Ceramic capacitor, 25V, X5R	0805	Murata	GRM21BR61E475KA12L
2	CIN1A, CIN2A	10µF	Ceramic capacitor, 25V, X7S	0805	Murata	GRM21BC71E106KE11L
4	COUT2A, CB1A, CB2A, COUT1A	22µF	Ceramic capacitor, 25V, X5R	0805	Murata	GRM21BR61E226ME44L
3	CS7, CS8, CS9	470µF	Capacitor, 20%, 50V	DIP	Wurth	860020675022
3	R5, R13, R31, R32, R27	0Ω	Film resistor, 1%	0603	Yageo	RC0603FR-070RL
2	ROA, ROC	0Ω	Film resistor, 1%	1210	Yageo	RC1210FR-070RL
12	R4, R9, R16, R19, R20, R21, R22, R23, R24, R25, R26	10kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710KL
1	R1	13kΩ	Film resistor, 1%	0805	Yageo	RC0805FR-0713KL
1	R17	39kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0739KL
1	R7	64.9kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0764K9L
3	R6, R10, R28	100kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-07100KL
1	R14	102kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-07102KL
1	R3	360kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-07360KL
1	D1	21.5V	TVS diode, 200W, 9.3A	SOD-123	MCC	SMF13A-TP
1	D2	9.2V	TVS diode, 200W, 21.7A	SOD-123FL	MCC	SMF5.0A-TP
1	D3	30V	Schottky barrier diode, 3A	3-2A1S	Toshiba	CRS30I30A
1	CN3	2.54mm	Digital interface connector, 2x10-pin	DIP	Wurth	612010235121
3	CN1, CN2, CN4	2.54mm	Straight header, 1x3-pin	DIP	Wurth	61300311121

EVL5520-QJ-00A BILL OF MATERIALS *(continued)*

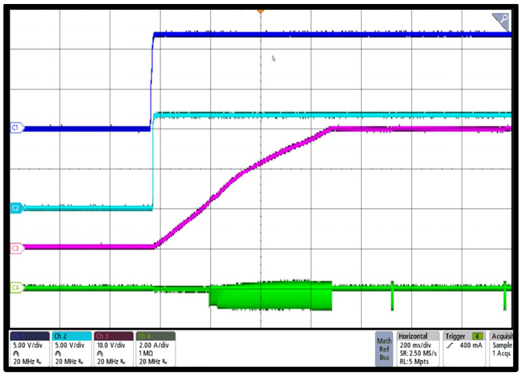
Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
12	VOUT1, VOUT2, VB1, VB2, GND, VSTRG, VIN1, VIN2	2mm	Copper pin	DIP	Custom	Custom
11	GND, PF1, ENDCDC, INT2, INT1, P1P2, P3, PGS	1mm	Copper pin	DIP	Custom	Custom
0	CIN1B, CIN2B, C1, CS2, CS3, CS4, CS5, CS6, C7, C10, C1, COUT2B, COUT2C, CB2B, CB2C, CB1B, CB1C	NS				
0	R2, R8, R11, R15, R18, R29, R30, RFB1, ROB, ROD	NS				
0	D4	NS				
2	L1, L2	1.5µH	Inductor, RDC = 3.4mΩ, I_{SAT} = 26.5A	1050	MPS	MPL-AY1050-1R5
1	U1	MP5520	2.7V to 16V power outage protection management IC with dual e-fuses and power-sharing function	QFN-37 (5mmx 6mm)	MPS	MP5520GQJ-xxxx

EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board V_{IN1} = 12V, V_{IN2} = 0V, V_{STRG} = 27.2V, V_{DET1} = 8.96V, V_{BUS_RLS} = 6V, L_{PLP} = L_{PS} = 1.5µH, T_A = 25°C, unless otherwise noted.

Input Start-Up

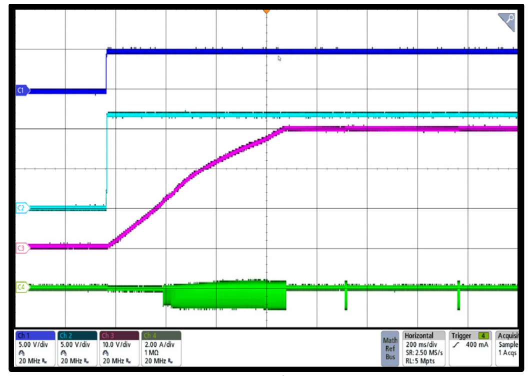
I_{VB1} = 3A



200ms/div.

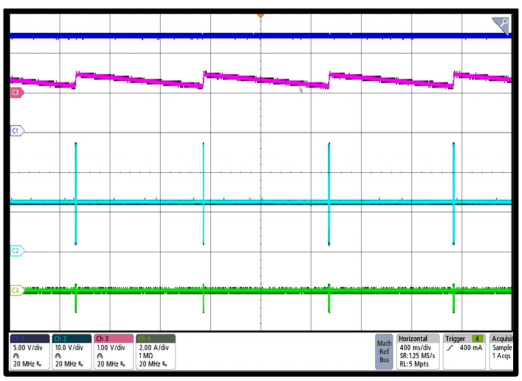
Start-Up through EN

I_{VB1} = 3A



200ms/div.

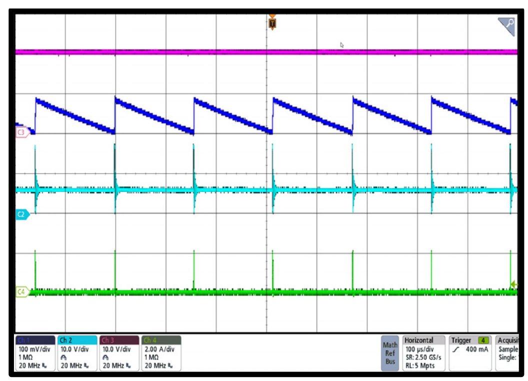
Boost Steady State



400ms/div.

PLP Buck Steady State

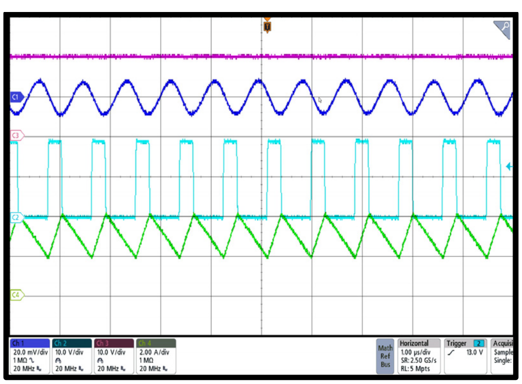
V_{STRG} = 20V, I_{VB1} = 0A, 22µF ceramic capacitor on VB1



100µs/div.

PLP Buck Steady State

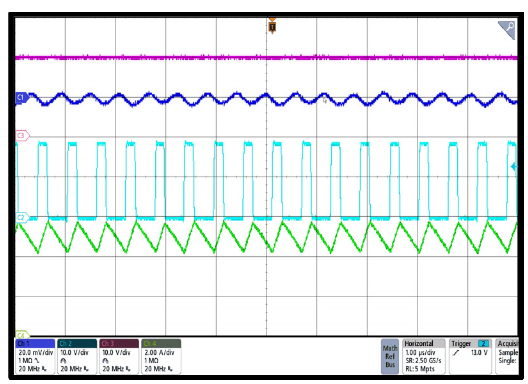
V_{STRG} = 20V, I_{VB1} = 3A, 22µF ceramic capacitor on VB1



1µs/div.

PLP Buck Steady State

V_{STRG} = 20V, I_{VB1} = 5A, 22µF ceramic capacitor on VB1



1µs/div.

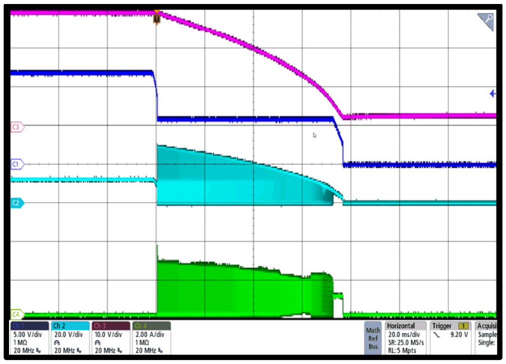
EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board V_{IN1} = 12V, V_{IN2} = 0V, V_{STRG} = 27.2V, V_{DET1} = 8.96V, V_{BUS_RLS} = 6V, L_{PLP} = L_{PS} = 1.5µH, T_A = 25°C, unless otherwise noted.

PLP Buck Release

I_{VB1} = 1A

CH3: V_{STRG} 10V/div.
CH1: V_{B1} 5V/div.
CH2: V_{SW2} 20V/div.
CH4: I_L 2A/div.

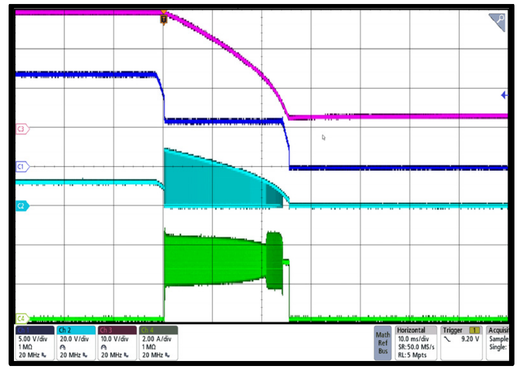


20ms/div.

PLP Buck Release

I_{VB1} = 3A

CH3: V_{STRG} 10V/div.
CH1: V_{B1} 5V/div.
CH2: V_{SW2} 20V/div.
CH4: I_L 2A/div.

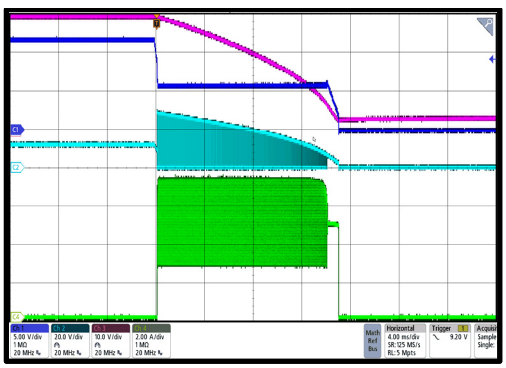


10ms/div.

PLP Buck Release

I_{VB1} = 5A

CH3: V_{STRG} 0V/div.
CH1: V_{B1} 5V/div.
CH2: V_{SW2} 20V/div.
CH4: I_L 2A/div.

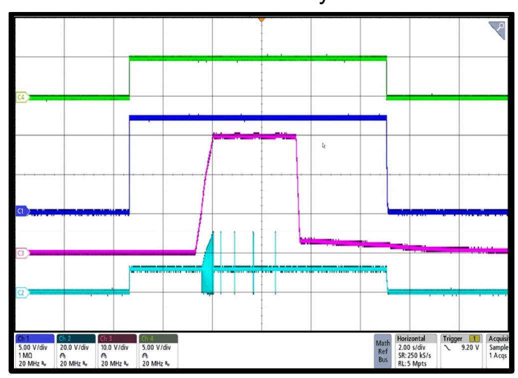


4ms/div.

Start-Up Sequence

EN starts up first followed by ENCH, then ENCH shuts down followed by EN

CH4: V_{EN} 5V/div.
CH1: V_{B1} 5V/div.
CH3: V_{STRG} 10V/div.
CH2: V_{SW2} 20V/div.

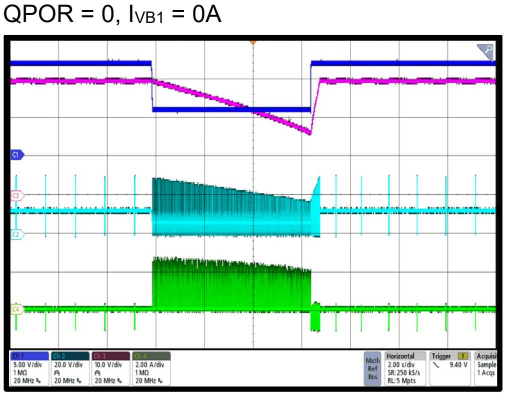


2s/div.

VIN1 Shutdown and Recovery during Release

QPOR = 0, I_{VB1} = 0A

CH1: V_{B1} 5V/div.
CH3: V_{STRG} 10V/div.
CH2: V_{SW2} 20V/div.
CH4: I_L 2A/div.

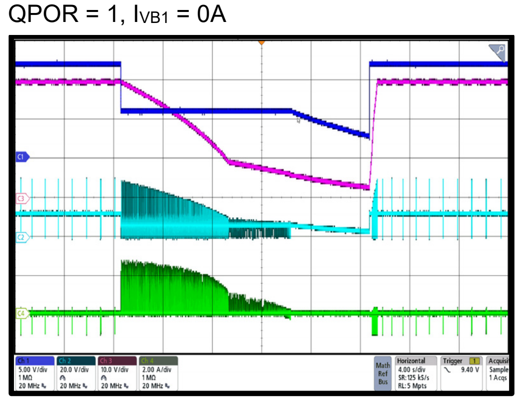


2s/div.

VIN1 Shutdown and Recovery during Release

QPOR = 1, I_{VB1} = 0A

CH1: V_{B1} 5V/div.
CH3: V_{STRG} 10V/div.
CH2: V_{SW2} 20V/div.
CH4: I_L 2A/div.



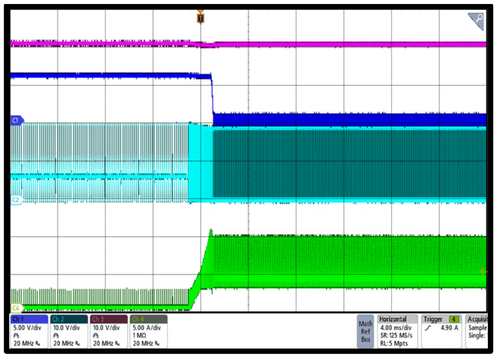
4s/div.

EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board V_{IN1} = 12V, V_{IN2} = 0V, V_{STRG} = 27.2V, V_{DET1} = 8.96V, V_{BUS_RLS} = 6V, L_{PLP} = L_{PS} = 1.5µH, T_A = 25°C, unless otherwise noted.

PLP Buck OCP

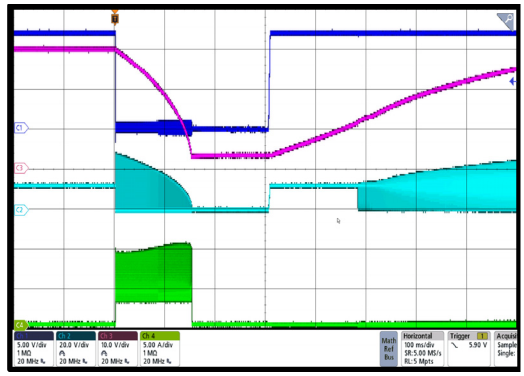
V_{STRG} = 20V, ILIM_RLS = 3A, add 7A load (3.2mA/µs) on VB1



4ms/div.

VB1 SCP and Recovery

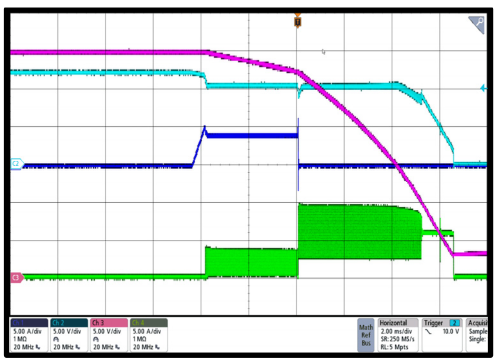
ILIM_RLS = 3A, short VB1 with wire, then recover



100ms/div.

CLBK Function

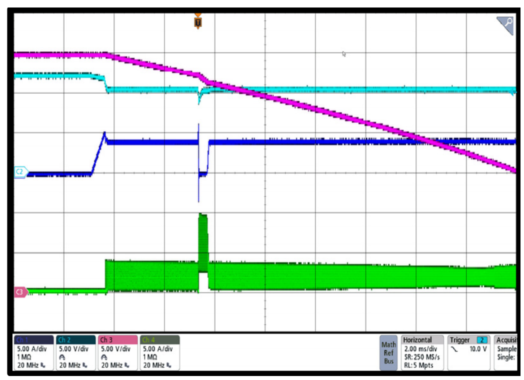
QPOR = 1, MAX_RLS_TIMER_CLBK = 6.3ms, VS_TH_CLBK = 92%



2ms/div.

CLBK Function

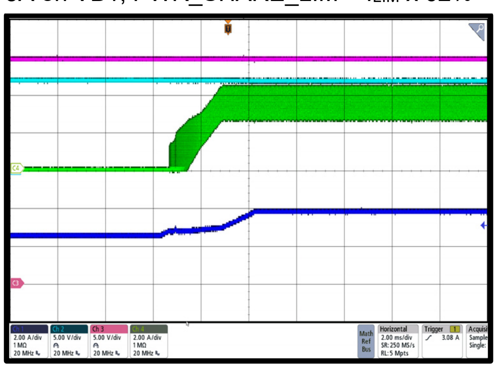
QPOR = 0, MAX_RLS_TIMER_CLBK = 6.3ms, VS_TH_CLBK = 92%



2ms/div.

Boost Power Sharing

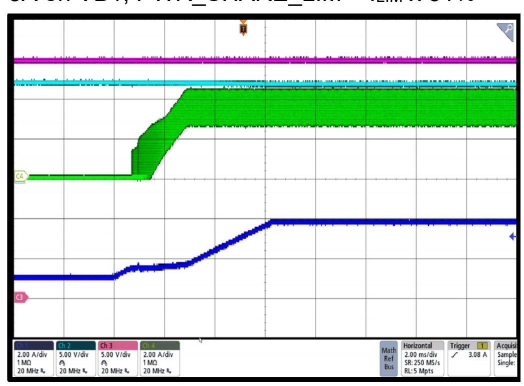
SAS mode, V_{IN1} = 12V, V_{IN2} = 5V, e-fuse 1 I_{LIM} = 4A, e-fuse 2 I_{LIM} = 6A, add load from 2.5A to 5A on VB1, PWR_SHARE_LIM = I_{LIM} x 62%



2ms/div.

Boost Power Sharing

SAS mode, V_{IN1} = 12V, V_{IN2} = 5V, e-fuse 1 I_{LIM} = 4A, e-fuse 2 I_{LIM} = 6A, add load from 1A to 5A on VB1, PWR_SHARE_LIM = I_{LIM} x 31%



2ms/div.

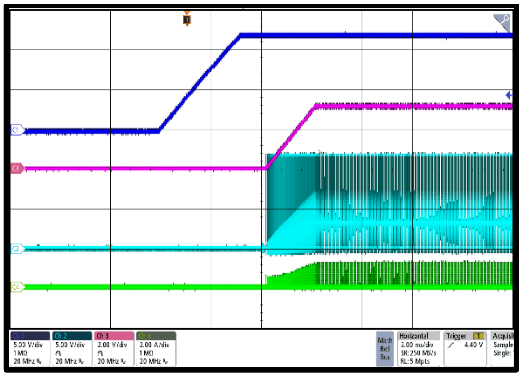
EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board V_{IN1} = 12V, V_{IN2} = 0V, V_{STRG} = 27.2V, V_{DET1} = 8.96V, V_{BUS_RLS} = 6V, L_{PLP} = L_{PS} = 1.5μH, T_A = 25°C, unless otherwise noted.

Power-Sharing Converter Input Start-Up

Standalone mode, R_{FB1} = 64.9kΩ / 15kΩ, start-up without load

CH1: V_{B1} 5V/div.
CH3: PS OUTPUT 2V/div.
CH2: V_{SW1} 5V/div.
CH4: I_{L_PS} 2A/div.

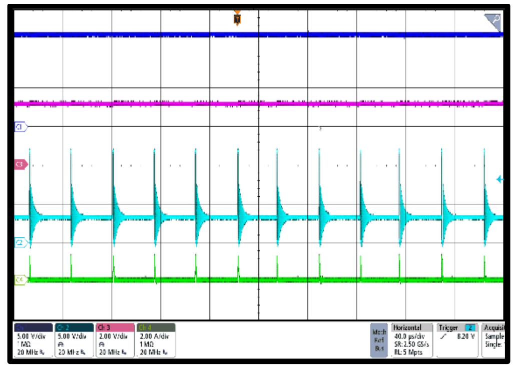


2ms/div.

Power-Sharing Converter Steady State

Standalone mode, without load

CH1: V_{B1} 5V/div.
CH3: PS OUTPUT 2V/div.
CH2: V_{SW1} 5V/div.
CH4: I_{L_PS} 2A/div.

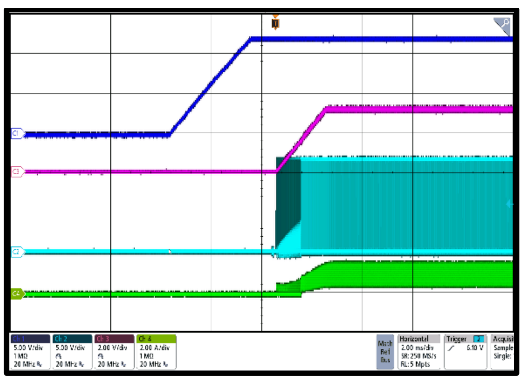


40μs/div.

Power-Sharing Converter Input Start-Up

Standalone mode, start-up with 1A load

CH1: V_{B1} 5V/div.
CH3: PS OUTPUT 2V/div.
CH2: V_{SW1} 5V/div.
CH4: I_{L_PS} 2A/div.

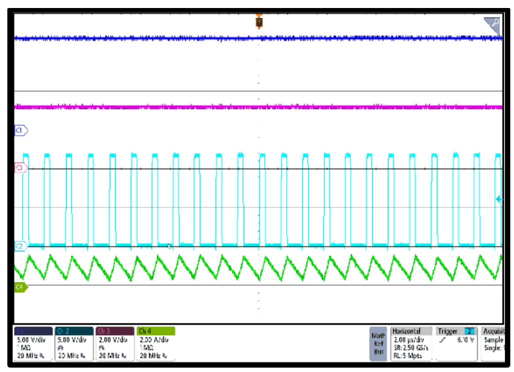


2ms/div.

Power-Sharing Converter Steady State

Standalone mode, 1A load

CH1: V_{B1} 5V/div.
CH3: PS OUTPUT 2V/div.
CH2: V_{SW1} 5V/div.
CH4: I_{L_PS} 2A/div.

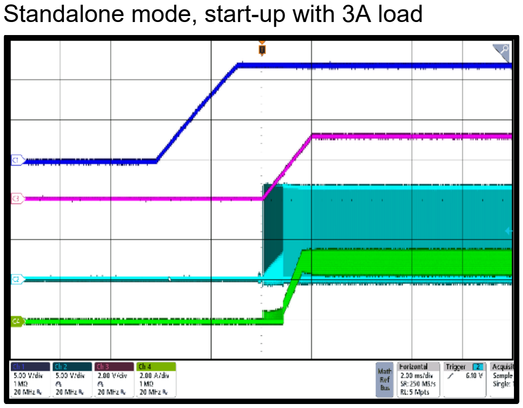


2μs/div.

Power-Sharing Converter Input Start-Up

Standalone mode, start-up with 3A load

CH1: V_{B1} 5V/div.
CH3: PS OUTPUT 2V/div.
CH2: V_{SW1} 5V/div.
CH4: I_{L_PS} 2A/div.



2ms/div.

Power-Sharing Converter Steady State

Standalone mode, 3A load

CH1: V_{B1} 5V/div.
CH3: PS OUTPUT 2V/div.
CH2: V_{SW1} 5V/div.
CH4: I_{L_PS} 2A/div.

2μs/div.

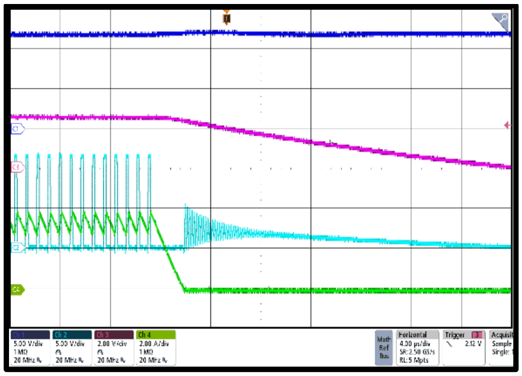
EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board V_{IN1} = 12V, V_{IN2} = 0V, V_{STRG} = 27.2V, V_{DET1} = 8.96V, V_{BUS_RLS} = 6V, L_{PLP} = L_{PS} = 1.5µH, T_A = 25°C, unless otherwise noted.

Power-Sharing Converter OCP

I_{LIM_RLS} = 3A

CH1: V_{B1} 5V/div.
CH3: PS OUTPUT 2V/div.
CH2: V_{SW1} 5V/div.
CH4: I_{L_PS} 2A/div.

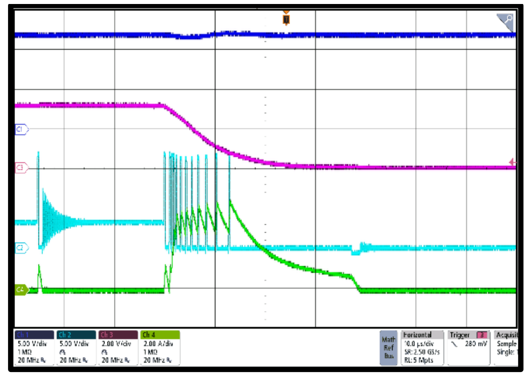


4µs/div.

Power-Sharing Converter SCP Entry

I_{LIM_RLS} = 3A

CH1: V_{B1} 5V/div.
CH3: PS OUTPUT 2V/div.
CH2: V_{SW1} 5V/div.
CH4: I_{L_PS} 2A/div.



10µs/div.

PCB LAYOUT

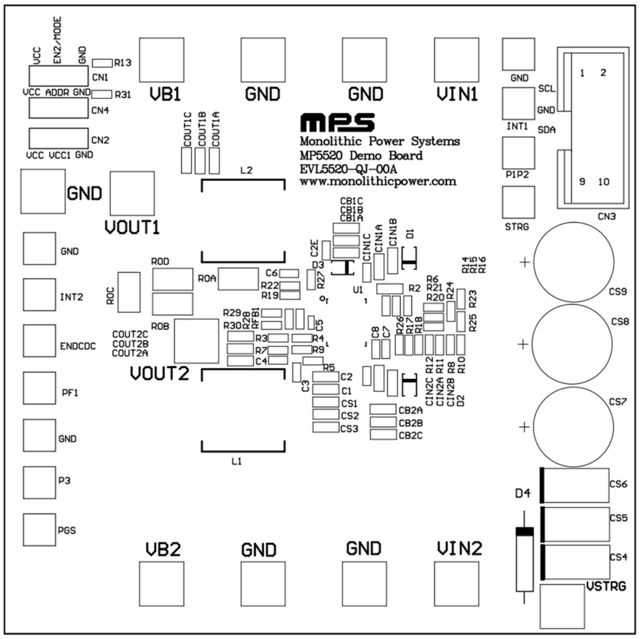


Figure 3: Top Silk

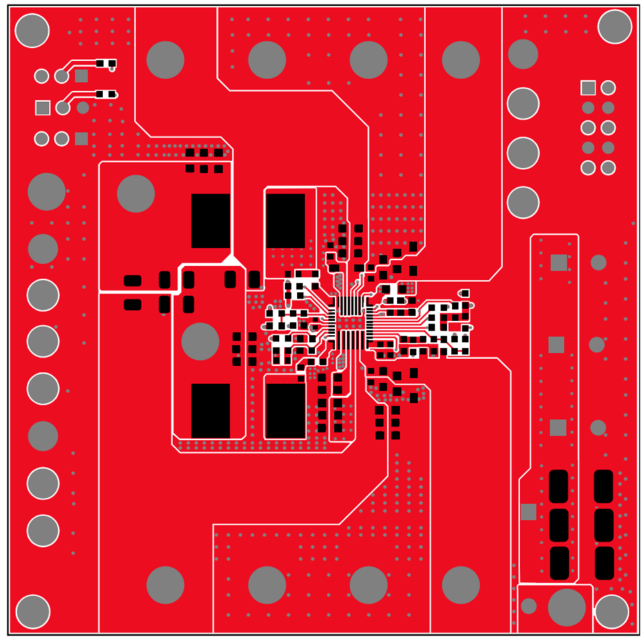


Figure 4: Top Layer

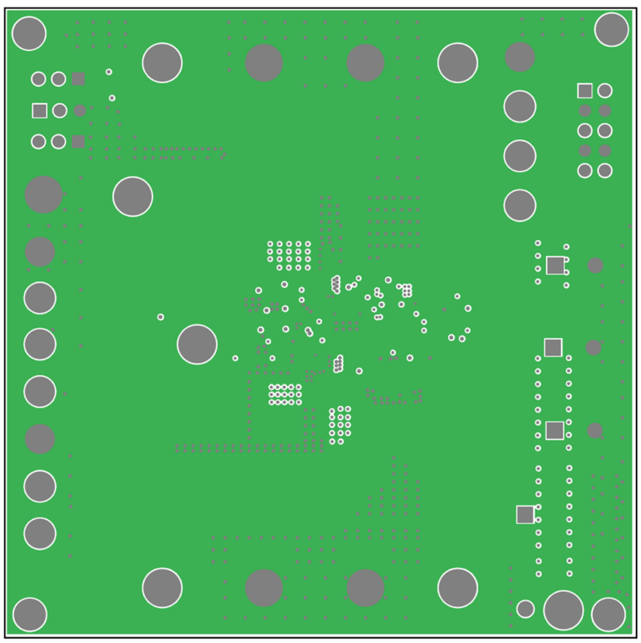


Figure 5: Mid-Layer 1

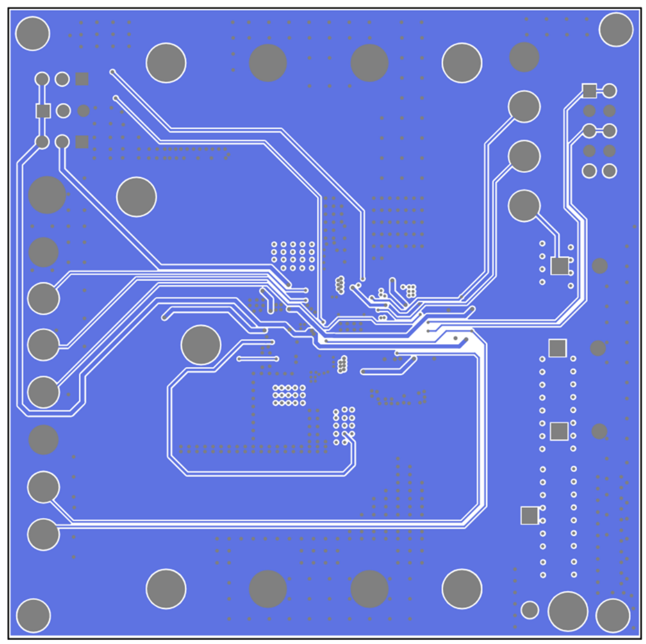


Figure 6: Mid-Layer 2

PCB LAYOUT *(continued)*

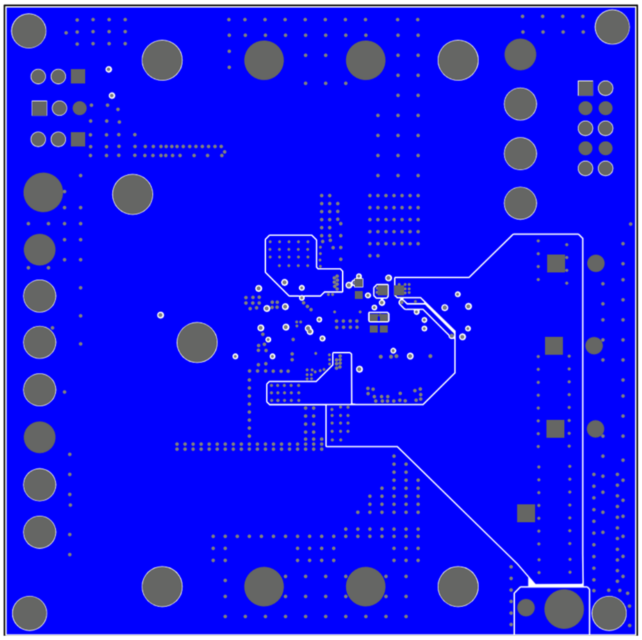


Figure 7: Bottom Layer

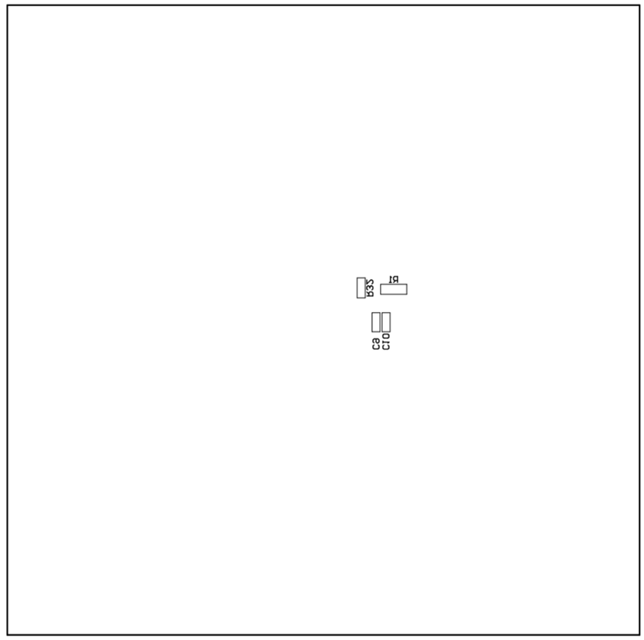


Figure 8: Bottom Silk

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	7/18/2023	Initial Release	-