EV9181DD-00A

High Effeciency, Fast Transient, 3A, 20V Synchronous Step-down Converter

The Future of Analog IC Technology

DESCRIPTION

The EV9181DD-00A is a fully integrated high frequency synchronous rectified step-down switch mode converter. It offers a very compact solution to achieve 3A continuous output current over a wide input supply range with excellent load and line regulation. The MP9181 operates at high efficiency over a wide output current load range.

Constant-On-Time (COT) control mode provides fast transient response and eases loop stabilization.

Full protection features include OCP, OVP, UVP and thermal shut down.

The EV9181DD-00A requires a minimum number of readily available standard external components and is available in a space saving 2mm x 3mm 12-pin QFN package.

ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Value	Units
Input Voltage Range	V_{IN}	4.5-20	V
Output Voltage	V_{OUT}	1.2	V
Load Max	I_{OUT}	3	A

FEATURES

- Wide 4.5V to 20V Operating Input Range
- 3A Output Current
- Low R_{DS}(ON) Internal Power MOSFETs
- Proprietary Switching Loss Reduction Technique
- 1% Reference Voltage
- Soft Shutdown
- Programmable Switching Frequency
- OCP, OVP, UVP Protection and Thermal Shutdown
- Output Adjustable from 0.815V to 13V
- Available in 12-pin QFN2x3 Package

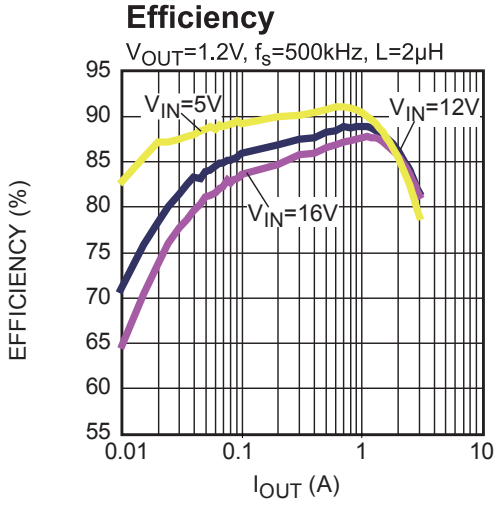
APPLICATIONS

- Notebook Systems and I/O Power
- Networking Systems
- Digital Set Top Boxes
- Personal Video Recorders
- Flat Panel Television and Monitors
- Distributed Power Systems

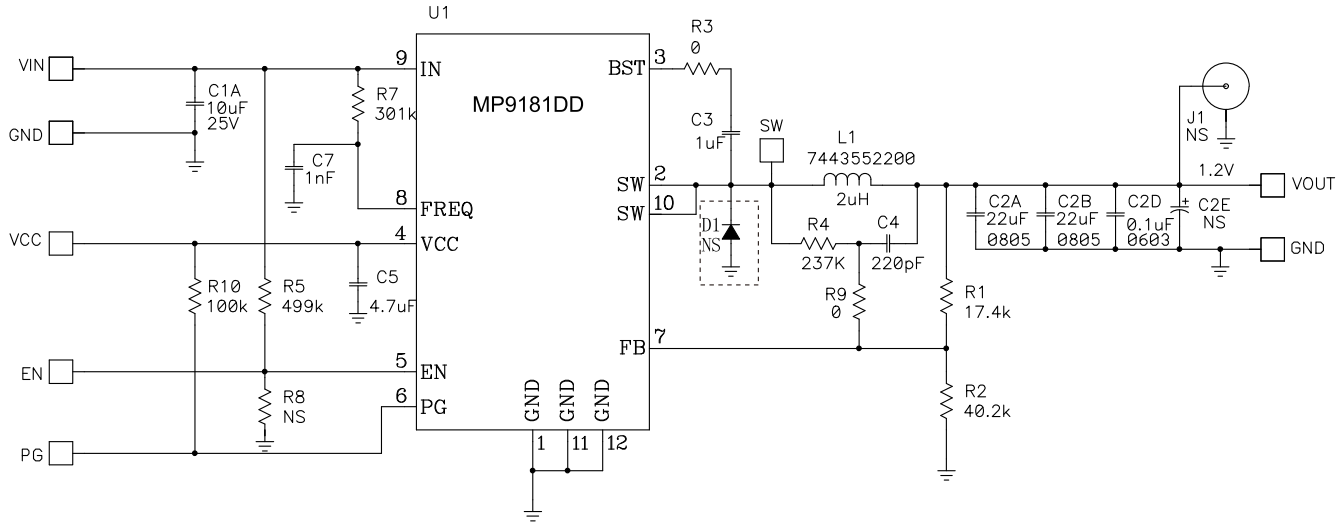
EV9181DD-00A EVALUATION BOARD

(L x W x H) 2.54'' X 2.54'' X 0.06''
(63.5mm x 63.5mm x 1.6mm)

Board Number	MPS IC Number
EV9181DD-00A	MP9181DD



EVALUATION BOARD SCHEMATIC



EV9181DD-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer P/N
1	C1A	10µF	Ceramic Cap., 25V, 10%, X7R	1210	muRata	GRM32DR71E106K
2	C2A,C2B	22µF	Ceramic Cap., 6.3V, 10%, X5R	1210	muRata	GRM32DR60J226K
1	C2D	0.1µF	Ceramic Cap., 50V, 10%, X7R	0603	muRata	GRM188R71H104K
0	C2E	NS	POSCAP	D SIZE		
1	C3	1µF	Ceramic Cap., 25V, 10%, X7R	0603	muRata	GRM188R71E104K
1	C4	220pF	Ceramic Cap., 50V, 5%, C0G	0603	muRata	GRM1885C1H221J
1	C5	4.7µF	Ceramic Cap., 6.3V, 10%, X7R	0603	muRata	GRM188R70J475K
1	C7	1nF	Ceramic Cap., 50V, 5%, C0G	0603	muRata	GRM1885C1H102J
0	D1	NS		SOD123		
0	J1	NS	socket	SMA		
1	L1	2µH	Inductor	10x10x5mm	Wurth	WE-7443552200
1	R1	17.4k	Film Res., 1%	0603	Yageo	RC0603FR-0717K4L
1	R2	40.2k	Film Res., 1%	0603	Yageo	RC0603FR-0740K2L
2	R3, R9	0	Film Res., 5%	0603	Yageo	RC0603JR-070R0L
1	R4	237k	Film Res., 1%	0603	Yageo	RC0603FR-07237KL
1	R5	499k	Film Res., 1%	0603	Yageo	RC0603FR-07499KL
1	R7	301k	Film Res., 1%	0603	Yageo	RC0603FR-07301KL
0	R8	NS		0603		
1	R10	100k	Film Res., 5%	0603	Yageo	RC0603JR-07100KL
1	U1	IC	Synch Step-Down converter	QFN12	MPS	MP9181DD

PRINTED CIRCUIT BOARD LAYOUT

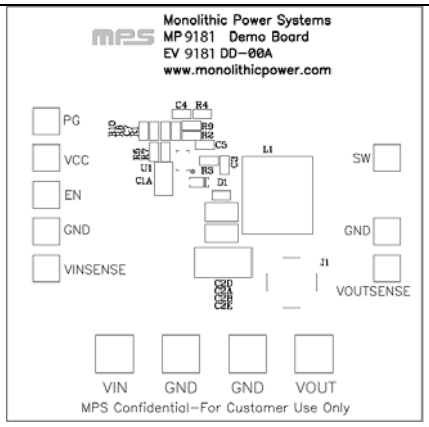


Figure 1—Top Silk Layer

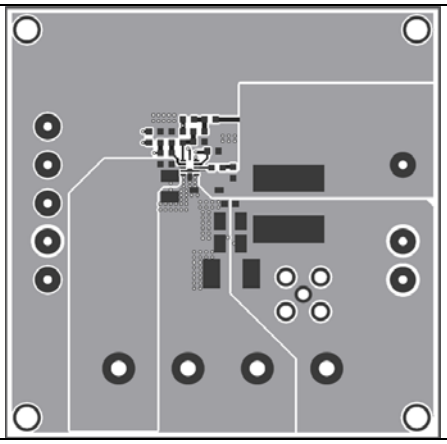


Figure 2—Top Layer

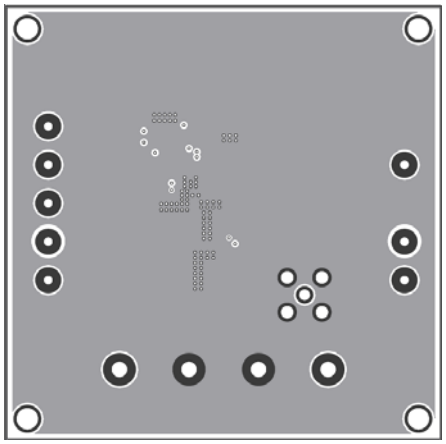


Figure 3—Inner Layer 1

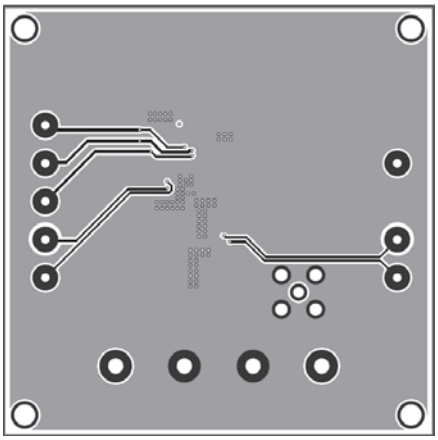


Figure 4— Inner Layer 2

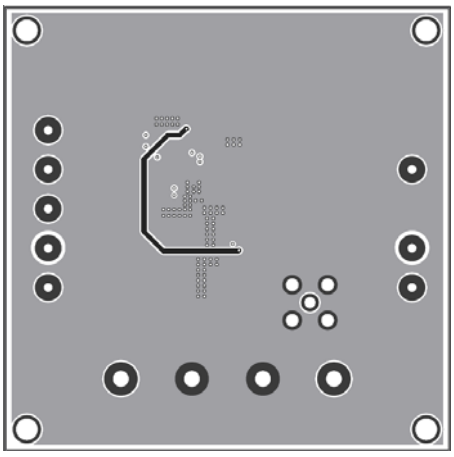


Figure 5—Bottom Layer

QUICK START GUIDE

The default output voltage of this board is set to 1.2V.
The board layout accommodates most commonly used inductors and output capacitors.

1. Attach the positive and negative ends of the load to the VOUT and GND pins, respectively.
2. Attach the input voltage (4.5V≤V_{IN}≤20V) and input ground to the VIN and GND pins, respectively. Then the board is powered up.
3. The EV9181DD-00A is enabled ON in default. It's turned on once the input voltage is applied. To enable the board externally, apply a voltage, V_{EN}≥2V, to the EN pin. To disable the board, apply a voltage, V_{EN}≤0.4V, to the EN pin.

Setting the Output Voltage

Case 1: POSCAP, OSCON or Aluminum capacitors used in the output

1. Choose a value for R2. A value within 5kΩ-40kΩ is recommended to ensure stable operation.
2. R1 is determined as follows:

$$R_1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_2$$

Where V_{REF} is 0.815V

Case 2: Ceramic capacitors used in the output

An external voltage ramp should be added to FB through resistor R_4 and capacitor C_4.

1. Choose a value for C4 within 100-680pF.
2. Determine R4 as follows:

$$V_{RAMP} = \frac{(V_{IN} - V_{OUT}) \times T_{ON}}{R4 \times C4}$$

Where Vramp is the external ramp voltage generated to FB. 30mV should be enough for most of the applications.

3. Choose a value within 5kΩ-40kΩ for R2.
4. The value of R1 then is determined as follows:

$$R1 = \frac{1}{\frac{V_{REF} + \frac{1}{2}V_{RAMP}}{R2(V_{OUT} - V_{REF} - \frac{1}{2}V_{RAMP})} - \frac{1}{R4}}$$

5. Make sure the ramp circuit impedance is much smaller than the FB circuit impedance as follows:

$$\frac{1}{2\pi \times Fs \times C4} < \frac{1}{5}\left(\frac{R1 \times R2}{R1 + R2}\right)$$

If not, restart from step 1 until it fulfills the above condition.

Layout Recommendation

1. Put the input capacitors (C1A) as close as to the VIN pin.
2. Put the decoupling capacitor (C5) as close as to the VCC pin.
3. Put the inductor as close as to SW pin. Make the SW pad as large as possible to minimize the switching noise interference.
4. The FB pin is directly connected to the PWM comparator. It should be routed away from the noisy SW node.