EV8606A-L-00A

High Effeciency, Fast Transient, 6A, 6V Synchronous Step-down Converter

The Future of Analog IC Technology

DESCRIPTION

The EV8606A-L-00A evaluation Board is designed to demonstrate the capabilities of MP8606A, a fully integrated high frequency synchronous rectified step-down switch mode converter. It offers a very compact solution to achieve 6A continuous output current over a wide input supply range with excellent load and line regulation. The MP8606A operates at high efficiency over a wide output current load range.

Constant-On-Time (COT) control mode provides fast transient response and eases loop stabilization.

Full protection features include OCP, OVP, UVP and thermal shut down.

The EV8606A-L-00A requires a minimum number of readily available standard external components and is available in a space saving 3mm x 4mm 20-pin QFN package.

FEATURES

- 6A Output Current
- 14mΩ Internal High-Side Power Switches
- 8mΩ Internal Low-Side Power Switches
- Input Operation Range: 2.9V to 6.5V
- Adjustable Output Down to 0.6V
- Programmable Switching Frequency
- Hiccup Over-Current Protection
- Programmable Soft-Start Time
- Thermal Shutdown
- Power-Good Output
- 3mmx4mm Flip-Chip Package

APPLICATIONS

- µP/ASIC/DSP/FPGA Core and I/O Supplies
- Portable Equipment / Notebook Computers
- Network and Telecom Equipment
- Point of Load Regulators

ELECTRICAL SPECIFICATIONS

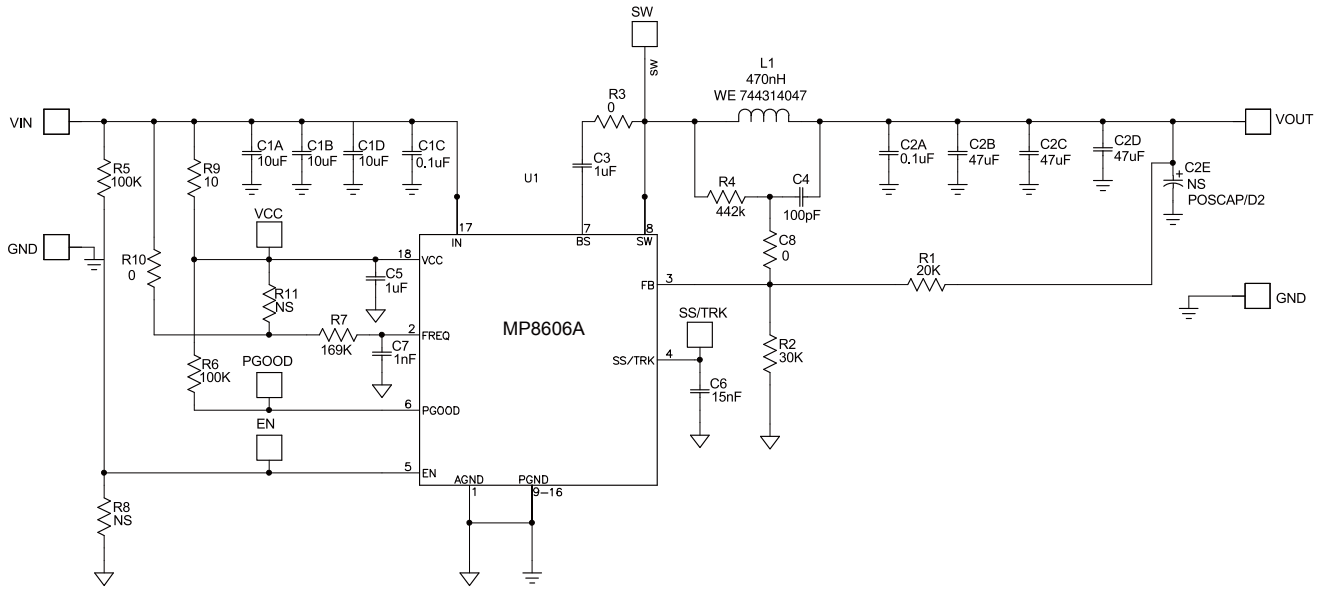
Parameter	Symbol	Value	Units
Input Voltage Range	V_{IN}	2.9-6	V
Output Voltage	V_{OUT}	1	V
Load Max	I_{OUT}	6	A

EV8606A-L-00A EVALUATION BOARD

(L x W x H) 2.54'' X 2.54'' X 0.06''
(63.5mm x 63.5mm x 1.6mm)

Board Number	MPS IC Number
EV8606A-L-00A	MP8606A

EVALUATION BOARD SCHEMATIC



EV8606A-L-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer P/N
3	C1A, C1B, C1D	10µF	Ceramic Cap., 10V, 10%, X7R	0805	Any	Any
1	C2A	0.1Mf	Ceramic Cap., 50V, 10%, X7R	0603	Any	Any
3	C2B, C2C, C2D	47µF	Ceramic Cap., 6.3V, 20%, X5R	1206	muRata	GRM31CR60J476M
0	C2E	NS	POSCAP	D SIZE		
1	C3	1µF	Ceramic Cap., 25V, 10%, X7R	0603	muRata	GRM188R71E104K
1	C4	100pF	Ceramic Cap., 50V, 5%, C0G	0603	muRata	GRM1885C1H101J
1	C5	1µF	Ceramic Cap., 6.3V, 10%, X7R	0603	muRata	GRM188R70J105K
1	C7	1nF	Ceramic Cap., 50V, 5%, C0G	0603	muRata	GRM1885C1H102J
0	J1	NS	socket	SMA		
1	L1	0.47µH	Inductor	1	Wurth	WE-744317047
1	R1	20k	Film Res., 1%	0603	Yageo	RC0603FR-0720K0L
1	R2	30k	Film Res., 1%	0603	Yageo	RC0603FR-0300K0L
3	R3, C8, R10	0	Film Res., 5%	0603	Yageo	RC0603JR-070R0L
1	R4	442k	Film Res., 1%	0603	Yageo	RC0603FR-07442KL
2	R5, R6	100k	Film Res., 1%	0603	Yageo	RC0603FR-07100KL
1	R7	169k	Film Res., 1%	0603	Yageo	RC0603FR-07169KL
0	R8, R11	NS		0603		
1	R9	10	Film Res., 5%	0603	Yageo	RC0603JR-0710L
1	U1	IC	Synch Step-Down converter	QFN20	MPS	MP8606A

PRINTED CIRCUIT BOARD LAYOUT

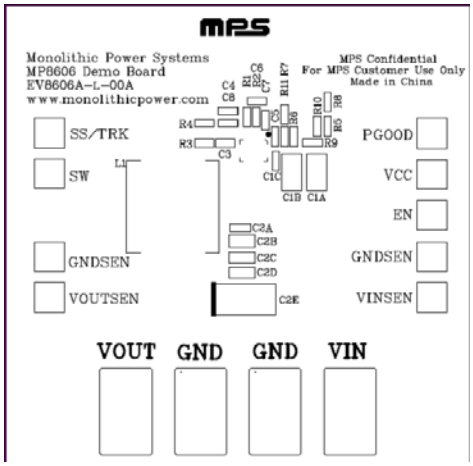


Figure 1—Top Silk Layer

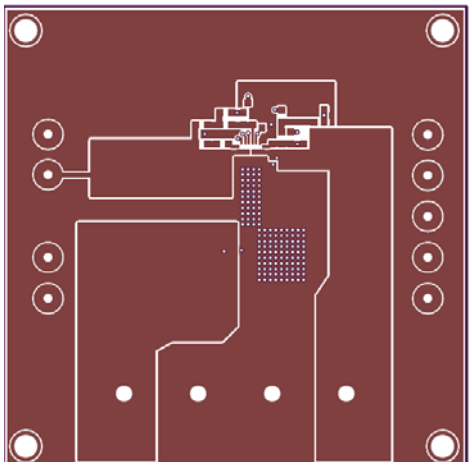


Figure 2—Top Layer

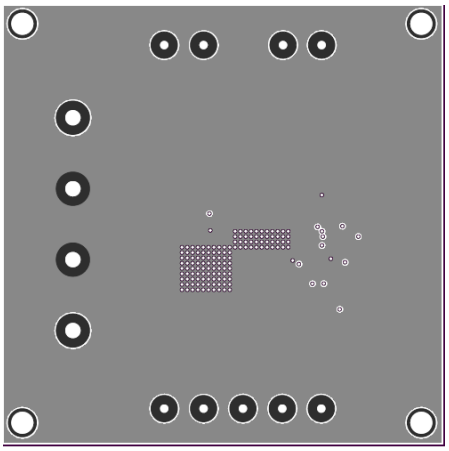


Figure 3—Inner Layer 1

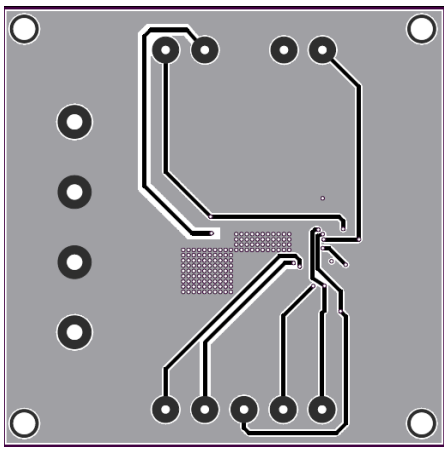


Figure 4— Inner Layer 2

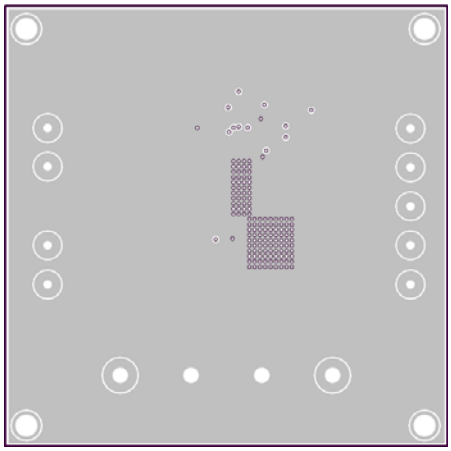


Figure 5—Bottom Layer

QUICK START GUIDE

The default output voltage of this board is set to 1V.

The board layout accommodates most commonly used inductors and output capacitors.

1. Attach the positive and negative ends of the load to the VOUT and GND pins, respectively.
2. Attach the input voltage (2.9V≤V_{IN}≤6V) and input ground to the VIN and GND pins, respectively. Then the board is powered up.
3. The EV8606A-L-00A is enabled ON in default. It's turned on once the input voltage is applied. To enable the board externally, apply a voltage, V_{EN}≥2V, to the EN pin. To disable the board, apply a voltage, V_{EN}≤0.4V, to the EN pin.

Setting the Output Voltage

Case 1: POSCAP, OSCON or Aluminum capacitors used in the output

1. Choose a value for R2. A value within 5kΩ-40kΩ is recommended to ensure stable operation.
2. R1 is determined as follows:

$$R_1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_2$$

Where V_{REF} is 0.6V

Case 2: Ceramic capacitors used in the output
An external voltage ramp should be added to FB through resistor R_4 and capacitor C_4.

1. Choose a value for C4 within 100-680pF.
2. Determine R4 as follows:

$$V_{RAMP} = \frac{(V_{IN} - V_{OUT}) \times T_{ON}}{R4 \times C4}$$

Where Vramp is the external ramp voltage generated to FB. 30mV should be enough for most of the applications.

3. Choose a value within 5kΩ-40kΩ for R2.
4. The value of R1 then is determined as follows:

$$R1 = \frac{1}{\frac{V_{REF} + \frac{1}{2}V_{RAMP}}{R2(V_{OUT} - V_{REF} - \frac{1}{2}V_{RAMP})} - \frac{1}{R4}}$$

5. Make sure the ramp circuit impedance is much smaller than the FB circuit impedance as follows:

$$\frac{1}{2\pi \times Fs \times C4} < \frac{1}{5}\left(\frac{R1 \times R2}{R1 + R2}\right)$$

If not, restart from step 1 until it fulfills the above condition.

Layout Recommendation

1. Put the input capacitors (C1A) as close as to the VIN pin.
2. Put the decoupling capacitor (C5) as close as to the VCC pin.
3. Put the inductor as close as to SW pin. Make the SW pad as small as possible to minimize the switching noise interference.
4. Place feedback resistor divider close to the FB pin. The FB pin is directly connected to the PWM comparator. It should be routed away from the noisy SW node.