EV2764-V-00B

I^2C/SMBus-Controlled Integrated Buck-Boost NVDC Charger with PSYS and PROCHOT for Multi-Cell Battery Pack with a Single Inductor Evaluation Board

DESCRIPTION

The EV2764-V-00B evaluation board is designed to demonstrate the capabilities of the MP2764 with a single inductor. The MP2764 is a highly integrated, buck-boost narrow-voltage DC (NVDC) charger IC with USB Power Delivery (PD) source mode, as well as PSYS monitoring and PROCHOT monitoring. It is designed for applications with 2-cell to 4-cell series battery packs.

The MP2764 can accept a wide 4V to 22V operating input voltage (V_{IN}) range for charging and provide a wide output voltage (V_{IN_SRC}) from 4V to 21V with 20mV/step at the input in USB PD source mode.

When V_{IN} is present, the EV2764-V-00B charges the battery automatically with a maximum 8A charge current (I_{CHG}).

When an input source is absent, the system is powered by the battery through the battery FET (BFET). The IC has output current (I_{IN_SRC}) limit regulation in USB PD source mode.

The EV2764-V-00B can be flexibly configured via the I^2C/SMBus interface to set the charging parameters, V_{IN_SRC}, and I_{IN_SRC} in USB PD source mode.

The MP2764 is available in a QFN-32 (4mmx5mm) package.

PERFORMANCE SUMMARY [1]

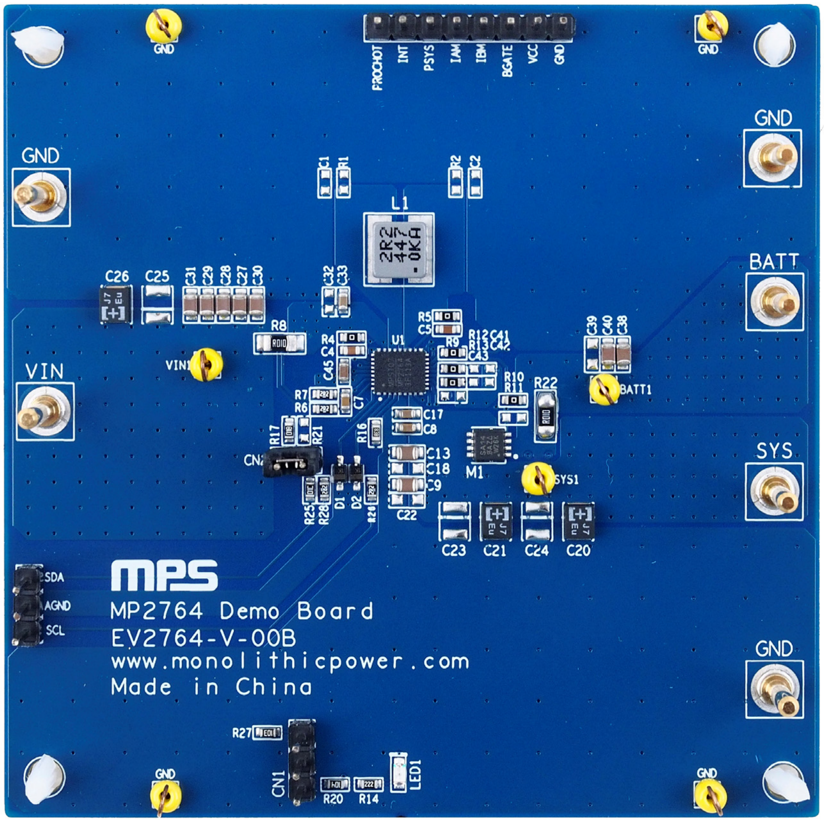
Specifications are at T_A = 25°C, unless otherwise noted.

Parameters	Conditions	Value
Input voltage (V_{IN}) range		4V to 22V
Input current limit (I_{IN_LIM})	V_{IN} = 4V to 22V	3A (I^2C-configurable)
Minimum input voltage regulation (V_{IN_LIM})		4.5V (I^2C-configurable)
Battery regulation voltage (V_{BATT_REG})	3 cells	12.6V (I^2C-configurable)
Fast charge current (I_{CC})	V_{IN} = 4V to 22V	3A (I^2C-configurable)
System voltage regulation ($V_{SYS\_MIN\_REG}$)	3 cells	9.3V (I^2C-configurable)
Output voltage range in source mode (V_{IN_SRC})		4V to 21V
Output current limit in source mode (I_{IN_SRC})		2.5A (I^2C-configurable)
Typical charge efficiency	V_{IN} = 20V, V_{BATT} = 11.1V, I_{CHG} = 5A	96.11%
charge efficiency	V_{IN} = 9V, V_{BATT} = 11.1V, I_{CHG} = 2A	97.28%
Typical source mode efficiency	V_{BATT} = 12V, V_{IN_OUT} = 5V, I_{IN_OUT} = 3A	94.25%
Peak source mode efficiency	V_{BATT} = 12V, V_{IN_OUT} = 12V, I_{IN_OUT} = 2A	96.92%
Switching frequency (f_{SW})		600kHz (I^2C-configurable)

Note:

1) Refer to the MP2764 datasheet for more details.

EVALUATION BOARD



LxWxH (8.9cmx8.9cmx0.8cm)

Board Number	MPS IC Number
EV2764-V-00B	MP2764GV-0001

QUICK START GUIDE

The EV2764-V-00B evaluation board is designed to demonstrate the capabilities of the MP2764 with a single inductor. It's a buck-boost narrow-voltage DC (NVDC) charger, which is used to charge a 2-cell to 4-cell battery pack. The board layout accommodates most commonly used resistors and capacitors. The board's default function is preset to charge mode, and the full charging voltage (V_{BATT_REG}) is preset to 12.6V. In charge mode, the MP2764 can work automatically in buck, buck-boost, or boost mode according to the input voltage (V_{IN}) and system voltage (V_{SYS}).

Follow the steps below to prepare the evaluation board:

1. Ensure that the computer has at least one USB port and a USB cable. The MP2764 evaluation software is embedded in Virtual Bench Pro 4.0. Virtual Bench Pro 4.0 can be downloaded from the MPS website, and should be properly installed step by step according to the installation wizard.
2. Connect the USB-to-I^{2}C communication kit (EVKT-USBI2C-02) (see Figure 1). The EVKT-USBI2C-02 is included with product evaluation kits, or it can be purchased separately. The EVKT-USBI2C-02 provides the communication interface for USB to I^{2}C or USB to PMBus. It is designed to work with MPS's I^{2}C and PMBus products, Virtual Bench Pro, and I^{2}C graphical user interface (GUI) tools.

Figure 1: USB-to-I^{2}C Communication Kit

3. Double-click "VirtualBenchPro_v4.exe" to enable and run the MPS evaluation software. The software supports Windows 7 and Windows 10 operating systems.

Original Test Set-Up for the MP2764

1. Connect the battery terminals to:
   a. Positive (+): BATT
   b. Negative (-): GND
2. If using a battery simulator, preset the battery voltage to be between 0V to 12.6V, then turn off the battery simulator.
3. Connect the battery simulator output to:
   a. Positive (+): BATT
   b. Negative (-): GND
4. Before starting the test, turn on the battery simulator.
5. For charge mode testing, connect the input terminals to:
   a. Positive (+): VIN
   b. Negative (-): GND
6. Connect the system load terminals to:
   a. Positive (+): SYS
   b. Negative (-): GND

Figure 2 shows the charge mode testing set-up.

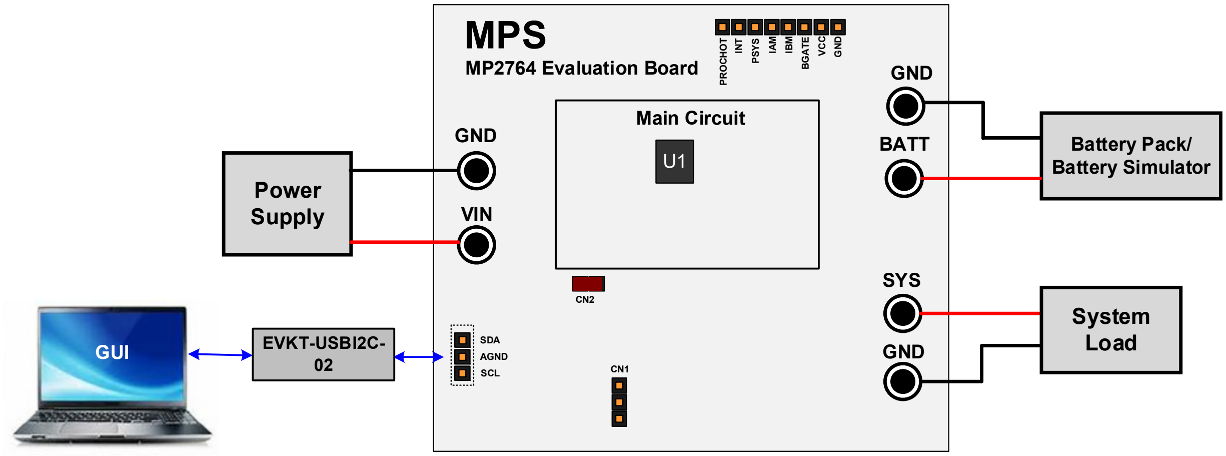


Figure 2: Test Set-Up for the EV2764-V-00B

7. For source mode testing, connect the load terminals to:
   a. Positive (+): VIN
   b. Negative (-): GND

Table 1 shows the jumper connection settings.

Table 1: Jumper Connections

Jack	Description	Factory Setting
CN1 (2)	For a V_{MIN} active protection (VAP) or USB On-The-Go (OTG) connection, connect CN4 to a pull-up voltage (enable) or GND (disable).	Short-to-bottom pin for OTG/VAP disabled
CN2	For a negative temperature coefficient (NTC) connection, short CN5 (NTC connected) or leave it open (NTC float).	Short

Note:

2) When REG13h, bit[5] = 0 (default), connecting CN1 to a pull-up voltage is used to enable V_{MIN} active protection (VAP). When REG13h, bit[5] = 1, connecting CN1 to a pull-up voltage is used to enable source mode.

8. Launch the MP2764 evaluation software.
   a. Double-click “VirtualBenchPro_v4.exe.” Figure 3 shows the software main window. Click “Help – User Manual” to access the Virtual Bench Pro 4.0 user guide.

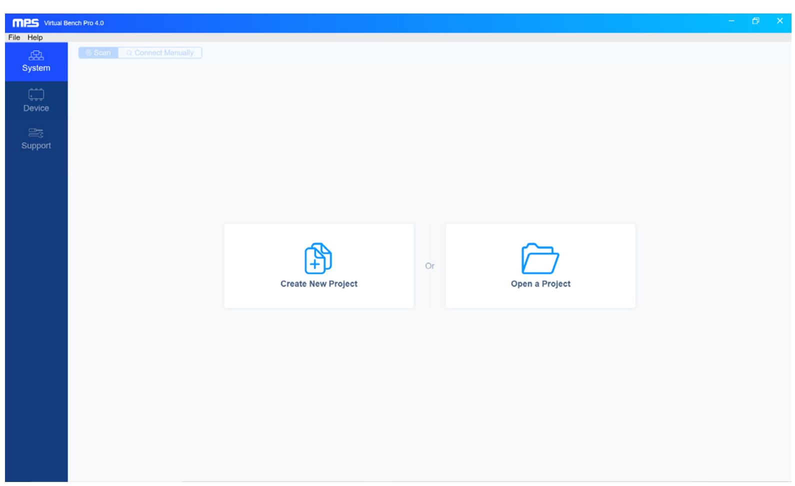


Figure 3: MPS Evaluation Software Main Window

b. Follow the Virtual Bench Pro 4.0 user guide to "Create New Project" and select the MP2764 by either clicking "Scan" or "Connect Manually".

c. If using the "Scan" method, click the "Scan" button. The software should automatically check the EVB connection.

- If the connection is successful, the device name (MP2764) should be listed; select the MP2764 to start the test.
- If the connection is unsuccessful, a warning window should appear that says, "No device found, please check the connection." If this occurs, check the connection between the EVB, EVKT-USBI2C-02, and the computer (see Figure 4).

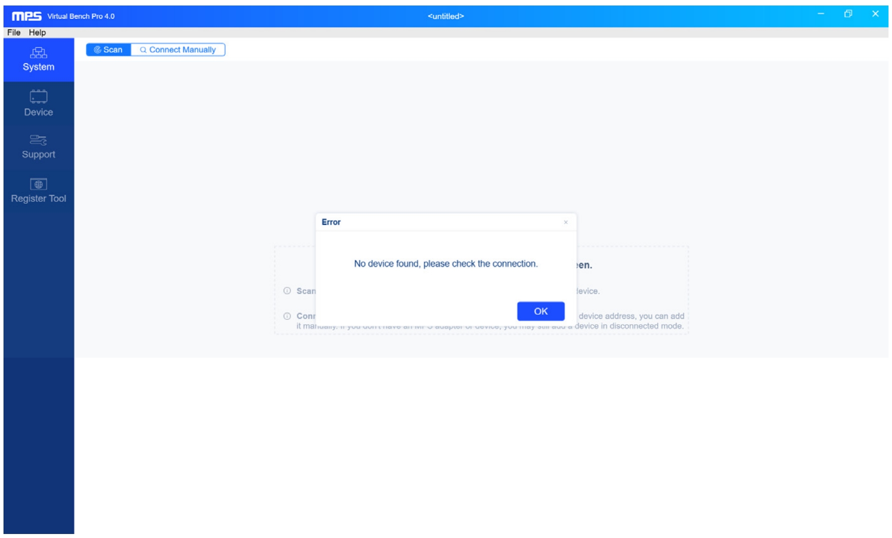


Figure 4: Warning Indicates Unsuccessful Connection

d. If using the "Connect Manually" method, the user can select the device name even when the evaluation board is disconnected. Select the device address to start testing and evaluating the MP2764 (see Figure 5).

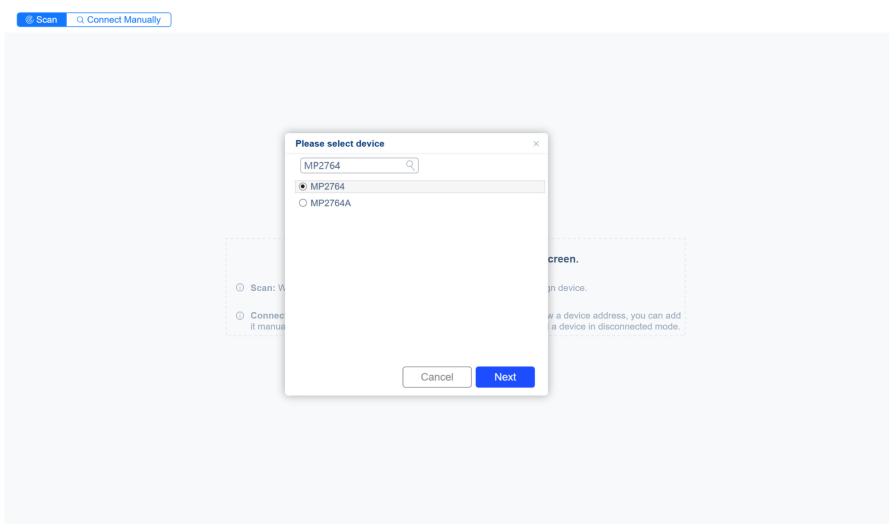


Figure 5: Select the MP2764

0x5C is the default address when the PROG pin is not configured to the device address function. If the PROG pin is configured to the device address function via the one-time programmable (OTP) memory, the address is configured to “0x10” to “0x16” via the external resistor connected between the PROG and GND pins while 0x5C is invalid (see Figure 6).

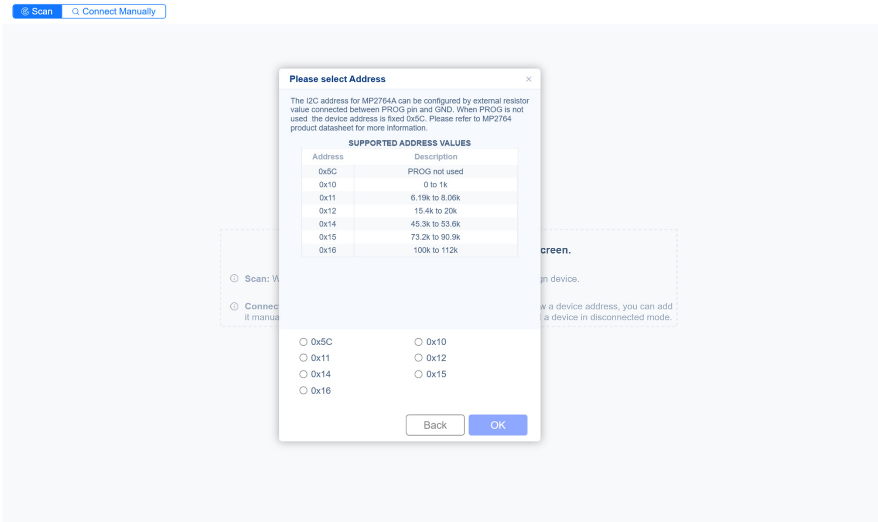


Figure 6: Select the MP2764 Device Address

e. After a new device is added, the light indicator behind the part number will show as green if the connection is correctly established (see Figure 7). Otherwise, the light indicator is orange.

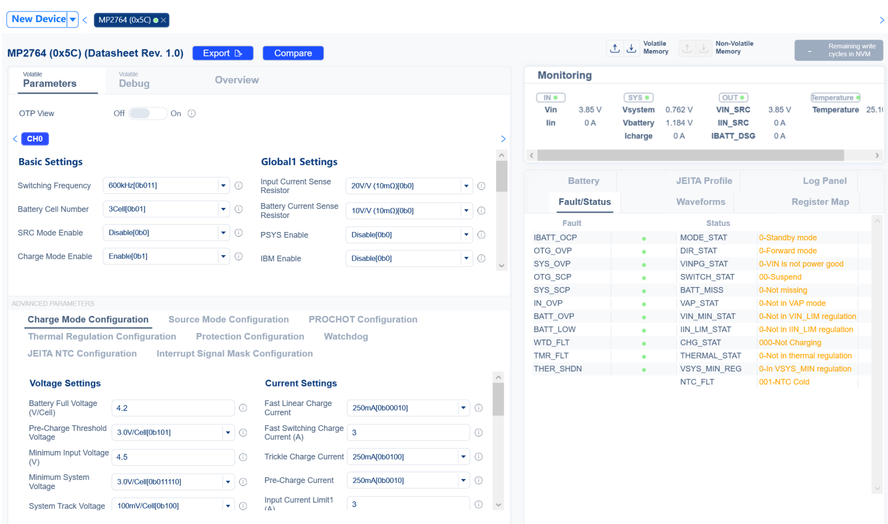


Figure 7: Status Shows Successful Connection

f. If the connection is successful, proceed to the next step. Otherwise, check the connections between the evaluation board, communication interface, and PC. Re-plug the USB into the computer and restart the GUI.

g. Click the up arrow before “Volatile Memory” to read the RAM. The default values are displayed.

h. Find the item to be changed, then select the desired value from the drop-down menu or fill the proper value in the blank field.

i. Click the down arrow before “Volatile Memory” to update the values. The changed information should be downloaded to the IC.

9. Turn on V_{IN} to charge the battery and power the system load with the default settings.

Modifying Parameters via the GUI

To use MPS's GUI, ensure that all the connections are successful, including the connections between the computer, USB-to-I^2C communication kit, and the evaluation board.

1. The MP2764 registers can be configured in the device configuration panel (see Figure 8). The analog-to-digital converter (ADC) results, chip fault and operating statuses, and register map can also be monitored in this panel.

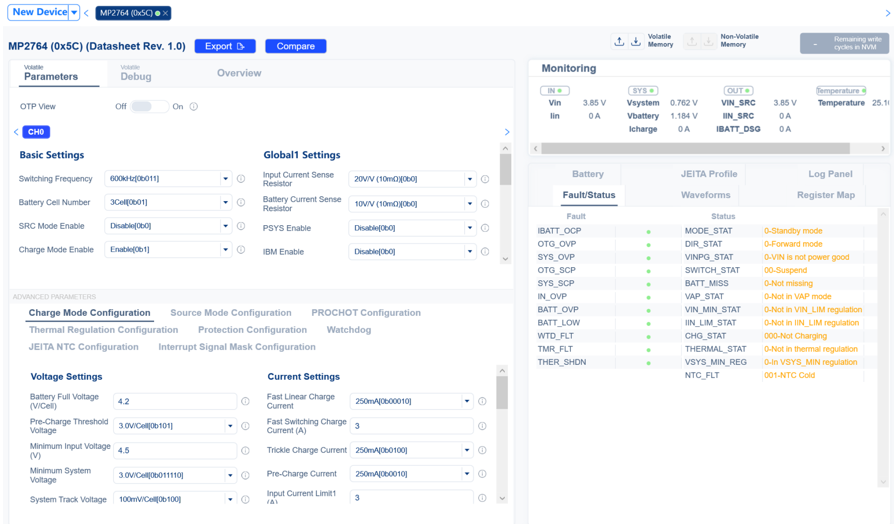


Figure 8: MP2764 Configuration Panel

2. Next, configure the parameters. All parameters can be directly inputted using the keyboard.

   a. Figure 9 shows the MP2764's basic parameter settings. These settings include the pulse-width modulation (PWM) frequency, battery cell count, enable bits for source mode and charge mode, enable bit for the DC/DC converter in charge mode, and safety timer.

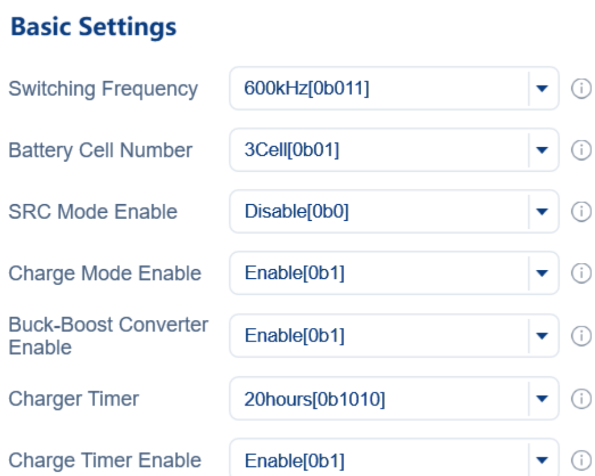


Figure 9: MP2764 Basic Settings

   b. Figure 10 on page 8 shows some global parameter (Global1) settings for the MP2764. These settings include the input current (I_{IN}) sense resistor and battery current (I_{BATT}) sense resistor, the PSYS and IBM monitoring enable bits, the PSYS gain, the weak source mode (when the MP2764 works in V_{IN_LIM} loop and I_{IN} is below 100mA, the DC/DC converter stops for 375ms) enable bit, and the ultrasonic mode (USM) enable bit to avoid audible noise with a switching frequency (f_{SW}) below 30kHz.

Figure 10: Global1 Settings

c. Figure 11 shows some other global parameter (Global2) settings for the MP2764. These settings include the ADC enable bit when V_{IN} is absent, I²C timeout (when an SMBus CLK low 25ms timeout occurs, the I²C state machine is reset) enable bit to avoid certain I²C communication failures, the clock enable bit when V_{IN} is absent, the I_{IN} sense gain and I_{BATT} sense gain, the low-power mode enable bit when V_{IN} is absent, and register reset.

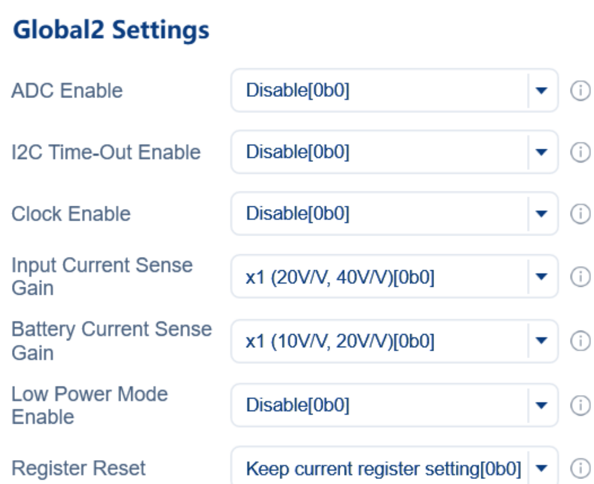


Figure 11: Global2 Settings

d. Figure 12 on page 9 shows the charge mode configuration voltage settings for the MP2764. These settings include the battery full voltage, pre-charge threshold voltage, minimum input voltage regulation (V_{IN_LIM}), system voltage regulation ($V_{SYS\_MIN\_REG}$), and system track voltage.

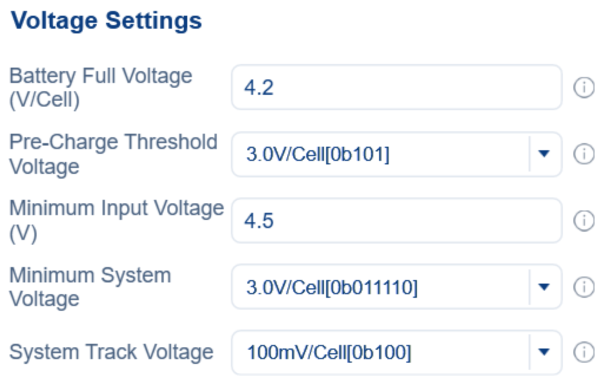


Figure 12: Voltage Settings

e. Figure 13 shows the charge mode configuration current settings for the MP2764. These settings include the fast linear charge current, fast switching charge current, trickle charge current, pre-charge current, and two I_{IN} limits (I_{IN_LIM1} and I_{IN_LIM2}).

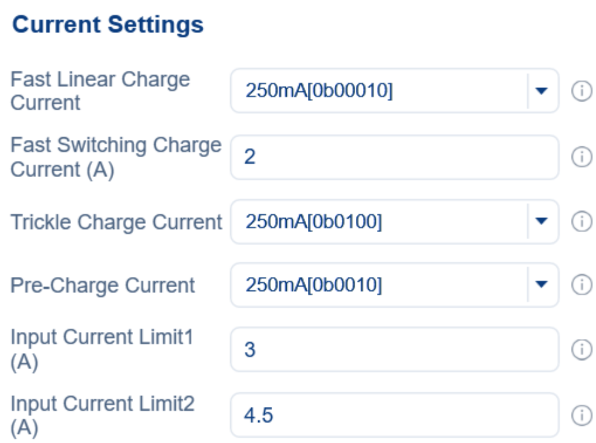


Figure 13: Current Settings

f. Figure 14 on page 10 shows the charge mode configuration protection settings for the MP2764. These settings include the system over-voltage protection (OVP) enable bit and its threshold, the battery OVP enable bit, the battery discharge over-current protection (OCP) enable bit and its threshold, as well as the deglitch time, V_{IN} OVP deglitch time, and system short-circuit protection (SCP) enable bit.

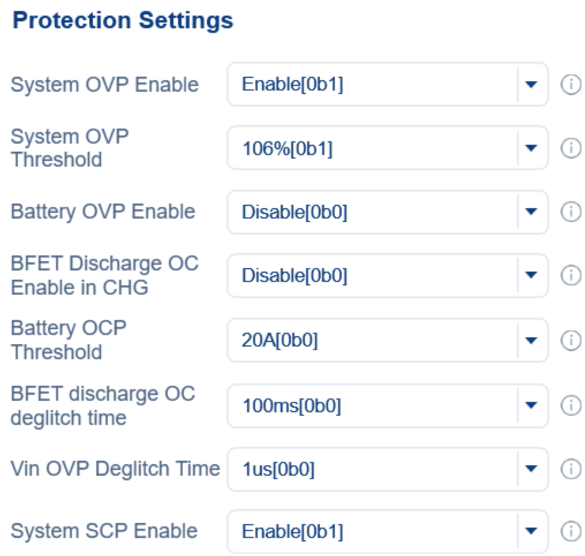


Figure 14: Protection Settings

g. Figure 15 shows the charge mode configuration charge termination settings for the MP2764. These settings include the termination enable bit, termination current, and battery recharge threshold.

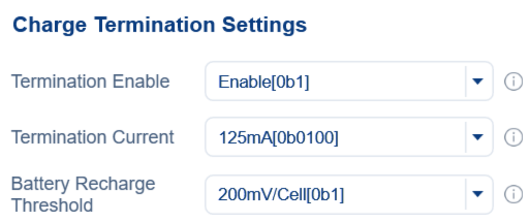


Figure 15: Charge Termination Settings

h. Figure 16 shows other charge mode configuration settings for the MP2764. These settings include the battery dummy load enable bit, the I_{IN_LIM} loop enable bit, the automatic input current limit (AICL) enable bit and its step, as well as the BGATE driver enable bit, battery impedance, and clamp voltage for battery full voltage compensation.

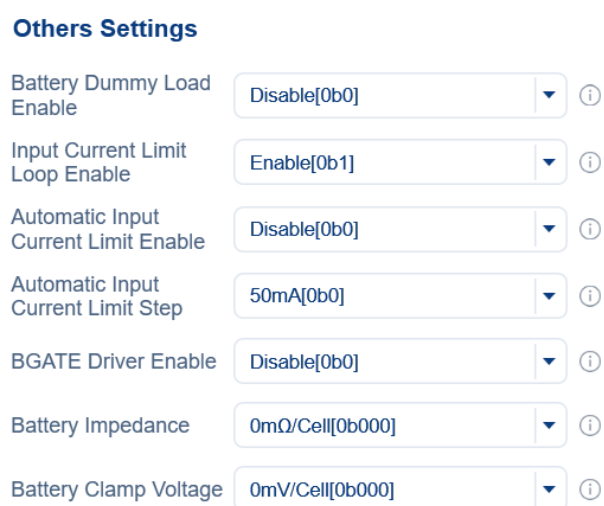


Figure 16: Other Settings

i. Figure 17 shows the basic source mode (SRC) configuration for the MP2764. These settings include the source output voltage (V_{IN_SRC}) and source output current limit (I_{IN_SRC}).

Figure 17: SRC Output Voltage and SRC Output Current Limit Settings

j. Figure 18 shows the source mode configuration protection settings for the MP2764. These settings include the SRC output OVP threshold, the battery under-voltage protection (UVP) enable bit in source mode, the battery low voltage protection enable bit (as well as its threshold and protection action), the SRC output SCP enable bit, and the battery OCP enable bit in source mode.

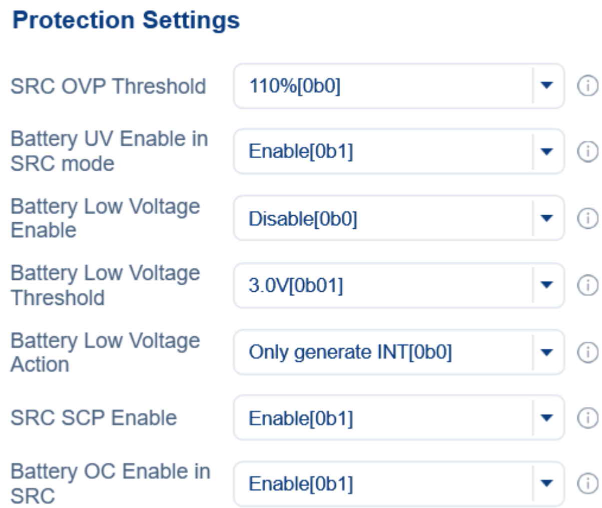


Figure 18: Protection Settings

k. Figure 19 shows other source mode configuration settings. These settings include the SRC under-voltage (UV) swap enable bit, the SRC fast on enable bit, the SRC I_{OUT} limit loop enable bit, the battery discharge current loop enable bit and its threshold, and the VIN dummy load enable bit.

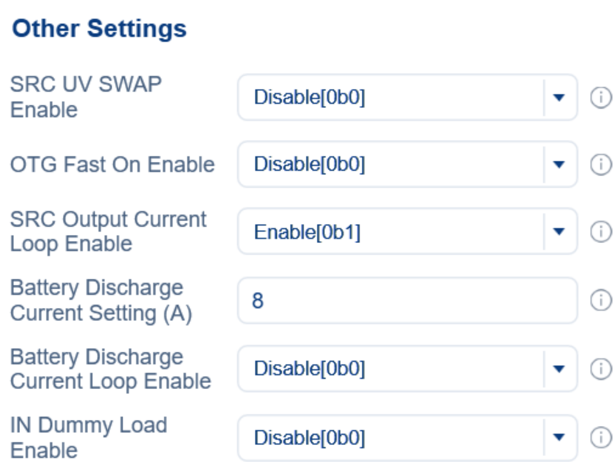


Figure 19: Other Settings

l. Figure 20 shows the PROCHOT output control settings. These settings include nine channel PROCHOT enable bits and the VSYS_UV_PROCHOT comparator enable bit when only the battery is present and there is no input voltage.

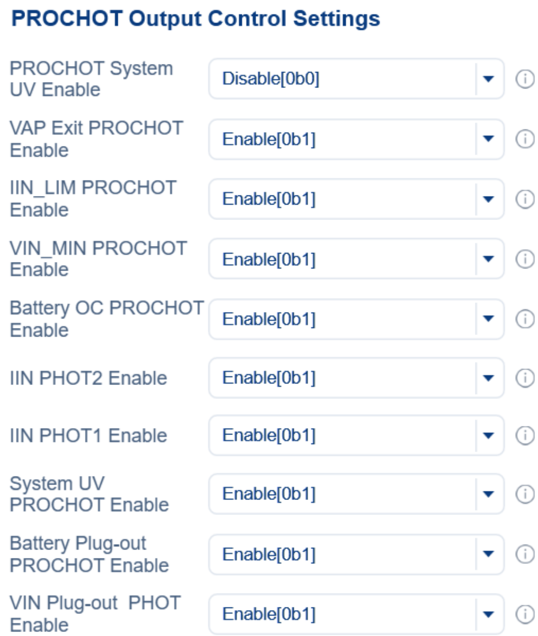


Figure 20: PROCHOT Output Control Settings

m. Figure 21 shows the PROCHOT functional settings. These settings include the system UV PROCHOT threshold and deglitch time, the battery over-current (OC) PROCHOT threshold and deglitch time, the battery plug PROCHOT deglitch time, the VIN plug PROCHOT deglitch time, the PROCHOT signal low state duration time, the IIN PROCHOT1 and PROCHOT2 deglitch times, and the IIN OC enable bit and threshold.

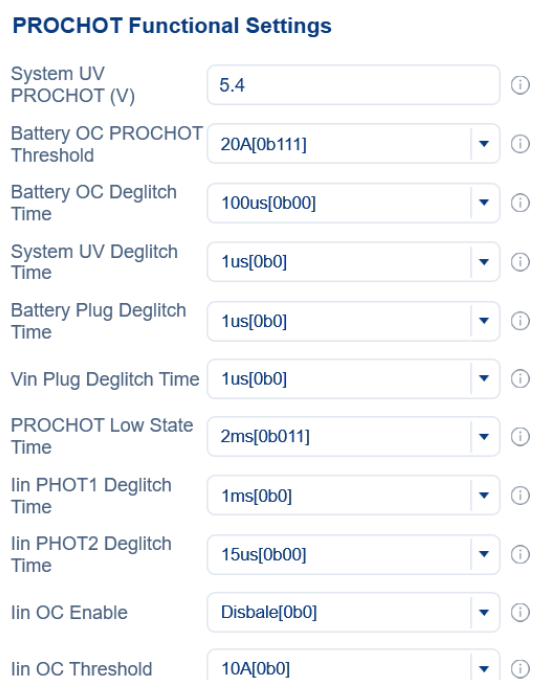


Figure 21: PROCHOT Functional Settings

n. Figure 22 shows the PROCHOT configuration two-level input current limit settings. These settings include the IIN_LIM1 and IIN_LIM2 total time, the IIN_LIM2 duration time, the IIN_LIM1 max time, the IIN_LIM2 max time, the two-level input current limit enable bit, and the IIN PROCHOT2 threshold.

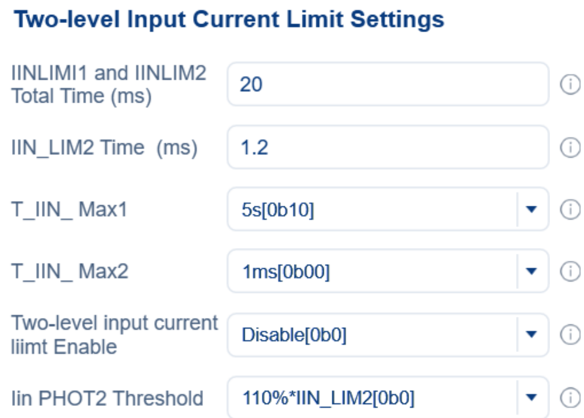


Figure 22: Two-Level Input Current Limit Settings

o. Figure 23 shows the PROCHOT configuration for the VAP settings. These settings include the VIN loop DAC output in VAP mode, system voltage regulation reference in VAP mode, and OTG/VAP selection.

Figure 23: VAP Settings

p. Figure 24 shows the thermal regulation configurations, including the thermal regulation loop enable setting and thermal regulation threshold setting.

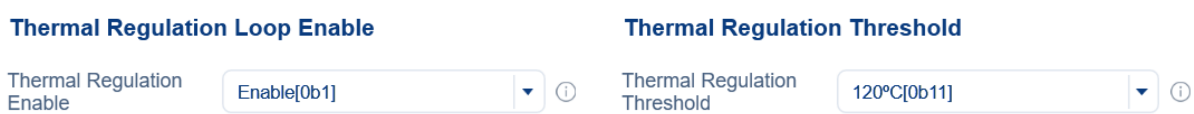


Figure 24: Thermal Regulation Loop Enable and Thermal Regulation Threshold Settings

q. Figure 25 shows other protection settings. These settings include the battery voltage lock and battery cell number lock.

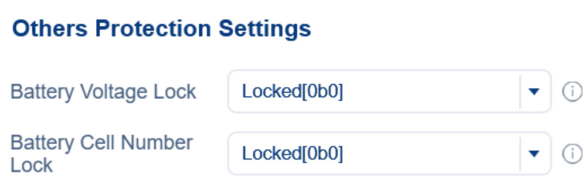


Figure 25: Other Protection Settings

r. Figure 26 on page 14 shows the watchdog timing settings. These settings include the watchdog enable bit in battery-only mode, the watchdog reset timer, and the watchdog timer.

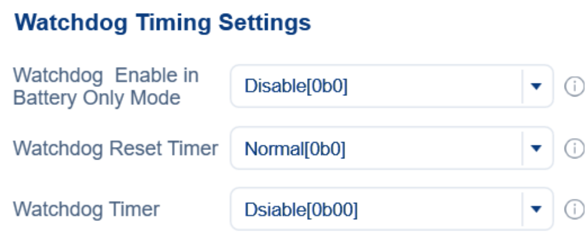


Figure 26: Watchdog Timing Settings

s. Figure 27 shows the JEITA NTC configuration NTC temperature threshold settings. These settings include the cold, cool, warm, and hot thresholds.

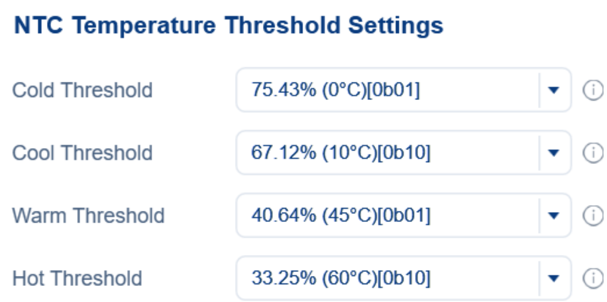


Figure 27: NTC Temperature Threshold Settings

t. Figure 28 shows the JEITA NTC configuration NTC action settings. These settings include the JEITA current set, JEITA voltage set, cool action, warm action, and NTC action.

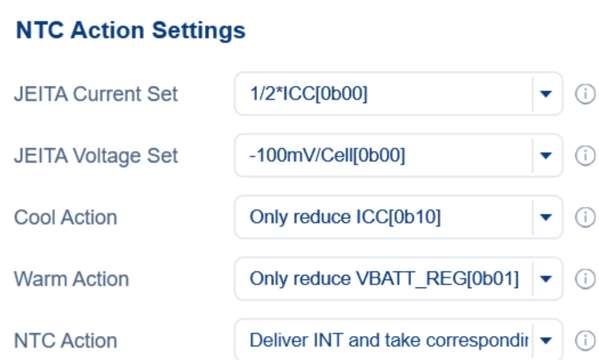


Figure 28: NTC Action Settings

u. Figure 29 shows the JEITA NTC configuration NTC enable bit settings.

Figure 29: NTC Enable

v. Figure 30 on page 15 shows the Interrupt Signal Mask Configuration Masks Interrupt Configuration1. These settings include the I_{BATT} OCP mask, I_{IN_LIM} regulation loop mask, V_{IN_LIM} regulation loop mask, thermal shutdown or thermal regulation loop mask, VAP mask, charge status mask, mode status mask, and NTC status mask.

Figure 30: Masks Interrupt Configuration1

w. Figure 31 shows the Interrupt Signal Mask Configuration Masks Interrupt Configuration2. These settings include the timer status mask, battery missing status mask, watchdog timer status mask, V_{BATT} OVP mask, power good (PG) status mask, V_{IN} OVP status mask, SRC OVP and SCP mask, and SYS OVP and SCP mask.

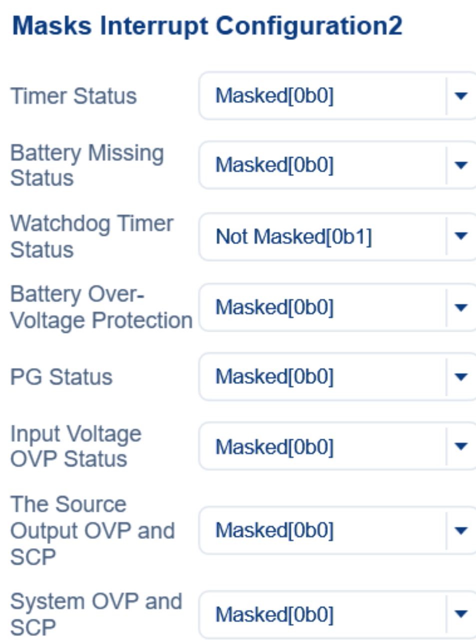


Figure 31: Masks Interrupt Configuration2

3. Next, monitor the relevant statuses.
   a. Figure 32 on page 16 shows ADC monitoring for the MP2764. It has nine channels including V_{IN}, I_{IN}, V_{SYS}, V_{BATT}, I_{CHG}, V_{IN_SRC}, I_{IN_SRC}, I_{BAT_DSG}, and T_J.

Monitoring

IN		SYS		OUT		Temperature	
Vin	4.05 V	Vsystem	13.013 V	VIN_SRC	4.05 V	Temperature	13.536 °C
Iin	0 A	Vbattery	13.05 V	IIN_SRC	0 A		
		Icharge	0 A	IBATT_DSG	0 A		

Figure 32: ADC Monitoring

b. Figure 33 shows the fault/operating statuses for the MP2764.

Fault		Status	
IBATT_OCP	●	MODE_STAT	0-Standby mode
OTG_OVP	●	DIR_STAT	0-Forward mode
SYS_OVP	●	VINPG_STAT	0-VIN is not power good
OTG_SCP	●	SWITCH_STAT	00-Suspend
SYS_SCP	●	BATT_MISS	0-Not missing
IN_OVP	●	VAP_STAT	0-Not in VAP mode
BATT_OVP	●	VIN_MIN_STAT	0-Not in VIN_LIM regulation
BATT_LOW	●	IIN_LIM_STAT	0-Not in IIN_LIM regulation
WTD_FLT	●	CHG_STAT	000-Not Charging
TMR_FLT	●	THERMAL_STAT	0-Not in thermal regulation
THER_SHDN	●	VSYS_MIN_REG	0-In VSYS_MIN regulation
		NTC_FLT	001-NTC Cold

Figure 33: Fault/Status

c. The GUI draws a curve in real time for the ADC T_J in the "Waveforms" tab of the GUI (see Figure 34).

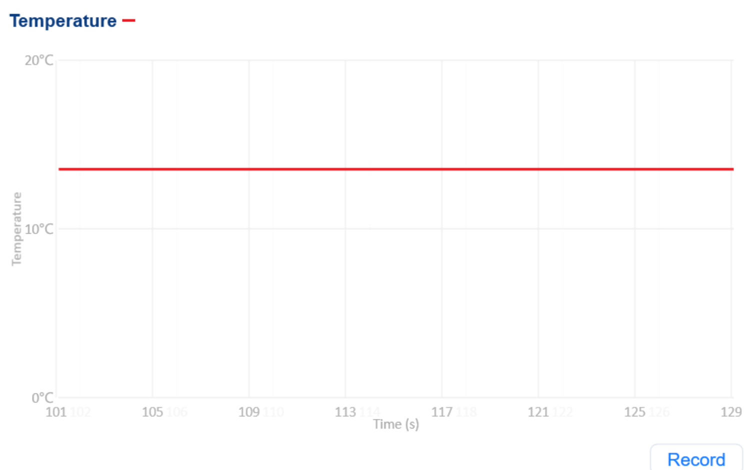


Figure 34: Waveforms

Click "Record" to start recording the ADC results. Click "Save" to save the data in a .txt file including the nine ADC channels: V_{IN}, I_{IN}, V_{SYS}, V_{BATT}, I_{CHG}, V_{IN_SRC}, I_{IN_SRC}, I_{BAT_DSG}, and T_J.

Figure 35 on page 17 shows the register map, which matches the registers on the configuration pages. Click any register to see the related parameter(s) and its locations listed below the map.

Register Name	Page	Address	Type	Right	Value
REG07h	**CH0**	**07**	**Word**	**RW**	**424**
REG08h	CH0	08	Word	RW	5A
REG09h	CH0	09	Word	RW	11E
REG0Ah	CH0	0A	Word	RW	9060
REG0Bh	CH0	0B	Word	RW	320
REG0Ch	CH0	0C	Word	RW	8028
REG0Dh	CH0	0D	Word	RW	07
REG0Eh	CH0	0E	Word	RW	3475
REG0Fh	CH0	0F	Word	RW	60
REG10h	CH0	10	Word	RW	399
REG11h	CH0	11	Word	RW	2F
REG12h	CH0	12	Word	RW	1004
REG13h	CH0	13	Word	RW	2A3
REG14h	CH0	14	Word	RW	220
REG15h	CH0	15	Word	RW	348
REG16h	CH0	16	Word	RW	10
REG17h	CH0	17	Word	RW	31
REG18h	CH0	18	Word	RW	6406

Related Parameters

Termination Current D[3:0] Parameters/CH0/Advanced Configuration/Charge Mode Configuration/Ch
Pre-Charge Current D[7:4] Parameters/CH0/Advanced Configuration/Charge Mode Configuration/Cu
Trickle Charge Current D[11:8] Parameters/CH0/Advanced Configuration/Charge Mode Configuratior

Figure 35: Register Map

Figure 36 shows the typical battery charging profile for an NVDC charger. It shows the system voltage, battery voltage, and charge current through the trickle charge, pre-charge, linear CC charge, switching CC charge, constant voltage charge, and charge termination stages.

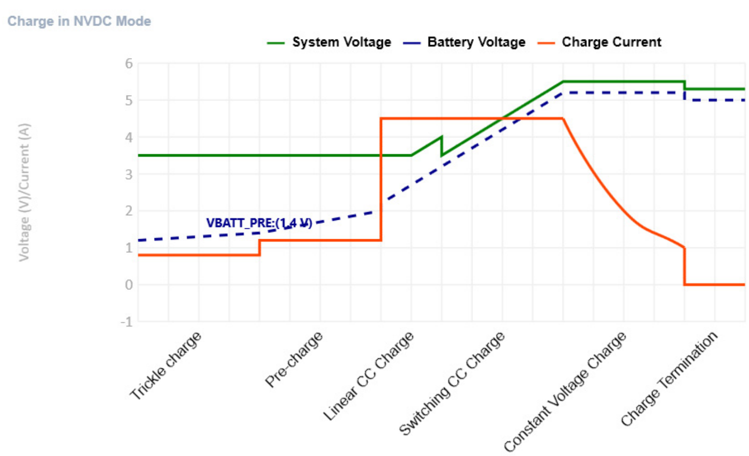


Figure 36: Battery Charging Profile

d. Click "NTC Monitor" to view the NTC JEITA general operation profile (see Figure 37 on page 18).

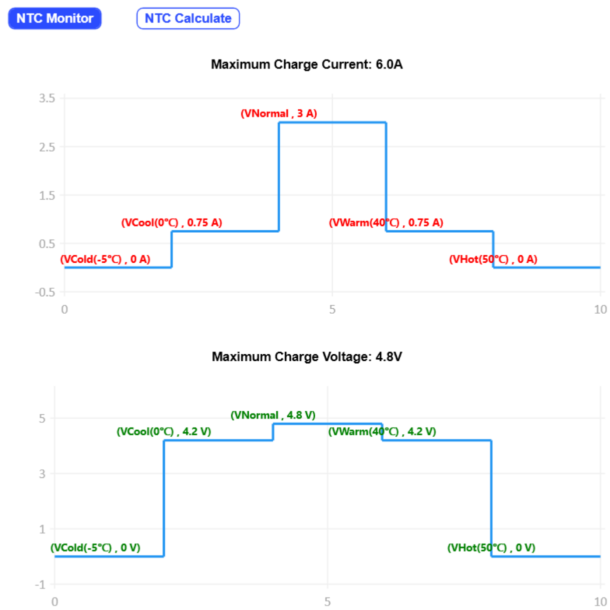


Figure 37: JEITA Profile – NTC JEITA Operation

Click “NTC Calculate” to view the NTC JEITA temperature threshold calculation based on the NTC JEITA voltage threshold setting in the configuration page (filled in automatically), the NTC resistance characteristics (which must be filled in manually), and the pull-up and parallel resistors on board (which must be filled in manually) (see Figure 38).

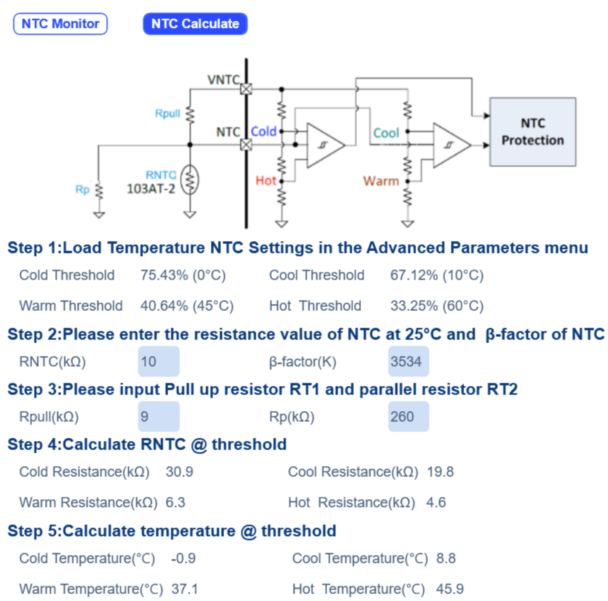


Figure 38: JEITA Profile – NTC JEITA Calculation

e. Figure 39 on page 19 shows the Log Panel.

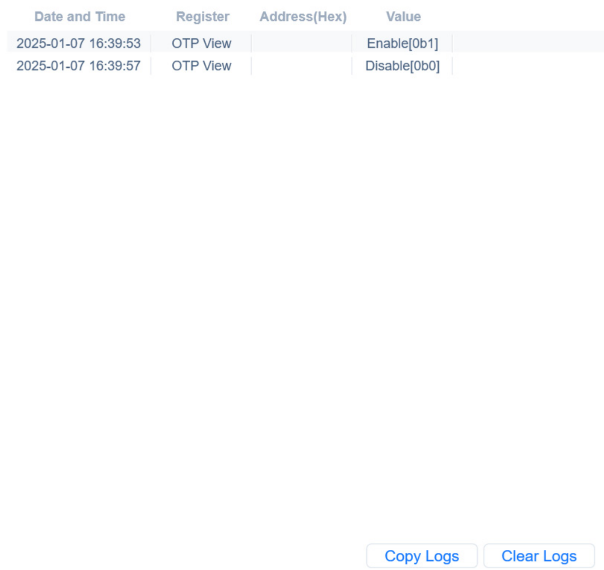


Figure 39: Log Panel

4. The Overview section shows the MP2764's description, features, and functional block diagram.
5. OTP configuration.
   a. Set the "OTP View" button to "On." The register bits with OTP will show as white input boxes and can be configured; the register bits without OTP will show as grey input boxes and cannot be configured (see Figure 40).

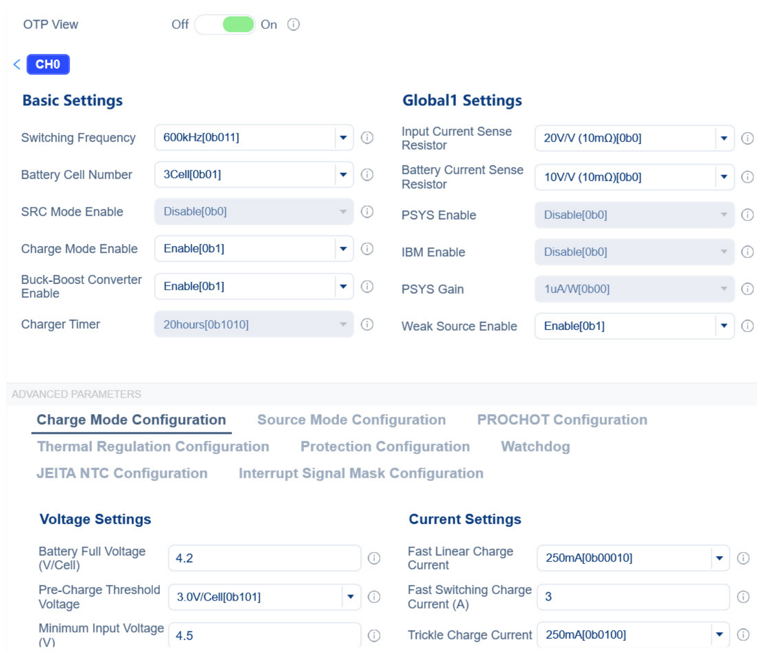


Figure 40: OTP View

   b. Generate a customized OTP configuration file. After configurating the register bits via the OTP, click "Export" to generate a customized OTP configuration file (see Figure 41 on page 20).

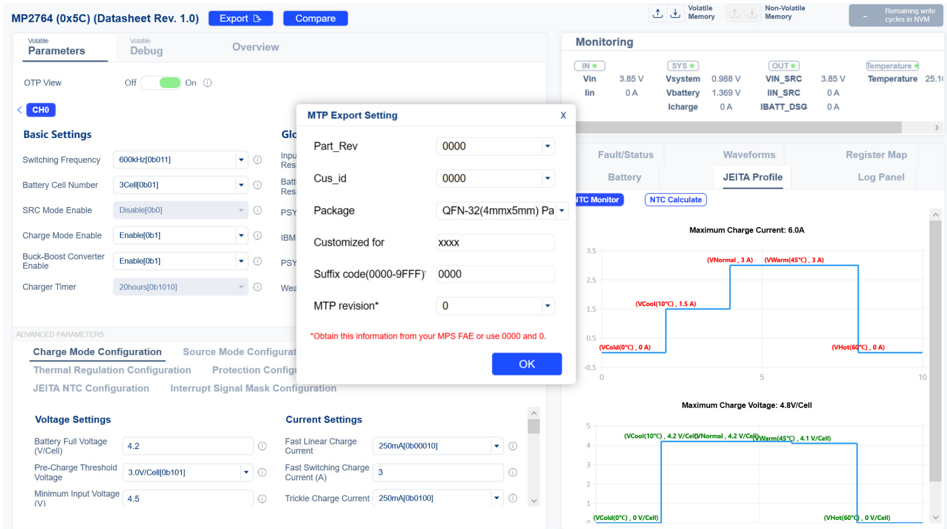


Figure 41: OTP Configuration File Generation

EVALUATION BOARD SCHEMATIC

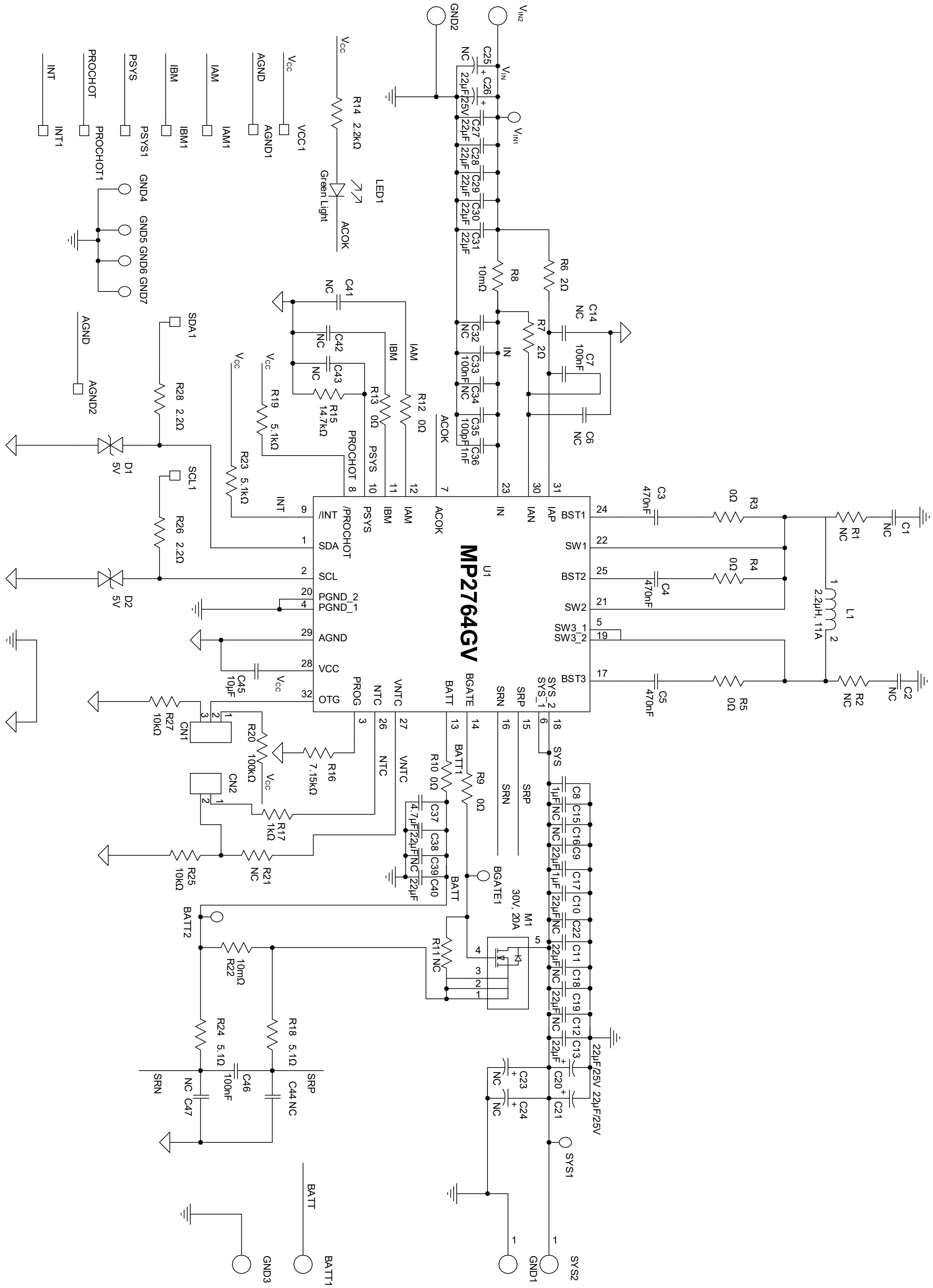


Figure 42: Evaluation Board Schematic

EV2764-V-00B BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
10	VCC1, SDA1, SCL1, PSYS1, PROCHOT1, INT1, IBM1, IAM1, AGND1, AGND2	2.54mm	1-row, 40-pin, 180° connector	2.54mm	Any	
6	GND1, BATT1, VIN2, SYS2, GND2, GND3	2cm	2.0 male connector	2cm	Any	
8	VIN1, SYS1, BGATE1, BATT2, GND4, GND5, GND6, GND7	2.54mm	Test point connector	2.54mm	Any	
1	CN1	2.54mm	1-row, 40-pin, 180° connector	2.54mm	Any	
1	CN2	2.54mm	1-row, 40-pin, 180° connector	2.54mm	Any	
1	CN2	2.54mm	Connector block jumper	2.54mm	Any	
3	C3, C4, C5	470nF	Capacitor, 50V, X7R	0603	TDK	C1608X7R1H474K
1	C7	100nF	Capacitor, 50V, X7R	0603	Murata	GRM188R71H104KA93D
2	C8, C17	1µF	Capacitor, 25V, X7R	0603	Murata	GRM188R71E105KA12D
12	C9, C10, C11, C13, C19, C27, C28, C29, C30, C31, C38, C40	22µF	Capacitor, 25V, X5R	0805	Murata	GRM21BR61E226ME44L
3	C20, C21, C26	22µF	Tantalum capacitor, 25V, 100mΩ	3528	Panasonic	25TQC22MYFB
1	C33	100nF	Capacitor, 25V, X7R	0603	Murata	GCJ188R71E104KA12D
1	C35	100pF	Capacitor, 50V, C0G	0603	Murata	GRM1885C1H101JA01D
1	C36	1nF	Capacitor, 50V, X7R	0603	Murata	GCM188R71H102KA37D
1	C37	4.7µF	Capacitor, 50V, X5R	0805	Murata	GRM21BR61H475KE51L
1	C45	10µF	Capacitor, 10V, X7R	0603	Murata	GRM188Z71A106KA73D
1	C46	100nF	Capacitor, 25V, X7R	0603	Murata	GCJ188R71E104KA12D
2	D1, D2		ESD diode, 5V	SOD-323	NXP	PESD5V0V1BA
1	LED1	Green	LED	0805	Bright	BL-HGE35A-AV-TRB
1	L1	2.2µH	L, 2.2µH, 9.8mΩ, 11A	SMD	Cyntec	HBED053T-2R2MS-99

EV2764-V-00B BILL OF MATERIALS *(continued)*

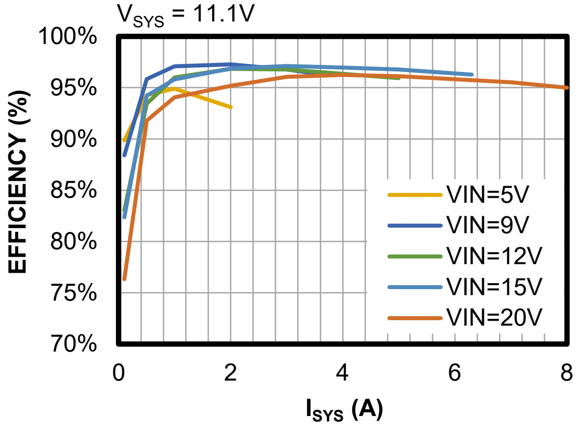
Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	M1	30V	N-channel MOSFET, 30V, 8.5mΩ, 9.4nC, 20A	PowerPAK -1212-8	Vishay	SISA14DN-T1-GE3
5	R3, R4, R5, R12, R13	0Ω	Film resistor, 1%	0603	Yageo	RC0603FR-070RL
4	R6, R7, R26, R28	2.2Ω	Film resistor, 1%	0603	Yageo	RC0603FR-7W2R2L
2	R8, R22	10mΩ	Film resistor, 1%	1206	Cyntec	SCRR1206S1-R010F-99
2	R9, R10	0Ω	Film resistor, 5%	0603	Yageo	RC0603JR-070RL
1	R14	2.2kΩ	Film resistor, 5%	0603	LIZ	CR0603JA0222G
1	R15	14.7kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0714K7L
1	R16	7.15kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-077K15L
1	R17	1kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-071KL
2	R18, R24	5.1Ω	Film resistor, 1%	0603	Yageo	RC0603FR-075R1L
2	R19, R23	5.1kΩ	Film resistor, 5%	0603	Yageo	RC0603JR-075K1L
1	R20	100kΩ	Film resistor, 5%	0603	Yageo	RC0603JR-07100KL
1	R25	10kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710KL
1	R27	10kΩ	Film resistor, 5%	0603	Yageo	RC0603JR-0710K
1	U1	MP2764	Buck-boost NVDC charger for 2S to 4S battery packs	QFN-32 (4mmx 5mm)	MPS	MP2764GV-0001

EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board, C_{IN} = 22µF x 1 POSCAP + 22µF x 5 MLCC + 1µF x 1 MLCC, C_{SYS} = 22µF x 2 POSCAP + 22µF x 5 MLCC + 1µF x 2 MLCC, C_{BATT} = 4.7µF x 1 MLCC + 22µF x 2 MLCC, L = 2.2µH/9.8mΩ, R_{SNS_IN} = R_{SNS_BAT} = 10mΩ, f_{SW} = 600kHz, 3-cell battery, T_A = 25°C, unless otherwise noted.

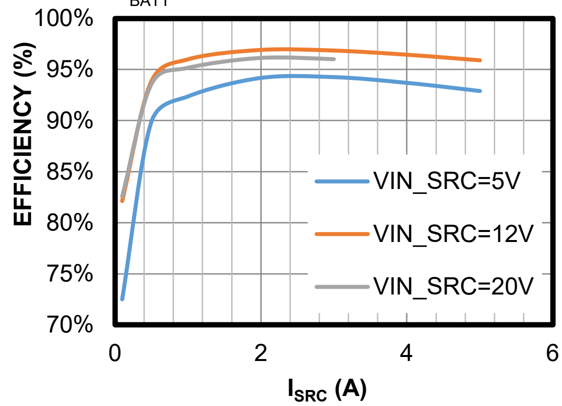
System Efficiency with 3S Battery

V_{SYS} = 11.1V



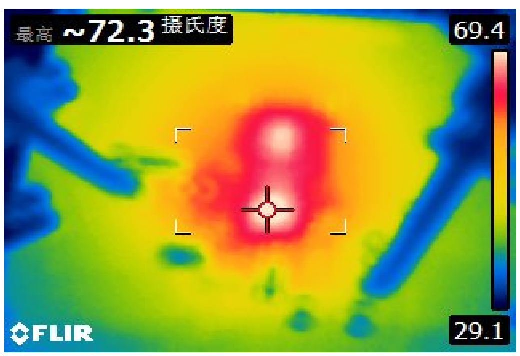
SRC Efficiency with 3S Battery

V_{BATT} = 12V



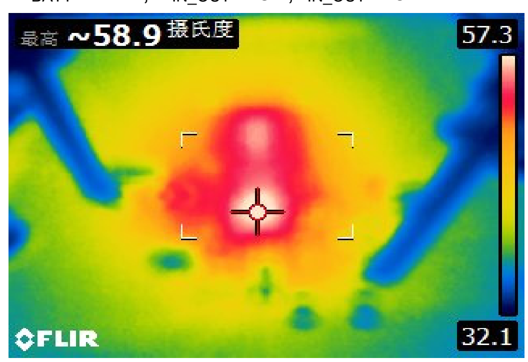
Thermal

V_{IN} = 20V, V_{SYS} = 11.1V, I_{SYS} = 6A



Thermal

V_{BATT} = 12V, V_{IN_OUT} = 5V, I_{IN_OUT} = 5A

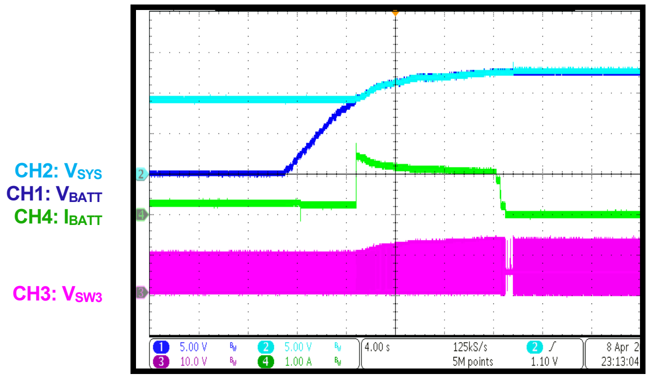


EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board, C_{IN} = 22µF x 1 POSCAP + 22µF x 5 MLCC + 1µF x 1 MLCC, C_{SYS} = 22µF x 2 POSCAP + 22µF x 5 MLCC + 1µF x 2 MLCC, C_{BATT} = 4.7µF x 1 MLCC + 22µF x 2 MLCC, L = 2.2µH/9.8mΩ, R_{SNS_IN} = R_{SNS_BAT} = 10mΩ, f_{SW} = 600kHz, 3-cell battery, T_A = 25°C, unless otherwise noted.

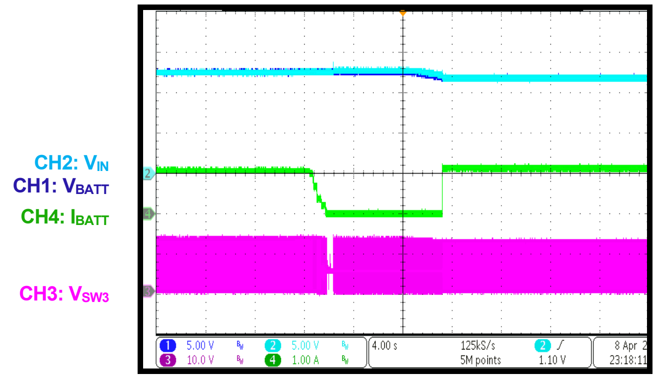
Battery Charge Curve

V_{IN} = 5V, V_{BATT} = 0V to 12.6V, I_{TERM} = 0.125A, I_{IN_LIM} = 3A, I_{CC} = 3A, auto-termination enabled



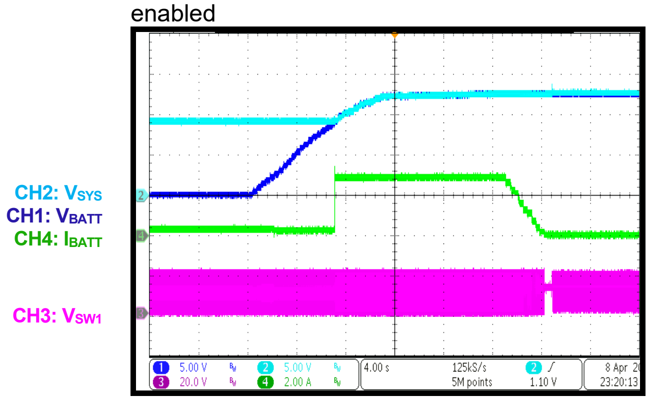
Auto-Recharge

V_{IN} = 5V, V_{BATT} = 12.6V to 12V, auto-termination enabled



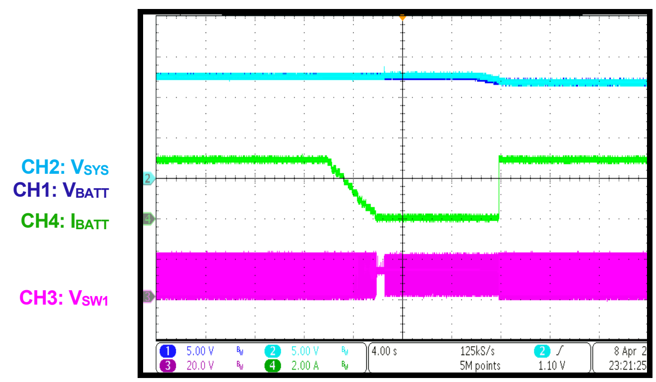
Battery Charge Curve

V_{IN} = 20V, V_{BATT} = 0V to 12.6V, I_{TERM} = 0.125A, I_{IN_LIM} = 3.25A, I_{CC} = 3A, auto-termination enabled



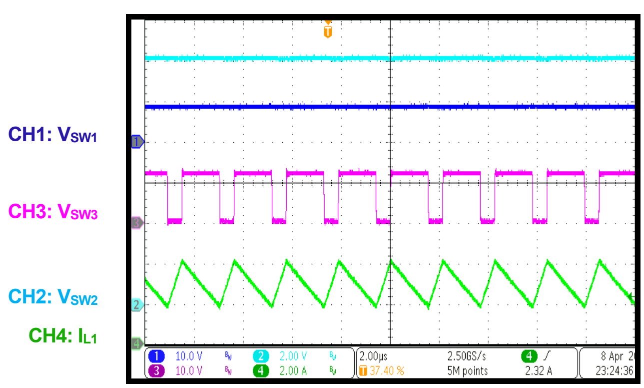
Auto-Recharge

V_{IN} = 20V, V_{BATT} = 12.6V to 12V



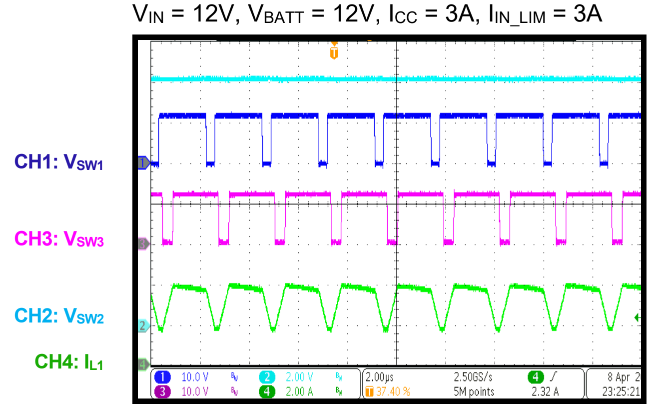
Boost Charge Steady Operation

V_{IN} = 9V, V_{BATT} = 12V, I_{CC} = 3A, I_{IN_LIM} = 3A



Buck-Boost Charge Steady Operation

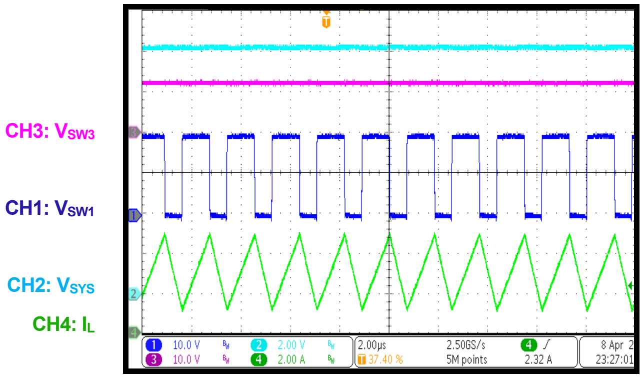
V_{IN} = 12V, V_{BATT} = 12V, I_{CC} = 3A, I_{IN_LIM} = 3A



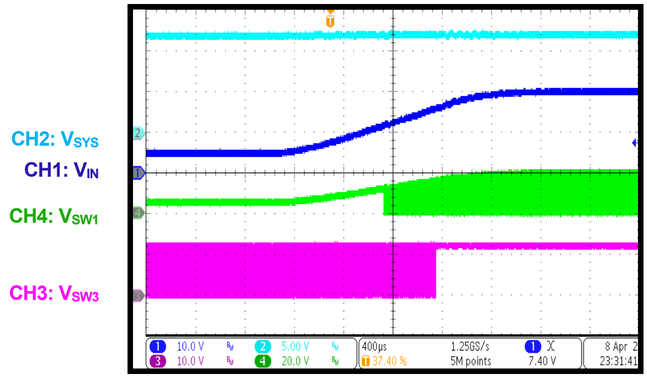
EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board, C_{IN} = 22µF x 1 POSCAP + 22µF x 5 MLCC + 1µF x 1 MLCC, C_{SYS} = 22µF x 2 POSCAP + 22µF x 5 MLCC + 1µF x 2 MLCC, C_{BATT} = 4.7µF x 1 MLCC + 22µF x 2 MLCC, L = 2.2µH/9.8mΩ, R_{SNS_IN} = R_{SNS_BAT} = 10mΩ, f_{SW} = 600kHz, 3-cell battery, T_A = 25°C, unless otherwise noted.

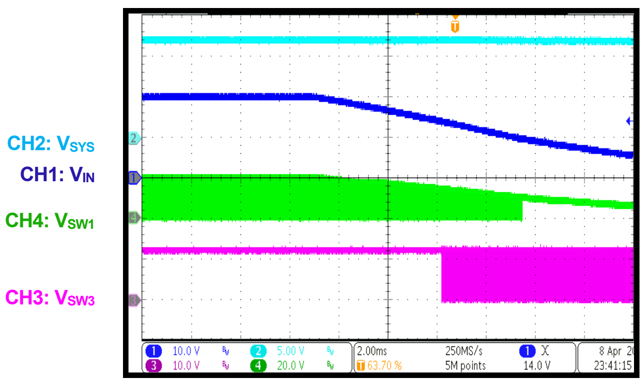
Buck Charge Steady Operation
Paralleled single inductor, V_{IN} = 20V, V_{BATT} = 12V, I_{CC} = 3A, I_{IN_LIM} = 3.25A



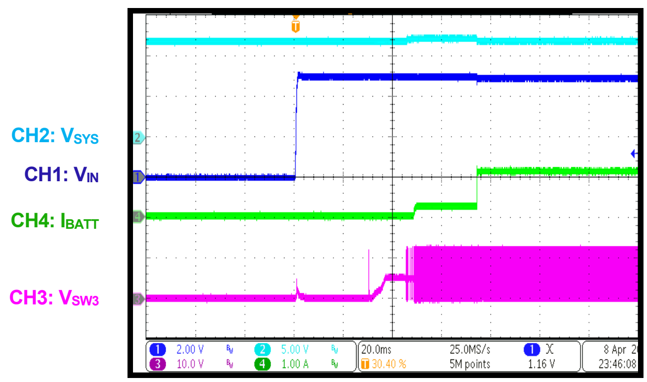
Boost to Buck-Boost to Buck Transition
V_{IN} = 5V to 20V, V_{BATT} = 12V, I_{CC} = 3A



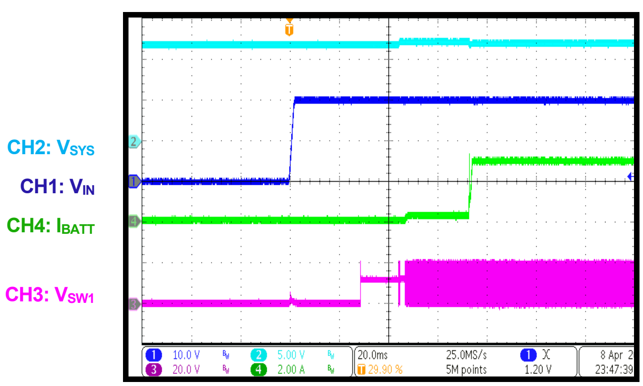
Buck to Buck-Boost to Boost Transition
V_{IN} = 20V to 5V, V_{BATT} = 12V, I_{CC} = 3A



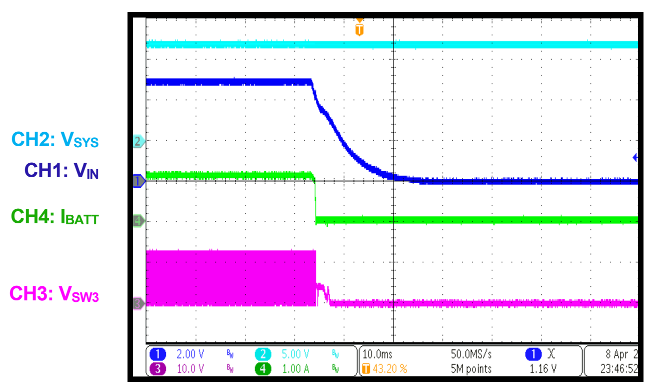
Start-Up through VIN
V_{IN} = 5V, V_{BATT} = 12V, I_{CC} = 3A



Start-Up through VIN
V_{IN} = 20V, V_{BATT} = 12V, I_{CC} = 3A



Shutdown through VIN
V_{IN} = 5V, V_{BATT} = 12V, I_{CC} = 3A

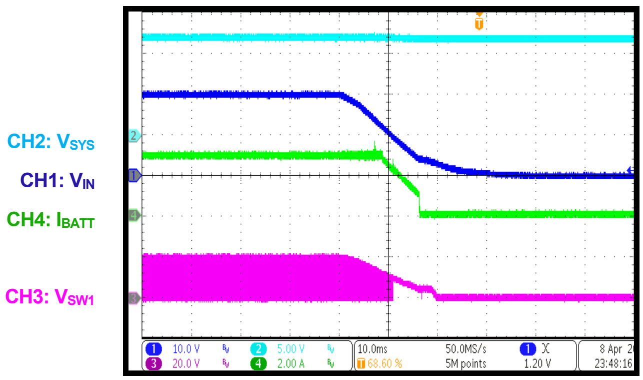


EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board, C_{IN} = 22µF x 1 POSCAP + 22µF x 5 MLCC + 1µF x 1 MLCC, C_{SYS} = 22µF x 2 POSCAP + 22µF x 5 MLCC + 1µF x 2 MLCC, C_{BATT} = 4.7µF x 1 MLCC + 22µF x 2 MLCC, L = 2.2µH/9.8mΩ, R_{SNS_IN} = R_{SNS_BAT} = 10mΩ, f_{SW} = 600kHz, 3-cell battery, T_A = 25°C, unless otherwise noted.

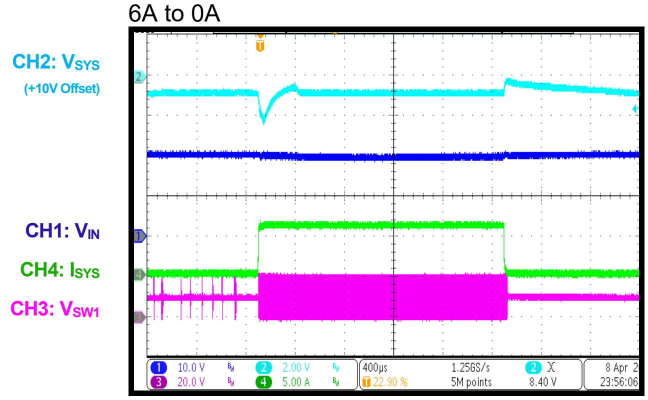
Shutdown through VIN

V_{IN} = 20V, V_{BATT} = 12V, I_{CC} = 3A



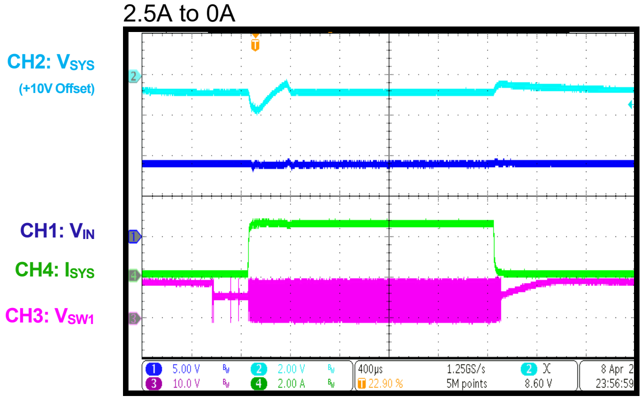
System Regulation in Buck Mode

V_{IN} = 20V, V_{SYS} = 9.3V, no BATT, I_{SYS} = 0A to 6A to 0A



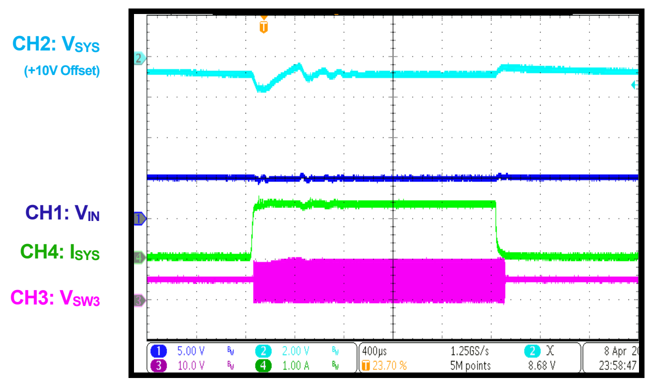
System Regulation in Buck-Boost Mode

V_{IN} = 9V, V_{SYS} = 9.3V, no BATT, I_{SYS} = 0A to 2.5A to 0A



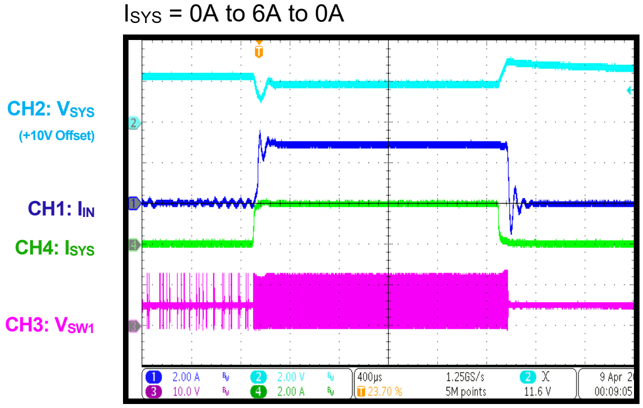
System Regulation in Boost Mode

V_{IN} = 5V, V_{SYS} = 9.3V, no BATT, I_{SYS} = 0A to 1.3A to 0A



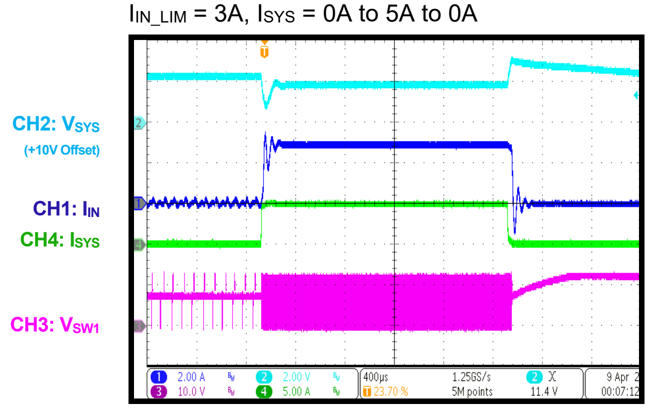
I_{IN} Regulation in Buck Mode

V_{IN} = 20V, V_{BATT} = 12V, charging disabled, I_{SYS} = 0A to 6A to 0A



I_{IN} Regulation in Buck-Boost Mode

V_{IN} = 12V, V_{BATT} = 12V, charging disabled, I_{IN_LIM} = 3A, I_{SYS} = 0A to 5A to 0A

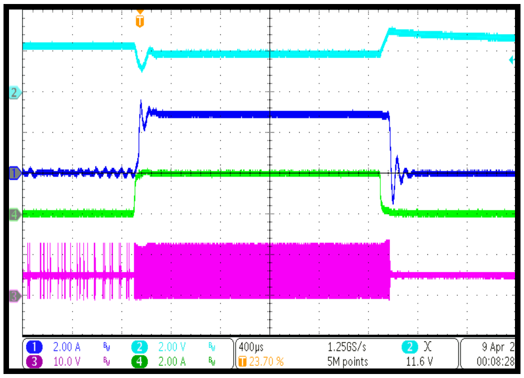


EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board, C_{IN} = 22µF x 1 POSCAP + 22µF x 5 MLCC + 1µF x 1 MLCC, C_{SYS} = 22µF x 2 POSCAP + 22µF x 5 MLCC + 1µF x 2 MLCC, C_{BATT} = 4.7µF x 1 MLCC + 22µF x 2 MLCC, L = 2.2µH/9.8mΩ, R_{SNS_IN} = R_{SNS_BAT} = 10mΩ, f_{SW} = 600kHz, 3-cell battery, T_A = 25°C, unless noted otherwise.

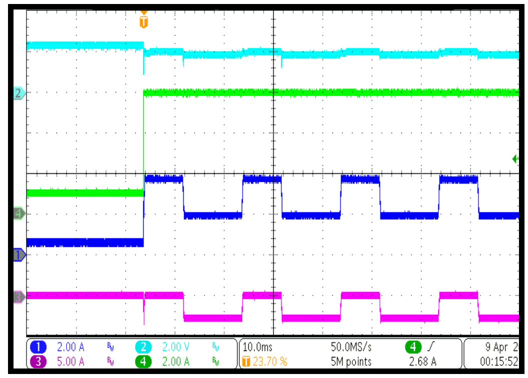
I_{IN} Regulation in Boost Mode

V_{IN} = 5V, V_{BATT} = 12V, charging disabled, I_{IN_LIM} = 3A, I_{SYS} = 0A to 2A to 0A



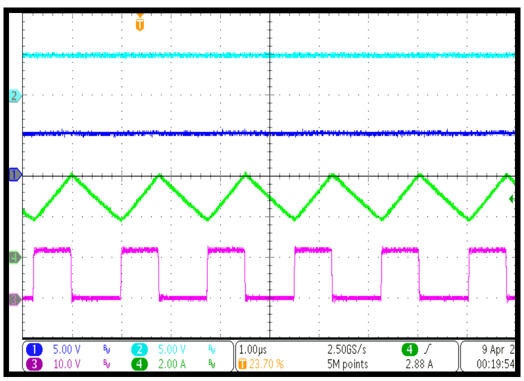
Two-Level I_{IN} Limit for Peak Power Mode

V_{IN} = 20V, V_{BATT} = 12V, charging disabled, $I_{INLIMT1}$ = 2A, $I_{INLIMIT2}$ = 4A, t_{PERIOD} = 20ms, t_{ILIM2} = 8ms, I_{SYS} = 1A to 6A



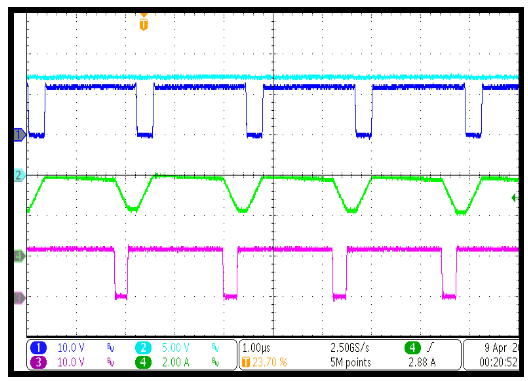
SRC Buck Operation

V_{BATT} = 12V, V_{IN_OUT} = 5V, I_{IN_OUT} = 3A



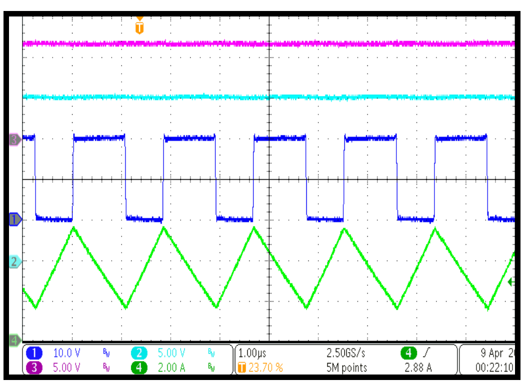
SRC Buck-Boost Operation

V_{BATT} = 12V, V_{IN_OUT} = 12V, I_{IN_OUT} = 3A



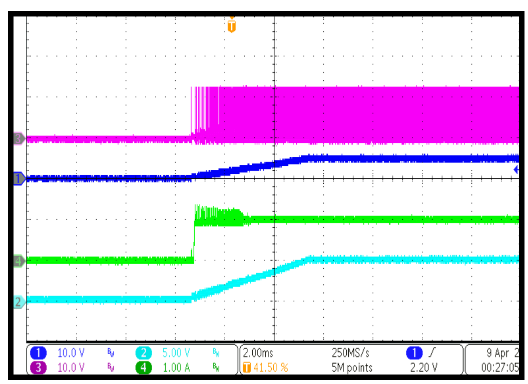
SRC Boost Operation

V_{BATT} = 12V, V_{IN_OUT} = 20V, I_{IN_OUT} = 2A



SRC Start-Up

V_{BATT} = 12V, V_{IN_OUT} = 5V, I_{IN_OUT} = 1A

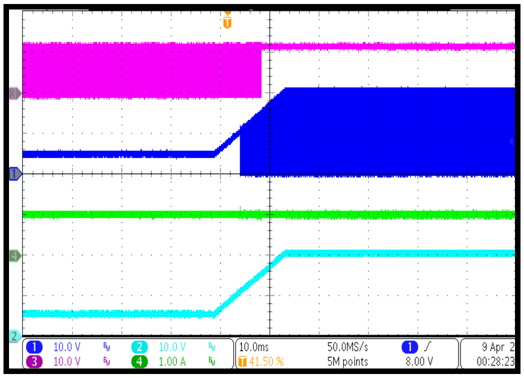


EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board, C_{IN} = 22µF x 1 POSCAP + 22µF x 5 MLCC + 1µF x 1 MLCC, C_{SYS} = 22µF x 2 POSCAP + 22µF x 5 MLCC + 1µF x 2 MLCC, C_{BATT} = 4.7µF x 1 MLCC + 22µF x 2 MLCC, L = 2.2µH/9.8mΩ, R_{SNS_IN} = R_{SNS_BAT} = 10mΩ, f_{SW} = 600kHz, 3-cell battery, T_A = 25°C, unless noted otherwise.

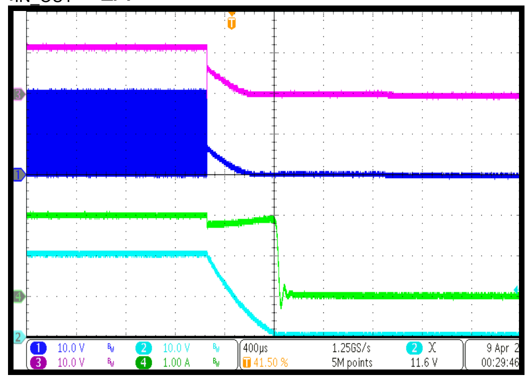
SRC Voltage Ramping Up

V_{BATT} = 12V, V_{IN_OUT} = 5V to 20V, I_{IN_OUT} = 1A



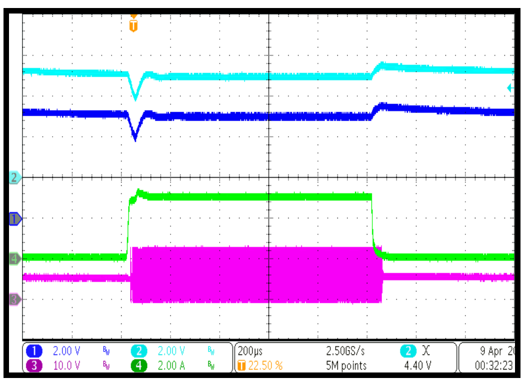
SRC Shutdown

V_{BATT} = 12V, V_{IN_OUT} = 20V, I_{IN_SRC} = 3A, I_{IN_OUT} = 2A



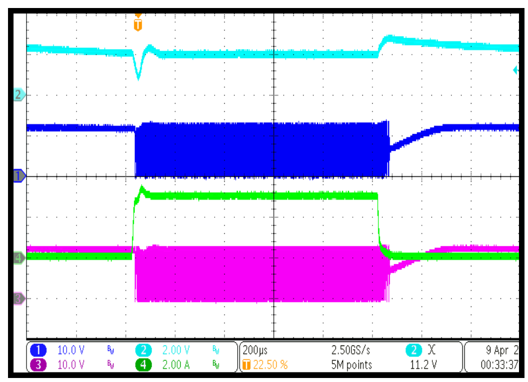
SRC Load Transient

V_{BATT} = 12V, V_{IN_OUT} = 5V, I_{IN_SRC} = 5A, I_{IN_OUT} = 0A to 3A to 0A



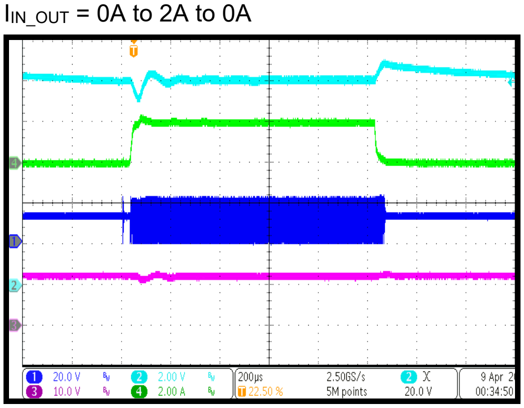
SRC Load Transient

V_{BATT} = 12V, V_{IN_OUT} = 12V, I_{IN_SRC} = 5A, I_{IN_OUT} = 0A to 3A to 0A



SRC Load Transient

V_{BATT} = 12V, V_{IN_OUT} = 20V, I_{IN_SRC} = 3A, I_{IN_OUT} = 0A to 2A to 0A



PCB LAYOUT

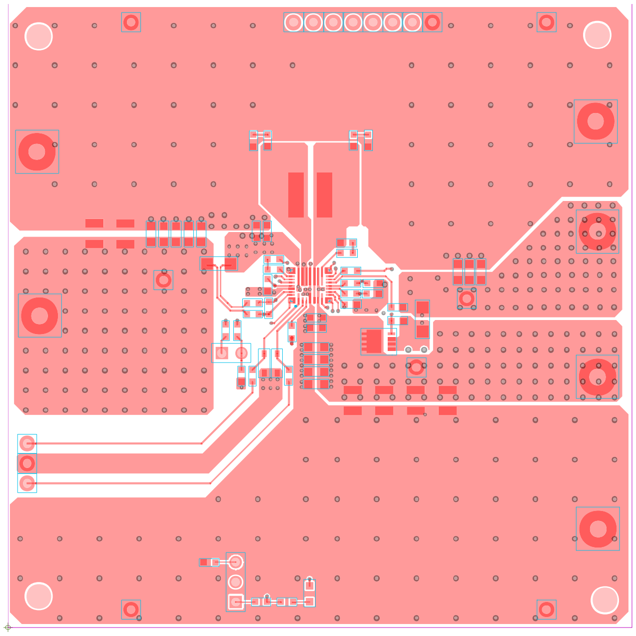


Figure 43: Top Layer

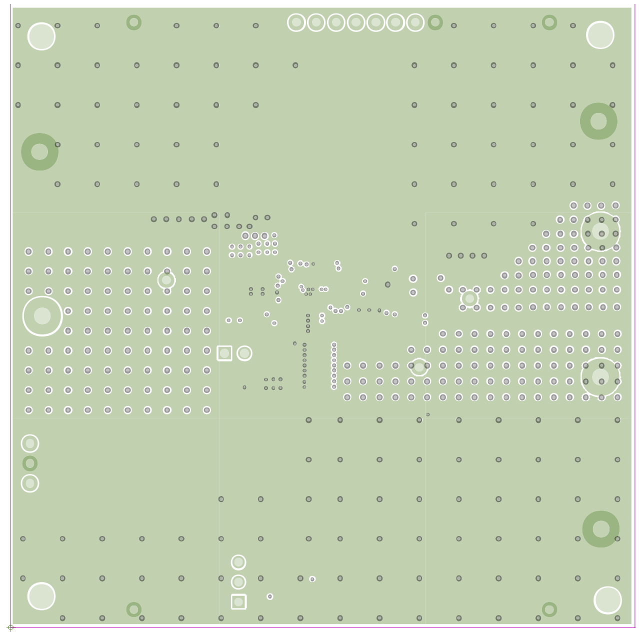


Figure 44: Mid-Layer 2

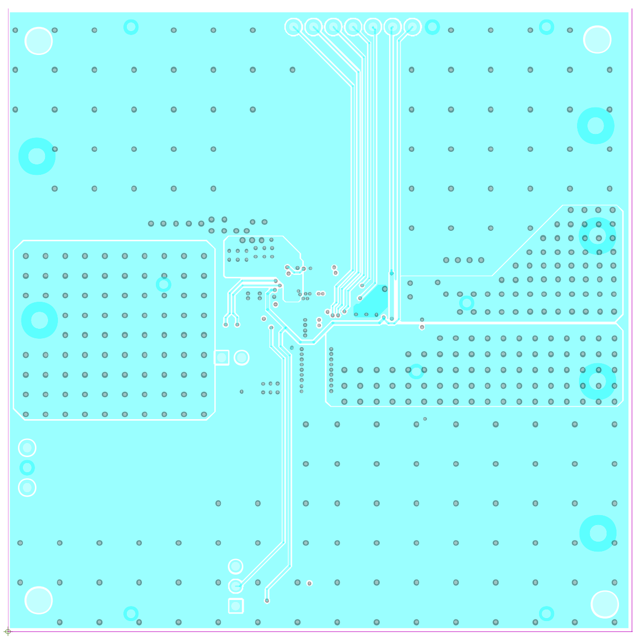


Figure 45: Mid-Layer 3

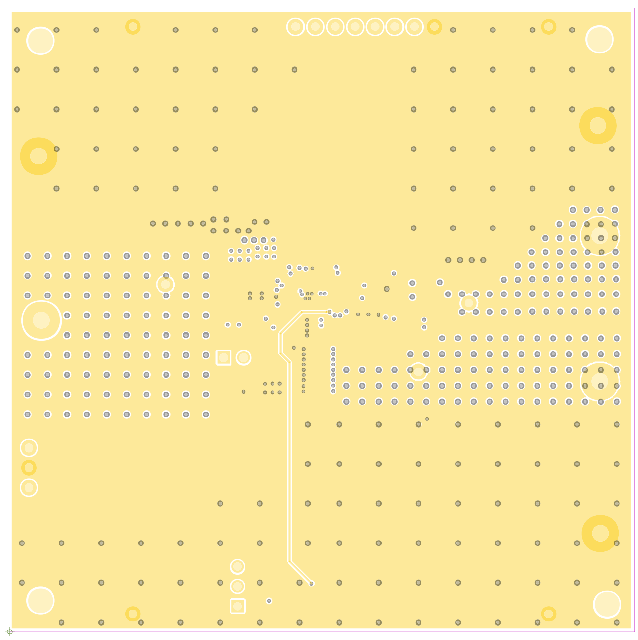


Figure 46: Mid-Layer 4

PCB LAYOUT *(continued)*

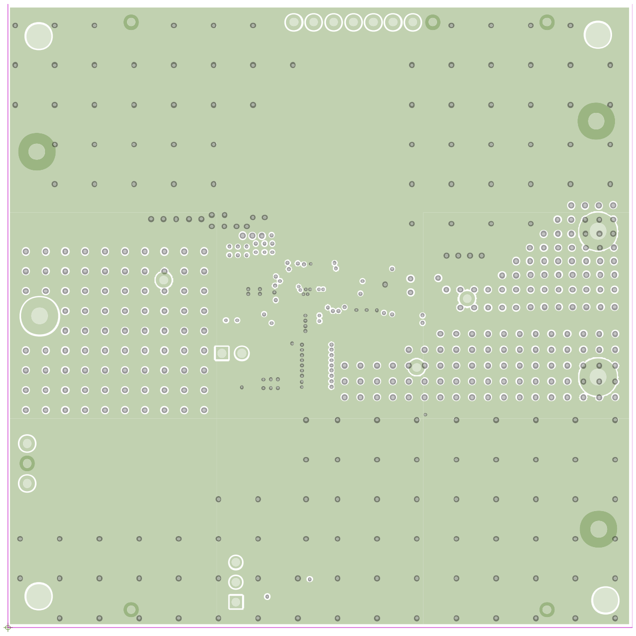


Figure 47: Mid-Layer 5

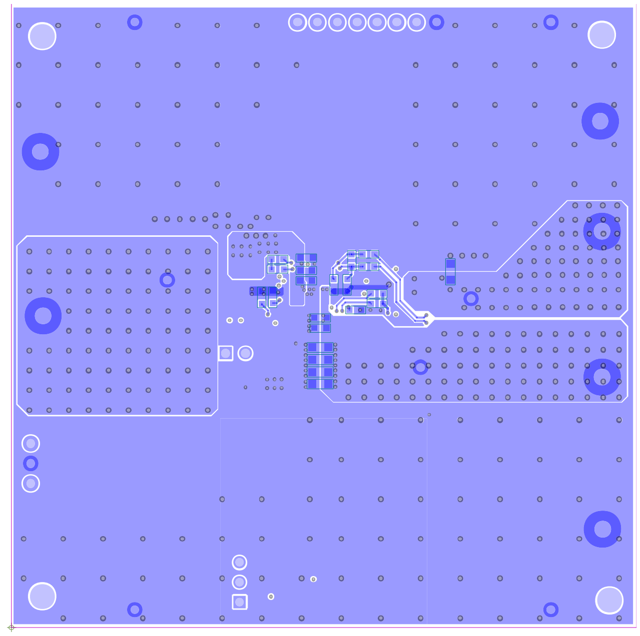


Figure 48: Bottom Layer

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	9/17/2025	Initial Release	-