EV188XX-XXX-SE-00A

$3kV_{RMS}$, Isolated, Dual-Channel Gate Driver Evaluation Board

DESCRIPTION

The EV188XX-XXX-SE-00A is an evaluation board designed to demonstrate the capabilities of the MP188xx family, a dual-channel, isolated gate driver solution for driving power switching devices with a short propagation delay and minimal pulse-width distortion.

By utilizing MPS's proprietary, capacitive-based isolation technology, the SOIC narrow-body (NB) package option can provide up to $3kV_{RMS}$ of withstand voltage (per UL 1577).

The MP188xx family can also provide a common-mode transient immunity (CMTI) rating exceeding 100kV/µs between the input side and output driver. With these advanced features, the driver operates at high efficiency, high power density, and with robustness across a wide variety of automotive power applications.

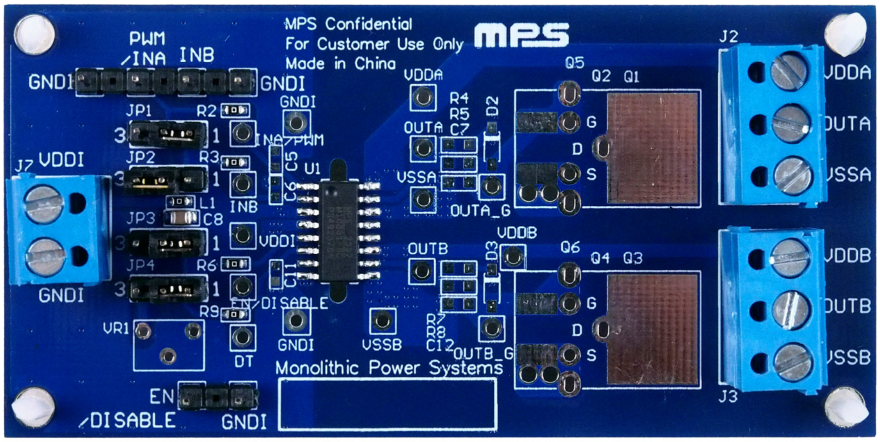
It is recommended to read the datasheet of the MP18831, MP18851, and MP18871 prior to making any changes to the EV188XX-XXX-SE-00A.

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C, unless otherwise noted.

Parameters	Conditions	Value
VDDI primary supply (V_{DDI} - V_{GNDI})		2.8V to 5.5V
VDDA or VDDB secondary supply (V_{DDA} - V_{SSA} or V_{DDB} - V_{SSB})	EV188xx-xxA-SE-00A, 3V under-voltage lockout (UVLO) threshold	4.2V to 30V
	EV188xx-xxB-SE-00A, 5V UVLO threshold	6.5V to 30V
	EV188xx-xxC-SE-00A, 8V UVLO threshold	9.2V to 30V
	EV188xx-xxE-SE-00A, 12V UVLO threshold	14.5V to 30V
Peak driver current (I_{OUTA} or I_{OUTB})		4A source, 4A sink

EV188XX-XXX-SE-00A EVALUATION BOARD



LxWxH (8.7cmx4.3cmx1.4cm)

Board Number	MPS IC Number
EV188XX-XXX-SE-00A	MP188xx-xxxGSE

EVALUATION BOARD BASIC INFORMATION

Table 1: EV188XX-XXX-SE-00A Basic Information

Evaluation Board Part Number (1) (2)	Output UVLO (V)	On/Off Logic	Input Logic	Configuration	IC Package Type
EV18831-4A-SE-00A	3	EN	INA/INB	High-side/ low-side half-bridge	SOIC-16 NB
EV18831-4B-SE-00A	5				
EV18831-4C-SE-00A	8				
EV18831-4E-SE-00A	12				
EV18831-A4A-SE-00A	3	DIS			
EV18831-A4B-SE-00A	5				
EV18831-A4C-SE-00A	8				
EV18831-A4E-SE-00A	12				
EV18851-4A-SE-00A	3	EN	INA/INB	Dual drivers	SOIC-16 NB
EV18851-4B-SE-00A	5				
EV18851-4C-SE-00A	8				
EV18851-4E-SE-00A	12				
EV18851-A4A-SE-00A	3	DIS			
EV18851-A4B-SE-00A	5				
EV18851-A4C-SE-00A	8				
EV18851-A4E-SE-00A	12				
EV18871-4A-SE-00A	3	EN	PWM	High-side/ low-side half-bridge	SOIC-16 NB
EV18871-4B-SE-00A	5				
EV18871-4C-SE-00A	8				
EV18871-4E-SE-00A	12				
EV18871-A4A-SE-00A	3	DIS			
EV18871-A4B-SE-00A	5				
EV18871-A4C-SE-00A	8				
EV18871-A4E-SE-00A	12				

Notes:

1) Contact MPS sales or an MPS distributor regarding the availability of the ordering part numbers.
2) These evaluation boards can only be ordered as customized boards though the MPS CSR team.

QUICK START GUIDE

Table 2: Jumper Setting Options

Jumper #	Jumper Name	Jumper Options		Default Setting
JP1	INA/PWM	Option A	Jumper cap not installed: INA/PWM is controlled via an external signal, and this pin is pulled low by default if left open.	Option A
		Option B	Jumper cap on connection points 2 and 3: Short INA/PWM to GNDI to set INA/PWM logic low.	
		Option C	Jumper cap on connection points 2 and 1: Short INA/PWM to VDDI to set INA/PWM logic high.	
JP2	INB	Option A	Jumper cap not installed: INB is controlled via an external signal, and this pin is pulled low by default if left open.	MP18831 and MP18851 are option A; MP18871 is option D
		Option B	Jumper cap on connection points 2 and 3: Short INB to GNDI to set INB logic low.	
		Option C	Jumper cap on connection points 2 and 1: Short INB to VDDI to set INB logic high.	
		Option D	Jumper cap not installed and not connected to the devices under testing.	
JP3	EN/DIS	Option A	Jumper cap not installed: The devices under testing are enabled if left open on the EN/DIS pin.	The part using DIS is option B; the part using EN is option C
		Option B	Jumper cap on connection points 2 and 3: Short EN/DIS to GNDI.	
		Option C	Jumper cap on connection points 2 and 1: Short EN/DIS to VDDI.	
JP4	DT	Option A	Jumper cap not installed: Interlock with the minimum dead time.	MP18831 and MP18871 are option C; MP18851 is option D
		Option B	Jumper cap on connection points 2 and 3: Short DT to VR1 to configured the dead time (in ns) ≈ 10 x R_{DT} (in kΩ). It is recommended to connect a minimum 220pF bypassing capacitor in parallel between DT and GNDI to achieve improved noise immunity.	
		Option C	Jumper cap on connection points 2 and 1: Short DT to VDDI to allow driver output overlap or follow the PWM input. The dead time is about 0ns for this option.	
		Option D	Jumper cap is not installed and not connected to the devices under testing.	

QUICK START GUIDE *(continued)*

1. Select the desired jumper setting.
2. Prepare DC power supply A, DC power supply B, and DC power supply C, and ensure that their outputs are insulated from each other.
3. Preset DC power supply A to 2.8V ≤ V_{DDI} - V_{GNDI} ≤ 5.5V. If the chip is controlled by external signals, ensure that V_{DDI} is not below the high level of these signals, then turn DC power supply A off.
4. Preset DC power supply B and DC power supply C to 4.2V, 6.5V, 9.2V, or 14.5V ≤ $V_{DDA/DDB}$ - $V_{SSA/SSB}$ ≤ 30V according to the UVLO option (see the Performance Summary section on page 1), then turn DC power supply B off.
5. If necessary, connect OUTx (where x = A or B) to the external loads.
6. Connect DC power supply A's output to J7.
7. Connect DC power supply B's output to J2.
8. Connect DC power supply C's output to J3.
9. After making the connections, turn DC power supply A, DC power supply B, and DC power supply C on.
10. If necessary, enable the external control signals.

EVALUATION BOARD SCHEMATIC

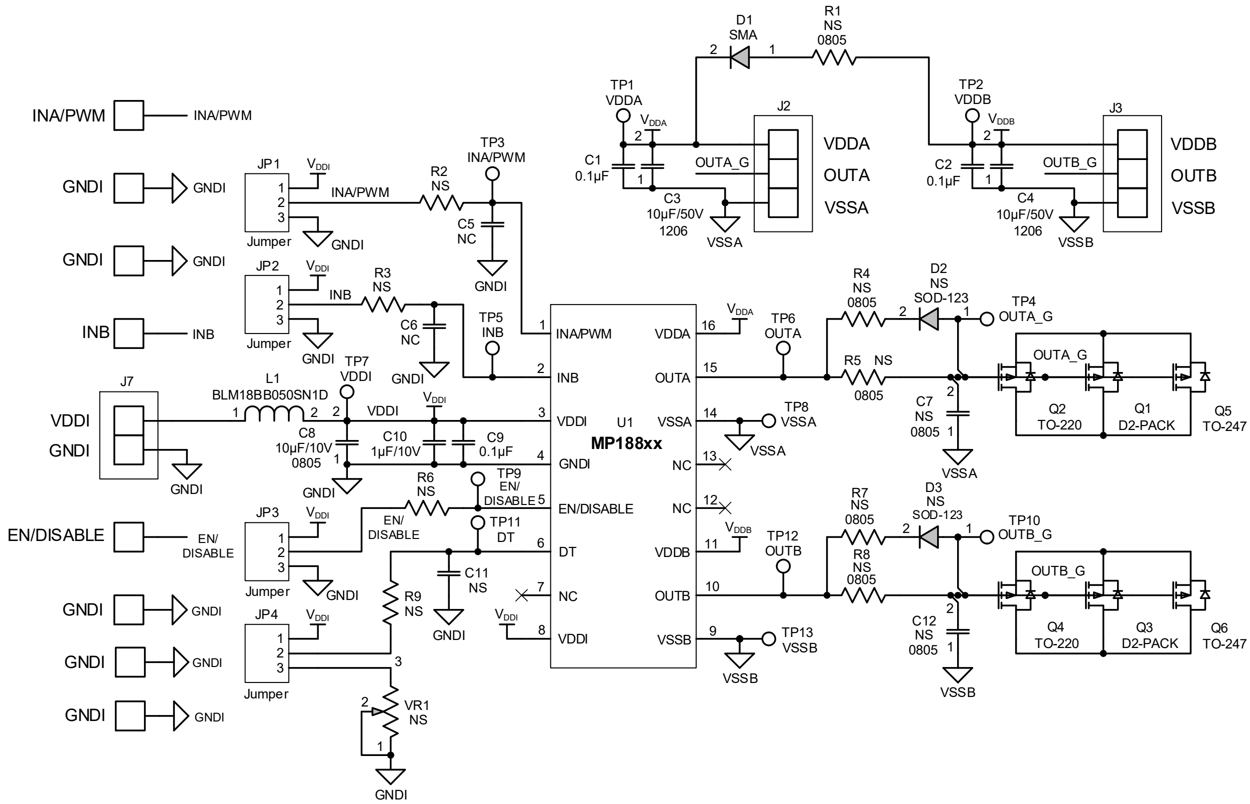


Figure 1: Evaluation Board Schematic

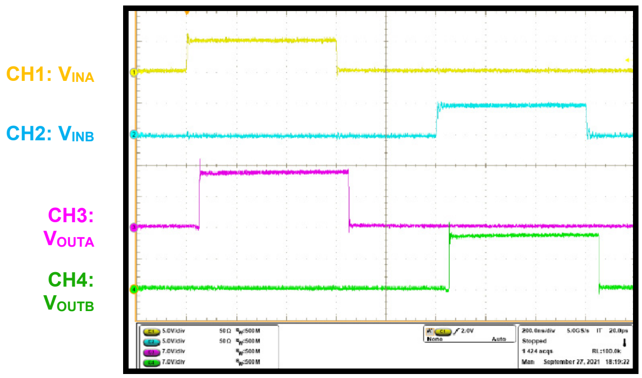
EV188XX-XXX-SE-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
3	C1, C2, C9	0.1µF	Ceramic capacitor, 16V, X7R	0603	Murata	GRM188R71C104KA01D
1	C10	1µF	Ceramic capacitor, 16V, X7R	0603	Murata	GRM188R71C105KA12D
2	C3, C4	10µF	Ceramic capacitor, 50V, X7T	1206	TDK	GRM31CD71H106KE11L
1	C8	10µF	Ceramic capacitor, 25V, X7S	0805	Murata	GRM21BC71E106KE11L
3	C5, C6, C11	NS				
2	C7, C12	NS				
1	D1	NS				
2	D2, D3	NS				
8	J1, J4, J5, J6, J8, J9, J10, J11	2.54mm	Pin header connector	SIP	Any	
2	J2, J3	5.08mm	Connection terminal block, 3-position	Through-hole	Any	
1	J7	5.08mm	Connection terminal block, 2-position	Through-hole	Any	
4	JP1, JP2, JP3, JP4	2.54mm	Pin header with jumper cap	SIP	Any	
1	L1	50mΩ	Ferrite bead, 5Ω at 100MHz, 700mA	0603	Murata	BLM18BB050SN1D
2	Q1, Q3	NS				
2	Q2, Q4	NS				
2	Q5, Q6	NS				
5	R1, R4, R5, R7, R8	NS				
4	R2, R3, R6, R9	0Ω	Thick film chip resistor, 5%	0603	Yageo	RC0603JR-070RL
13	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13	2.5mm	Test point	Through-hole	Any	
1	VR1	NS				
1	U1	MP188xx	3kV$_{RMS}$ isolated, dual-channel gate driver	SOIC-16 NB	MPS	MP188xx-xxxGSE

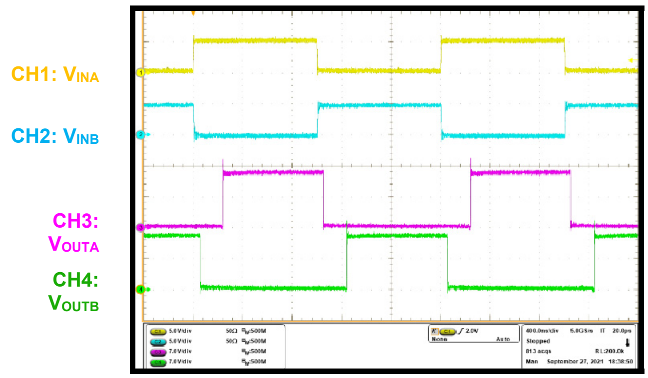
EVB TEST RESULTS

Performance waveforms are tested on the MP18831 evaluation board. V_{DDI} - V_{GNDI} = 5V, V_{DDA} - V_{SSA} = V_{DDB} - V_{SSB} = 12V, C_{LOAD} = 0pF, T_A = 25°C, all voltages with respect to the corresponding ground(s), unless otherwise noted.

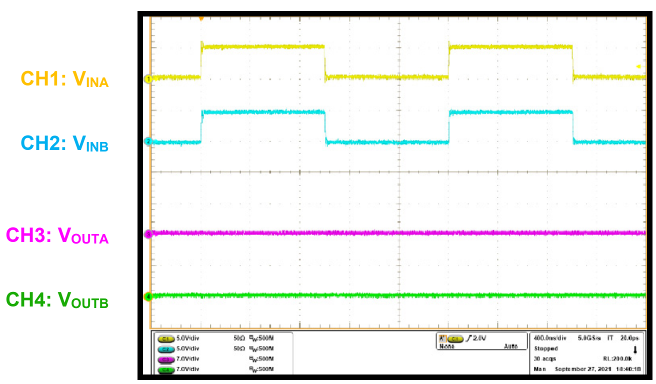
Typical Switching Waveforms
DT open



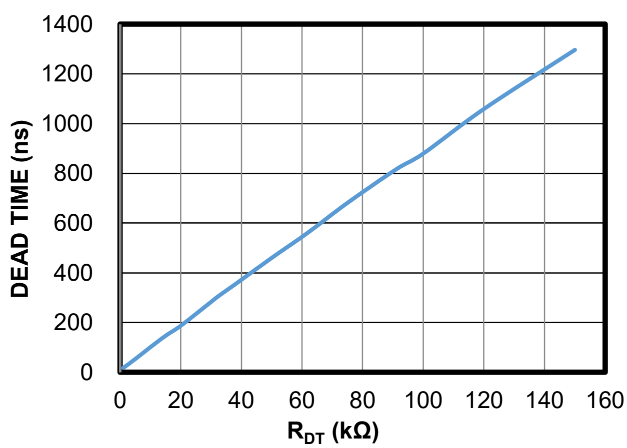
Dead-Time Control
R_{DT} = 20kΩ



Overlap Protection
R_{DT} = 20kΩ



Dead Time vs. Dead-Time Resistance



PCB LAYOUT

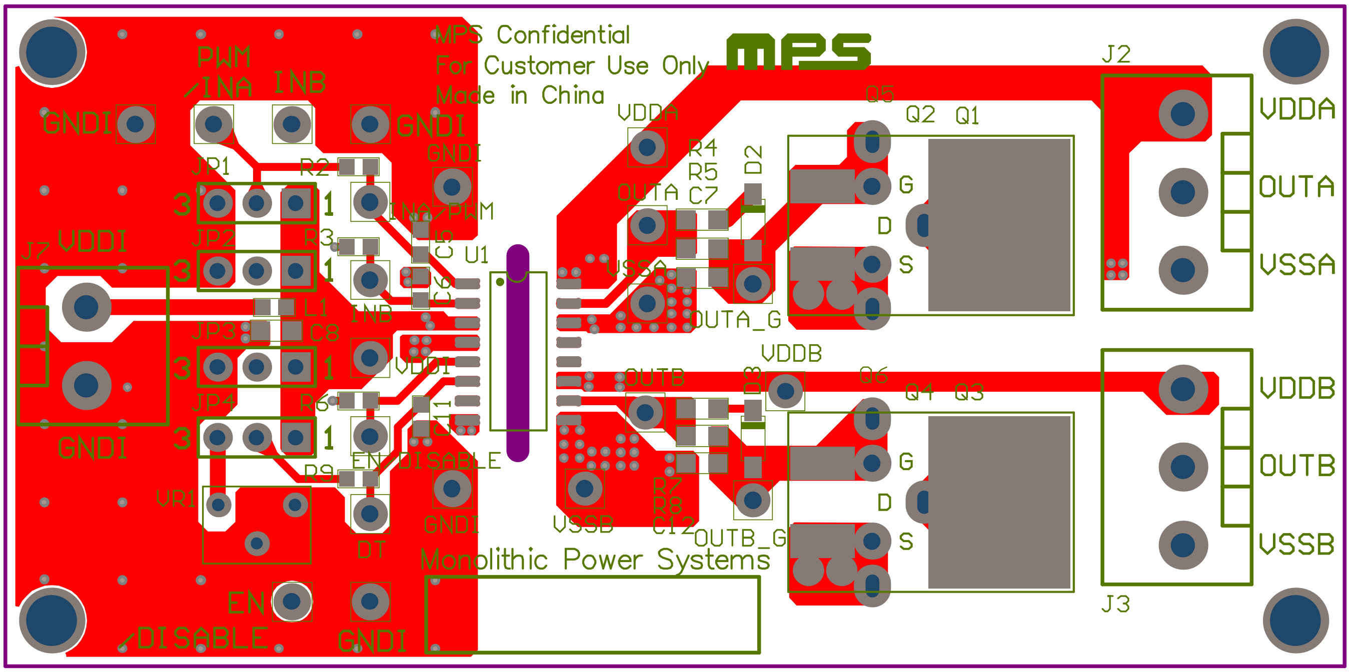


Figure 2: Top Silk and Top Layer

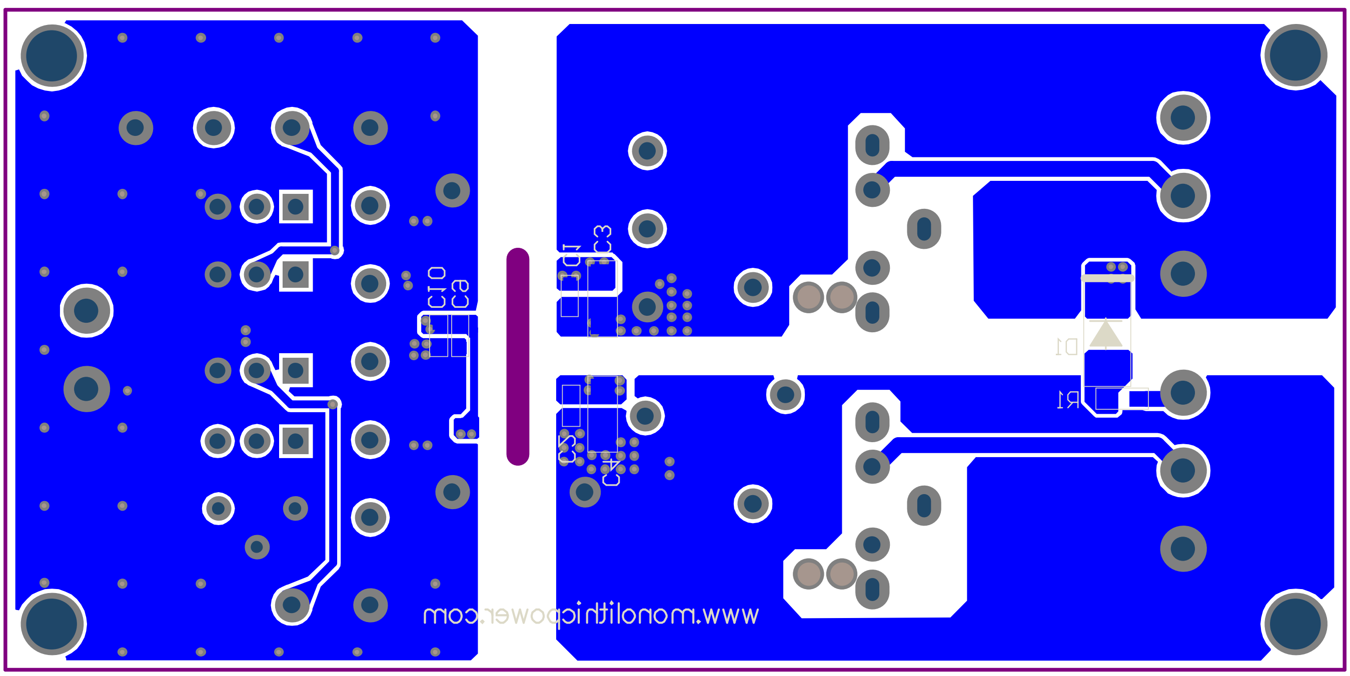


Figure 3: Bottom Layer and Bottom Silk

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	2/18/2025	Initial Release	-

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