

DESCRIPTION

The EV1720DQ-12-00A is the evaluation board for the MP1720DQ-012, a low-power mono BTL class-D audio amplifier. MP1720DQ-012 is one of MPS' products, which is low EMI, high efficiency, and full bridge output.

The EV board can also be used to evaluate the MP1720DQ-003, MP1720DQ-006, MP1720DQ-009, and MP1720DQ-216 (with IC replacement).

ELECTRICAL SPECIFICATIONS

| Parameter | Symbol | Value | Units |
|---|--------|-----------|-------|
| Supply Voltage | VIN | 2.5 – 5.5 | V |
| Gain | Av | 12 | dB |
| Maximum input signal (SE input) | | 3 | Vpp |
| Maximum input signal (Differential input) | | 6 | Vpp |

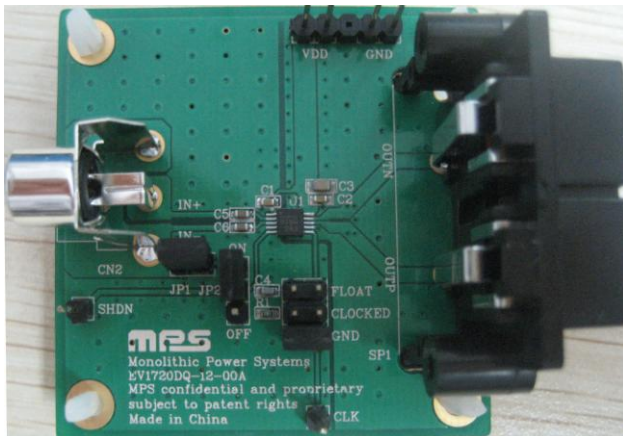
FEATURES

- Pass FCC-Radiated Emissions Standards with 24inch Cable without output filter
- 2.7W Into 4Ω with 5 V VIN @ 10% THD+N
- Up to 90% Efficiency
- Flexible Switching Frequency setting
- 2.5V~5.5V Operation from a Single Supply
- Low Noise (53μV Typical) with 3.3 V VIN
- Low Quiescent Current (4mA @3.3 V)

APPLICATIONS

- Cellular Phones
- PDAs
- MP3 Players
- Portable Audio

EV1720DQ-12-00A EVALUATION BOARD

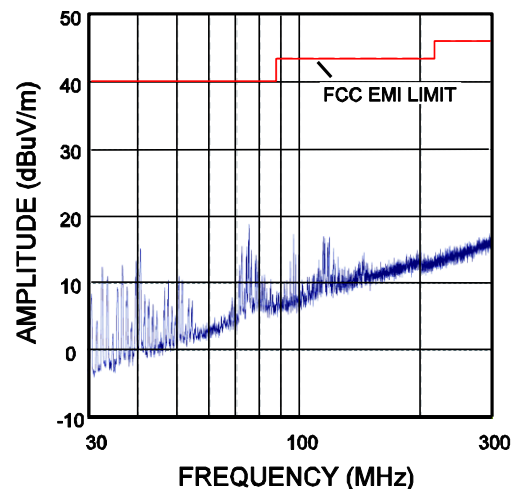


(L x W x H) 1.97" x 1.97" x 0.3"
 (5.0cm x 5.0cm x 0.7cm)

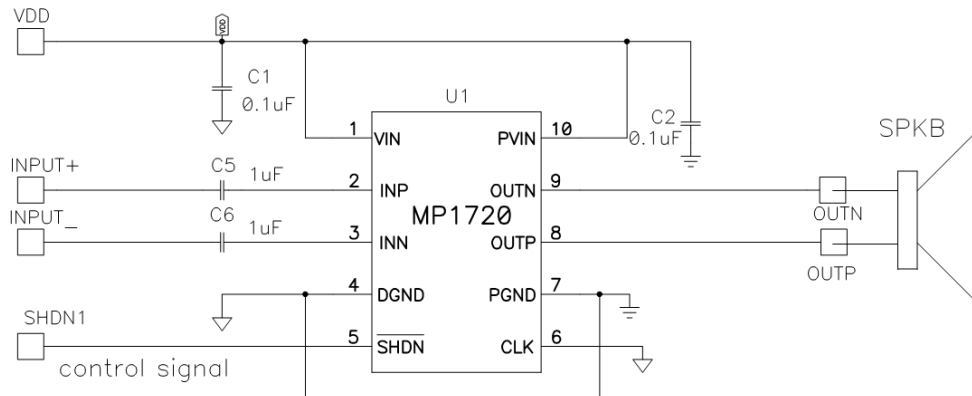
| Board Number | IC Number |
|-----------------|--------------|
| EV1720DQ-12-00A | MP1720DQ-012 |

EMI Spectrum Diagram

VIN=3.3V, R_{LOAD}=8Ω, no output filter,
 CLK=GND, Near field,
 6 inch unshielded twisted-pair-speaker cable



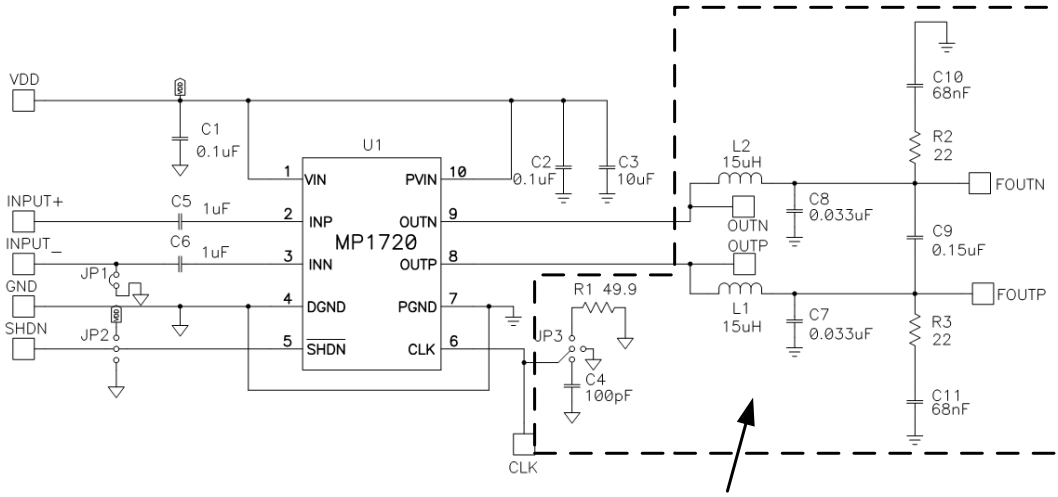
SCHEMATICS FOR ACTUAL APPLICATION



BILL OF MATERIALS FOR ACTUAL APPLICATION

| Qty | Ref | Value | Description | Package | Manufacture | Part Number |
|-----|-------|-------|------------------------------|---------|-------------|--------------------|
| 2 | C1,C2 | 0.1µF | Ceramic capacitor, X7R, 25V | 0603 | muRata | GRM188R71E104KA01 |
| 2 | C5,C6 | 1µF | Ceramic capacitor, X5R, 6.3V | 0603 | muRata | GRM188R60J105KA01D |
| 1 | U1 | | Amplifier | QFN10 | MPS | MP1720DQ-012 |

SCHEMATICS FOR TEST



NOT NEEDED FOR ACTUAL APPLICATION

BILL OF MATERIALS FOR TEST

| Qty | Ref | Value | Description | Package | Manufacture | Part Number |
|-----|------------------------|---------------|------------------------------|---------|-------------|---------------------|
| 2 | C1,C2 | 0.1 μ F | Ceramic capacitor, X7R, 25V | 0603 | muRata | GRM188R71E104KA01 |
| 1 | C3 ⁽¹⁾ | 10 μ F | Ceramic capacitor, X5R, 10V | 0805 | muRata | GRM21BR61A106KE19L |
| 1 | C4 | 100pF | Ceramic capacitor, C0G, 50V | 0603 | muRata | GRM1885C1H101JA01D |
| 2 | C5,C6 | 1 μ F | Ceramic capacitor, X5R, 6.3V | 0603 | muRata | GRM188R60J105KA01D |
| 2 | C7,C8 ⁽²⁾ | 33nF | Ceramic capacitor, X7R, 50V | 0603 | muRata | GRM188R71H333KA61D |
| 1 | C9 ⁽²⁾ | 0.15 μ F | Ceramic capacitor, X7R, 50V | 0805 | TDK | C2012X7R1H154K |
| 2 | C10,C11 ⁽²⁾ | 68nF | Ceramic capacitor, X7R, 50V | 0603 | muRata | GRM188R71H683KA93D |
| 2 | L1,L2 ⁽²⁾ | 15 μ H | Inductor, 1.9A | DS75LC | TOKO | DS75LC-B1047AS-150M |
| 1 | R1 | 49.9 Ω | Ceramic Resistor, 1% | 0603 | Yageo | RC0603FR-0749R9L |
| 2 | R2,R3 ⁽²⁾ | 22 Ω | Ceramic Resistor, 1% | 0603 | Yageo | RC0603FR-0722RL |
| 1 | U1 | | Amplifier | QFN10 | MPS | MP1720DQ-012 |
| 1 | JP1 | | JUMPER/2PIN/0.1 | | any | |
| 1 | JP2 | | JUMPER/3PIN/0.1 | | any | |
| 1 | JP3 | | JUNPER/3PIN&3PIN/0.1 | | any | |

Note:

- 1) It is required in system design.
- 2) These external components are used for performance test. For audio performance test, a LC low-pass filter (33nF, 15 μ H, 0.15 μ F) is required even if the analyzer has a low-pass filter. They are optional for normal operation

PRINTED CIRCUIT BOARD LAYOUT

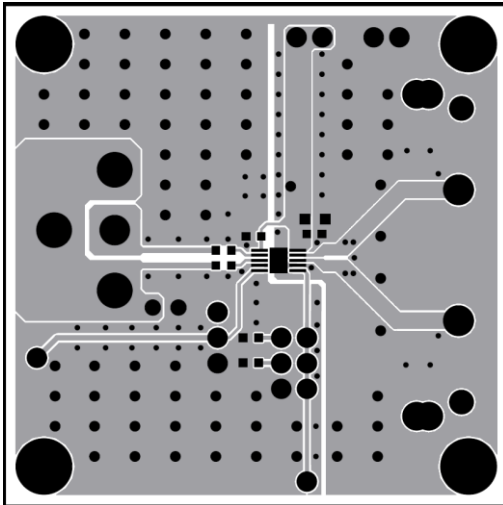


Figure 1—Top Layer

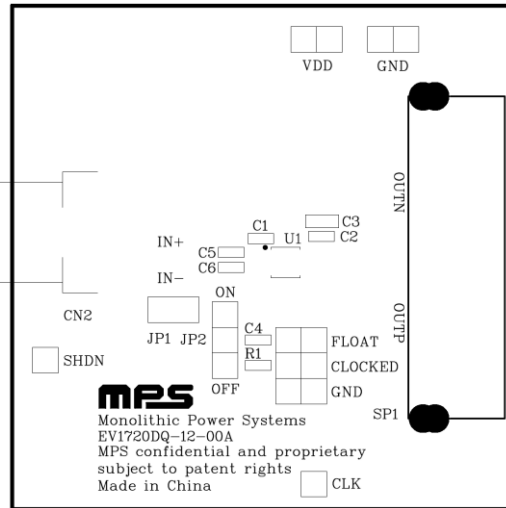


Figure 2—Top silk Layer

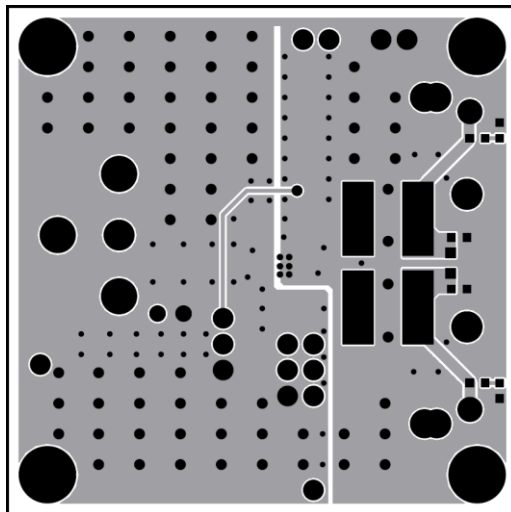


Figure 3—Bottom Layer

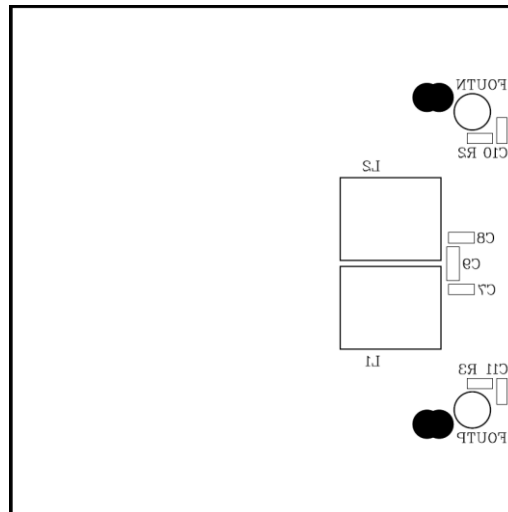


Figure 4—Bottom Silk Layer

QUICK START GUIDE

This board is set up from the factory for MP1720DQ-012 evaluation. This EV board can also be used to evaluate the MP1720DQ-003, MP1720DQ-006, MP1720DQ-009, and MP1720DQ-216 (with IC replacement).

For audio performance test, the LC low-pass filter is required even if the analyzer has a low-pass filter. Please use FOUTP and FOUTN as the output terminals (see Figure 6).

For more information, refer to the MP1720 datasheet.

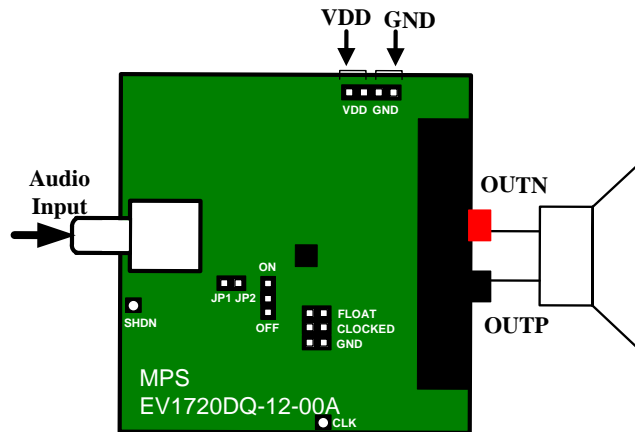


Figure 5—Connection for Normal Application (Top View)

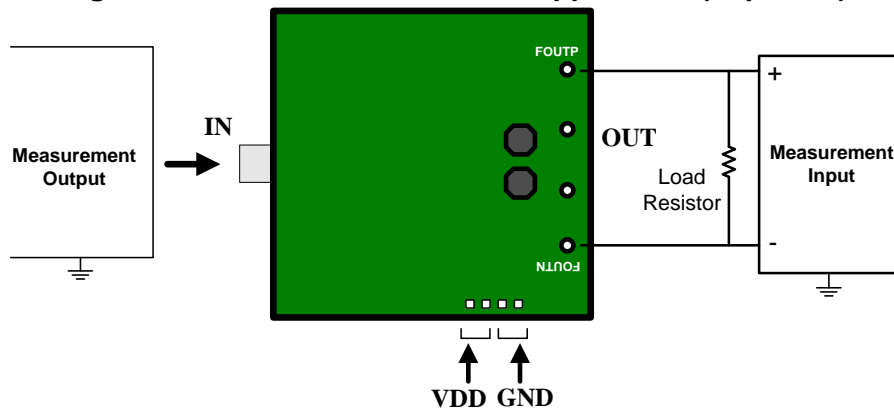


Figure 6—Connection for Audio Performance Test (Bottom View)

1. Setups for 5V operation
 - a) Connect the external power supply to the VDD terminal, and adjust to 5V (do not turn on).
 - b) Connect the SE input signal to the input terminals. If the input is differential configuration, remove the shunt of jumper JP1.
 - c) Connect the speaker to the output terminals.

- d) Set the amplifier CLK frequency as the table1.

Table1—CLK Operating Modes

| | |
|-------------|--|
| CLK=GND | $f_{CLK}=1.0\text{MHz}$ |
| CLK=FLOAT | $f_{CLK}=1.3\text{MHz}$ |
| CLK=Clocked | $f_{CLK}=\text{external clock frequency (0.5~1.4MHz)}$ |

- e) Turn on the power supply.
2. Turn on music
 - a) Set the jumper JP2 to 'ON', or drive /SHDN high.
 - b) Adjust the input signal to expected level.
 3. Turn off music
 - a) Set the jumper JP2 to 'OFF', or drive /SHDN low.
 - b) Turn off the power supply.

NOTICE: The information in this document is subject to change without notice. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.