DIY8886

45V Input, 6A Ouptut Digital Programmable Synchronous Buck Regulator

DESCRIPTION

The DIY8886 is a 45V input, dual-phase, single-output, high-efficiency, synchronous step-down converter with a PMBus control interface. It can provide up to 6A continuous output current with excellent load and line regulation over a wide input supply range.

The DIY8886 integrates high-side and low-side power MOSFETs for high efficiency without an external Schottky diode and is available in a FCQFN (5mmx5mm) package. With an internal programmable compensation network, the DIY8886 offers a very compact solution with a minimal number of external components.

The output voltage can be controlled through the PMBus serial interface or the external voltage divider connected to the FB pin. The output voltage can be adjusted on-the-fly from 0.6V to 20V. The voltage slew rate, switching frequency, enable, and power save mode are also selectable through the PMBUS interface.

Peak-current-mode control provides fast transient response and eases loop stabilization. Full protection features include under-voltage lockout, over-voltage protection, over-current protection, and thermal shutdown.

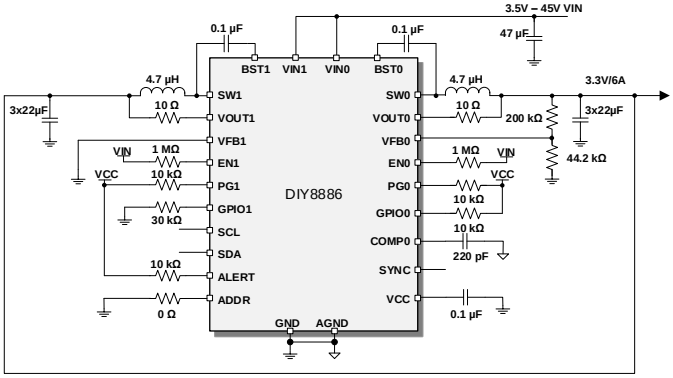
FEATURES

- Wide V_{IN} Range: 3.5V to 45V
- Wide V_{OUT} Range: 0.6V to 20V
- Output Current up to 6A
- 1% V_{OUT} Accuracy Over Operation Temperature Range
- Programmable Constant Switching Frequency (150kHz – 2.2MHz) with External Clock Synchronization
- Internal 60mΩ/34mΩ Low $R_{DS(ON)}$ MOSFETs
- Frequency Spread Spectrum Option for Low EMI
- OVP, UVP, OCP, UVLO, Thermal Shutdown Protection
- Programmable MTP Parameters Include: V_{IN}, V_{OUT}, I_{OUT}, Temperature, and Faults
- CRC Protection for OTP Integrity
- Available in FCQFN (5mmx5mm) Package

APPLICATIONS

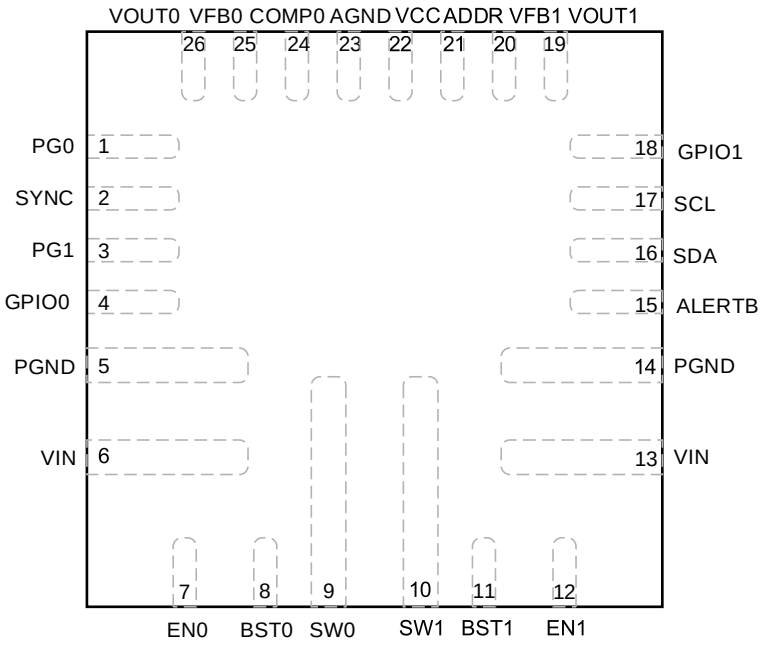
- Industrial Power Systems
- Automotive Power Systems
- USB PD and Type C Applications

TYPICAL APPLICATION



Dual-Phase Single Output

PACKAGE REFERENCE



QFN26 (5x5mm)

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} .....-0.3V to 48V
V_{SW}.....-0.3V to V_{IN}+0.3V
V_{EN} .....-0.3V to 45V
V_{BST} ..... V_{SW}+5.5V
V_{CC} 5.5V
All Other Pins.....-0.3V to 5V
Continuous Power Dissipation(T_A = +25°C) **(2)**
QFN-16 (3mmX4mm) 2.6W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... -65°C to +150°C

Recommended Operating Conditions

Supply Voltage (V_{IN}).....3.5V to 45V
Output Voltage (V_{OUT}) .....0.6V to 20V
Operating Junction Temp.(T_J).. -40°C to +125°C

Thermal Resistance (3)	θ_{JA}	θ_{JC}
QFN26 (5×5mm)……..	TBD	TBD °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS (1)

V_{IN} = 12V, V_{EN} = 2V, T_A= -40°C to 125°C, Typical values refer to T_J =25°C,unless otherwise noted.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
V_{IN} under-voltage lockout rising threshold	$INUV_{Vth}$	PMBUS default set	3.2	3.5	3.7	V
V_{IN} UVLO threshold hysteresis	$INUV_{HYS}$	PMBUS default set		380		mV
V_{IN} UVLO threshold DAC range	$INUV_{Vth}$	PMBUS set range	3.5		7.5	V
V_{IN} quiescent current	I_Q	V_{OUT}=6V, with BIAS power, no load,		12		uA
	I_Q	V_{FB}>V_{REF}, no load		TBD		μA
V_{IN} shutdown current	I_{SD}	V_{EN}=0V, T_J = 25 °C			1	μA
Default output voltage	V_{OUT}	PMBUS default set, T_J =25°C	-2%	3.3	2%	V
		T_J =-40°C to -125°C		3.3		V
Operation V_{OUT} range	V_{OUT}	PMBUS set range	0.6		20	V
Default switching frequency	f_{SW}	PMBUS default set	500	600	700	kHz
Frequency programmable range	f_{PROG}	PMBUS set range	150		2200	kHz
Sync frequency range	f_{SYNC}	Sync clock set range	150		2200	kHz
Sync voltage high threshold	$V_{SYNC-HIGH}$			1.4	1.8	V
Sync voltage low threshold	$V_{SYNC-LOW}$		0.4	0.8		V
Minimum on time(5)	T_{ON-MIN}	With peak current mode		100		ns
Minimum off time(5)	$T_{OFF-MIN}$				150	ns
HS switch on resistance for each channel	R_{DSON-H}	V_{BST}-V_{SW}=5V		60		mΩ
LS switch on resistance for each channel	R_{DSON-L}			34		mΩ
Switch leakage current	I_{SW-LKG}	T_J = 25 °C			1	μA
Default soft-start time	T_{SS}	PMBUS default set		1		ms
Soft-start time range	T_{SS}	PMBUS set range	0.5		8	ms
Default EN voltage threshold	V_{EN}	PMBUS default set	1	1.2	1.4	V
Default EN voltage hysteresis	V_{EN-HYS}	PMBUS default set		200		mV
EN voltage hysteresis range	V_{EN-HYS}	PMBUS set range	200		400	mV
Default PG upper trip threshold		As percentage of V_{OUT} set		117		%
Default PG lower trip threshold		As percentage of V_{OUT} set		90		%
Default PG trip threshold hysteresis		As percentage of V_{OUT} set		5		%

ELECTRICAL CHARACTERISTICS (1)

V_{IN} = 12V, V_{EN} = 2V, T_A= -40°C to 125°C, Typical values refer to T_J =25°C,unless otherwise noted.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
PG trip threshold hysteresis range		PMBUS set range	5		10	%
PG output voltage low	$V_{PG-SINK}$	I_{SINK} = 1mA		0.1	0.3	V
PG deglitch timer	$T_{PG-DELAY}$			20		µs
VCC regulator	V_{CC}	I_{CC}=0mA	4.7	4.9	5.1	V
Default peak current limit	$I_{PEAK-LIMIT}$	PMBUS default set	8	10	12	A
Peak current limit range	$I_{PEAK-LIMIT}$	PMBUS set range	7		14	A
Default valley current limit	$I_{VALEY-LIMIT}$	PMBUS default set	5	6	7	A
Valley current limit range	$I_{VALEY-LIMIT}$	PMBUS set range	3		9	A
Default input OVP threshold		PMBUS default set		50.8		
Input OVP threshold range		PMBUS set range	28		40	V
Input OVP threshold accuracy		PMBUS set 36V	34	36	38	V
Default input OVP hysteresis		As percentage of input OVP threshold set		1.08		V
Input OVP hysteresis range		PMBUS set range	1.08		2.16	V
Default thermal shutdown(5)	T_{SD}	PMBUS default set	150	175		°C
Thermal shutdown range(5)	T_{SD}	PMBUS set range	125		175	°C
Default thermal shutdown hysteresis(5)	T_{SD-SYS}	PMBUS default set		25		°C
Thermal shutdown hysteresis range(5)	T_{SD-SYS}	PMBUS set range	25		50	°C

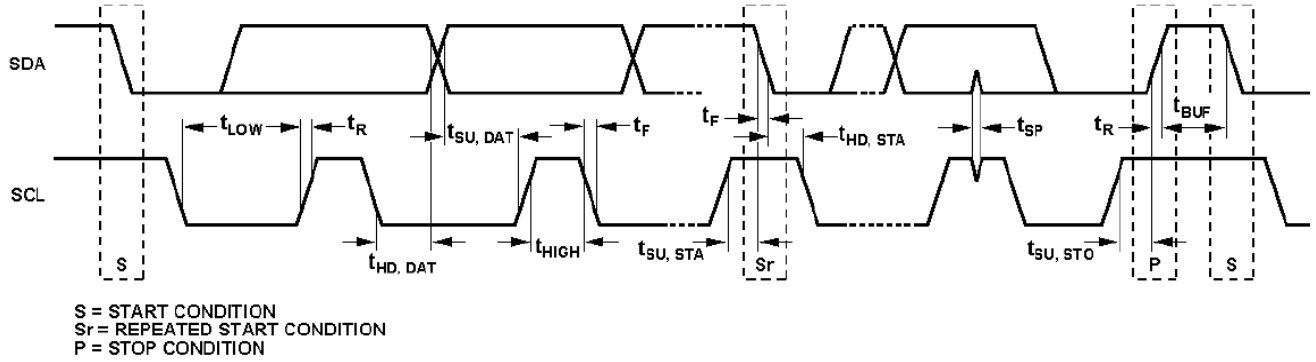
Notes:

(5)Not tested in production and guaranteed by design and characterization.

PMBUS PORT SIGNAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_A= -40°C to 125°C, Typical values refer to T_J =25°C,unless otherwise noted.

Parameters	Symbol	Condition	Min.	Typ.	Max.	Units
PMBUS Interface Specifications						
Input logic low	V_{IL}		0		0.4	V
Input logic high	V_{IH}		1.3			V
Output logic low	V_{OL}	I_{LOAD}=3mA			0.4	V
SCL clock frequency	f_{SCL}				400	kHz
SCL high time	t_{HIGH}		0.6			µs
SCL low time	t_{LOW}		1.3			µs
Data setup time	$t_{SU,DAT}$		100			ns
Data hold time	$t_{HD,DAT}$		0		0.9	µs
Setup time for repeated start	$t_{SU,STA}$		0.6			µs
Hold time for start	$t_{HD,STA}$		0.6			µs
Bus free time between a start and a stop condition	t_{BUF}		1.3			µs
Setup time for stop condition	$t_{SU,STO}$		0.6			µs
Rise time of SCL and SDA	t_R		20+0.1 ×C_B		120	ns
Fall time of SCL and SDA	t_F		20+0.1 ×C_B		120	ns
Pulse width of suppressed spike	t_{SP}		0		50	ns
Capacitance bus for each bus line	C_B				400	pF



PMBUS Compatible Interface Timing Diagram

PIN FUNCTIONS

Package Pin #	Name	Description
1	PG0	**Power good indicator for channel 0**. The output of PG is an open drain. Connect a resistor to a pull-up power source if used.
2	SYNC	**Synchronized to external clock signal.** SYNC can be programmed by the PMBus to the sync input or sync output.
3	PG1	**Power good indicator for channel 1.** The output of PG is an open drain. Connect a resistor to a pull-up power source if used.
4	GPIO0	**General I/O port 0.**
5,14	PGND	**Power ground.** Reference ground of the regulated output voltage. Connect these pins to larger copper areas to the negative terminals of the input and output capacitors.
6,13	VIN	**Supply voltage.** VIN supplies all power to the converter. Place a decoupling capacitor to ground as close as possible to the IC to reduce switching spikes. Connect using a wide PCB trace.
7	EN0	**Enable for channel 0**. Drive EN0 high to turn on channel 0, and drive it low or float it to turn off the device. It has an internal 1MΩ pull-down resistor to ground.
8	BST0	**Bootstrap for channel 0.** BST0 requires a capacitor connected between SW and BST to form a floating supply across the high-side switch driver. A 20Ω resistor placed between the SW and BST capacitor is strongly recommended to reduce the SW spike voltage.
9	SW0	**Switch output for channel 0.** Internally connect to the high-side and low-side power switches. Externally connect to the output inductor. Connect using a wide PCB trace.
10	SW1	**Switch output for channel 1.** Internally connect to the high-side and low-side power switches. Externally connect to the output inductor. Connect using a wide PCB trace.
11	BST1	**Bootstrap for channel 1.** BST1 requires a capacitor connected between SW and BST to form a floating supply across the high-side switch driver. A 20Ω resistor placed between the SW and BST capacitor is strongly recommended to reduce the SW spike voltage.
12	EN1	**Enable for channel 1.** Drive EN1 high to turn on channel 1, and drive it low or float it to turn off the device. It has an internal 1MΩ pull-down resistor to ground.
15	/ALERTB	**PMBus alert.**
16	SDA	**PMBus serial data.**
17	SCL	**PMBus serial clock.**
18	GPIO1	**General I/O port 1.**
19	VOUT1	**Sense input of output voltage for channel 1.**
20	FB1	**Error amplifier feedback inputs for channel 1**. FB1 receives sensed voltage feedback voltage for channel 1 from an external resistive divider across the output. In multi-phase mode, FB1 needs to be pulled high to disable this channel's error amplifier.
21	ADDR	**Address setting for the PMBus.**
22	VCC	**Internal 5V LDO regulator output.** Decouple with 0.22µF capacitor.
23	AGND	**Signal ground.** Ground for the internal logic and signal circuit. AGND is not connected internally to power ground. Ensure AGND is connected to power ground in the PCB layout.
24	COMP0	**Channel 0 error amplifier output.** For multi-chip, multi-phase application, connect COMP0 for each chip for current sharing.
25	FB0	**Error amplifier feedback inputs for channel 0**. FB0 receives sensed voltage feedback voltage for channel 0 from an external resistive divider across the output.
26	VOUT0	**Sense input of the output voltage for channel 0.**

FUNCTIONAL BLOCK DIAGRAM

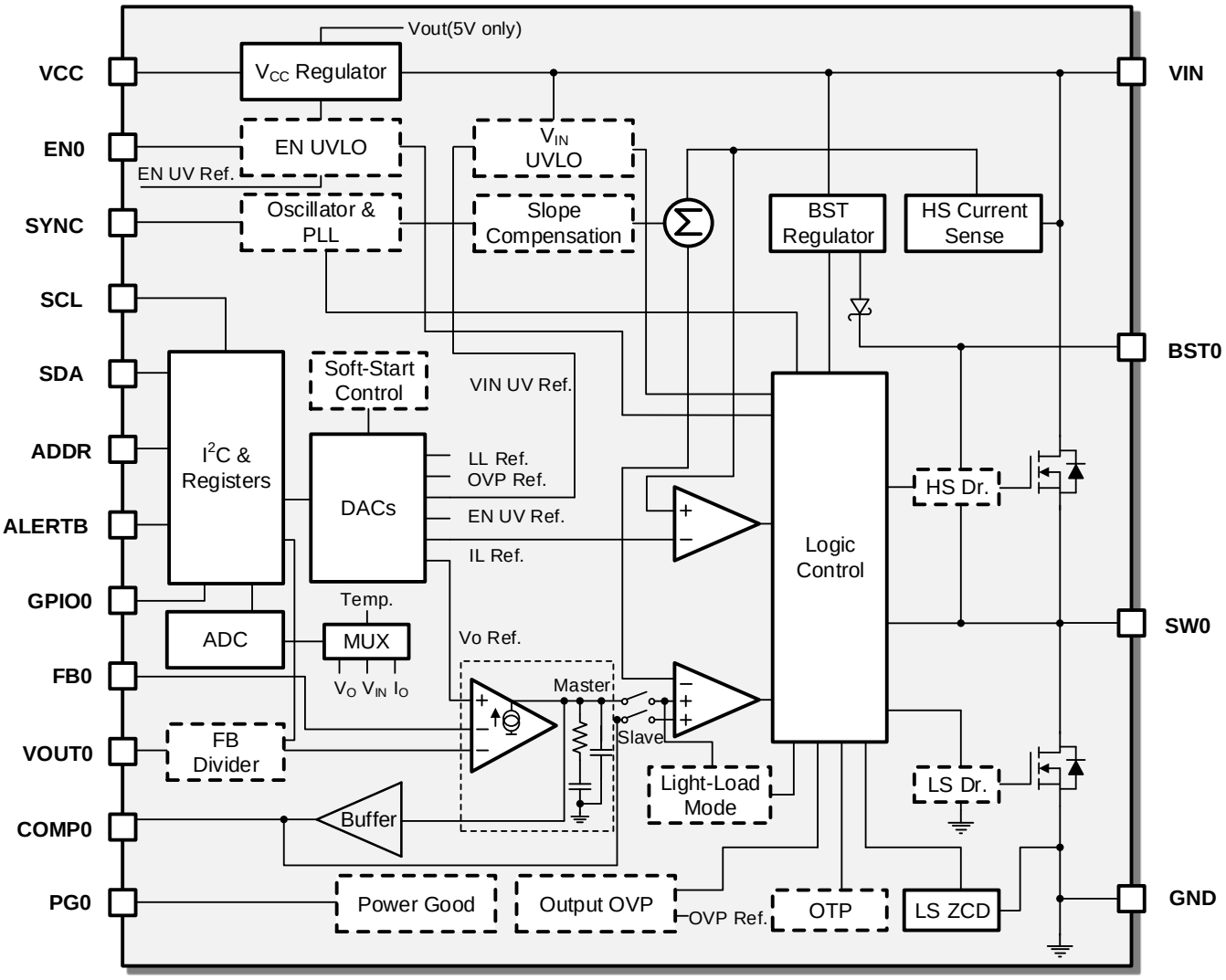


Figure 1: Functional Block Diagram (Only one channel is shown; blocks in dashed lines are programmable)

REGISTER DESCRIPTION

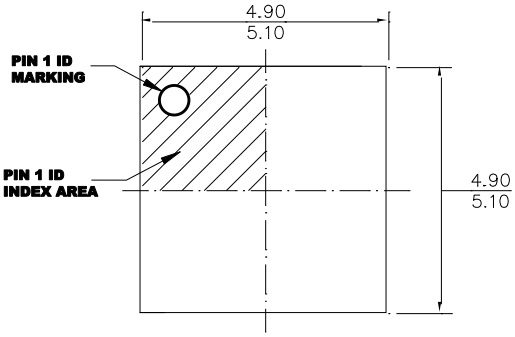
CMD Name	CMD Code	Description	Type	Data Format	Units	MTP	Default Value
PAGE	0X00		R/W Byte	Reg		N	00h
OPEARTION	0x01	ON/OFF/Margin High/Margin Low/Soft-OFF	R/W Byte	Reg		Y	80h
CLEAR_FAULTS	0x03		Send Byte	Reg		N	
WRITE_PROTECT	0x10		R/W Byte	Reg		N	00h
STORE_USER_ALL	0x15	When sending this command, the converter will pull EN down first, then release it.	Send Byte	Reg		N	
RESTORE_USER_ALL	0x16	When sending this command, the converter will pull EN down first, then release it.	Send Byte	Reg		N	
VOUT_COMMAND(10 bit)	0x21	10-bit Vout setpoint, 0-1.536V Vout_command=vout/(1.5mV*FB divider ratio)	R/W Word	Direct	V	Y	226h
VOUT_MAX (10-bit)	0x24	Vout_max=vout/(1.5mV*FB divider ratio)	R/W Word	Direct	V	Y	3FFh
VOUT_MARGIN_HIGH(10 bit)	0x25	Default 1.075V (+7.5%) Vout_margin high=vout/(1.5mV*FB divider ratio)	R/W Word	Direct	V	Y	252h
VOUT_MARGIN_LOW(10 bit)	0x26	Default 0.925V (-7.5%) Vout_margin low=vout/(1.5mV*FB divider ratio)	R/W Word	Direct	V	Y	1FAh
VIN_ON(9bit)	0x35	Note: 9 bits, lsb=108mV	R/W Word	Direct	V	Y	20h
VIN_OFF(9bit)	0x36	Note: 9 bits, lsb=108mV	R/W Word	Direct	V	Y	1Dh
VIN_OV_FAULT_LIMIT(9bit)	0x55	Note: 9 bits, lsb=108mV	R/W Word	Direct	V	Y	1D6h
TON_DELAY(7bit)	0x60	0-127	R/W Word	Direct	mS	Y	0
TON_RISE(5bit)	0x61	0-31	R/W Word	Direct	mS	Y	1
TOFF_DELAY(7bit)	0x64	0-127	R/W Word	Direct	mS	Y	0
TOFF_FALL(5bit)	0x65	0-31	R/W Word	Direct	mS	Y	1
STATUS_BYTE	0x78		R Byte	Reg		N	
STATUS_WORD	0x79		R Word	Reg		N	
STATUS_VOUT Combine for MFR	0x7A		R Byte	Reg		N	
STATUS_IOUT Combine for MFR	0x7B		R Byte	Reg		N	
STATUS_INPUT Combine for MFR	0x7C		R Byte	Reg		N	
STATUS_TEMPERATURE	0x7D		R Byte	Reg		N	
STATUS_CML	0x7E		R Byte	Reg		N	
READ_VIN(9bit)	0x88	1. 9bits ,108mV LSB	R Word	Direct	V	N	
READ_IIN(9bit)	0x89	1. 9bits, LSB=66.7mA	R Word	Direct	V	N	
READ_VOUT(9bit)	0x8B	Read FB voltage, 9 bits. LSB=3mV. Vout=FB voltage*FB divider ratio	R Word	Direct	V	N	
READ_IOUT(9bit)	0x8C	1. 9bits, LSB=66.7mA	R Word	Direct	A	N	
READ_TEMPERATURE(10bit)	0x8D	10bits. LSB=1C	R Word	Direct	degC	N	

MFR Command Description

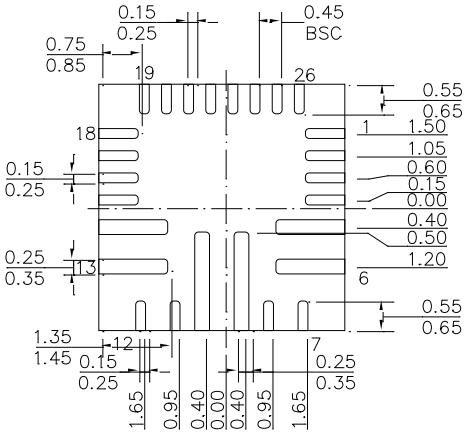
CMD Name	CMD Code	Description	Type	Data Format	Units	MTP	Default Value
MFR_ADDRESS(4bit)	0XD0	High 4-bit pmbus address	R/W Byte	Reg		Y	00
MFR_DITHER_CTRL(8bit)	0xD1		R/W Byte	Reg		Y	00
MFR_VOUT_CTRL(5bit)	0xD2		R/W Byte	Reg		Y	1Ah
MFR_VOUT_TRAN_RATE(3bit)	0xD3		R/W Byte	Reg		Y	04h
MFR_FREQ_SWITCH(3bit)	0xD4		R/W Byte	Reg		Y	03h
MFR_PHASE_CTRL	0xD5		R/W Byte	Reg		Y	00h
MFR_COMP1_CTRL	0xD6		R/W Byte	Reg		Y	40h
MFR_COMP2_CTRL	0xD7		R/W Byte	Reg		Y	2Ah
MFR_SLOPE_CTRL	0xD8		R/W Byte	Reg		Y	00h
MFR_HYS_CTRL	0xD9		R/W Byte	Reg		Y	00h
MFR_PWM_CTRL	0xDA		R/W Byte	Reg		Y	11h
MFR_GPIO_CTRL	0xDB		R/W Byte	Reg		Y	00h
MFR_GPIO_MODE	0xDC		R/W Byte	Reg		Y	00h
MFR_PRODUCT_ID	0xDD		R/W Byte	Reg		Y	00h
MFR_PRODUCT_VERSION	0xDE		R/W Byte	Byte		Y	00h
MFR_USER_VERSION	0xDF		R/W Byte	Reg		Y	00h
MFR_OC_FAULT_LIMIT	0xE0		R/W Byte	Reg		Y	53h
MFR_OC_RESPONSE	0xE1		R/W Byte	Reg		Y	BCh
MFR_VIN_OV_FAULT_RESPONSE	0xE2		R/W Byte	Reg		Y	A0h
MFR_VOUT_OV_ FAULT_LIMIT	0xE3		R/W Byte	Reg		Y	00h
MFR_VOUT_OV_ FAULT_RESPONSE	0xE4		R/W Byte	Reg		Y	C0h
MFR_VOUT_UV_ FAULT_LIMIT	0xE5		R/W Byte	Reg		Y	01h
MFR_VOUT_UV_ FAULT_RESPONSE	0xE6		R/W Byte	Reg		Y	BCh
MFR_OT_FAULT_LIMIT	0xE7		R/W Byte	Reg		Y	96h
MFR_RAIL_ADDRESS(8bit)	0xE8		R/W Byte	Reg		Y	00h
MFR_LIGHT_CTRL	0xE9		R/W Byte	Reg		Y	09h
MFR_PWR_STAGE_SET	0xEA		R/W Byte	Reg		Y	00h

PACKAGE INFORMATION

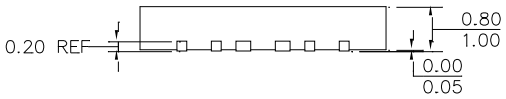
QFN26 (5×5mm)



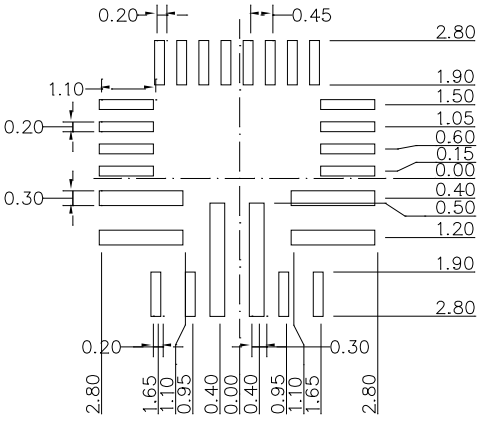
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERNS OF PIN5,PIN6 AND PIN13,PIN14 HAVE THE SAME LENGTH AND WIDTH.
2) LAND PATTERNS OF PIN9,PIN10 HAVE THE SAME LENGTH AND WIDTH.
3) ALL DIMENSIONS ARE IN MILLIMETERS.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) REFERENCEIS MO-220.
6) DRAWING IS NOT TO SCALE.