MP5515 Capacitor Health Measurement Accuracy andRecommendedMethod

Application Note

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ABSTRACT

This application note discussesthe MP5515back-up capacitor measurementaccuracy and recommended capacitance measurement method.

The first section of this application note introducesthe back-up capacitor test measurement accuracy. The impactof the keyparameters, which contribute to the overall capacitance accuracy, will be discussed.Based on this understanding, an equation to calculate the capacitance is provided.The second section of this application note provides arecommendedsystem capacitance measurement methodto achieve better accuracy of the capacitance, which may decrease due to aging or other reasons.

INTRODUCTION

The MP5515 is a wide2.7-18Vinput, 5A, high-efficiency,bidirectional power back-upmanager with integrated hot swap, I^2C, and ADC. The MP5515 integrates a back-up capacitor health test feature. Target applications include SSDs, NVDIMMs, and other power back-up systems. Forenterprise SSD applications, the back-up capacitor provides energy to the system when a power outage occurs during data consolidation. The capacitance must be large enough to support long enough back-up times for the system. The capacitance may possibly decrease due to aging,extreme operating environments, or other conditions. The capacitance health test feature provides a method to monitor the capacitance during operation and ensure that the system is robust under different conditions.

CAPACITANCE TEST PROCESS OF THE MP5515

The capacitance test process is initiated by setting an internal “Start Cap Test” bit. Once this bit is set, the whole capacitance test process is conductedautomatically.

Boost charging mode is disabled first, and the external discharge resistor is connected to the STRG pin to discharge the storage voltage. The internal timer starts to count the discharge time when discharging occurs. Once the storage voltage drops to the PGS threshold,the discharging resistor is disconnected from the storage capacitor. The whole discharging process is now finished.

The initial and final storage voltages are stored in specific registers. The discharging time is also stored in the discharging timer register.

After the process is done, the MP5515 issues an interrupt I/O signal to inform the system, and thesystem is able to access the registers to read the related parameters to calculate the capacitance.

The typical waveform of the discharge process is shown in Figure 1.

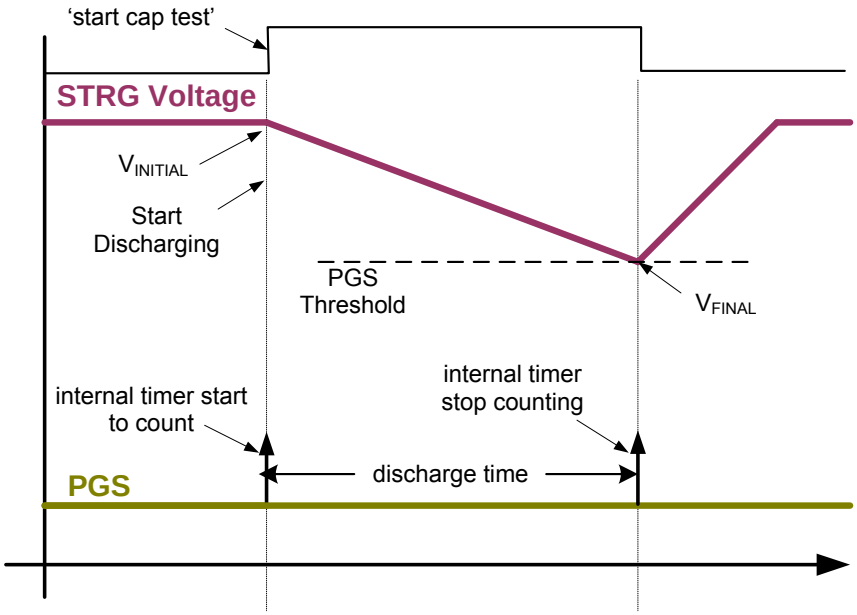

Figure 1: Back-Up Capacitor Discharging Process

ANALYSIS OF THE CAPACITANCE CALCULATION EQUATION

By using the above process, the ideal capacitance equation can be derived with Equation (1):

$$C_{Back-up}(\mu F) = \frac{Time}{R_{DISH} \times \ln(\frac{V_{INITIAL}+R_{DISCH}\times I_{LDO}}{V_{FINAL}+R_{DISCH}\times I_{LDO}})} \quad (1)$$

Where$V_{INITIAL}$ is V_{STRG} before the discharge timer starts(in V), $V_{FINAL}$is V_{STRG} after the discharge completes(in V), R_{DISCH} is the discharge resistance between STRG and RTEST(in kΩ), Time is the discharge time of V_{STRG}discharging from $V_{INITIAL}$ to V_{FINAL}(in ms), and I_{LDO} is the VCC LDO drawing currentfrom VSTRG if it is enabled, which istypically 2mA±2%.

The overall calculated capacitance accuracy is determined by all of the parameters given above.

The discharging time or the discharging timer is the key parameter for overall accuracy. The clock of the timer is generated from an integrated oscillation circuit. The variation of the internal oscillation circuit parameters (like R, C, current mirror matching, etc.)is similar to variations of each LSB of the timer. From our test data based on three lots, the variation of the internal time LSB is around ±8%.

The external discharging resistor accuracy is another factor contributing to the overall capacitance accuracy. Using a highly accurate discharge resistor,typically in the range of ±1%, is recommended in system designs.

The internal I_{LDO} hasa ±2% variation if it is disabled. For 12V applications, the internal LDO does not need to be enabled. The internal LDO is used to improve ADC performance in 3.3V applications.

The internalADC reading has a ±1% error.

The overall capacitance measure accuracy is mainly determined by the parameters given above.

Based on test variation data and that of the external components, the typical variation of the above key parameters is listedin Table 1.

Table1: Typical Variation of Key Parameters

	Timer	R_{DISH}	$V_{INITIAL}$&V_{FINAL}	Overall Accuracy
Tolerance	±8%	±1%	±1%	±9.0%

Considering the accuracy of the above parameters, the error of the calculated back-up capacitancevalue is in ±9% range, which is mainly caused by the part-to-part timer error.

RECOMMENDED CAPACITANCE TEST METHOD

The main variation is from the part-to-part timer error. For each specific part, the parameters, such as the internal clock frequency, do not change. This can be leveraged to have an indirect method for evaluating the capacitance fromthe system perspective to improve test accuracy.

For every fresh system start with a fresh capacitor, the system is recommended to conduct the capacitance test once or several times and store the timer or the calculated capacitance into the non-volatile memory. The stored timer or the calculated capacitance can be used as the reference for the capacitance test later. Periodically, the system conducts the capacitance. The future-tested timer or calculated capacitance is compared with the stored reference.

With age or the system running at extreme conditions, the capacitance of the back-up capacitor may decrease. When the tested value is compared with the reference value, the system can determine how much capacitance has decreased during operation.

The accuracy of using this method can be calculated with Equation (2):

$$\frac{C'_{Back-up}-C''_{Back-up}}{C'_{Back-up}} = 1 - \frac{Time''}{Time'} \times \frac{R'_{DISH}}{R''_{DISH}} \times \frac{\ln(\frac{V'_{INITIAL}}{V'_{FINAL}})}{\ln(\frac{V''_{INITIAL}}{V''_{FINAL}})} \quad (2)$$

Where$Parameter'$denotes the parameters for first test result, and $Parameter''$denotes the parameters for further testresults.

In normal conditions, the error of the timerand RDISH does not change with each specific part. The error can be eliminated through this method.

The only concern is when the above parameters are changed over time or over temperature. Through the internal test, before and after 1000 hours of burn-in testing, the internal timer has almost no shift at all, well below 0.1%. Similarly, in the temperate range of 0°C to 85°C, the shift of the timer is below ±1% (see Table 2).

Table2: The Typical Variation of Key Parameters vs. Time/Temperature

	Timer	R_{DISH}	Overall Error Over Time and Over Temperature
Over time variation	<±0.1%	0	<±0.1%
Over temp variation (0°C to 85°C)	<±1%	0	<±1%
Test overall error	<±1.1%	0	<±1.1%

Based on the above data, storing the fresh capacitance and using that as a reference achieves <1.1% of overall accuracy.

CONCLUSION

With the internal clock variation and external discharge resistance variation, etc., the capacitance variation is calculated to be around ±9% from part to part and from design to design.

This application note discussed a recommended test method to provide better accuracy for capacitor health monitoring.