MP4653 Real LIPS

Pure 2-stage CC/CV Mode LED Driver Application Note

Prepared by Bairen Liu

May, 2012

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

ABSTRACT

The MP4653 is high-performance pure 2-stage CC/CV mode LED driver specially designed for isolated high-power application, such as TV LED backlighting. It is a system solution for the LED driver and system power supply. As shown in figure 1, the MP4653 provides a simple 2-stage solution for the LED driver. It regulates the current through the TV LED and also controls a DC supply voltage for the system power supply.

Comparing with the traditional 3-stage solution as shown in figure 2, it saves components and improves the efficiency.

Comparing with a normal 2-stage structure as shown in figure 3, the MP4653 solution integrates the flyback DC/DC stage to the LLC stage and thus improves the efficiency. What's more, the MP4653 solution can eliminate the audio noise during PWM dimming which attempts to be a big issue in the normal 2-stage solution, as the MP4653 LLC stage outputs both the LED driver and a DC supply voltage for the system power supply, which results in a continuous power through the MP4653 LLC stage.

This application note describes the concept how the MP4653 eliminates audible noise, the MP4653 operation functions, the application information and a design example for the MP4653.

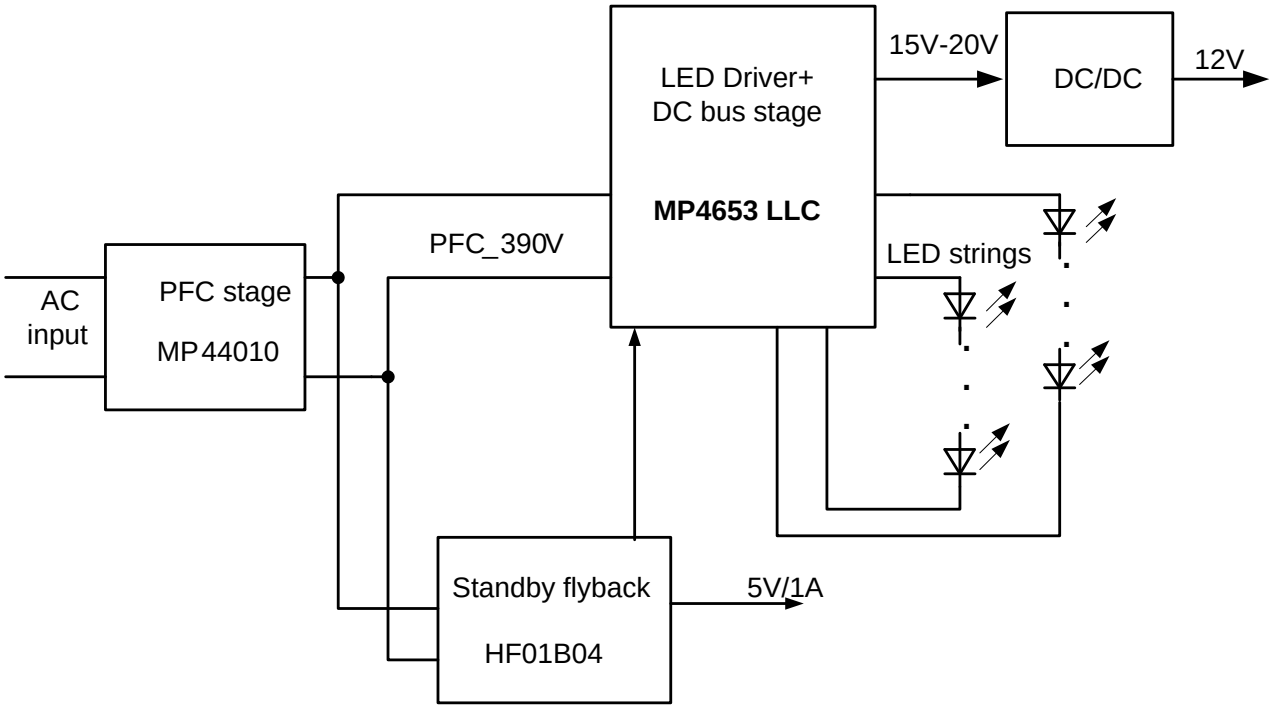


Figure 1— MP4653-Based 2-stage TV LED Driver Power Structure

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

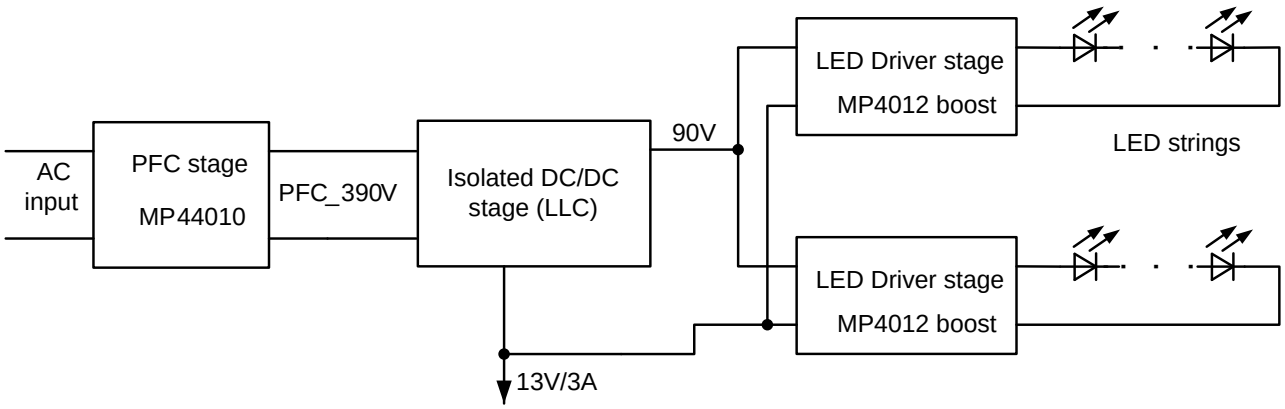


Figure 2—Traditional 3-stage TV LED Driver Power Structure

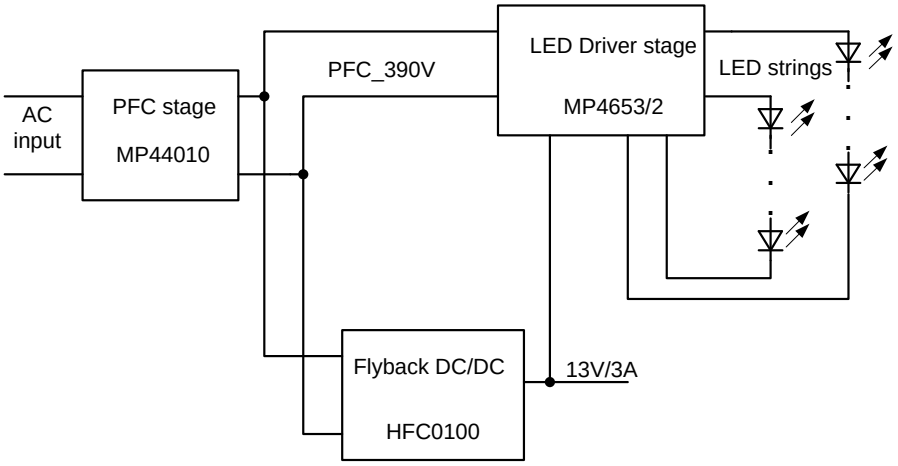


Figure 3— A Normal 2-stage TV LED Driver Power Structure

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

INDEX

1. Introduction 5
2. Audible noise elimination 9
    2.1 Audible Noise Origins 9
    2.2 Issues with the 2-Stage Solution and the Discontinuous Gate Drive during PWM Dimming 9
    2.3 Concept of MP4653 Audible Noise Elimination 10
3. Operation and pin description 16
    3.1 Operation 16
    3.2 Pin Description 19
4. application example and desing procedure 30
    4.1 Specification 30
    4.2 Schematics 31
    4.3 Power Stage Design 32
    4.4 Control Circuit Design 48
    4.5 Test Results 53

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

1. INTRODUCTION

The MP4653 is a CC/CV mode LLC TV LED driver for LED backlighting, especially for large size TV LED backlighting. Powered by 9V to 30V input supplies, the MP4653 outputs two 180 degree phase shifted driving signals for the external power stages. Its enhanced 9V gate driver provides adequate driving capability and can directly drive the external MOSFETs through an external gate driving transformer.

The MP4653 integrates a constant current control loop for the LED current regulation and also a constant voltage control loop for the DC bus voltage, which is used to generate system power supplies like 12V/5V with other DC/DC converters. The CC/CV control loop programs the operating frequency of the LLC power stage and thus regulates the LED current and also the bus voltage.

The MP4653 incorporates both analog dimming and PWM dimming to the LED current. A driving signal is output to directly drive the dimming MOSFET, which helps to achieve fast and high contrast ratio PWM dimming.

The PWM dimming signal is also used for the CC/CV mode control. At PWM on interval, the CC mode is effective and the LED current is regulated; at PWM off interval, the CV mode is effective and the DC bus voltage is regulated. The gate driving signal and thus the energy through the power stage are continuous at both the PWM on interval and the PWM off interval. This helps to eliminate the system audible noise at PWM dimming.

The MP4653 features sufficient and smart protection to increase system reliability. It protects the fault condition at both the DC bus stage and the LED driver stage.

The protection for the DC bus stage includes the over voltage protection and over current protection (short protection).

The protection for the LED driver stage includes the open LED protection, short LED protection, over LED current protection and any point of LED string short to ground protection.

Thermal protection is integrated in MP4653. The MP4653 is available in SOIC20 package.

Figure 4 shows a typical application circuit of MP4653 LLC for TV LED Driver, it drives the LED and outputs a DC bus voltage for the system power supply. The MP4653 can directly support 1 string, 2 string and 4 string LED application. Figure 5 shows the block diagram of MP4653.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

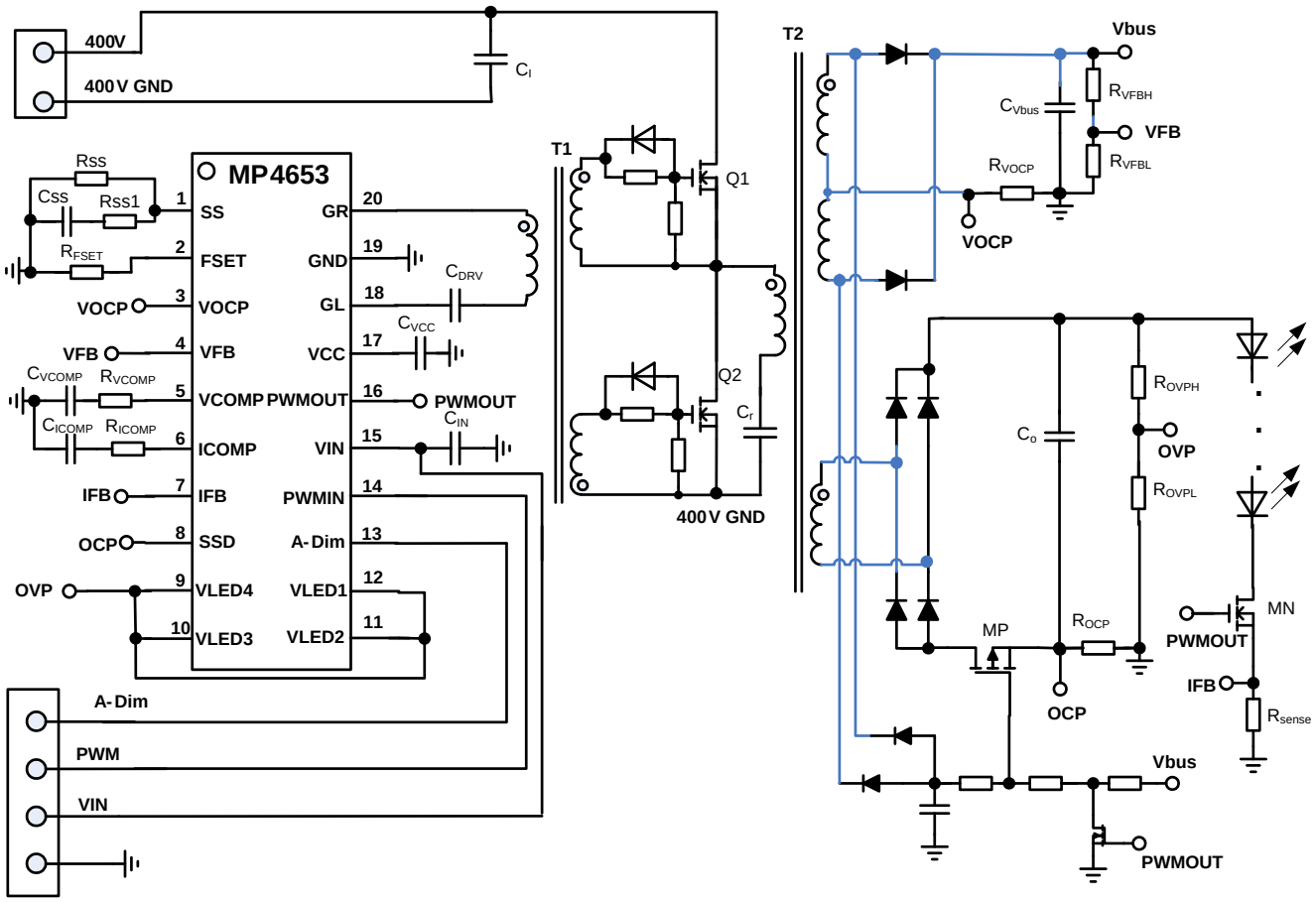


Figure 4— MP4653 LLC TV LED Driver

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

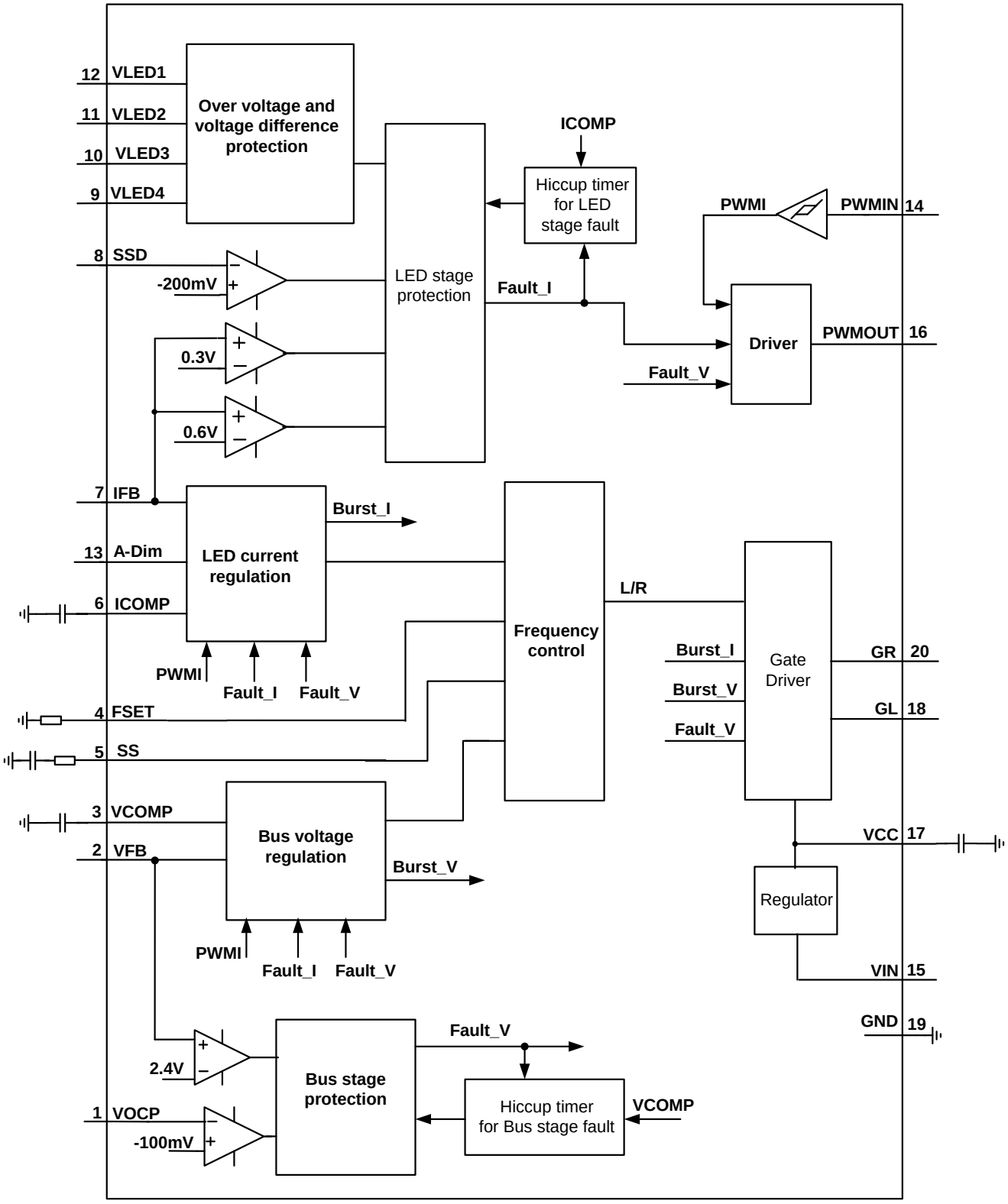


Figure 5—MP4653 Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

The MP4653 has the following features that make it perfect for TV LED backlighting.

- Secondary Side Pure 2-stage LLC Controller
- CC/CV Mode Frequency Control Loop
- Audible Noise Elimination
- 0% to 100% Analog Dimming
- 500:1 PWM dimming ratio
- DC Bus Output Over Voltage Protection
- DC Bus Short Protection
- System Auto-recovery and Hiccup Timer
- LED Open, Short Protection
- LED Output Over Voltage, Over LED Current Protection
- Any Point of LED String Short to GND Protection

In the TV LED backlighting application, the audible noise becomes an obvious issue when in PWM dimming mode. The MP4653-based pure 2-stage solution eliminates audible noise and improves system performance.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

2. AUDIBLE NOISE ELIMINATION

Many TV LED drivers use PWM dimming to limit the LED current. However, the dimming frequency is usually in the audible range and leads to audible noise issues.

2.1 Audible Noise Origins

The audible noise usually originates from magnetic components—such as transformers and inductors—vibrating as the current flowing through the winding induces a force against the core. As shown in Figure 6, during PWM dimming, if the output power of the LED driver is discontinuous then the current through the transformer is also discontinuous, which introduces a fluctuating mechanical force that leads to audible vibrations.

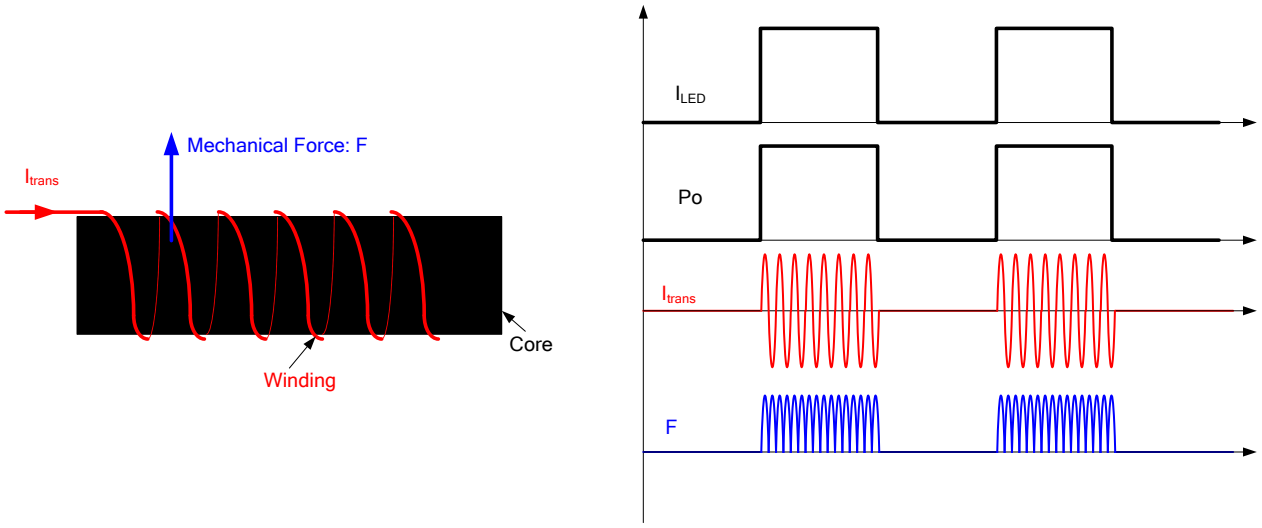


Figure 6—Transformer Current and Mechanical Force during PWM Dimming

2.2 Issues with the 2-Stage Solution and the Discontinuous Gate Drive during PWM Dimming

Figure 7 shows an operating waveform for a typical 2-stage solution with a discontinuous gate drive during PWM dimming. It uses fast PWM dimming, where the LED current responds quickly with the PWM dimming signal, and can achieve a high PWM dimming ratio. However, there is an audible noise issue with the power transformer because the resulting current through the transformer is discontinuous.

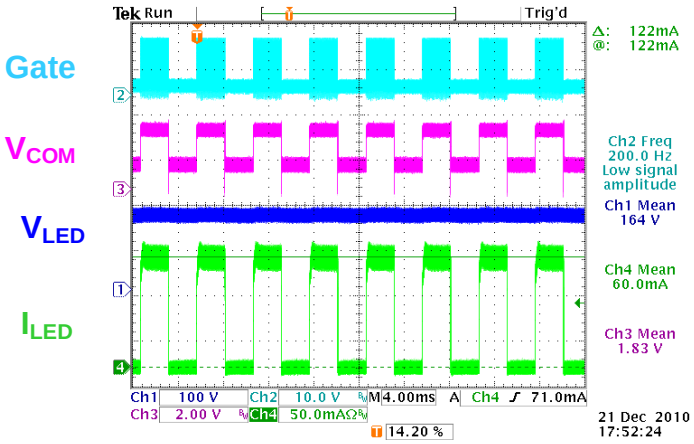


Figure 7—Operating Waveforms for a 2-Stage Solution with Discontinuous Gate drive and Fast PWM Dimming

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

Figure 8 shows a different operating waveform. It uses soft PWM dimming to reduce the audible noise: The LED current responds slowly to PWM dimming signal, and the transformer current reflects the LED current. This gradual current change means a reduction (not elimination) in the audible noise. However, the gradual transition reduces the dimming ratio, and the minimum PWM dimming duty cycle is only 10% to 15%.

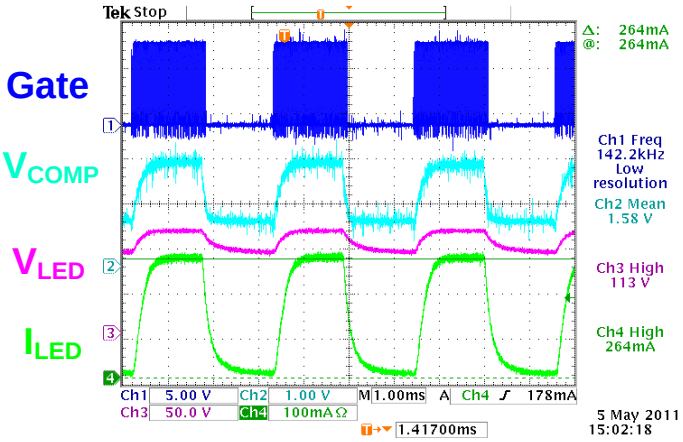


Figure 8— Operating Waveforms for a normal 2-stage solution with Discontinuous Gate drive and Soft PWM Dimming

As a result the normal 2-stage structure must trade off between audible noise and a lower PWM dimming ratio.

2.3 Concept of MP4653 Audible Noise Elimination

The MP4653 LLC stage outputs both the LED driver and a DC bus voltage for the system power supply. At PWM on interval, the CC control loop is effective and the LED current is regulated; at PWM off interval, the CV loop for the DC bus voltage regulation is effective. Therefore, MP4653 LLC stage outputs a continuous power at PWM on interval and PWM off interval. The power through the transformer or the current through the transformer is continuous. This eliminates the audible noise.

The MP4653 outputs a continuous gate drive signal for the LLC power stage at PWM on interval and PWM off interval. On the other hand, the MP4653 outputs a dimming gate signal for the external dimming MOSFET in series with the LED string for fast PWM dimming and high PWM dimming ratio. Figure 9 shows the control scheme of MP4653 LLC stage. At PWM on interval, the internal control voltage which determines the operating frequency follows the ICOMP voltage which is the output of the CC control loop (LED current control loop). The LED stage is turned on and the output power is high. The IC outputs a low operating frequency to deliver a larger power. The current through the transformer is a little larger. At PWM off interval, the internal control voltage follows the VCOMP voltage which is the output of the CV control loop (DC bus stage control loop). The LED stage is turned off and only the DC bus stage outputs power. The IC operates at a little higher operating frequency and delivers a relatively smaller power to the output. The current through the transformer is also relatively smaller.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

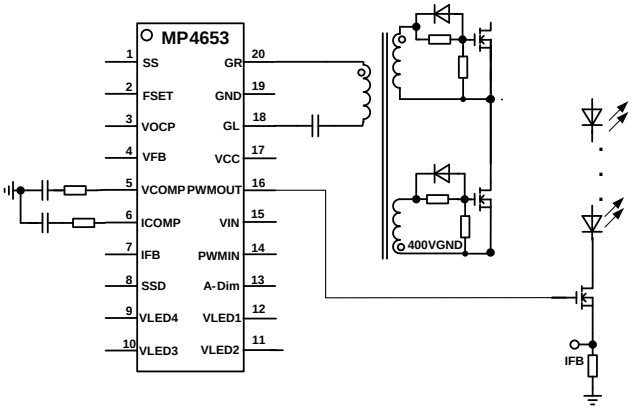


Figure 9A

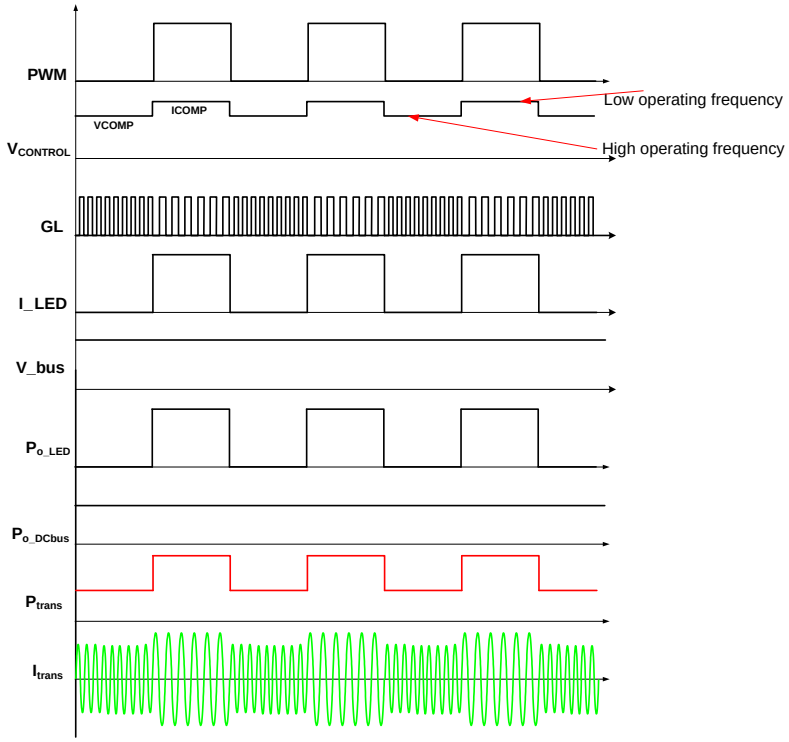


Figure 9B

Figure 9—MP4653 Control Scheme

As the current through the transformer at PWM on interval and PWM off interval determines the audible noise performance, following estimates the current through the transformer.

Figure 10 shows the LLC power stage of an MP4653-controlled TV LED driver and its equivalent circuit. The resonant capacitor (C_r), the leakage inductance of the power transformer (L_k), and the magnetic inductance of the power transformer (L_m) compose the LLC network. The LED load on the secondary side n_2 represented as an equivalent load resistor R_{e_LED}, and the DC bus load on the secondary side n_3 represented as an equivalent load resistor Re_Bus, as shown in figure 9B. The equivalent resistors are:

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

$$R_{e_LED} = \frac{8n_1^2(V_{LED} + 2V_{D_LED})^2}{\pi^2 n_2^2 P_{o_LED}(\frac{V_{LED} + 2V_{D_LED}}{V_{LED}})} = \frac{8n_1^2(V_{LED} + 2V_{D_LED})V_{LED}}{\pi^2 n_2^2 P_{o_LED}} \quad (2\text{-}1)$$

$$R_{e_Bus} = \frac{8n_1^2(V_{bus} + V_{D_Bus})^2}{\pi^2 n_3^2 P_{o_Bus}(\frac{V_{bus} + V_{D_Bus}}{V_{bus}})} = \frac{8n_1^2(V_{bus} + V_{D_Bus})V_{bus}}{\pi^2 n_3^2 P_{o_Bus}} \quad (2\text{-}2)$$

$$\frac{n_3}{n_2} = \frac{(V_{bus} + V_{D_Bus})}{(V_{LED} + 2V_{D_LED})} \quad (2\text{-}3)$$

Where the P_{o_Bus} is the output power of the DC bus, the P_{o_LED} is the output power of the LED strings, V_{LED} is the average voltage of the LED strings, V_{D_LED} is the voltage drop on the rectifier diode in the LED stage and the V_{D_Bus} is the voltage drop on the rectifier diode in the DC bus stage.

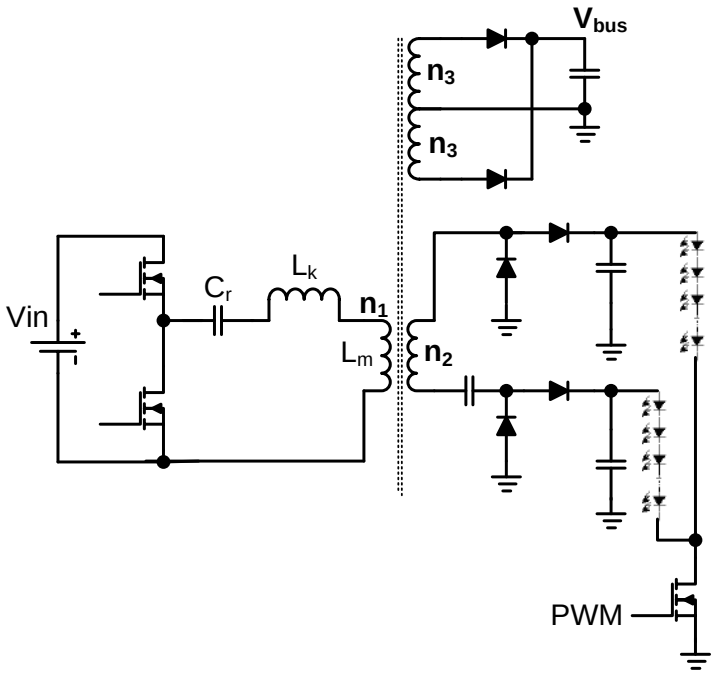


Figure 10A—MP4653 LLC Power Stage

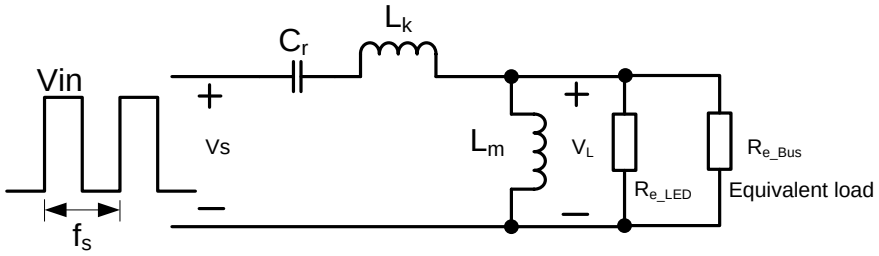


Figure 10B—Equivalent Circuit of MP4653 LLC Power Stage

Figure 10—MP4653-based LLC Power Stage and Its Equivalent Circuit

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

The quality factor (Q) of the LLC network is:

$$Q = \sqrt{L_k / C_r}\left(\frac{1}{R_{e_LED}} + \frac{1}{R_{e_Bus}}\right) \quad (2\text{-}4)$$

The LLC network gain is:

$$Gain(f) = \left|\frac{V_L}{Vs}\right| = \left|\frac{\dfrac{1}{\dfrac{1}{j2\pi f L_m} + \dfrac{1}{R_{e_LED}} + \dfrac{1}{R_{e_Bus}}}}{\dfrac{1}{\dfrac{1}{j2\pi f L_m} + \dfrac{1}{R_{e_LED}} + \dfrac{1}{R_{e_Bus}}} + j2\pi f L_k + \dfrac{1}{j2\pi f C_r}}\right| = \left|\frac{L_n \dfrac{f^2}{f_0^{\,2}}}{L_n \dfrac{f^2}{f_0^{\,2}} + \left(\dfrac{f^2}{f_0^{\,2}} - 1\right)\left(\dfrac{f}{f_0} + 1 + j\dfrac{f}{f_0} L_n Q\right)}\right| \quad (2\text{-}5)$$

Where:

$$f_0 = \frac{1}{2\pi\sqrt{L_k C_r}} \quad (2\text{-}6)$$

$$L_n = \frac{L_m}{L_k} \quad (2\text{-}7)$$

At PWM off interval, the LED stage is cut off from the power stage, and its equivalent resistor Re_LED is deleted or say is ∞, the quality factor at PWM off interval is then:

$$Q_{PWM_off} = \frac{\sqrt{L_k / C_r}}{R_{e_Bus}} \quad (2\text{-}8)$$

The gain of the LLC network at PWM off interval is got by replacing Q with Q_{PWM_off} in (2-5).

$$Gain_{PWM_off}(f) = \left|\frac{L_n \dfrac{f^2}{f_0^{\,2}}}{L_n \dfrac{f^2}{f_0^{\,2}} + \left(\dfrac{f^2}{f_0^{\,2}} - 1\right)\left(\dfrac{f}{f_0} + 1 + j\dfrac{f}{f_0} L_n Q_{PWM_off}\right)}\right| \quad (2\text{-}9)$$

Assuming for a typical application, the output power of the LED stage P_{o_LED}=60W, the output power of the DC bus stage P_{o_Bus}=30W, the designed quality factor Q=0.3, Ln=4 and the operating frequency at PWM on interval $f_{s_PWM_on}=0.8f_0$. From (2-1) to (2-3), if neglecting the voltage drop on the rectifier diodes, the equivalent resistor is inversely proportional to the output power.

$$\frac{R_{e_LED}}{R_{e_Bus}} \approx \frac{P_{o_Bus}}{P_{o_LED}} = 0.5 \quad (2\text{-}10)$$

Then the quality factor at PWM off interval $Q_{PWM_off} \approx Q/3 = 0.1$.

Figure 11 shows the gain curve of the LLC network at PWM on interval and PWM off interval, where the blue line is the gain during the PWM-ON interval and the red curve is the gain during PWM off interval. As the voltage on the DC bus is regulated the same at PWM on interval and PWM off interval, the two gain curves should have a same value at PWM on interval and PWM off interval. Then from (2-5) and (2-9), the operating frequency at PWM off interval is around $f_{s_PWM_off}=0.81f_0$, very close to the operating frequency at PWM on interval.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

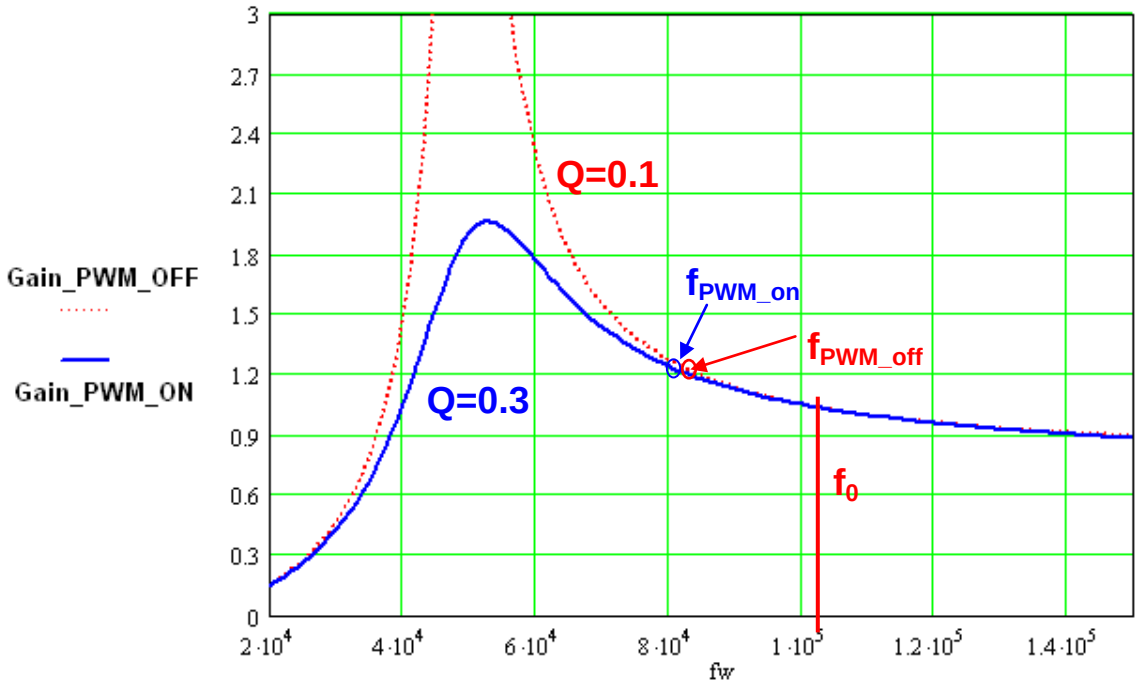


Figure 11—Gain Curves of MP4653 LLC Network During PWM ON and PWM OFF

The input impedance of the MP4653 LLC network as shown in figure 10B is:

$$Z_{in}(f)=\frac{1}{\frac{1}{j2\pi fL_m}+\frac{1}{R_{e_LED}}+\frac{1}{R_{e_Bus}}}+j2\pi fL_k+\frac{1}{j2\pi fC_r}=\sqrt{\frac{L_k}{C_r}}\left(\frac{jL_n\frac{f}{f_0}}{1+jQL_n\frac{f}{f_0}}+j\frac{f}{f_0}+\frac{1}{j\frac{f}{f_0}}\right) \quad (2\text{-}11)$$

The transformer current is:

$$I_{in}(f)=\frac{V_s}{|Z_{in}(f)|}=\frac{V_s}{\left|\sqrt{\frac{L_k}{C_r}}\left[\frac{jL_n*\frac{f}{f_0}}{1+jQL_n\frac{f}{f_0}}+j\frac{f}{f_0}+\frac{1}{j\frac{f}{f_0}}\right]\right|} \quad (2\text{-}12)$$

During PWM on interval, the current through the transformer is:

$$I_{in_PWM_ON}=\frac{V_s}{|Z_{in}(f_{S_PWM_on})|}=\frac{V_s}{2.01\sqrt{\frac{L_k}{C_r}}} \quad (2\text{-}13)$$

During PWM off interval, the current through the transformer could be got by replacing the f and Q in (2-12) with $f_{S_PWM_off}$ and Q_{PWM_off}:

$$I_{in_PWM_OFF}=\frac{V_s}{2.68\sqrt{\frac{L_k}{C_r}}} \quad (2\text{-}14)$$

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

From (2-13) and (2-14), the transformer current during the PWM-OFF interval is around 75% of the current during the PWM-ON interval. Therefore, the transformer currents of the MP4653 based LLC stage during PWM on interval and PWM off interval do not get much difference. This similar current through the transformer during PWM on interval and PWM off interval ensures the audible noise performance at the PWM dimming of the LED driver stage.
Summarizing, the MP4653-based LLC power stage has the following features:

(1) The MP4653 LLC stage drives the LED strings and also outputs a DC bus voltage for the system power supply.

(2) The MP4653 regulates the LED current during the PWM dimming on interval and controls the DC bus voltage during the PWM dimming off interval.

(3) The gate drive signals for the power switches and also the power through the transformer are continuous during PWM on interval and PWM off interval.

(4) The currents through the transformer during PWM on interval and PWM off interval do not get much difference. It eliminates the audible noise during PWM dimming which is observed a big issue in a normal 2-stage structure.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

3. OPERATION AND PIN DESCRIPTION

3.1 Operation

3.1.1. Steady State

The MP4653 is a CC/CV mode LLC TV LED driver, especially designed for the 2-stage structure for the large size TV LED backlighting. Powered by 9V to 30V input supplies, the MP4653 outputs two 180 degree phase shifted driving signals for the external power stages. Its enhanced 9V gate driver provides adequate driving capability and can directly drive the external MOSFETs through an external gate driving transformer.

Figure 12 shows the gate drive signal diagram. The gate drive signals GL and GR are 180° phase-shifted pulse waveforms with full duty cycle. Simultaneously running the signals GL and GR produces a symmetric pulse signal with both negative and positive values at the input of the gate drive transformer. The driver voltages on the two secondary-side windings are polar opposites of the same signal and drive the high-side and low-side power MOSFETs. The gate drive current from the MP4653 includes two parts: One is the pulse driving current for the power MOSFETs at switch-on and switch-off; the other is the magnetic current of the gate drive transformer. Use a magnetic inductor with a value greater than 2mH to limit this magnetic current.

The MP4653 employs frequency control for the LLC power stage. Both the LED current and the bus voltage are controlled.

The MP4653 includes an internal linear regulator VCC. It is the supply voltage for the gate driver and also for the internal circuit. The MP4653 features Under Voltage Lockout. The chip is disabled until VCC exceeds the UVLO threshold.

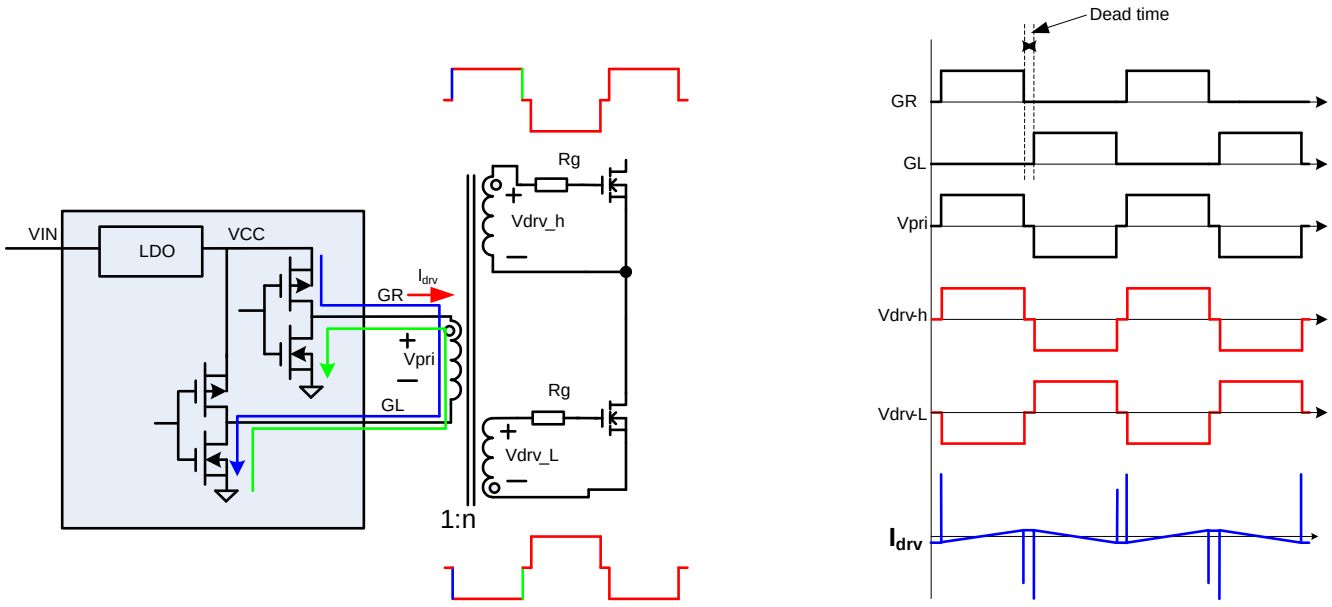


Figure 12—MP4653 Gate drive Signal Diagram

When the MP4653 is powered up, the VCC is charged up, and when it passes the UVLO threshold, IC starts up. It resets the voltage control loop, the current control loop and discharges the soft start capacitor. The MP4653 enjoys a soft start up.

The PWM dimming signal controls the start up of the LED driver stage. The system operates in constant voltage mode and the DC bus voltage is controlled before PWM signal applied.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

The start up sequence of the MP4653 power system is shown in figure 13. After the AC power is applied, the PFC output “400V bus” is charged up (PFC does not work yet), and then the standby power supply (5V) starts to work. This standby power supply will power up the MP4653 when it gets the order to turn on the system. The MP4653 outputs the gate drive signals for the LLC power stage and regulates the DC bus voltage (CV mode) when it is powered up. The MP4653 will change to CC mode to regulate the LED current when system applies a high level to PWMIN pin.

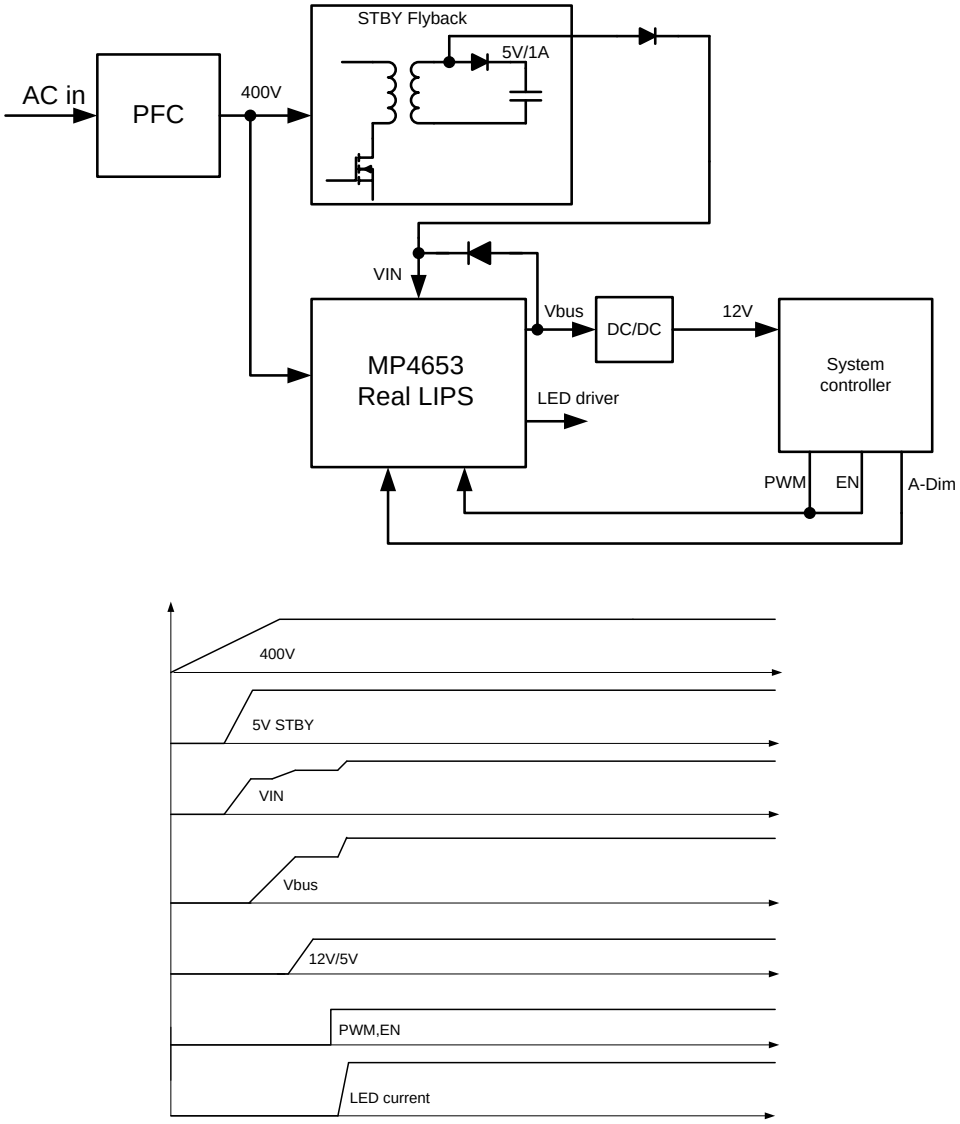


Figure 13—MP4653 Power System and Start Up Sequence

The MP4653 integrates a constant voltage control loop (CV) and a constant current control loop (CC), both the LED current and the bus voltage are controlled. The PWM dimming signal is used to distinguish these two modes. At PWM on interval, the current control loop is effective (CC mode) and the LED current is regulated. At PWM off interval, the voltage control loop is effective and the DC bus voltage is controlled (CV mode).

For the current control loop for the LED current regulation, the LED current is fed back to IFB pin. The internal error amplifier regulates the average value of IFB signal to the internal 200mV reference voltage. Its output is connected to the external current loop compensation network on ICOMP pin

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

through an inner switch S1. At PWM on interval, S1 is on, and the output of error amplifier is connected to the external compensation network on ICOMP pin. The LED current is regulated by this control loop. At PWM off interval, S1 is turned off, and the compensation network on ICOMP is disconnected from the error amplifier and holds its value until next PWM on interval. The output of the error amplifier is pulled low at PWM off interval.

MP4653 integrates burst mode for the LED current regulation. When IFB voltage is higher than 1.1 times of its reference voltage and the ICOMP voltage is sufficiently low (which means a highest operating frequency), the IC skips some switching cycles until IFB voltage decreases sufficiently.

For the voltage control loop for the bus voltage regulation, the bus voltage is fed back on VFB pin. MP4653 automatically samples the FB voltage at PWM on interval and uses it as the reference for the voltage control loop. The internal voltage-loop error amplifier regulates the average value of the VFB voltage to this reference voltage. Its output is connected to the external voltage loop compensation network on VCOMP pin through an inner switch S2. At PWM off interval, S2 is on, and the output of the voltage-loop error amplifier is connected to the external compensation network on VCOMP pin. The bus voltage is regulated by this control loop. At PWM on interval, S2 is turned off, and the compensation network on VCOMP is disconnected from the error amplifier and holds its value until next PWM off interval. The output of the voltage-loop error amplifier is pulled low at PWM on interval.

MP4653 also integrates burst mode for the voltage regulation. When VFB voltage is higher than 1.1 times of the reference voltage and the VCOMP voltage is sufficiently low (which means a highest operating frequency), the IC skips some switching cycles until VFB voltage decreases sufficiently.

The operating frequency is controlled by the larger one of the outputs of the current-loop error amplifier and the voltage-loop error amplifier. A high compensation output voltage gets a low operating frequency.

3.1.2. Dimming Control

The MP4653 provides two dimming methods: PWM Dimming Mode and Analog Dimming Mode. Applying a digital PWM signal on the PWMIN pin allows the PWM dimming. The brightness of the LED string is proportional to the duty cycle of the external PWM signal. A driving signal on PWMOUT pin is output to directly drive the dimming MOSFET in series with the LED string, which helps to achieve fast and high contrast ratio PWM dimming. The MP4653 can achieve 500:1 PWM dimming ratio at 200Hz. The PWM dimming ratio may get lower with a higher PWM dimming frequency.
The P-MOSFET which is used for protection of the LED stage is also controlled by the PWMOUT signal. The P-MOSFET is turned off and the LED stage is cut off at PWM off interval, and thus the LED stage voltage is hold and not influenced by the bus stage operation.
A DC analog signal from 0V to 1.2V on A-Dim pin dims the LED current amplitude from 0 to 100%. The MP4653 LLC stage can achieve much smaller analog dimming current comparing with a normal 2-stage LLC structure，as MP4653 LLC stage outputs the DC bus voltage as its “dummy load”.

For PWM and analog dimming control, apply the PWM dimming signal on PWMIN pin and apply the analog dimming signal on A-dim pin.

3.1.3. DC Bus Voltage Stage Protection

The MP4653 features rich and smart protection to increase system reliability. It protects the fault condition at both the DC bus voltage stage and the LED driver stage.
The protection for the DC bus voltage stage includes the over voltage protection and over current protection (short protection).
The VFB pin senses the bus stage voltage for voltage regulation and also for over voltage protection. When the VFB pin voltage gets higher than 2.4V for 2us, IC triggers the Bus Voltage Stage Protection.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

The secondary side current of bus voltage stage is sensed on VOCP pin. When VOCP voltage gets lower than -100mV, IC triggers the Bus Voltage Stage Protection.
At Bus Voltage Stage Protection, the whole gate driving signals are disabled and no power is delivered to the output, including both the DC bus voltage stage and the LED driver stage. The current loop compensation node ICOMP pin and the soft start SS pin are pulled low. The bus voltage stage hiccup timer starts. The voltage loop compensation node VCOMP pin is disconnected from the internal amplifier and holds its value until the fault condition disappears. A 2uA current source charges the VCOMP pin capacitor till VCOMP voltage hits 3V, and then a 2uA current source discharges VCOMP pin until 0.45V and then the system recovers.

3.1.4. LED Driver Stage Protection

The fault protection for the LED driver stage includes the open LED protection, short LED protection, over LED current protection and any point of LED string short to ground protection.
The voltage of the LED strings are sensed on VLED1~VLED4 pins. The maximum value of VLED1~VLED4 and their voltage difference are used for protection. When the maximum value of VLED1~VLED4 gets higher than 2.4V or their voltage difference get larger than 120mV (this value can be adjusted by the external input resistance on VLED# pins), IC triggers the LED Driver Stage Protection.
The LED current feedback IFB is also used for over LED current protection. When IFB voltage gets higher than 300mV for 200us or when IFB voltage gets higher than 600mV, IC triggers the LED Driver Stage Protection.
The secondary side current of the LED driver stage is sensed on SSD pin. When SSD pin voltage gets lower than -200mV for 2us, IC triggers the LED Driver Stage Protection.
At the LED Driver Stage Protection, the driving signal for the dimming MOSFET is disabled to turn off the dimming MOSFET and also to disconnect the LED driver stage from the power stage. The current loop compensation node ICOMP is disconnected from the internal amplifier and holds its value until the fault condition on the LED driver stage disappears. A 2uA current source charges the ICOMP pin capacitor till ICOMP voltage hits 3V, and then a 2uA current source discharges ICOMP pin until 0.45V and then the LED driver stage recovers.
During the LED driver stage protection, the gate drive signals for the MOSFETs in the power stage are continuous and the DC bus voltage is regulated. Therefore, the system power supplies are not influenced by the fault protection of the LED driver stage.
Thermal protection is integrated in MP4653.

3.2 Pin Description

3.2.1 Pin 1(SS), Pin 2 (FSET):

These two pins are used for frequency set and soft start. The figure 14 shows the scheme of MP4653 frequency set and soft start. The sourcing current through the SS pin and the FSET pin determines the operating frequency. At normal operation, the SS pin is connected to an internal 1.5V voltage source; at fault condition of the DC bus stage, the SS pin is pulled low. The FSET voltage is connected to the CC control loop ICOMP during PWM on interval at normal operation and is connected to the CV control loop VCOMP during PWM off interval or at LED stage fault condition. The operating frequency is calculated as:

$$f_{op} = (2I_{SS} - I_{FSET}) \times 1.98 \times 10^9 \quad (3\text{-}1)$$

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

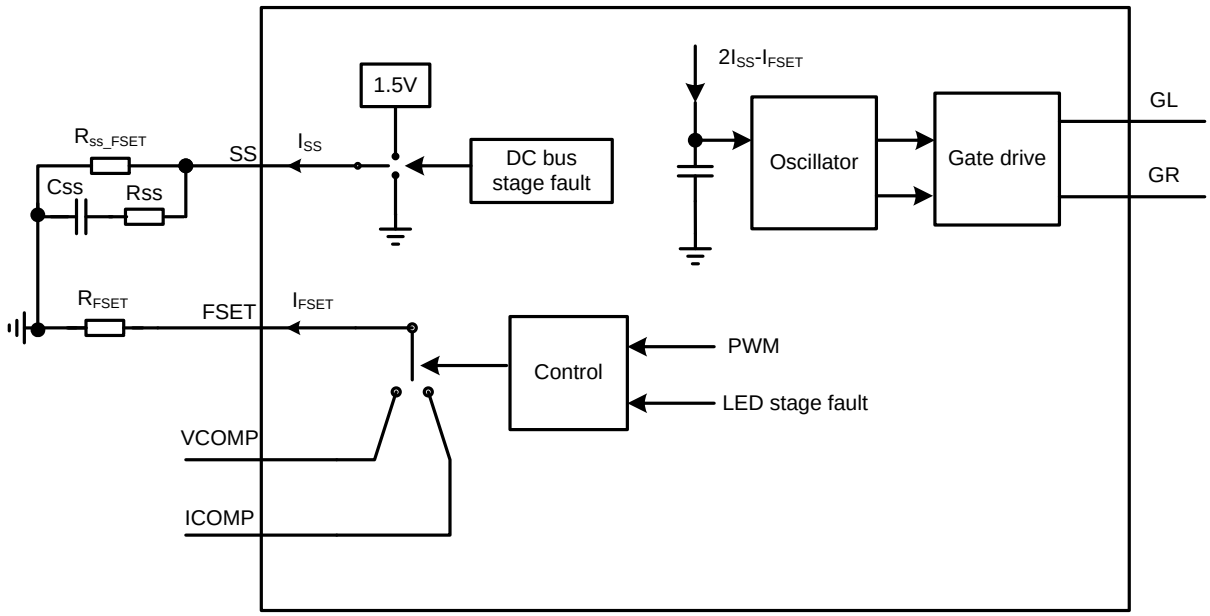


Figure 14—MP4653 Frequency Set and Soft Start

At stable operation, the soft start RC network on SS pin is charged up and the operating frequency is:

$$f_{op} = (\frac{2\times 1.49V}{R_{SS_FSET}} - \frac{V_{FSET}}{R_{FSET}})\times 1.98\times 10^9 \quad (3\text{-}2)$$

The FSET voltage is determined by the CC and CV control loop, and the voltage of the compensation outputs VCOMP and ICOMP are in range of 1V to 2.2V. The maximum stable operating frequency occurs when VCOMP or ICOMP is at its minimum voltage, that is:

$$f_{max} = (\frac{2\times 1.49V}{R_{SS_FSET}} - \frac{1V}{R_{FSET}})\times 1.98\times 10^9 \quad (3\text{-}3)$$

The minimum stable operating frequency occurs when VCOMP or ICOMP is at its maximum value, that is:

$$f_{min} = (\frac{2\times 1.49V}{R_{SS_FSET}} - \frac{2.2V}{R_{FSET}})\times 1.98\times 10^9 \quad (3\text{-}4)$$

At start up, the capacitor on SS pin should be charged up firstly by an extra sourcing current through SS pin. It results in a high frequency at start up and achieves soft start up for the LLC power stage. The start up frequency is:

$$f_{s_start} = (\frac{2\times 1.49V\times (R_{SS_FSET}+R_{SS})}{R_{SS_FSET} * R_{SS}} - \frac{1V}{R_{FSET}})\times 1.98\times 10^9 \quad (3\text{-}5)$$

The soft start process continues until the capacitor of the RC network on SS pin is fully charged up. The soft start time is determined by the RC Constant on SS pin, and it can usually be estimated with 3 times of the RC Constant.

$$T_{SS} \approx 3\times R_{SS}\times C_{SS} \quad (3\text{-}6)$$

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

At fault condition of the DC bus voltage stage, the SS pin is pulled low and system enjoys a soft start up when it recovers from the DC bus voltage stage fault condition.

At LED stage fault condition, the SS pin voltage does not change, and system operates at a frequency determined by the CV control loop.

3.2.2 Pin 3(VOCP):

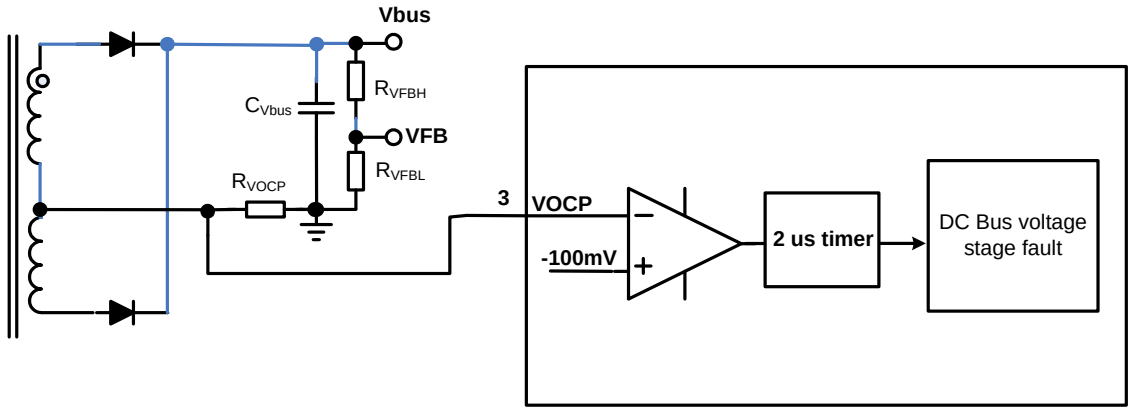


Figure 15—MP4653 VOCP Pin Function for Over Current Protection of DC Bus Voltage Stage

This pin is for the over current protection for the DC bus voltage stage. The voltage on this pin is compared with an internal -100mV threshold voltage. If the voltage on this pin gets smaller than -100mV for 2us, IC triggers the DC bus voltage stage fault protection. For a typical application, the current though the DC bus voltage stage is sensed to VOCP pin though a resistor R_{VOCP} with a negative polarity. When the current through the DC bus voltage stage gets large or short condition occurs, the voltage on VOCP pin get more negative and triggers the protection threshold.

The protection point of the current through the DC bus voltage stage is:

$$I_{OCP_Bus} = \frac{100mV}{R_{VOCP}} \quad (3\text{-}7)$$

This protection point could usually be around 1.5 to 2.5 times of the normal operation current.

3.2.3 Pin 4(VFB):

This pin is for the voltage feedback of the DC bus voltage stage. As shown in figure 16, the DC bus voltage is sensed to VFB pin through a voltage divider (R_{VFBH} and R_{VFBL}). At PWM off interval, S2 is turned on and the VFB pin voltage is regulated to the reference voltage (on the non-inverting input of the error amplifier) through the compensation network on VCOMP pin. What is special, the reference voltage for VFB is not a constant value. MP4653 implements adaptive voltage regulation for the DC bus voltage stage. This reference voltage for VFB is sampled from VFB pin at PWM on interval when the CV loop for DC bus regulation is ineffective. The DC bus voltage is regulated as its value at PWM on interval, and therefore it gets a same DC value through the whole PWM dimming cycle. This feature not only provides a DC voltage on the DC bus but also helps to improve the PWM dimming performance for the LED current. The voltage on VFB pin should between 1.2V and 2V at normal operation. Set the voltage feedback divider (R_{VFBH} and R_{VFBL}) and make the feedback voltage in this range at normal operation.

$$1.2V < V_{VFB} = \frac{R_{VFBL}}{R_{VFBH} + R_{VFBL}} \times V_{bus} < 2V \quad (3\text{-}8)$$

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

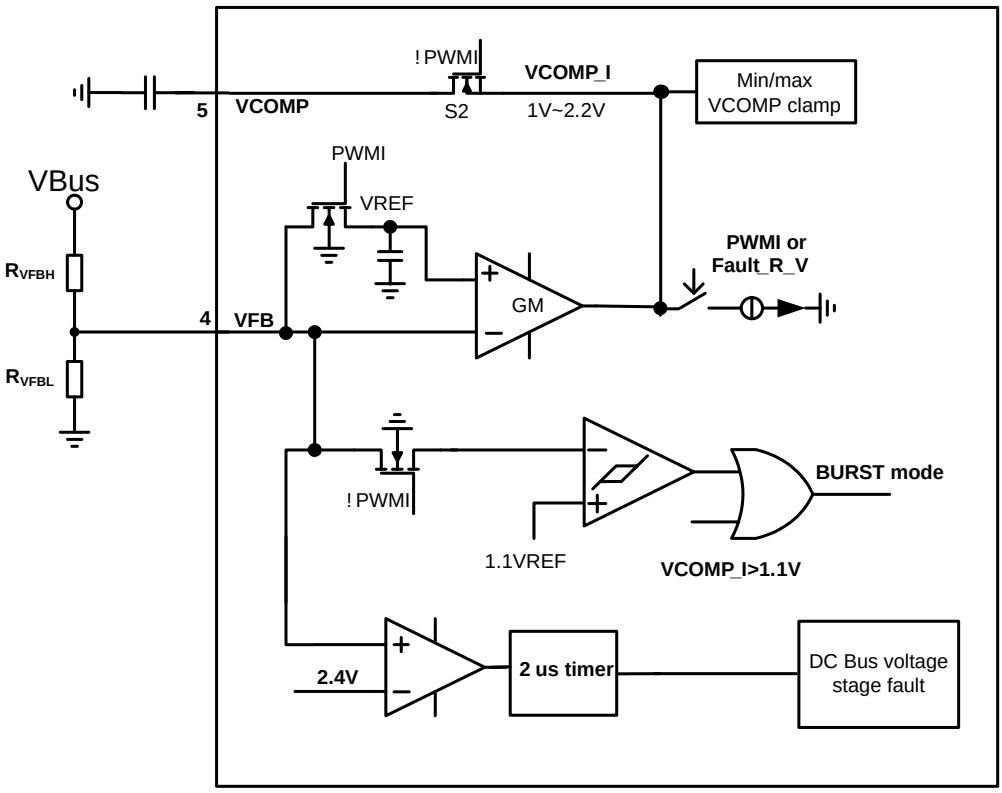


Figure 16—MP4653 FB Pin Function

Burst mode is integrated for the DC bus voltage regulation. At PWM off interval, if the voltage on VFB pin gets higher than 1.1 times of the reference voltage and the VCOMP voltage is lower than 1.1V, the MP4653 enters burst mode and disables the output of the gate drivers (GL and GR) for the power stage.

The VFB pin also functions as the over voltage protection for the bus stage. When the voltage on VFB gets higher than 2.4V, IC triggers bus stage protection. The over voltage protection point for the DC bus is then:

$$V_{OVP_Bus} = \frac{R_{VFBL} + R_{VFBH}}{R_{VFBL}} \times 2.4V \quad (3\text{-}9)$$

If requiring to set the over voltage protection point at a lower value, use a Zener diode in the feedback divider as figure 17.

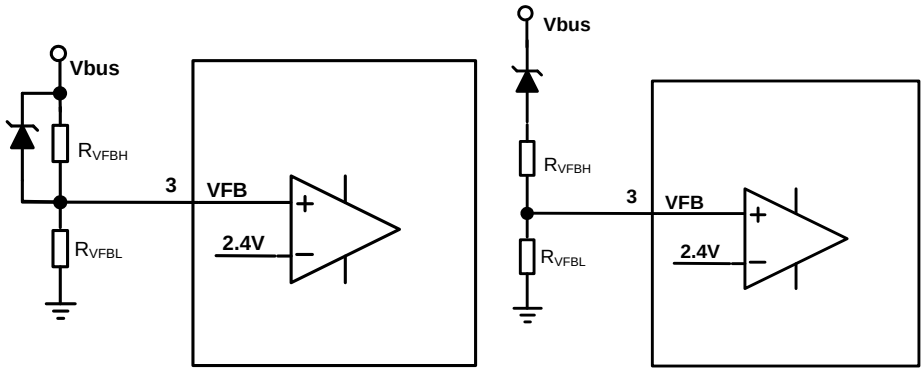


Figure 17—Use a Zener Diode in the Feedback Divider to Decrease the OVP Point

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

3.2.4 Pin 5 (VCOMP):

This pin is for the compensation of the CV loop for the DC bus voltage regulation. The external compensation network (it could be a single capacitor, a RC network or a R-C-C network) is connected to this pin as shown in figure 18. At PWM off interval at normal operation, the VCOMP pin is connected to the output of the error amplifier for the CV loop and gets it compensated. At PWM on interval, the VCOMP pin is disconnected from the error amplifier and holds its value for a quick response for the next dimming cycle.

The VCOMP pin is also used as the hiccup timer for the DC bus voltage stage protection. When fault occurs at the DC bus stage, the VCOMP is disconnected from the error amplifier, and an internal 2uA current source charges up VCOMP to 3V and then discharges it to 0.45V. The system auto recovers when VCOMP is discharged to 0.45V. The duration of the hiccup timer is:

$$T_{Hiccup_V} = C_{VCOMP} \times (\frac{3V - V_{VCOMP0}}{2\mu A} + \frac{2.55V}{2\mu A}) \quad (3\text{-}10)$$

Where V_{VCOMP0} is the voltage on VCOMP pin when fault occurs at DC bus stage.

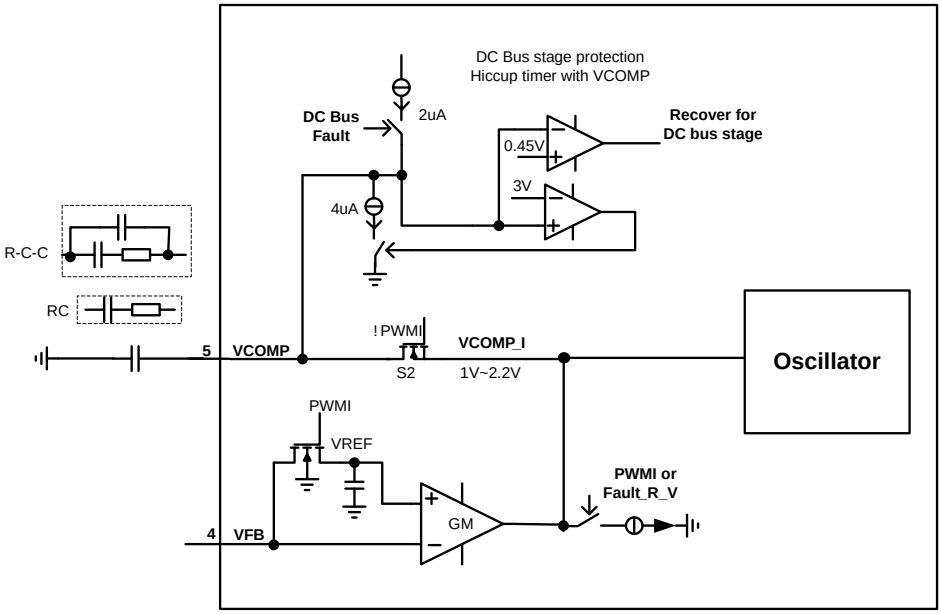


Figure 18—MP4653 VCOMP pin Function

3.2.5 Pin 7 (IFB), Pin 13 (A-Dim):

The IFB pin feeds back the LED current through a sensing resistor R_{sense}. The IFB pin voltage is regulated to 0.2V at PWM on interval if no analog dimming is applied. The amplitude of the LED current is:

$$I_{LED} = \frac{0.2V}{R_{sense}} \quad (3\text{-}11)$$

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

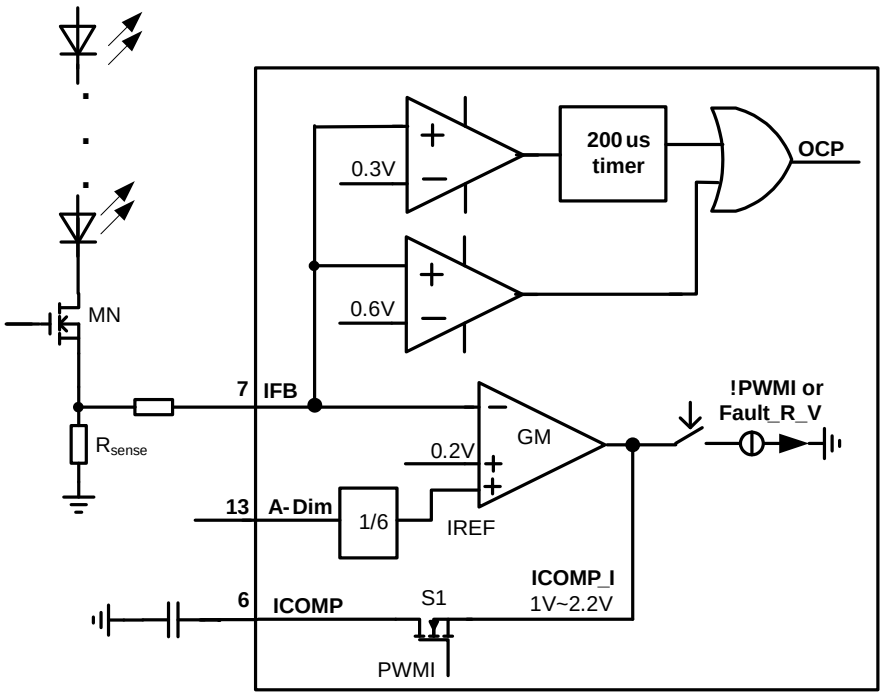


Figure 19—MP4653 IFB Function

The IFB pin is also used for the short protection of the LED string. When the LED string is shorted, the current through the sensing resistor gets larger, and IFB pin voltage gets higher. If the voltage on IFB pin is higher than 0.3V (1.5 times of 0.2V) for 200us or IFB voltage hits 0.6V, IC triggers the LED stage fault protection.

The reference voltage (IREF) for IFB pin is controlled by A-Dim pin. A 0~1.2V voltage on A-Dim pin programs this reference voltage from 0 to 0.2V. If the voltage on A-Dim pin is higher than 1.2V, this reference voltage is clamped at 0.2V. Therefore, the 0~1.2V voltage on A-Dim pin dims the LED current from 0 to 100%.

3.2.6 Pin 6 (ICOMP)

The ICOMP pin is for the compensation of the CC loop for the LED current regulation. The external compensation network (it could be a single capacitor, a RC network or a R-C-C network) is connected to this pin as shown in figure 20. The ICOMP pin is connected to the error amplifier for CC loop through an internal switch S1. At PWM on interval, S1 is turned on. The ICOMP pin is connected to the error amplifier and gets the CC loop compensated. The ICOMP voltage is clamped between 1V to 2.2V.

MP4653 implements burst mode for the LED current regulation. When the IFB voltage gets higher than 1.1 times of its reference voltage and the ICOMP voltage is lower than 1.1V, the IC enters burst mode and disables the output of the gate drivers (GL and GR) for the LLC power stage.

The ICOMP pin is also used for the hiccup timer for the LED stage protection. When fault occurs in the LED stage, an internal 2uA current source charges ICOMP pin to 3V and then discharges it to 0.45V. The LED stage recovers when ICOMP hits 0.45V. The hiccup timer for LED stage is:

$$T_{Hiccup_I} = C_{ICOMP} \times (\frac{3V - V_{ICOMP0}}{2uA} + \frac{2.55V}{2uA}) \quad (3\text{-}12)$$

Where the V_{ICOMP0} is the voltage on ICOMP pin when fault of the LED stage occurs.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

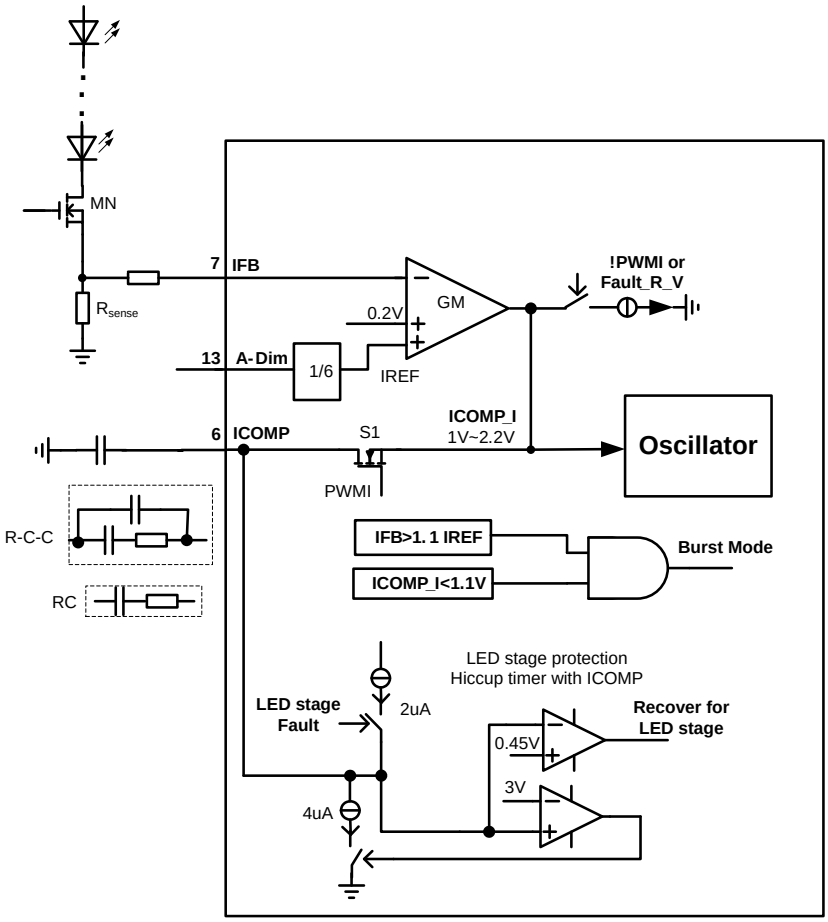


Figure 20—MP4653 CC Loop Compensation Function

3.2.6 Pin 8 (SSD)

The SSD pin is for short circuit protection of the LED stage. When any node of the LED string is shorted to ground, such as the anode, the cathode or a middle point of the LED string is shorted to ground, the current through the LED stage gets larger and the SSD pin senses a more negative voltage. When the SSD voltage gets lower than -200mV, the IC triggers the LED stage fault protection, as shown in figure 21. The short circuit protection current is:

$$I_{OCP_LED} = \frac{200mV}{R_{OCP}} \quad (3\text{-}13)$$

The short circuit protection point could usually be 1.5 to 2 times of the normal operating current (total current of the LED strings).

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

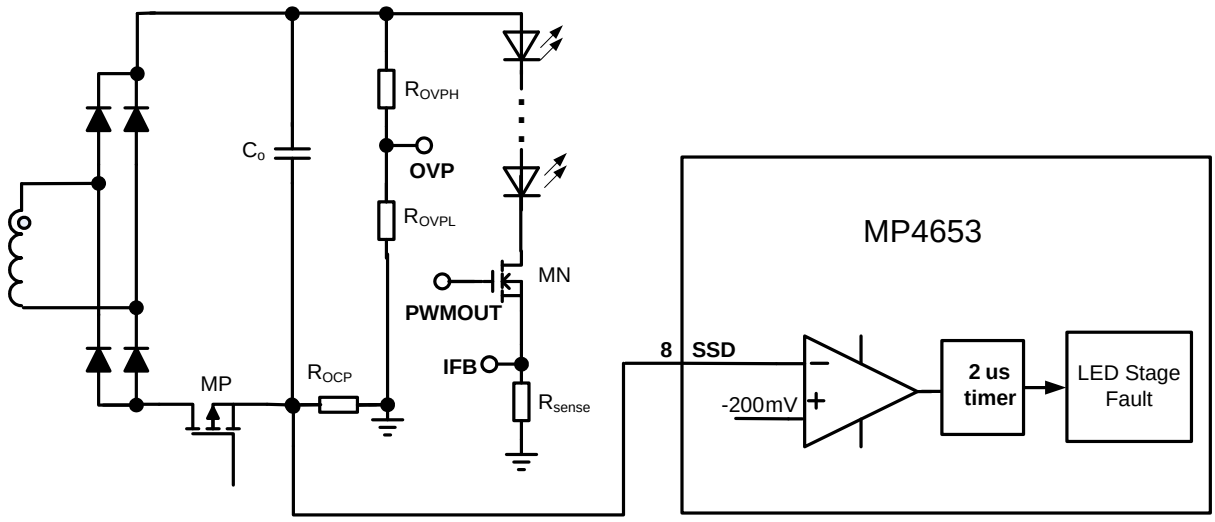


Figure 21—MP4653 SSD Function for Short Circuit Protection of the LED Stage

3.2.7 Pin 9,10,11,12 (VLED4, VLED3, VLED2, VLED1)

These four pins feedback the voltage of the LED strings. MP4653 implements over voltage protection and voltage difference protection on these four pins. The protection scheme is shown in Figure 22.

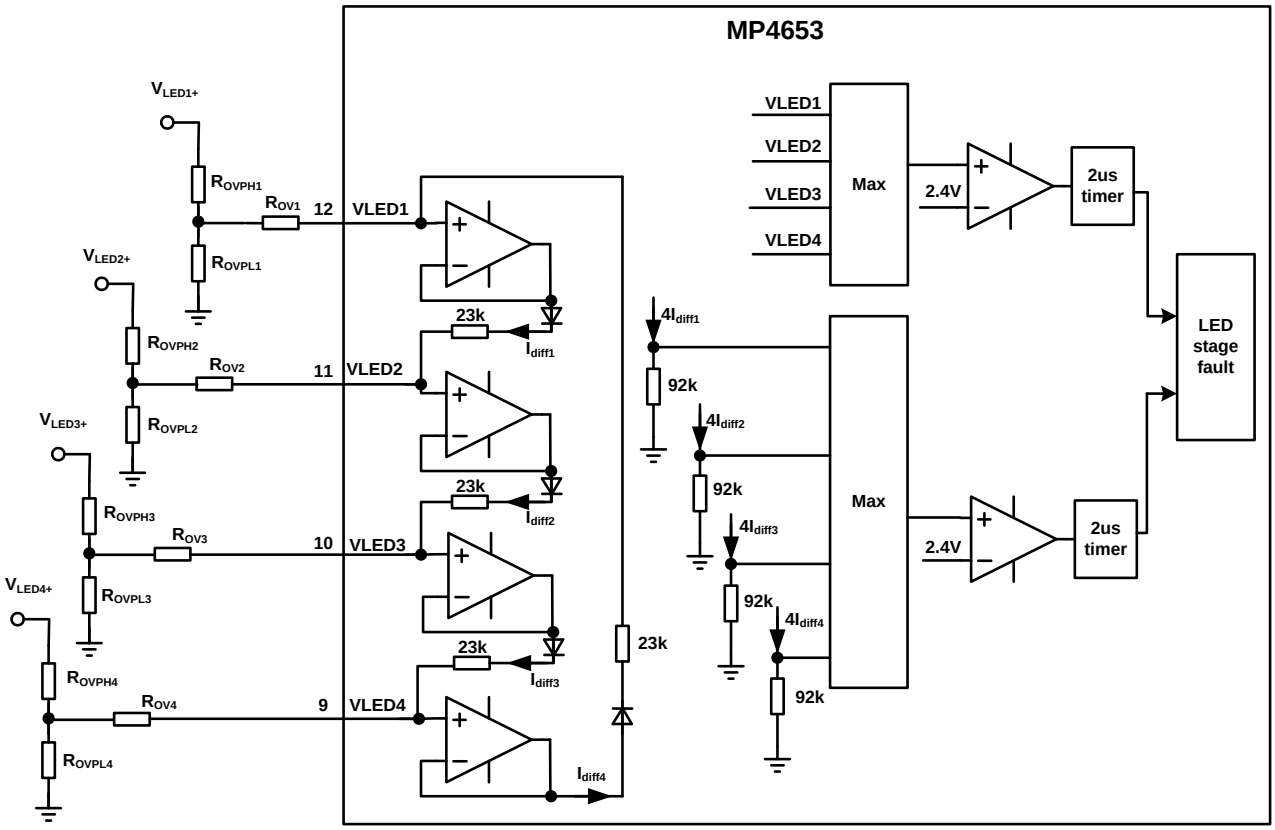


Figure 22—MP4653 LED# (#=1,2,3,4) Pins Protection Scheme

As shown in figure 22, the LED voltages are feedback to VLED# (#=1,2,3,4) pins through a voltage divider. The maximum one of the VLED# voltages is compared with the internal 2.4V threshold. If it is

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

higher than the 2.4V threshold for 2us, IC triggers the LED stage fault protection. This provides over voltage protection or open LED protection for the LED strings. The over voltage protection point is set as:

$$V_{OVP} = \frac{R_{OVPH} + R_{OVPL}}{R_{OVPL}} \times 2.4V \quad (3\text{-}14)$$

MP4653 also implements voltage difference detection on the VLED# pins. The voltage differences (VLED1-VLED2, VLED2-VLED3, VLED3-VLED4, VLED4-VLED1) are converted to current sources $I_{diff\#}$ through the internal 23kΩ resistor. After amplifying the current source, 16 times of the voltage differences are got and the maximum value is compared with the internal 2.4V threshold. If it gets higher than 2.4V for 2us, IC triggers LED stage fault protection. This voltage difference detection provides a protection for the condition when several LEDs of a LED string are shorted. It can also protect the LED string open or short condition.

If any one of the LED strings gets several LEDs shorted, the voltage difference protection point could be set by:

$$\Delta V_{pro} = \frac{R_{OVPH} + R_{OVPL}}{R_{OVPL}} \times 2.4V \times \frac{23k + R_{input}}{16 \times 23k} \quad (3\text{-}15)$$

Where R_{input} is input resistance of the VLED# pin.

$$R_{input} = \frac{R_{OVPH} \times R_{OVPL}}{R_{OVPL} + R_{OVPH}} + R_{OV} \quad (3\text{-}16)$$

The resistor $R_{OV\#}$ in series with VLED# pin could program the voltage difference protection point.

3.2.8 Pin 14 (PWMIN)

This pin is for PWM dimming signal input. Applying a PWM dimming signal with frequency in range of 100Hz to 2kHz on this pin. It has positive polarity for the PWM dimming.

At PWM on interval, the LED current is regulated and at PWM off interval, the voltage control loop for the DC bus voltage stage functions. The DC bus voltage is regulated to the value at PWM on interval.

3.2.8 Pin 15 (VIN)

This pin is the supply input voltage for the IC. Bypass this pin with a 0.1uF or larger ceramic capacitor.

IC starts to work when the VIN voltage is applied. If PWMIN pin is high, the LED current control loop is effective and if the PWMIN pin is low, the voltage control loop for the DC bus voltage stage is effective. If an “Enable” signal is required to control the starting operation of the IC, use this “Enable” signal to control this supply input voltage with following circuit in figure 23.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

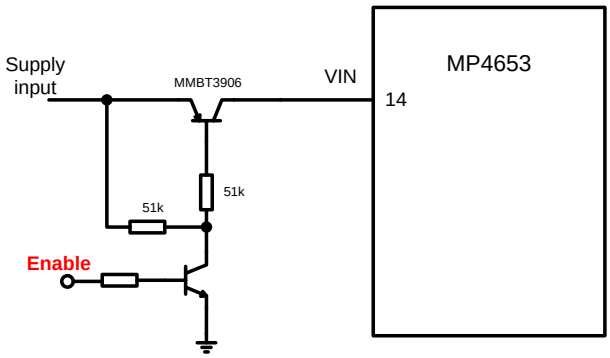


Figure 23—MP4653 Enable control circuit

3.2.9 Pin 16 (PWMOUT)

This pin outputs a PWM dimming signal to drive the external dimming MOSFET (MN) in series with the LED string, and achieve fast PWM dimming. The LED current rises and falls rapidly with the PWMOUT signal. Connect a resistor in series with this pin to adjust the driving speed and to eliminate the LED current spike during PWM dimming. Figure 24 shows the scheme.

The PWMOUT signal is also used to control the external P-MOS (MP) for protection. A negative voltage source (-Vbus) is generated from the secondary winding of the DC bus voltage stage. A pulse waveform at “VX“ with a magnitude smaller than Vbus is generated through the PWMOUT signal. By summing the negative voltage source and VX, a pulse waveform with a negative magnitude is generated on “P_Drive” (the P-MOS gate) and is used to drive the P-MOS.

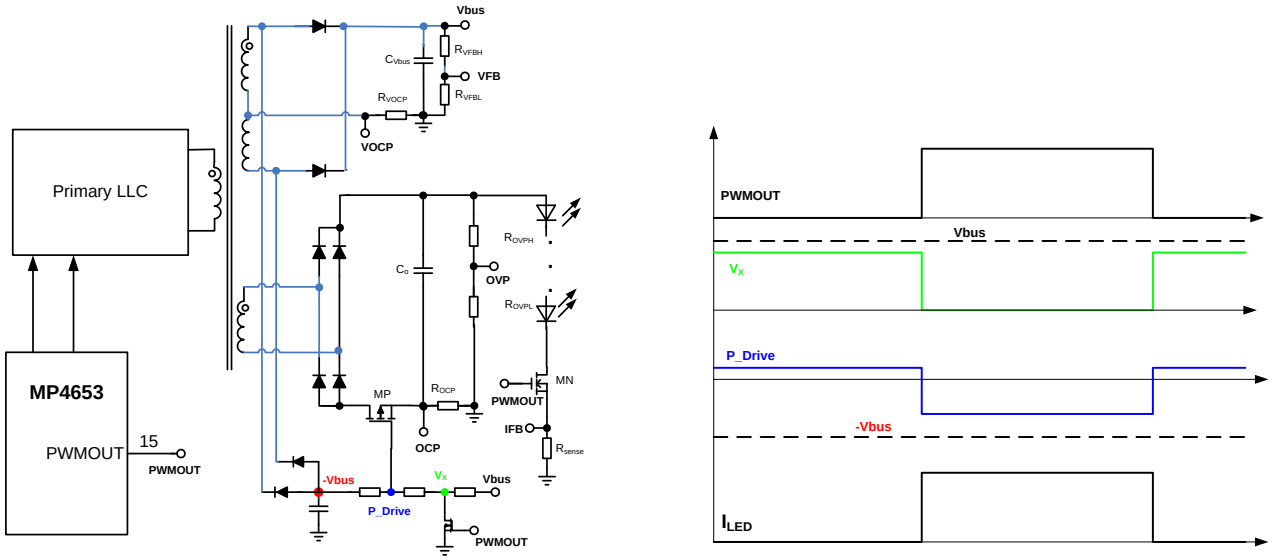


Figure 24—MP4653 PWMOUT Driving the Dimming MOS and P_MOS

PWMOUT signal can output an error signal to the system, as shown in Figure 25. During normal operation, the PWMOUT pin outputs the dimming signal and the capacitor Cerror charges to VIN during every PWM-ON interval. In addition, the QNPN and the QPNP turn on and the Error node goes high at this time. During the PWM-OFF interval, QNPN turns off, Rerror and QPNP discharge the Cerror capacitor, and the voltage on the error node remains relatively high throughout the PWM dimming cycle. However, under fault condition (either open or short fault), the PWMOUT is pulled low, Rerror fully discharges Cerror, QPNP turns off, and the voltage on the error node goes low.

Design the Rerror and Cerror time constant for the PWM dimming period: for example, Cerror=0.1µF and Rerror=100k can cover the dimming frequency over 100Hz.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

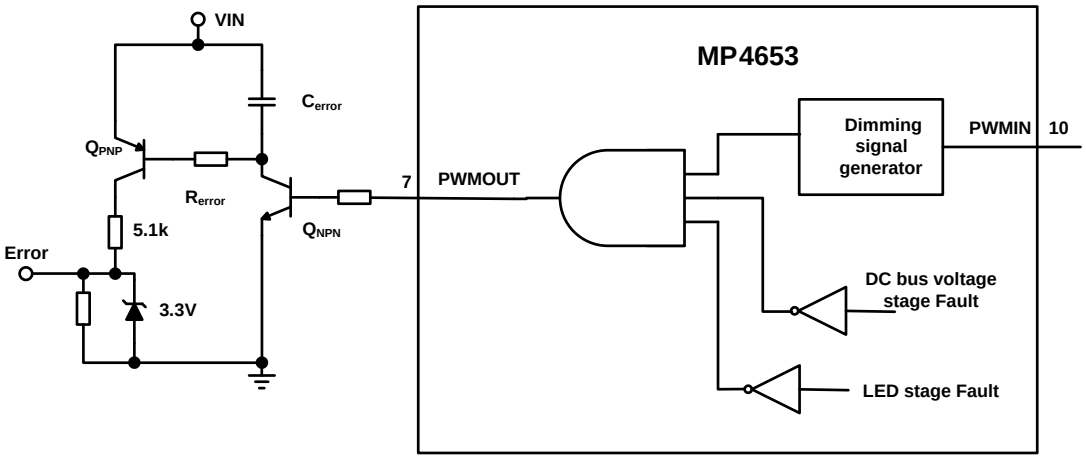


Figure 25—System Error Signal from PWMOUT Signal

3.2.10 Pin 17 (VCC)

This pin supplies the gate drive signals GL, GR and PWMOUT. Bypass this pin with a 1uF or larger ceramic capacitor. This pin could also be used to supply an external circuit.
The VCC voltage is generated from VIN through a LDO, as shown in figure 26.

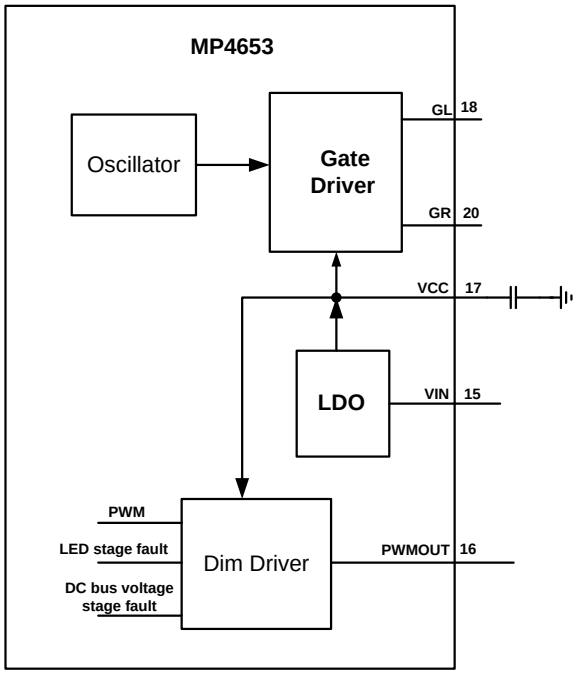


Figure 26—MP4653 VCC Supply Scheme

3.2.11 Pin 18, 20 (GL,GR)

Gate driver signals output. GL and GR are 180-degree phase-shifted driver signals. GL and GR can directly drive the external MOSFETs in the LLC power stage through a gate driver transformer with enhanced driver capability. Connect two 5.1Ω resistors in series with GL and GR to reduce the EMI noise.
Place a 2.2nF Y capacitor between the primary reference ground and the secondary reference ground for better EMI performance.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

4. APPLICATION EXAMPLE AND DESING PROCEDURE

TV LED Backlighting

This application example introduces a MP4653 based Real LIPS 2-stage LLC TV LED driver designed for a 4-strings TV LED backlighting application. Figure 27 shows the entire system power structure. It uses the Real LIPS pure 2-stage structure with high efficiency and low cost. The MPS PFC controller MP44010 regulates the PFC stage output to around 390V: the MP44010 works in boundary conduction mode (BCM). The MP4653 Real LIPS controller controls the LLC power stage. It directly drives the LED strings and also outputs a DC bus voltage for the system power supply. Both the LED current and the DC bus voltage are controlled. A DC/DC converter MP8778 is used to further convert the DC bus voltage to the system power supply like 12V. A standby flyback DC/DC stage outputs the 5V STB voltage for the system standby power supply. It uses MPS flyback driver HF01B04 with MOSFET integrated. This 5V standby power supply powers up the MP4653 at the system start up.

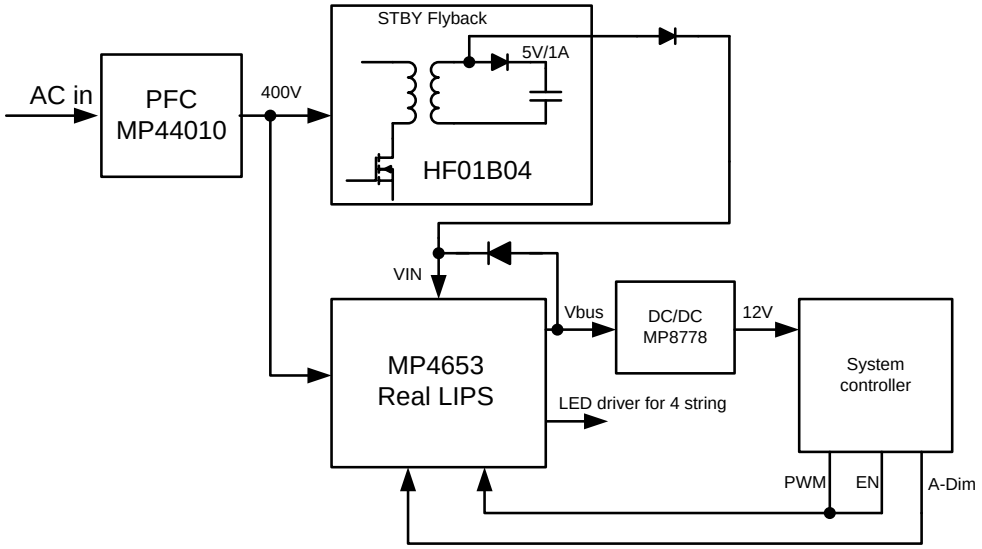


Figure 27—System Power Structure of MP4653 Based Real LIPS TV LED driver

4.1 Specification

Table 2—Specification for the TV LED Driver

Parameter	Symbol	Value
Input voltage	VIN	Typical 390V, 380V to 410V
LED Voltage	V_{LED}	Typical 110V, 95V to 120V
LED current	I_{LED}	130mA
No. of LED strings		4
Operating frequency	f_s	Around 70kHz
PWM dimming frequency	f_{PWM}	480Hz
DC/DC output voltage	V_{DCOUT}	12V
DC/DC output current	I_{OUT}	3A
Protection		Open LED protection, short LED string protection, short protection against any point of the LED string to ground, DC bus voltage short to GND protection

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

4.2 Schematics

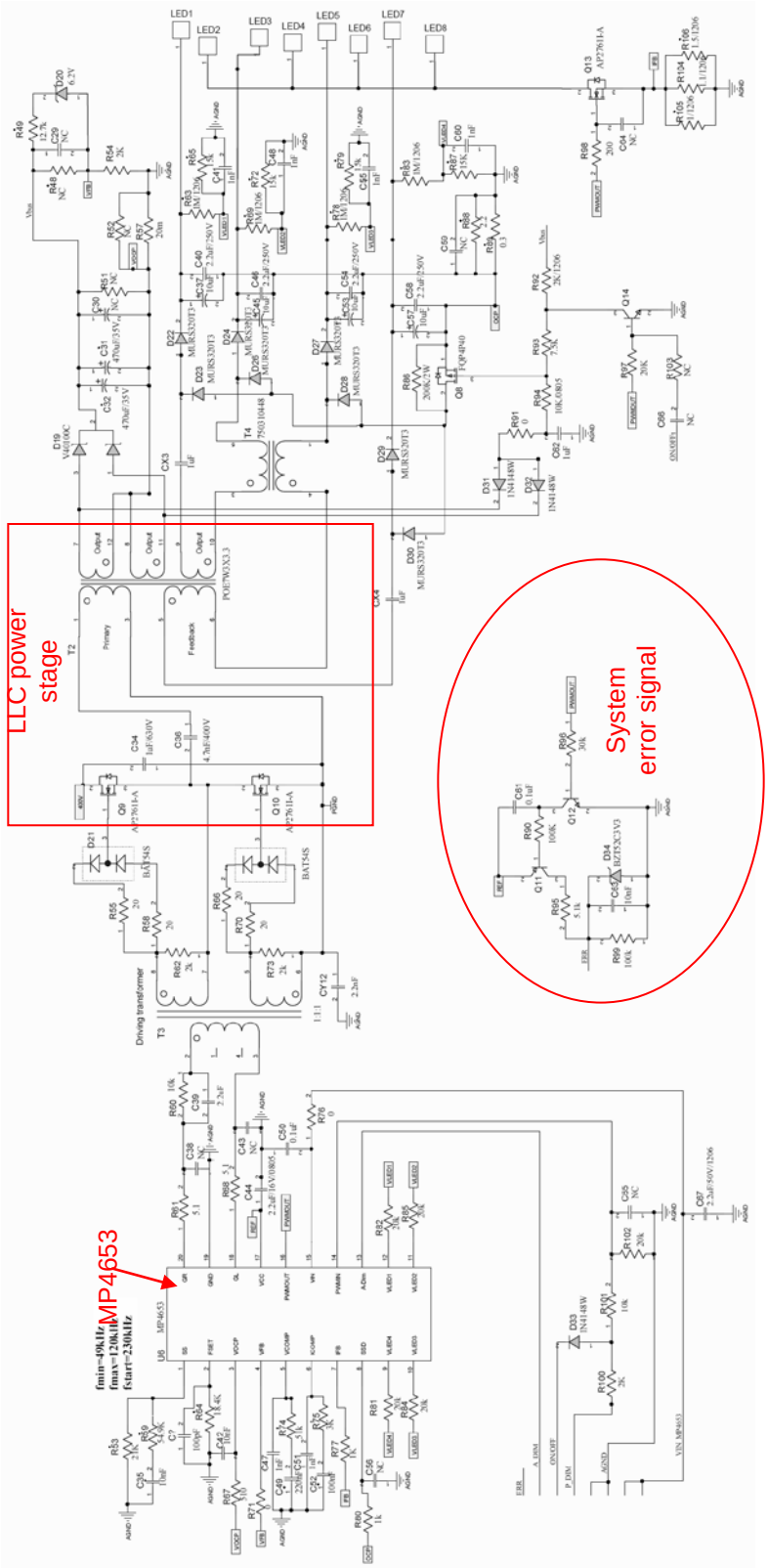


Figure 28—MP4653-Based Real LIPS 2-Stage LLC TV LED Driver

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

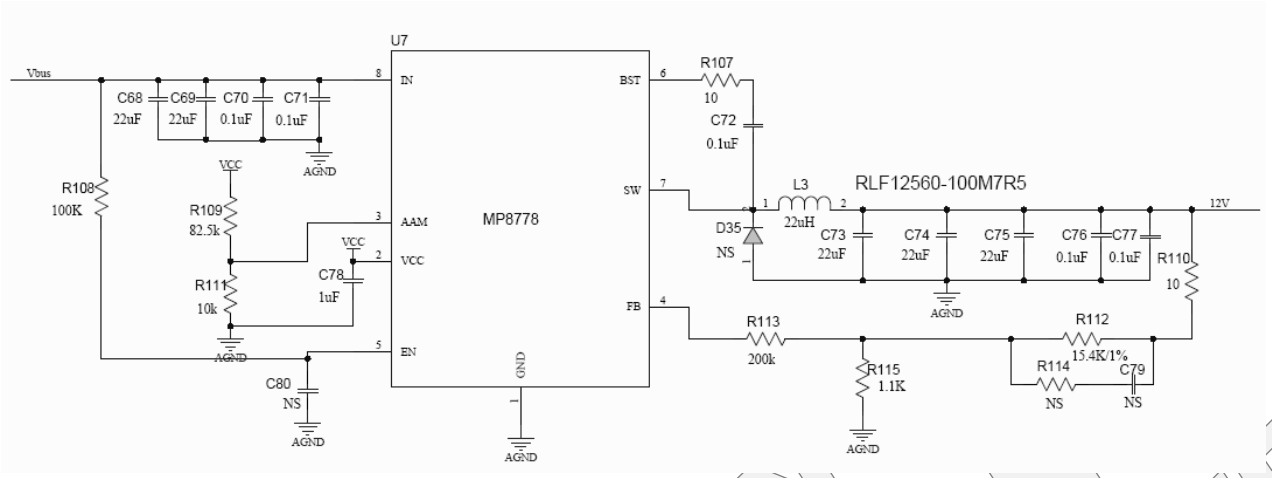


Figure 29—MP8778 DC/DC Converter

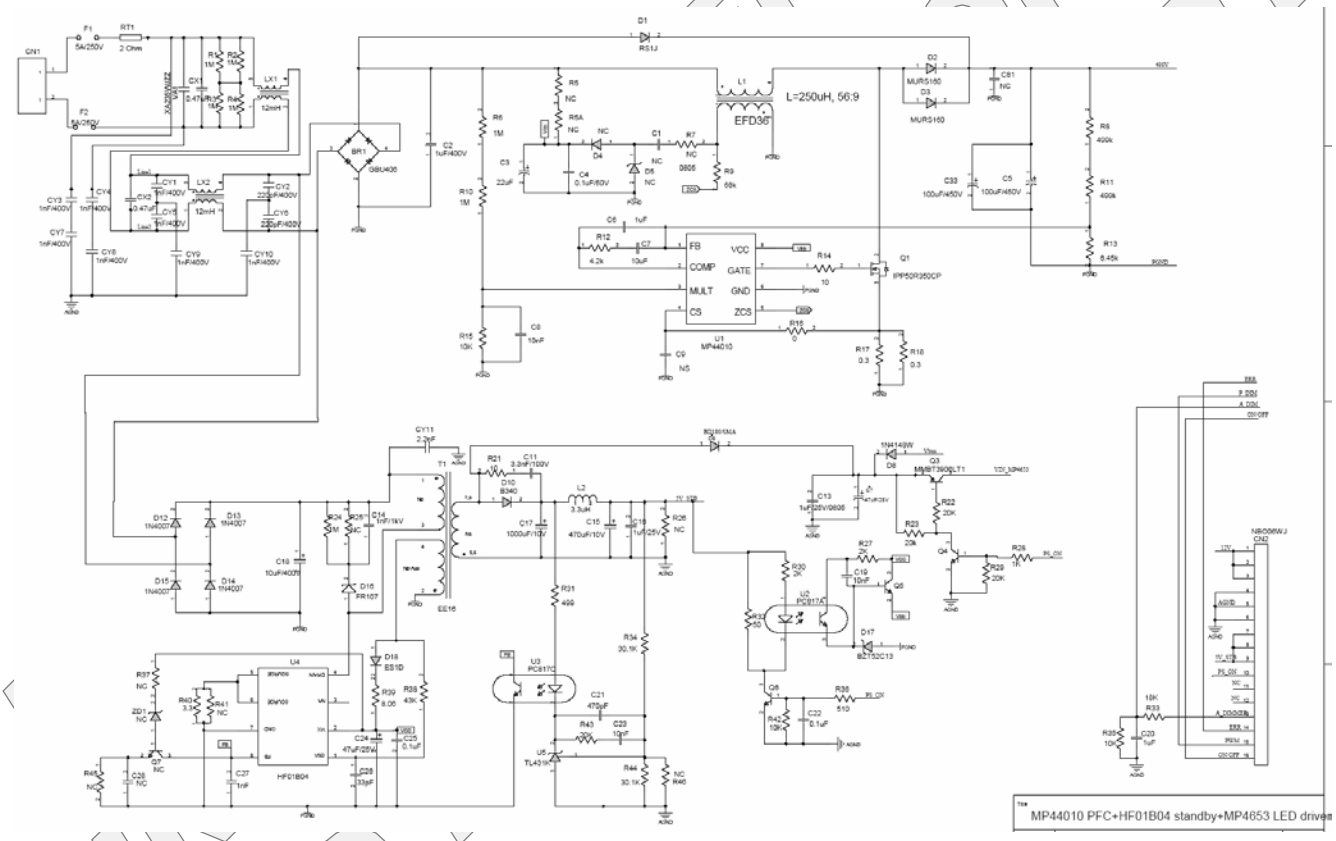


Figure 30—MP44010 PFC and HF01B04 STB Flyback

In this application note, the design of the MP44010 PFC stage, the MP8778 DC/DC stage and the HF01B04 STB 5V flyback stage will not be included, please refer to related design material of these ICs. The MP4653 Real LIPS LLC design is described as following. Please refer to the MP4653 design spread sheet for auto calculation.

4.3 Power Stage Design

The power stage uses a half-bridge LLC topology. The power MOSFETs Q9 and Q10 comprise the half bridge and generate a square-wave source on the LLC network—a circuit composed of the resonant

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

capacitor (C36), the leakage inductance (L_k) of T2, the magnetic inductance (L_m) of T2, and the load. The power stage design depends on the input voltage, the load condition, and the desired operating frequency. Following induces the details of the design.

4.3.1 Power MOSFET (Q9, Q10)

The selection of the power MOSFET needs to consider the voltage stress, the current, the conduction resistance R_{Dson} and the package.

(1) The voltage stress of the MOSFETs in the half bridge LLC power stage is equal to the input voltage. For a typical PFC output of 390V, select MOSFETs rated between 500V and 650V.
(2) Selecting the MOSFET current rating requires considering the output power range—typically a 60W to 100W power range requires MOSFETs rated between 5A and 10A.
(3) The MOSFET R_{Dson} require consideration:—usually MOSFETs below 1Ω R_{Dson} work well for this power range.
(4) A TO-220 MOSFET package works well for this range for its good thermal performance.

4.3.2 LLC Parameters and Power Transformer Design (C36, T2)

Designing the LLC involves considerations for the following parameters: the resonant capacitor (C_r), the leakage inductance of the transformer (L_k), the magnetic inductance of the transformer (L_m), the input voltage (VIN), the output voltage and current, and the desired operating frequency.

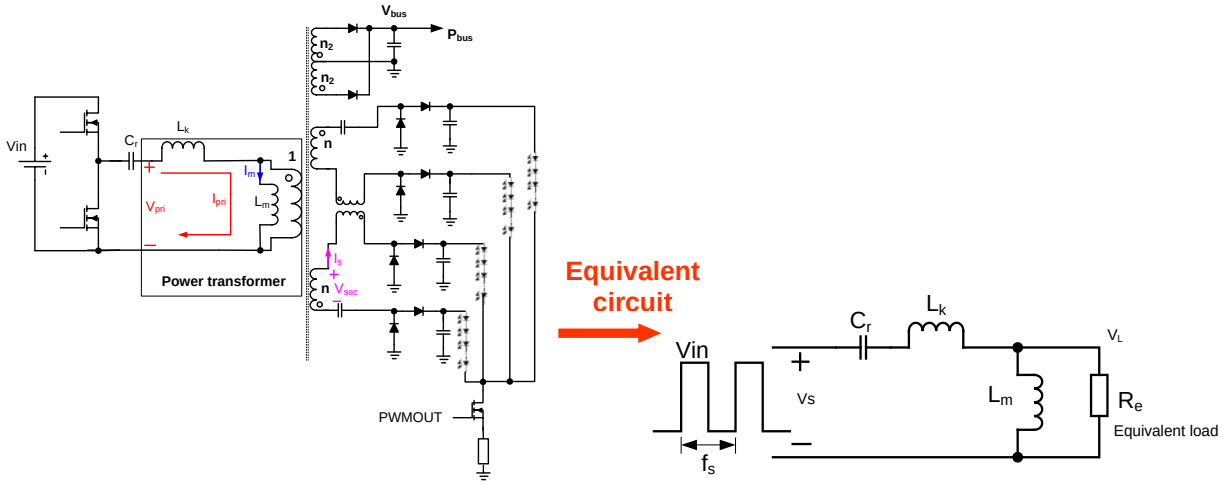


Figure 31—LLC Power Stage and Equivalent Circuit

Based on the circuits in Figure 31 showing the LLC power stage for LED driver and its equivalent circuit at normal operation, the load on the secondary side is reflected to the primary side and is equivalent to a load resistor R_e. In the MP4653 Real LIPS power stage, the DC bus voltage follows the LED voltage with the ratio of the secondary windings.

$$R_e = \frac{8V_{LED}^2}{\pi^2 n^2 (P_{LED} + P_{bus})} \quad (4\text{-}1)$$

Where V_{LED} is the average output LED voltage and P_{LED} and P_{bus} are the output power of the LED stage and DC bus stage. The efficiency of the transformer is not considered here.

In the LLC circuit, there are 2 resonant points: one (f_0) is composed by L_k and C_r (short load condition), the other (f_1) is composed by L_k+L_m and C_r (load open condition).

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

$$f_0 = \frac{1}{2\pi\sqrt{L_k C_r}} \quad (4\text{-}2)$$

$$f_1 = \frac{1}{2\pi\sqrt{(L_k + L_m)C_r}} \quad (4\text{-}3)$$

The operating frequency is recommended between these 2 resonant points to obtain a soft switching and high efficiency.

Step 1: Set the ratio (L_n) of L_m to L_k

To limit the operating frequency range and also to get a high efficiency, the range between f_0 and f_1 should not be too wide. Usually, choose the f_0 at 2 to 3 times of f_1 and then:

$$\frac{f_0}{f_1} = \frac{2\pi\sqrt{(L_k + L_m)C_r}}{2\pi\sqrt{L_k C_r}} = 2 \text{ to } 3 \quad (4\text{-}4)$$

$$L_n = \frac{L_m}{L_k} = 3 \text{ to } 8 \quad (4\text{-}5)$$

Usually L_n =4 is a good selection.

Step 2: Set the transformer turn ratio n, n_2

The quality factor and the gain of the LLC resonant circuit are:

$$Q = \frac{\sqrt{L_k / C_r}}{R_e} \quad (4\text{-}6)$$

$$Gain(f) = \left|\frac{V_L}{Vs}\right| = \left|\frac{\frac{j2\pi f L_m * R_e}{j2\pi f L_m + R_e}}{\frac{j2\pi f L_m * R_e}{j2\pi f L_m + R_e} + j2\pi f L_k + \frac{1}{j2\pi f C_r}}\right| = \left|\frac{L_n \frac{f^2}{f_0^2}}{L_n \frac{f^2}{f_0^2} + (\frac{f^2}{f_0^2} - 1)(\frac{f}{f_0} + 1 + j\frac{f}{f_0} L_n Q)}\right| \quad (4\text{-}7)$$

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

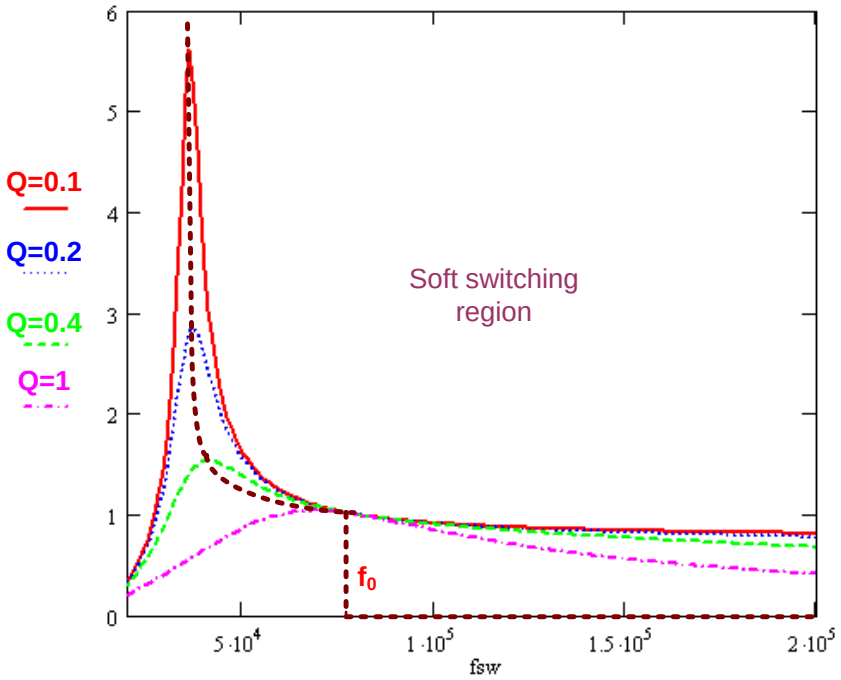


Figure 32—Gain of an LLC Circuit at Different Quality Factor

Figure 32 shows the gain vs. frequency of an LLC circuit at different quality factor Q, and shows the soft-switching region where the circuit should operate. The plot shows that as Q increases, the gain decreases.

The LLC power stage design should cover the input and output voltage ranges. This requires the gain of the circuit gets a fair range.

From the gain curves in Figure 32, there are basically two methods.

(1) Design for high Q (Q>1) and the operating frequency higher than f_0

(2) Design for low Q. As the gain curve flattens at $f_s>f_0$, operating beyond f_0 becomes undesirable.

Another power stage design consideration is efficiency. Figure 33 shows the operating waveforms when $f_s>f_0$ and $f_s<f_0$. Method 2 operates at a lower frequency with a discontinuous secondary current through the rectifier diodes that eliminates the recovery influence of the diodes. This method usually has higher efficiency for high output voltage, making it the preferred LCC power stage design.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

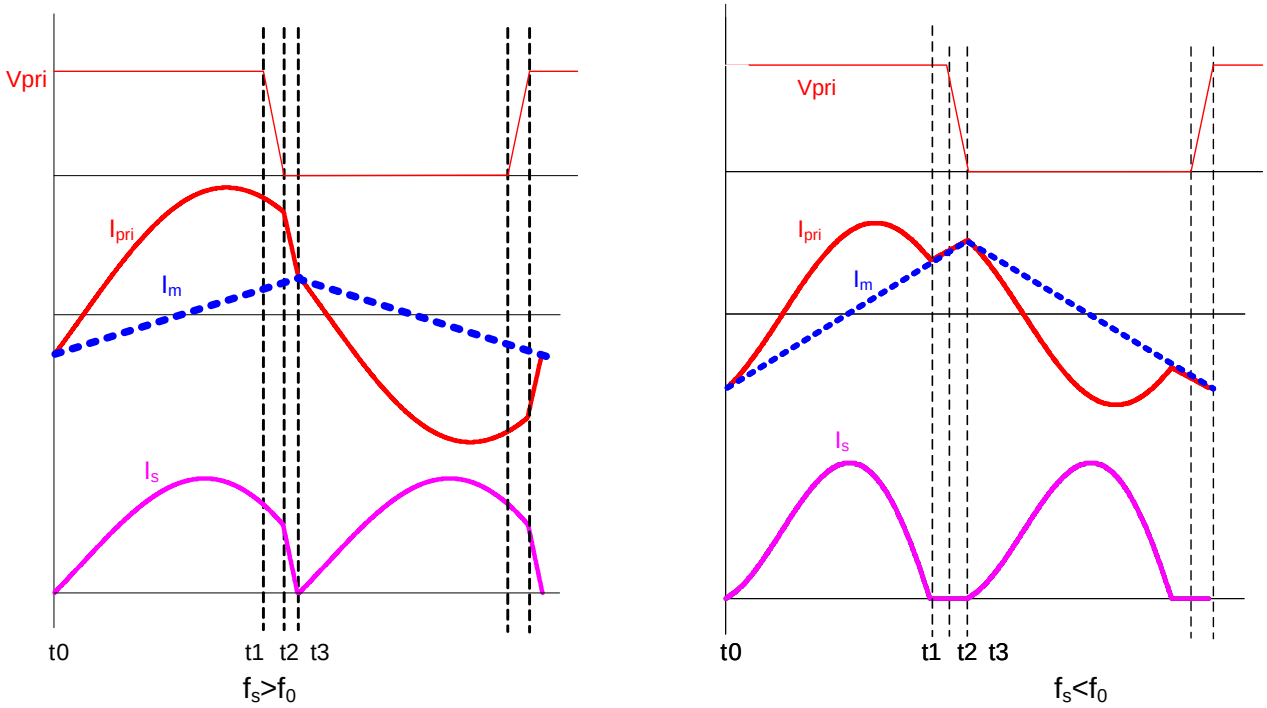


Figure 33—LLC Operating Waveforms at $f_s>f_0$ and at $f_s<f_0$

One more consideration is that the LED driver is a constant current load, not a constant voltage load for the LLC power stage. The LED voltage may get a ±15% variation if considering the analog dimming function. This requires the LLC power stage to cover a wider gain range. Method 2 is still preferred.

Using method 2 to design the LLC power stage, select a maximum operating frequency slightly higher than f_0, with a minimum LLC network gain of 0.9 to 0.95. This minimum gain should cover the maximum input and minimum output condition. Then the turn ratio of the transformer is:

$$Gain_{_min} = 0.9 \text{ to } 0.95 \tag{4-8}$$

$$n = \frac{Ns}{Np} = \frac{2V_{o_min}}{V_{in_max} \cdot Gain_{_min}} = \frac{(2.1 \text{ to } 2.2)V_{o_min}}{V_{in_max}} \tag{4-9}$$

For simplicity, these equations only consider the fundamental harmonic of the LLC input V_s, as do the remaining calculations for this section.

Given that this design has a minimum LED voltage of 95V (V_{o_min}=95V) and maximum input voltage of 410V (V_{in_max}=410V), the turn ratio ranges from 0.487 to 0.509 (the actual turn ratio of this design is NS:NP=37:78).

The selection of n_2 for the DC bus voltage should consider the input voltage range of the DC/DC converter. For a 13V system supply voltage and 21V max input voltage DC/DC converter, the DC bus voltage range could be selected between 15V to 20V. Select the DC bus voltage slightly higher than 15V at the minimum LED voltage. Then the n_2 is:

$$n_2 = \frac{1.05 * n * V_{DCbus_min}}{V_{LEDmin}}$$

The actual turn ratio of this design is NS_{DC}:NS_{LED}:NP=6:37:78.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

Step 3: Set the Quality Factor Q

The gain curves in Figure 32 show that changing the quality factor Q changes the maximum gain. The maximum gain for the designed quality factor should cover the input and output range. However, an extremely high gain may cause system instability. The maximum gain then becomes:

$$Gain_{require_max} = \frac{2V_{o_max}}{nV_{in_min}} \quad (4\text{-}10)$$

For this design, given that the minimum input voltage is 380V and the maximum output voltage is 120V, then the required maximum gain ($Gain_{require_max}$) is 1.33. Choose a quality factor in the range of 0.2 to 0.4. The actual quality factor of this design is around 0.2.

Step 4: Set the Resonant Frequency f0 to the Desired Operating Frequency

The resonant frequency of the LLC circuit could be the desired operating frequency, as the normal operating frequency is close to the resonant frequency. For the TV LED backlighting applications, the resonant frequency is usually in range of 60kHz to 120kHz. In this design, f_0≈80kHz.

Step 5: Determine the Resonant Parameters

From the equations (4-1), (4-2), (4-5), (4-6), the resonant parameters are:

$$C_r = \frac{1}{2\pi R_e Q f_0} = \frac{\pi n^2 (P_{LED} + P_{Bus})}{16 V_{LED}{}^2 Q f_0} \approx 21.7nF \rightarrow C_r = 22nF \quad (4\text{-}11)$$

Using a 22nF resonant capacitor.

$$L_k = C_r Q^2 R_e{}^2 = C_r Q^2 \left(\frac{8 V_{LED}{}^2}{\pi^2 n^2 (P_{LED} + P_{Bus})}\right)^2 = 180\mu H \quad (4\text{-}12)$$

In this design, L_k is around 170uH.

The magnetic inductance is then:

$$L_m = L_n \times L_k = 0.54 \text{ to } 1.44mH \quad (4\text{-}13)$$

L_m is 680μH in this design.

Step 6: Estimate the Primary Current and Choose the Resonant Capacitor

We have estimated the value of the resonant capacitor in equation (4-11): Now we need the voltage stress and the RMS current for the resonant capacitor.

(1) The voltage stress of the resonant capacitor can stand in as the reference for the input voltage. For the maximum 410V input voltage in this design, the voltage rating of the resonant capacitor could be 630V.

(2) The RMS current through the resonant capacitor could be estimated as:

$$I_{pri_rms} \approx \frac{P_{LED} + P_{Bus}}{\eta \times \cos\theta \times V_{s_rms(1)}} = \frac{\pi (P_{LED} + P_{Bus})}{\sqrt{2} V_{in_min} \times \eta \times \cos\theta} \quad (4\text{-}14)$$

Where η is the efficiency of the circuit, which is usually in range of 0.92 to 0.95. θ is the phase between the primary voltage and the primary current. $V_{s_rms(1)}$ is the fundamental harmonic of the LLC input voltage V_s.

$$V_{s_rms(1)} = \frac{2Vin}{\sqrt{2}\pi} \quad (4\text{-}15)$$

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

The input impedance of the LLC network (Figure 31) is:

$$Z_{in}(f)=\frac{j2\pi fL_m * R_e}{j2\pi fL_m + R_e} + j2\pi fL_k + \frac{1}{j2\pi fC_r} = \sqrt{\frac{L_k}{C_r}}\left(\frac{jL_n * \frac{f}{f_0}}{1+jQL_n\frac{f}{f_0}} + j\frac{f}{f_0} + \frac{1}{j\frac{f}{f_0}}\right) \quad (4\text{-}16)$$

Its phase is the phase difference between the primary voltage and the primary current θ. Figure 34 shows the phase of the LLC network for different quality factors. The θ can be over 30° at Q=0.2. Selecting a reasonable cosθ=0.85 the primary current is:

$$I_{pri_rms} \approx \frac{\pi(P_{LED}+P_{Bus})}{\sqrt{2}V_{in_min}\times\eta\times\cos\theta} = 0.75A \quad (4\text{-}17)$$

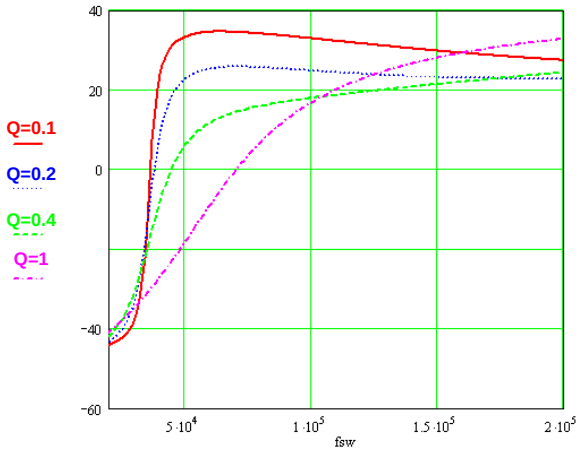


Figure 34—Phase of the LLC Network at Different Quality Factor

(3) Use an MMKP- or CBB-type resonant capacitor to handle a high current, as shown in Figure 35.

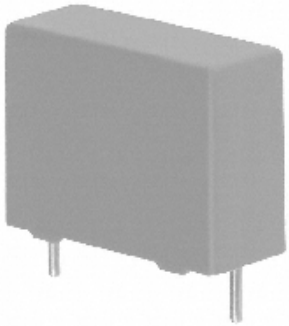


Figure 35—MMKP Capacitor

Step 7: Design the power transformer

The parameters of the turn ratio n and n_2, the leakage inductance and the magnetic inductance are obtained as previously described. The design of the power transformer is as below:

(1) The leakage inductance of the power transformer is usually large (like 170μH in this design) and requires keeping a distance between the primary winding and the secondary winding. This distance can also help to isolate the primary side and the secondary side to meet safety requirements. For designs with height limitations, such as for a TV LED driver, choose an EFD core and bobbin with 2 slots, as shown in Figure 36.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

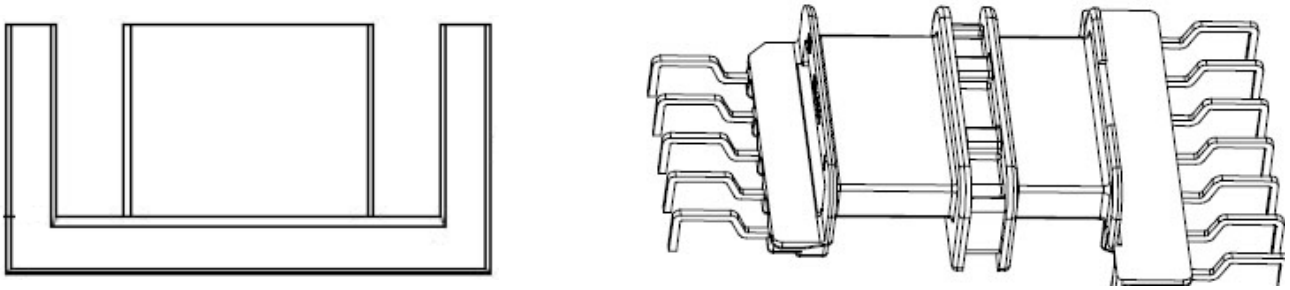


Figure 36—EFD Core and Its Bobbin with 2 Slots

(2) Determine the number of windings. The power transformer should have enough turns to ensure against saturation.

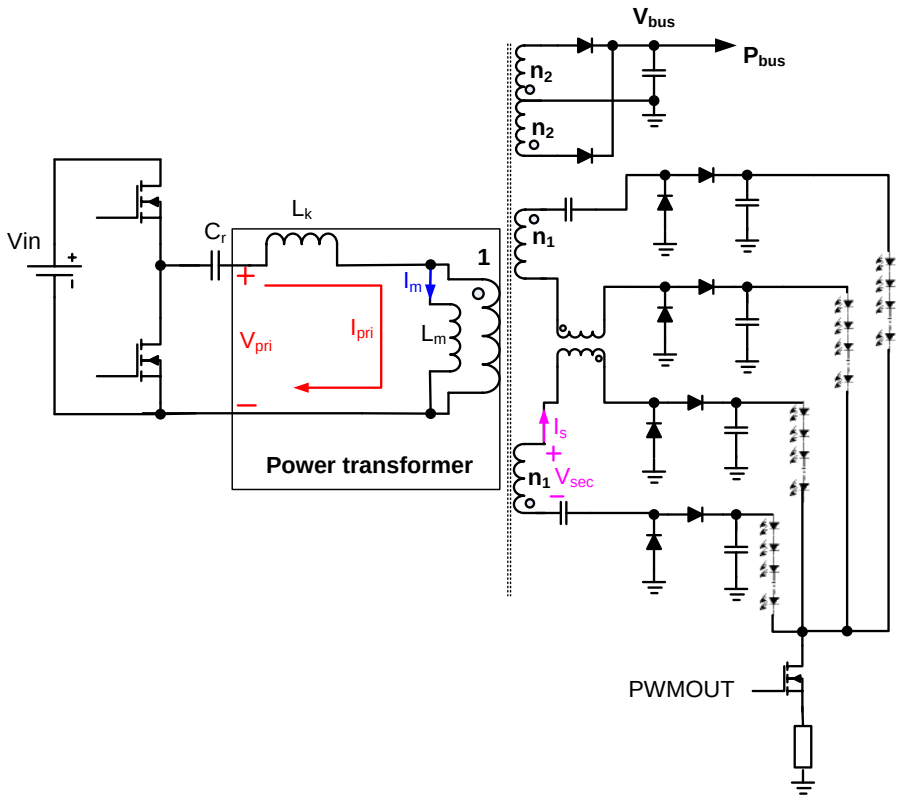


Figure 37A—Real LIPS LLC Power Stage for TV LED Driver

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

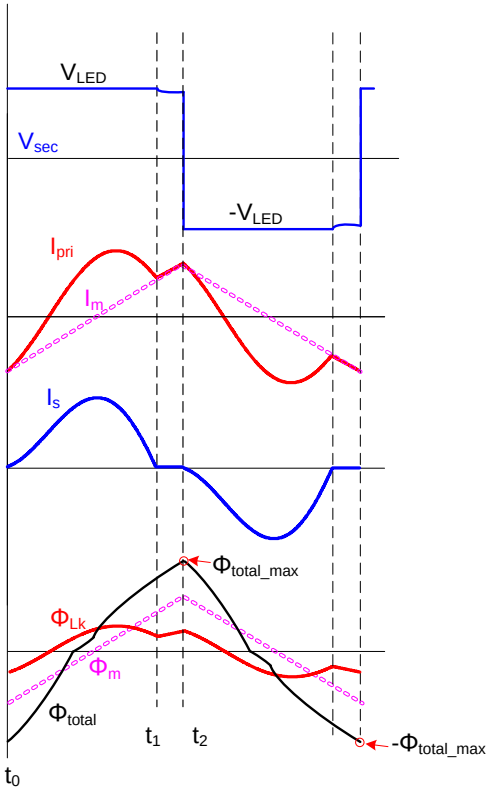


Figure 37B—Waveforms of the LLC Power Stage at $f_s<f_0$

Figure 37—LLC Power Stage and Its Operating Waveforms

Figure 37 shows the LLC power stage (Figure 37A) and some of its operating waveforms when $f_s<f_0$ (Figure 37B).

The high-side power MOSFET turns on at t_0. During the t_0-to-t_1 interval, the primary current is larger than the magnetic current, the secondary rectifier diodes are conducting, and the secondary-side voltage equals the output voltage V_{LED} as energy transfers from the primary side to the secondary side.

At t_1, the primary current falls to the magnetic current and the secondary side rectifier becomes discontinuous. As the secondary current can not reverse because of the rectifier diodes, then the primary current equals to the magnetic current and no secondary side current I_s goes through the rectifier diodes during the t_1-to-t_2 interval. The load is cut from the power stage during this interval and the primary resonant capacitor C_r, the leakage inductance L_k, and the magnetic inductance L_m resonate. No power is delivered to the secondary side at this interval, and the secondary voltage falls slightly below the output voltage V_{LED}.

To ensure against transformer saturation, the total flux through the transformer should satisfy:

$$\Phi_{total_max} \leq N_p \times Ae \times B_{max} \quad (4\text{-}18)$$

Where N_p is the turns of primary side, Ae is the effective cross-sectional area of the core and B_{max} is the desired maximum magnetic field intensity, which is usually between 0.2T and 0.3T.

The total flux Φ_{total} of the core is composed of two parts: the magnetic inductance flux, Φ_m, and the leakage inductance flux, Φ_{Lk}.

$$\Phi_{total}(t) = \Phi_m(t) + \Phi_{Lk}(t) = L_m \times I_m(t) + L_k \times I_{pri}(t) \quad (4\text{-}19)$$

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

Figure 37B shows the flux waveform through the core. The total flux increases from $-\Phi_{total_max}$ to $+\Phi_{total_max}$ from t_0 to t_2. The maximum total flux occurs at t_2, when the primary current is equal to the magnetic current, so:

$$\Phi_{total_max} = L_m \times I_{m(t2)} + L_k \times I_{pri(t2)} = (L_m + L_k) I_{m_max} = (1 + \frac{L_k}{L_m}) \cdot L_m \times I_{m_max} \quad (4\text{-}20)$$

Then L_m x I_{m_max} is the maximum magnetic flux as estimated from voltage-second (the multiple of the voltage and time) on the primary magnetic inductance or the secondary winding. For this LLC application, estimating the voltage-second from the secondary side is more convenient.

$$L_m * I_{m_max} = \frac{1}{2} \int_{t_0}^{t_2} \frac{V_{sec}(t)}{n} dt \approx \frac{1}{2} \cdot \frac{V_{LED}}{n} \cdot \frac{1}{2f_s} \quad (4\text{-}21)$$

The difference between the secondary voltage V_{sec} and the output voltage V_{LED} during the t_1-to-t_2 interval is negligible.

Considering the whole operating range, the maximum magnetic flux occurs at the minimum operating frequency condition. That is:

$$L_m \times I_{m_max} \approx \frac{1}{2} \frac{V_{LED_max}}{n} \cdot \frac{1}{2f_{s_min}} \quad (4\text{-}22)$$

From (4-18), (4-20) and (4-22), the number of primary-side windings is:

$$Np \geq \frac{\Phi_{total_max}}{A_e \times B_{max}} = (1 + \frac{L_k}{L_m}) \cdot \frac{V_{LED_max}}{4nf_{s_min} \times Ae \times B_{max}} \quad (4\text{-}23)$$

The minimum operating frequency f_{s_min} occurs at the minimum input voltage and maximum output voltage condition and could be estimated from the gain curve in figure 32 and following (4-24).

$$Gain(f_{s_min}) = \frac{2V_{o_max}}{nV_{in_min}} \quad (4\text{-}24)$$

The number of secondary-side windings is:

$$\begin{aligned} N_{SLED} &= n \times Np \\ N_{SBus} &= n_2 \times Np \end{aligned} \quad (4\text{-}25)$$

For this application, L_k/L_m=1/4, V_{LED_max}=120V, n≈0.49, the minimum operating frequency is around 55kHz, the Ae is 69mm^2, B_{max}=0.27T, then the turns of the primary side is:

$$Np \geq (1 + \frac{L_k}{L_m}) \cdot \frac{V_{LED_max}}{4nf_{s_min} \times Ae \times B_{max}} \approx 75 \quad (4\text{-}26)$$

Usually, designing the turns of DC bus winding first is a reasonable choice, as it gets the smallest number of turns. In this design the turns of the windings are N_{Sbus}=6, N_{SLED}=37, Npri=78.

(3) Estimate Ae x Aw. Select an appropriate core for the transformer before calculating the number of windings. One way is to estimate Ae x Aw, where Aw is the winding area of core.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

$$Aw = \frac{Np \times I_{pri(RMS)} + Ns \times I_{s(RMS)}}{J_c \times k_c} = \frac{Np \times I_{pri(RMS)} + Np \times (I_{pri} - I_m)_{(RMS)}}{J_c \times k_c} \quad (4\text{-}27)$$

J_c is the desired current density through the wire (usually 5 to 7A/mm^2), k_c is coefficient for the winding window (0.1 to 0.2 for isolated applications).

As I_m is not the main part of the primary current, it could be neglected here, so that:

$$Aw \approx \frac{2Np \times I_{pri(RMS)}}{J_c \times k_c} \quad (4\text{-}28)$$

From (4-23), Aw is:

$$Aw \geq (1 + \frac{L_k}{L_m}) \frac{V_{LED_max} \times I_{pri(RMS)}}{2nf_{s_min} \times Ae \times B_{max} \times J_c \times k_c} \quad (4\text{-}29)$$

Then Ae x Aw is:

$$Ae \times Aw \geq (1 + \frac{L_k}{L_m}) \frac{V_{LED_max} \times I_{pri(RMS)}}{2nf_{s_min} \times B_{max} \times J_c \times k_c} \quad (4\text{-}30)$$

Where the primary current $I_{pri(RMS)}$ is estimated in (4-17).

(4) Select the wire for the winding.

The secondary winding currents could be roughly estimated from the average current of the LED and DC bus, assuming the winding currents are sinusoid.

$$I_{s_Bus(RMS)} \approx \frac{\sqrt{2}}{2} \frac{\pi}{2\sqrt{2}} I_{Bus(avg)} = \frac{\pi P_{Bus}}{4 \times V_{bus}} = \frac{\pi \times n \times P_{Bus}}{4 \times n_2 * V_{LED}} = 2A$$
$$I_{s_LED(RMS)} \approx \frac{\pi}{\sqrt{2}} I_{LED(avg)} = 0.3A \quad (4\text{-}31)$$

Note that the actual currents would be a little higher as the winding currents are discontinuous and not standard sinusoid. Usually, using 1.2 times of these values to estimate the winding currents is reasonable. With the primary current and the secondary current, the size of the wire could be selected accordingly.

4.3.3 Rectifier Diodes Selection (DCbus :D19, LED driver : D22,D23,D24,D26,D27,D28,D29,D30)

(1) The rectifier diodes should be fast recovery diodes.

(2) The voltage stress of the rectifier diodes equals the output voltage. The voltage rating of the diodes should be over 1.5 times of the maximum output voltage. For this application, use 200V diodes for the LED driver rectifier and 100V diodes for the DC bus rectifier.

(3) The average current through the rectifier diodes for the LED driver equals to the LED current. The current rating for these diodes should be at least 3 times of the LED current. For this 130mA application, select diodes with 0.5A or 1A current rating.

(4) The average current through the rectifier diode for the DC bus equals to the DC bus current. The current rating for this diode should be at least 5 times of the DC bus current. For this application, select diode with 20A current rating.

(5) The power consumption of the rectifier-diode packages requires consideration. Usually the rectifier diode for the DC bus could choose TO-220 package and SMA package will work for the LED driver rectifier diodes.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

This design uses rectifier diodes with a 200V/3A rating in SMB packages for the LED driver and 100V/20A in TO-220 package for the DC bus.

4.3.4 Current Balance Capacitor Selection (CX3, CX4)

The current balance capacitors CX3 and CX4 are used to balance the currents through LED strings connected to same winding. They block the different voltages between the LED strings and balance the LED current.

Figure 38 shows the capacitor current balance circuit for 2 LED strings. Figure 39A shows the operating waveforms when $f_s<f_0$ and Figure 39B shows the operating waveforms when $f_s>f_0$.

In the positive half-cycle from Figure 39A and Figure 39B, I_s goes through D22 and D26 and equals I1. In the negative half cycle, I_s goes through D24 and D23, and equals to I2. As the balance capacitor CX3 blocks the DC current, I1 and I2 have the same average value.

$$Avg(I1) = Avg(I2) \tag{4-32}$$

The average value of I1 equals the LED current I_{LED1}, and the average value of I2 equals the LED current I_{LED2}, allowing the capacitor C23 to balance the LED current.

$$I_{LED1} = Avg(I1) = Avg(I2) = I_{LED2} \tag{4-33}$$

When $f_s<f_0$, the secondary current I_s is discontinuous. The conduction time of D22 and D24 (also the width of the currents I1 and I2 through the rectifier diodes) is less than 50% switching cycle. The voltage V1 and V2 are shown in Figure 39A. The average value of V1 is a little smaller than ½ V_{LED1}, and the average value of V2 is a little smaller than ½ V_{LED2}. As the secondary winding of the transformer cannot handle a DC voltage, the DC voltage across the balance capacitor C23 is:

$$V_{C_fs<f0} = Avg(V1_{fs<f0}) - Avg(V2_{fs<f0}) \approx \frac{1}{2}(V_{LED1} - V_{LED2}) \tag{4-34}$$

When $f_s>f_0$, the secondary current is continuous. The conduction time of D22 and D24 is 50% of the switching cycle. The average value of V1 is ½ V_{LED1}, and the average value of V2 is ½ V_{LED2}, as shown in Figure 39B. Then the DC voltage across the balance capacitor C23 is:

$$V_{C_fs>f0} = Avg(V1_{fs>f0}) - Avg(V2_{fs>f0}) = \frac{1}{2}(V_{LED1} - V_{LED2}) \tag{4-35}$$

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

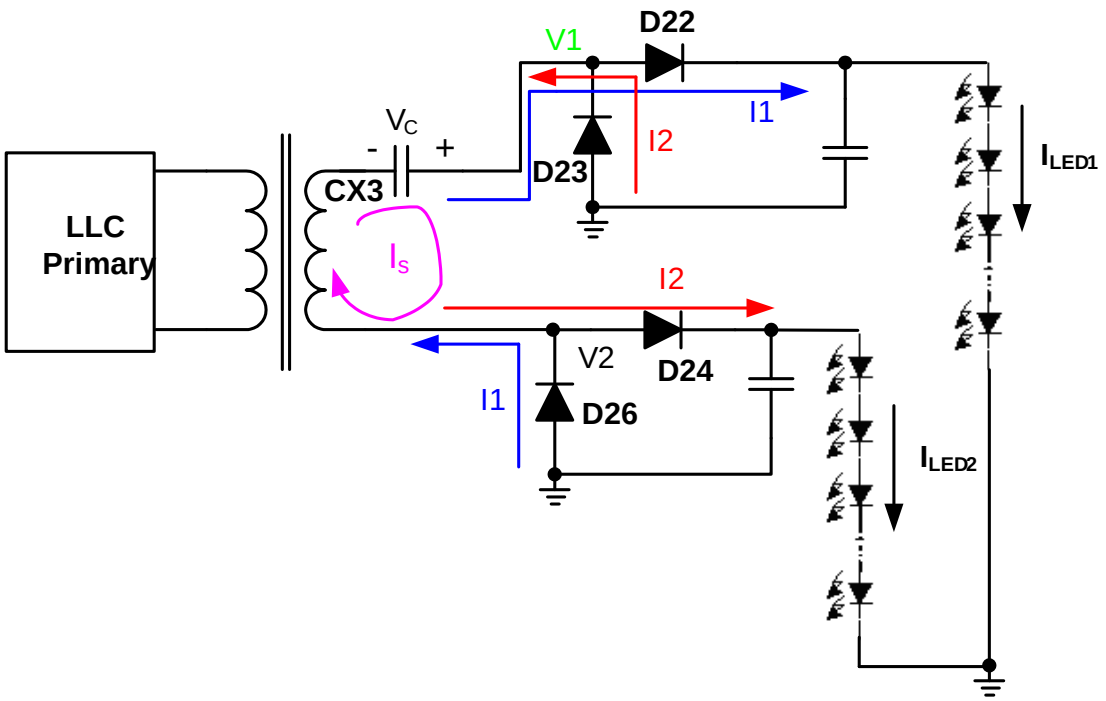


Figure 38—Power Stage of Capacitor Current Balance Circuit for 2 LED Strings

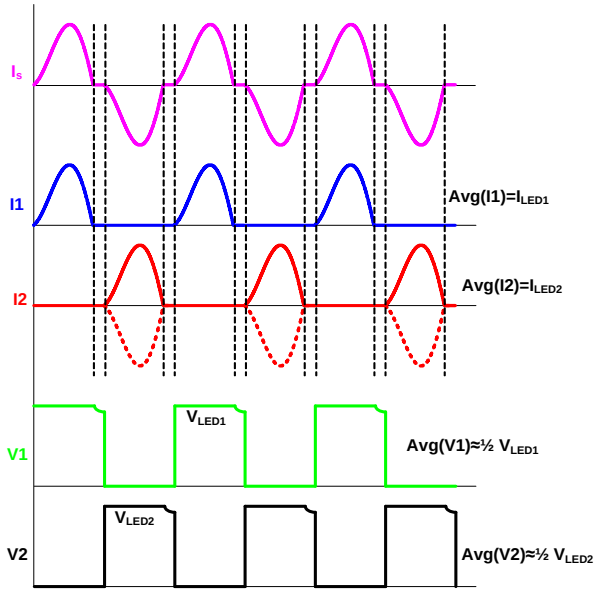


Figure 39A—Operating Waveforms When $f_s<f_0$

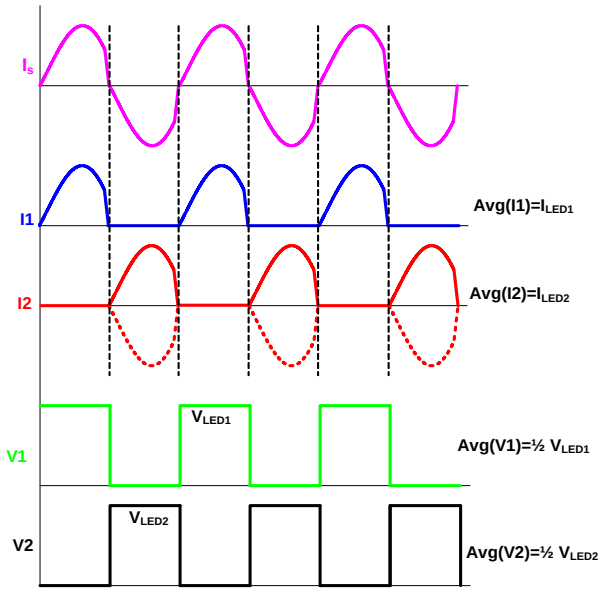


Figure 39B—Operating Waveforms When $f_s>f_0$

Figure 39—Operating Waveforms of Capacitor Current Balance Circuit

The current balance capacitor CX3 blocks the voltage difference between the LED strings, ensures that no DC voltage is applied to the secondary winding, and ensures stable operation.

(1) The value of CX3 and CX4 could be in range of 0.22μF to 1μF to limit their influence on the resonant tank.

(2) The voltage rating of these current balance capacitors should be higher than the maximum output voltage, to guard against short LED string condition,

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

(3) The RMS currents through CX3 and CX4 are the secondary winding currents for LED driver, RMS value as calculated by (4-31).

$$I_{Cb} = I_{s_LED(RMS)} \approx \frac{\pi}{\sqrt{2}} I_{LED(avg)} = 0.3A \quad (4\text{-}36)$$

The actual current could be higher than this value, use 1.2 times of this value to select the current rating.

(4) Use a MMKP or CBB capacitor for CX3 and CX4 to handle the current.

4.3.5 Current Balance Choke Selection (T4)

The balance choke T4 is used to balance the current through the two secondary windings. And therefore, the currents through the whole 4 LED strings are balanced. Figure 40 shows the balance scheme and its operating waveforms. The voltage across the balance caps in 4.3.4.

$$\begin{aligned} V_{Cb1} &\approx \frac{1}{2}(V_{LED1} - V_{LED2}) \\ V_{Cb2} &\approx \frac{1}{2}(V_{LED3} - V_{LED4}) \end{aligned} \quad (4\text{-}37)$$

At the positive half switching cycle, the currents through the secondary windings go through the loops as I1 and I3 (red loop), the voltages across the windings of the choke are:

$$\begin{aligned} V_{Choke1}(t_p) &= V_x(t_p) - V_{Cb1} - V_{LED1} = V_x(t_p) - \frac{1}{2}(V_{LED1} + V_{LED2}) \\ V_{Choke2}(t_p) &= -(V_x(t_p) - V_{Cb2} - V_{LED4}) = -(V_x(t_p) - \frac{1}{2}(V_{LED3} + V_{LED4})) \end{aligned} \quad (4\text{-}38)$$

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

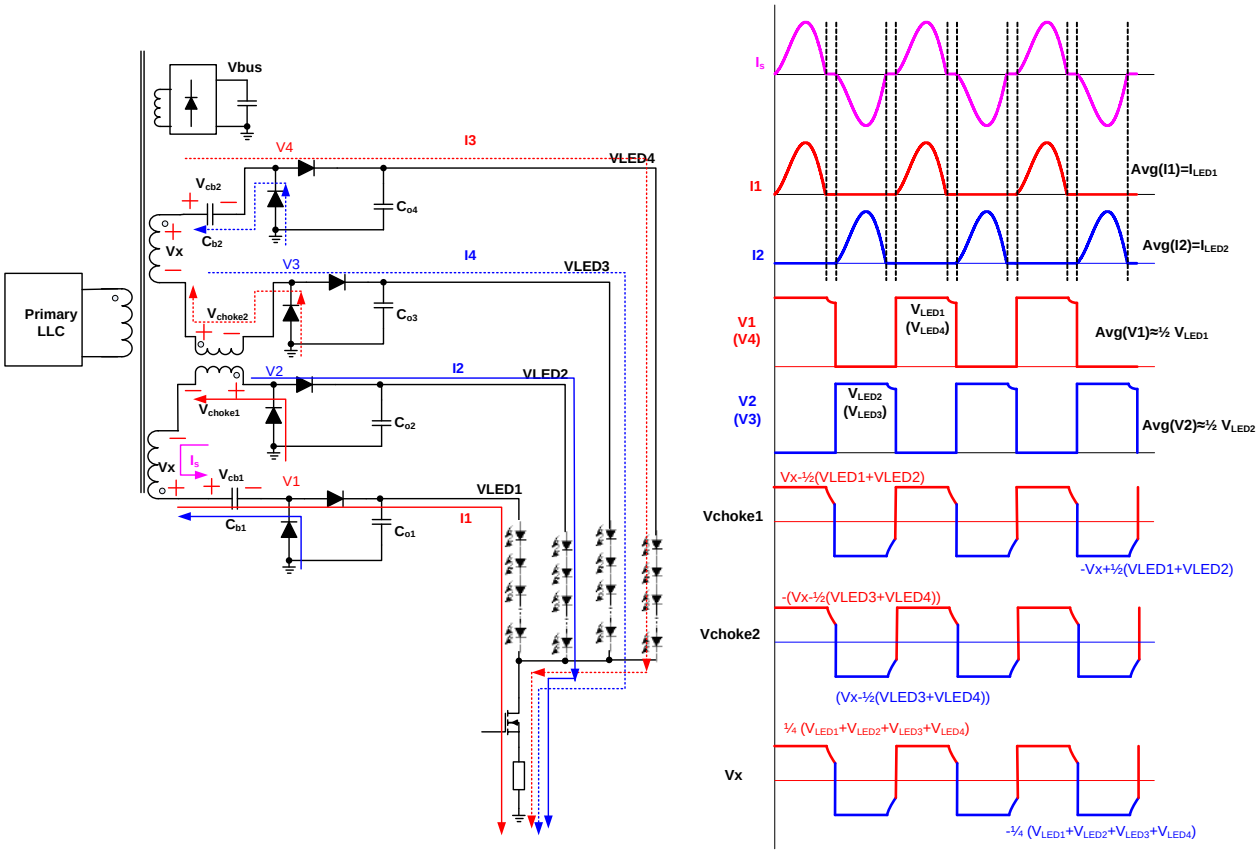


Figure 40—Choke+ Cap Balance Circuit and Operating Waveforms

As the turn ratio of the choke is 1:1, V_{choke1} should be equal to V_{choke2}, and then can get:

$$V_x(t_p) = \frac{1}{4}(V_{LED1} + V_{LED2} + V_{LED3} + V_{LED4}) \quad (4\text{-}39)$$

At the negative half switching cycle, the currents through the secondary windings go through the loops as I2 and I4 (blue loop), the voltages across the windings of the choke are:

$$V_{Choke1}(t_n) = V_x(t_n) - V_{Cb1} + V_{LED2} = V_x(t_n) + \frac{1}{2}(V_{LED1} + V_{LED2})$$
$$V_{Choke2}(t_n) = -(V_x(t_n) - V_{Cb2} + V_{LED3}) = -(V_x(t_n) + \frac{1}{2}(V_{LED3} + V_{LED4})) \quad (4\text{-}40)$$

The V_{choke1} should also be equal to V_{choke2} at the negative half switching cycle.

$$V_x(t_n) = -\frac{1}{4}(V_{LED1} + V_{LED2} + V_{LED3} + V_{LED4}) \quad (4\text{-}41)$$

From (4-38) to (4-41), can get the amplitude of the voltages across the secondary windings is the average voltage of the total four LED strings. The amplitude of the voltage across the choke winding is the different voltage of the LED strings on the two secondary windings.

As the choke T4 is used to balance the current through the two secondary windings, following could be the selection of it parameters:

(1) Turn ratio: 1:1

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

(2) Inductance: The inductance of the choke winding should be larger than 5mH to make the magnetic current negligible comparing to the LED current. For a smaller LED current, the inductance should be larger.

(3) Winding current: the winding current of the choke equals to the secondary winding current of the transformer as shown in (4-36).

4.3.6 Output Capacitor Selection (C37, C45, C53, C57, and DC bus output cap C30)

The output caps C37, C45, C53,C57 filter the rectified secondary currents to obtain a DC current through the LED strings, and also to hold the output voltage at PWM off interval.

For stable operation, as shown in Figure 41, the current though the output capacitors are:

$$I_{Cout}(t) = I1(t) - I_{LED1} \quad (4\text{-}42)$$

Assuming a sinusoid current through the secondary winding, its RMS value is:

$$I_{Cout_RMS} = RMS(I1(t) - I_{LED1}) = \sqrt{\frac{1}{2}I_{s_LED(RMS)}^{2} - I_{LED1}^{2}} = \frac{\sqrt{\pi^2 - 4}}{2}I_{LED1} \quad (4\text{-}43)$$

Estimate the RMS current of the output cap at 1.2 times of the value in (4-43), as the current is not standard sinusoid.

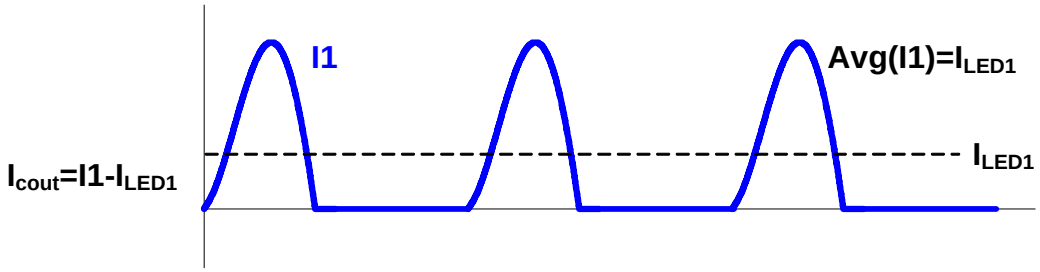


Figure 41—Current though the Output Capacitors of LED Stage

(1) The values of C37, C45, C53 and C57 could between 10uF and 100uF
(2) The voltage rating should be over 1.2 times of the maximum output voltage.
(3) The current rating should be over 1.2 times of the value in (4-43)

The selection for the DC bus output capacitor C30 should also consider its RMS current. Similar to the RMS current of the output capacitor of the LED stage, the current through the capacitor is shown as figure 42.

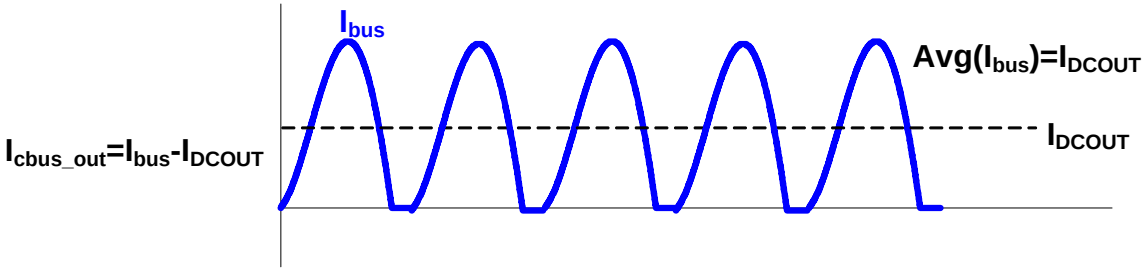


Figure 42—Current through the output capacitor of Bus Stage

The RMS current through the output capacitor of the DC bus could be estimated with 1.2 times of the following value:

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

$$I_{cbus_out_RMS} = RMS(I_{bus} - I_{DCOUT}) = \sqrt{\frac{\pi^2}{8} I_{DCOUT}^2 - I_{DCOUT}^2} = 0.48 I_{DCOUT} \quad (4\text{-}44)$$

C30 could be selected with the following:
(1) The value of C30 could be in range of 470uF to 2mF considering the output power range
(2) The voltage rating of C30 is usually 35V
(3) The current rating of C30 should be over 1.2 times of the value of (4-44)

4.3.7 Dimming MOSFET Selection (Q13)

The dimming MOSFET Q13 directly dims the LED current for fast PWM dimming and to achieve a high PWM dimming ratio. Choose a MOSFET based on the following criteria:

(1) The voltage rating of Q13 should be over 1.2 times of the maximum output voltage
(2) The current through the MOSFET is the sum of the currents through all the LED strings: the current rating of Q13 should be over 3 times of this current.
(3) Consider the power consumption and system efficiency when selecting the conduction resistance R_{Dson} and the package.

4.3.8 Protection MOSFET Selection (Q8)

The protection P-Chanel MOSFET Q8 is used to disconnect the LED driver stage from the system at LED driver stage fault condition, and therefore the DC bus stage (the system power supply) would not be influenced by the protection of the LED driver stage. The selection of the P-Channel MOSFET is similar to Q13, per the following criteria:

(1) Voltage rating: over 1.2 times of the maximum output voltage.
(2) Current rating: over 3 times of the total winding current.
(3) Should consider the power consumption and system efficiency when selecting the Rdson and package.

4.4 Control Circuit Design

The control circuit design includes the gate drive transformer design, the frequency setup, the DC bus feedback, the DC bus short protection, open LED protection and short LED protection.

4.4.1 Gate drive Transformer

The MP4653 controls the LLC power stage from the secondary side. It uses a gate drive transformer to drive the power MOSFETs in the power stage.

(1) As the MP4653 provides a regulated 9.3V driver voltage, use a gate-drive–transformer turn ratio of 1:1:1 to 1:1.6:1.6 so that the amplitude of the driver voltage for the MOSFETs is in the 9.3V to 15V range, as shown in figure 43A. Usually, a 1.3 or 1.5 turn ratio is preferred considering the start up voltage at around 5V.
(2) The drive current consists of 2 parts: one part drives the power MOSFETs in the power stage, the other part is the magnetic current of the gate drive transformer. Make the magnetic inductance higher than 2mH to reduce this magnetic current. The principle is described in 3.1 and shown in Figure 15.
(3) Usually, an EE16 core will suffice for the gate drive transformer. As the gate-drive transformer isolates the hot-side power stage and the cold-side control circuit, use triple isolated wires for the cold side (winding N2 in figure 43), such as TEX-EΦ0.2. Use the sandwich winding method to decrease the leakage inductance, as shown in figure 43B.
(4) Add a 1nF or 2.2nF Y capacitor between the hot-side ground and the cold-side ground to reduce EMI noise.

MPS CONFIDENTIAL
INTERNAL USE ONLY
DO NOT DISTRIBUTE

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

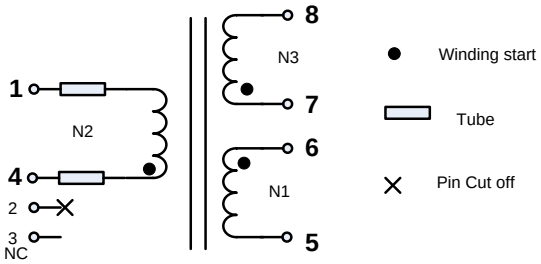


Figure 43A—Schematic

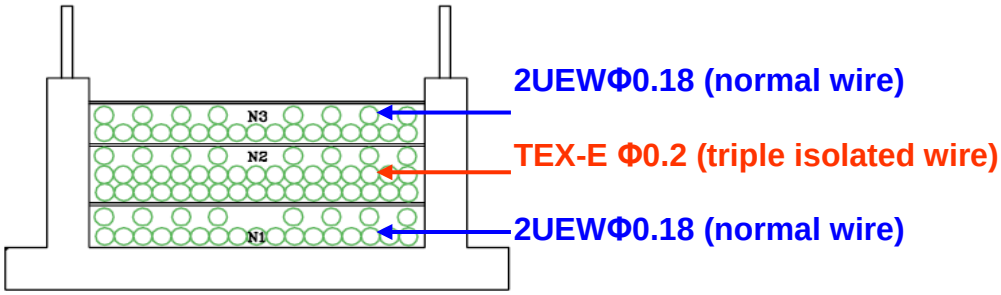


Figure 43B—Winding structure and Wire

Figure 43—Gate drive Transformer Schematic and Its Winding

4.4.2 DC Bus Voltage Feedback Network Design

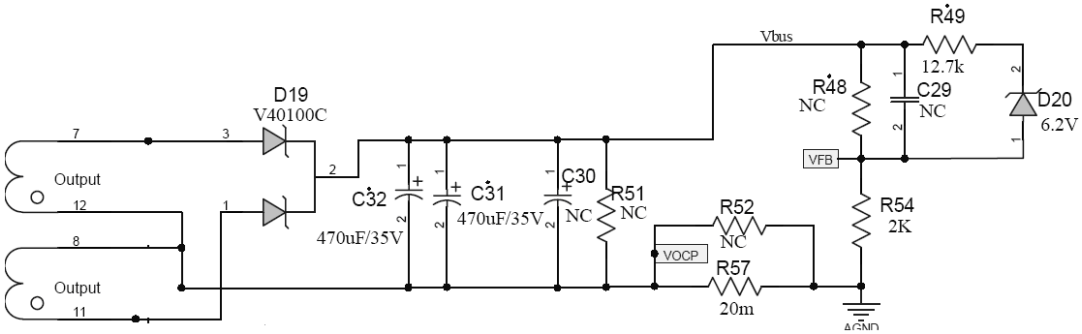


Figure 44—DC Bus Voltage Feedback

The DC bus voltage feedback network is shown as figure 44. It uses a voltage divider and a zener diode to feed back the bus voltage. As described in previous, the bus voltage is designed in range of 15V to 20V for the full LED voltage range, the protection point of the bus voltage could be 22V to 24V. As the VFB voltage gets a low clamp voltage at 1.2V and its over voltage protection threshold is 2.4V, the voltage divider and zener diode could be selected with following equations:

$$\begin{aligned} 1.2V * \frac{R49 + R54}{R54} + V_{ZD20} &= 15V * 0.97 \\ 2.4V * \frac{R49 + R54}{R54} + V_{ZD20} &= 23V \end{aligned} \quad (4\text{-}45)$$

The resistor R54 could be 1kΩ to 10kΩ, choose a 2kΩresistor for R54. The zener diode D20 is selected a 6.2V zener diode and R49=12.7kΩ.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

The selection of R57 for over current protection for the DC bus stage could be:

$$R57 = \frac{100mV}{2 * I_{DCOUT_max}} \approx 20m\Omega \quad (4\text{-}46)$$

Please refer to 3.2.2 for the details.

4.4.3 LED Voltage Feedback Network Design

The design of the LED voltage feedback network is described as 3.2.7. Setting the over voltage protection point at 1.2 times of the maximum LED voltage and the voltage difference protection at 20% of the LED voltage, from 3-14 and 3-15 can get:

R_{OVPH} is usually choose 1MΩ to limit the leakage current through the output, and then:

$$R_{OVPL} = \frac{R_{OVPH}}{\frac{1.2V_{LED_max}}{2.4V} - 1} = 17k\Omega$$

$$R_{input} = \frac{16 * 23k\Omega * 20\% * V_{LED}}{1.2V_{LED_max}} - 23k\Omega = 33k\Omega \quad (4\text{-}47)$$

$$R_{OV} = R_{input} - \frac{R_{OVPH} * R_{OVPL}}{R_{OVPH} + R_{OVPL}} = 16.3k\Omega$$

4.4.4 Frequency Set and Soft Start

As describe in 3.2.1, the frequency setting and soft start resistors on FSET and SS pin could be get from 3-3,3-4 and 3-5. Choose the minimum frequency limit at around 50kHz and maximum frequency limit at 180kHz, can get:

$$R_{FSET} = \frac{(2.2V - 1V) * 1.98 * 10^9}{f_{max} - f_{min}} = 18.2k\Omega$$

$$R_{SS_FSET} = \frac{2 * 1.49V}{\frac{f_{min}}{1.98 * 10^9} + \frac{2.2V}{R_{FSET}}} = 20k\Omega \quad (4\text{-}48)$$

Setting the soft start frequency at around 300kHz, can get:

$$R_{SS} = \frac{2 * 1.49V}{\frac{f_{s_start}}{1.98 * 10^9} + \frac{1V}{R_{FSET}} - \frac{2 * 1.49V}{R_{SS_FSET}}} = 52k\Omega \quad (4\text{-}49)$$

Choose around 2ms soft start time, can get:

$$C_{SS} \approx \frac{T_{SS}}{3R_{SS}} = 13nF \quad (4\text{-}50)$$

Choose C_{SS}=10nF.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

4.4.5 LED Current Feedback and Short Protection

Figure 45 shows the feedback network of the LED stage. The current feedback design is described in 3.2.5. The current sensing resistor is:

$$R_{sense} = \frac{0.2V}{I_{LED_total}} = \frac{0.2V}{0.13A * 4} = 0.385\Omega \quad (4\text{-}51)$$

A 1kΩ resistor is recommended between the IFB pin and the LED current sensing resistor to protect the condition when the LED+ is short to LED- at operation. A high voltage may be applied to the IFB pin directly if without this resistor (R77 in figure 45).

The secondary side current of the LED stage is sensed to SSD pin for over current protection (short protection). Choose the over current protection point at 2 times of the normal current, then the over current protection resistor is:

$$R_{OCP} = \frac{0.2V}{2 * I_{LED_total}} = \frac{0.2V}{2 * 0.13A * 4} = 0.192\Omega \quad (4\text{-}52)$$

A 1kΩ resistor is recommended between the SSD pin and the over current sensing resistor R_{OCP} to protect the condition when the LED+ is short to GND at operation. A high voltage may be applied to the SSD pin directly if without this resistor (R80 in figure 45). A small capacitor like 1nF could be added from SSD to GND to filter the switching noise.

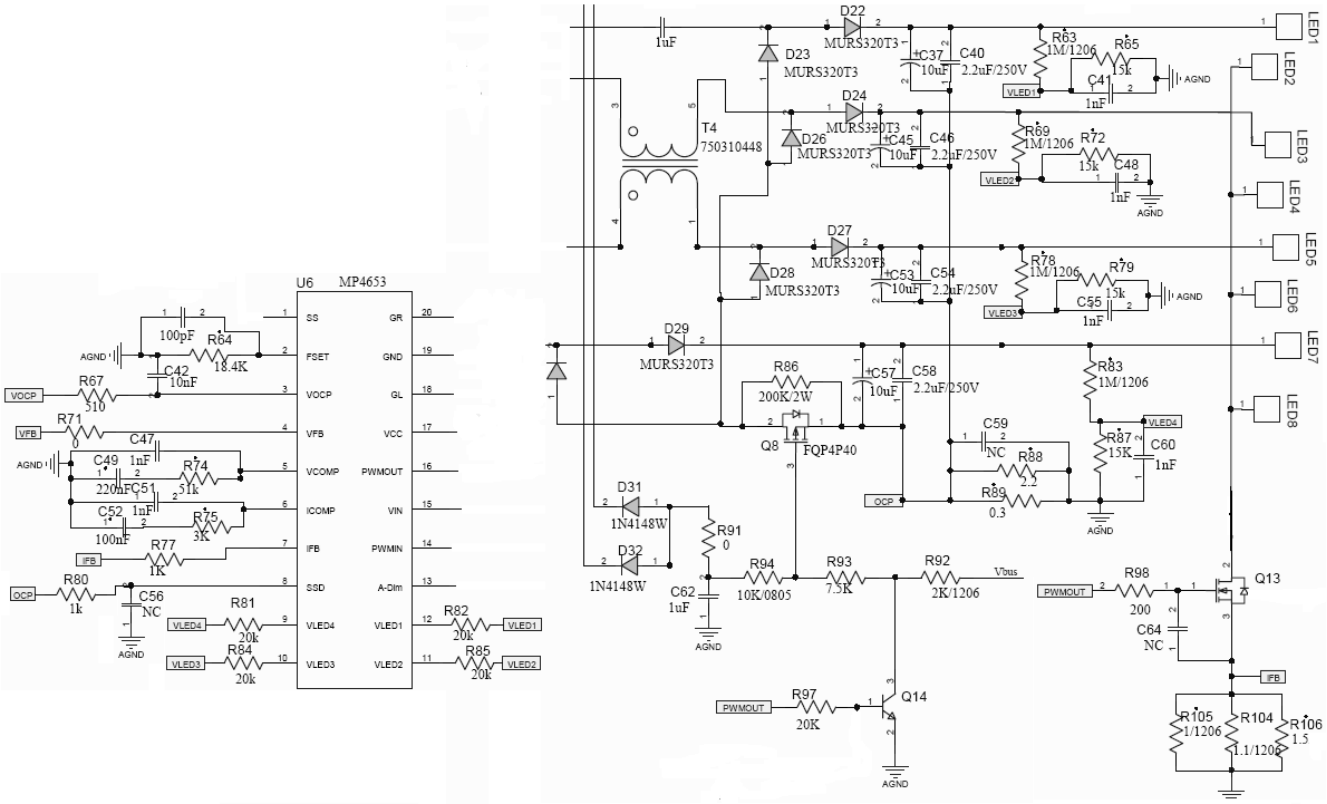


Figure 45—MP4653 LED Stage Feedback Network

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

4.4.6 System Error Signal

The MP4653 uses the PWMOUT signal to generate a system error signal as described in section 3.2.9, with the schematic shown by Figure 25. In this design, the RC time constant is 10ms, R_{error}=100kΩ, C_{error}=0.1μF.

4.4.7 System Power Start Up

Figure 46 shows the MP4653 system power start up scheme and its sequence. The MP4653 is directly supplied by the system standby flyback through a diode. When the AC input power is applied, the STB flyback operates gradually, the MP4653 is supplied by the STB flyback through a diode and gets around 5V voltage on VIN pin. The MP4653 starts to operate with this 5V voltage and outputs energy to the secondary side, and then the V_{bus} voltage is charged up gradually. When the V_{bus} voltage is higher than 5V, it starts to supply the MP4653. The 12V output for system supply will be set up after the V_{bus} voltage is established.

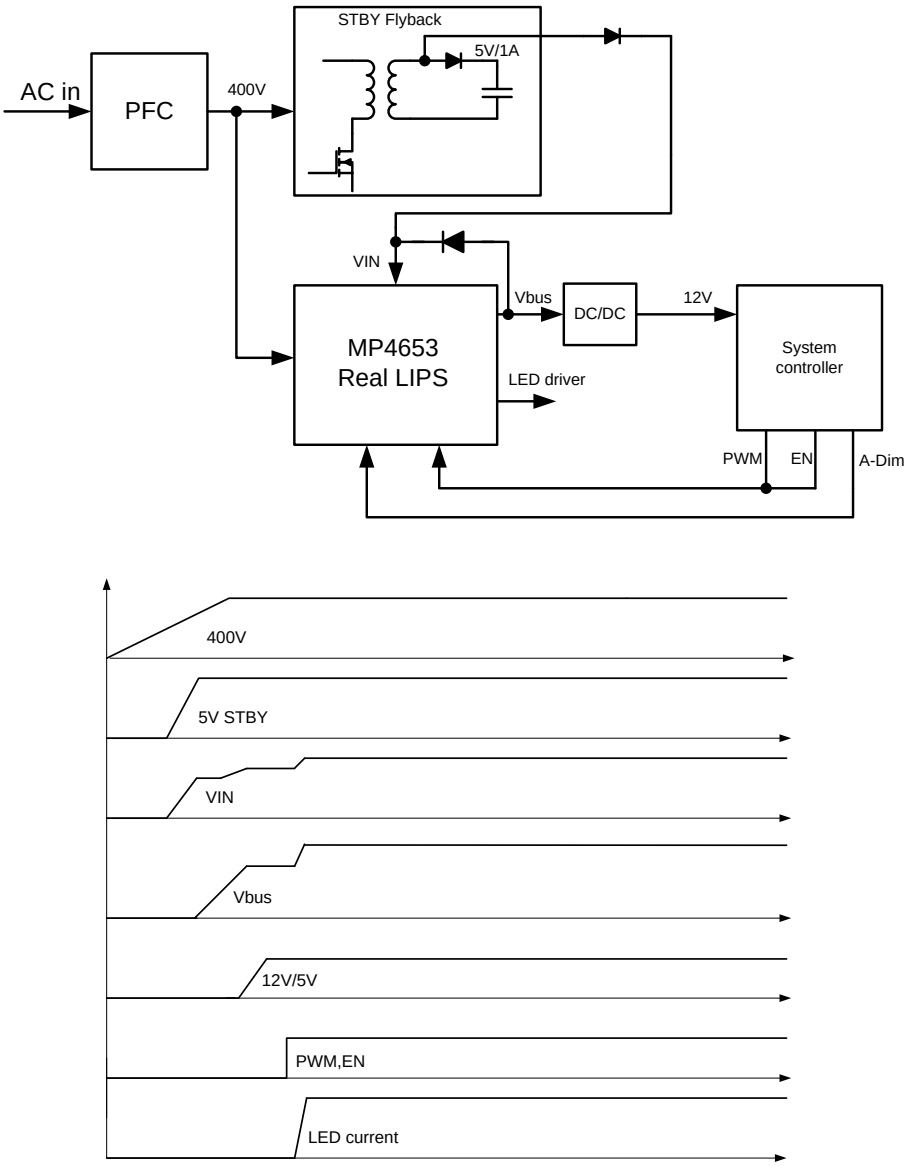
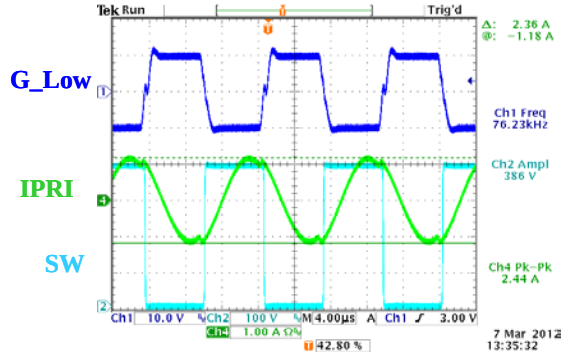


Figure 46—MP4653 System Power Start up Scheme and Sequence

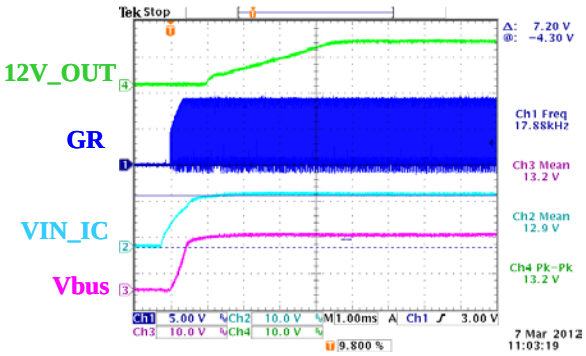
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.

4.5 Test Results

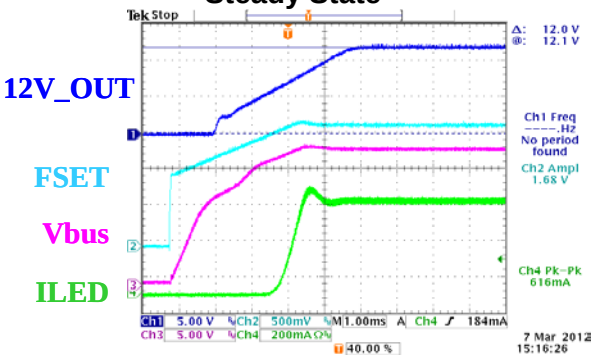
Test condition: VIN_IC=12V, VLED=120V, ILED=130mA, 4 strings, DC/DC output=12V/1.5A, unless otherwise noted.



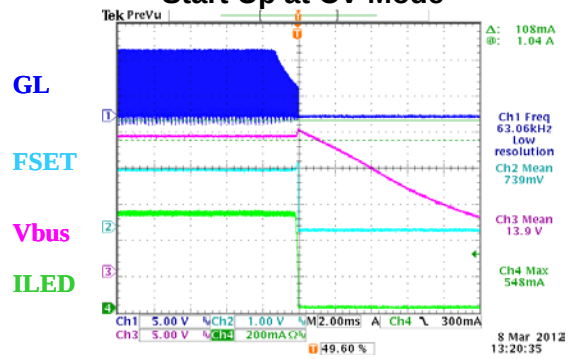
Steady State



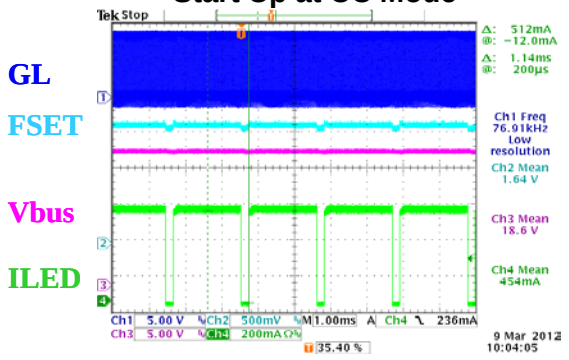
Start Up at CV Mode



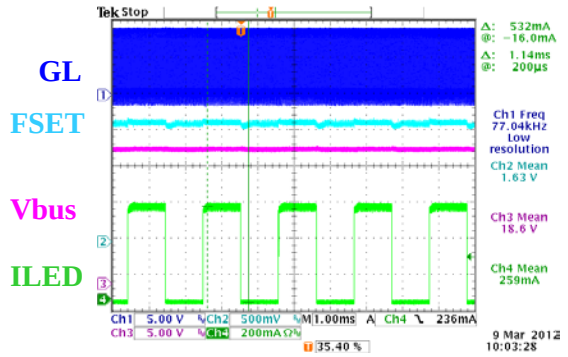
Start Up at CC Mode



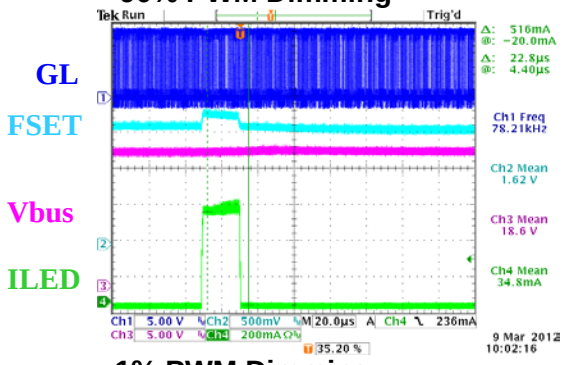
IC Power Off



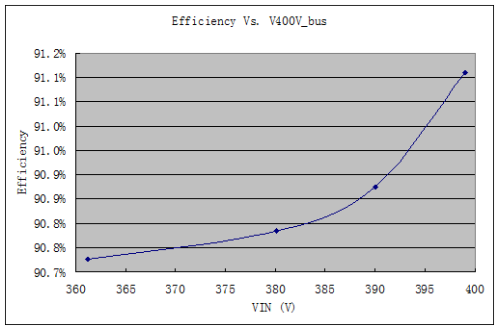
90% PWM Dimming



50% PWM Dimming

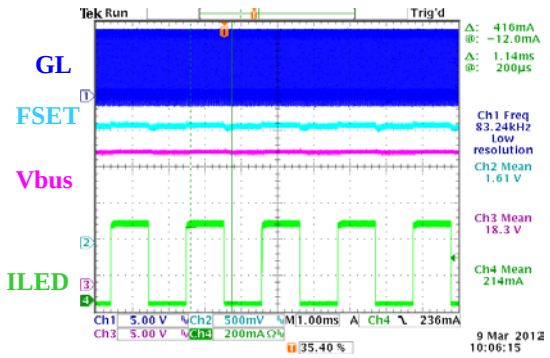


1% PWM Dimming

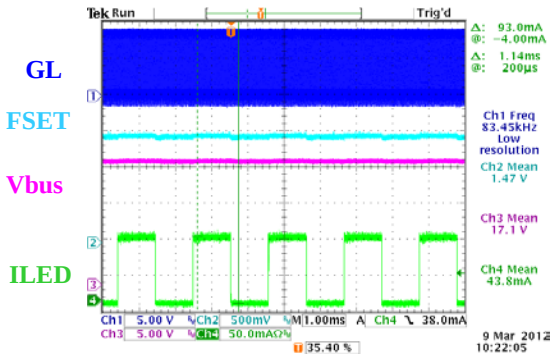


Efficiency (12V/3A output for DC/DC)

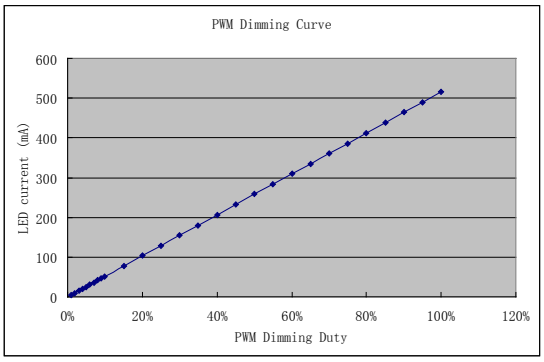
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.



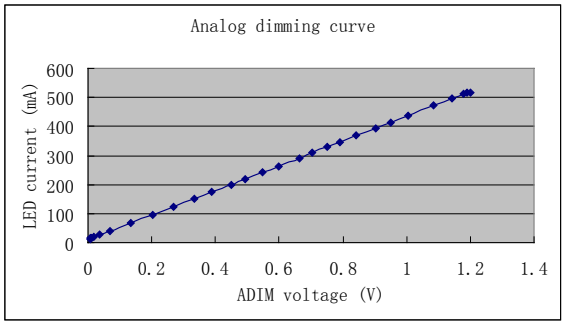
PWM+ Analog Dimming (A_Dim=0.99V)



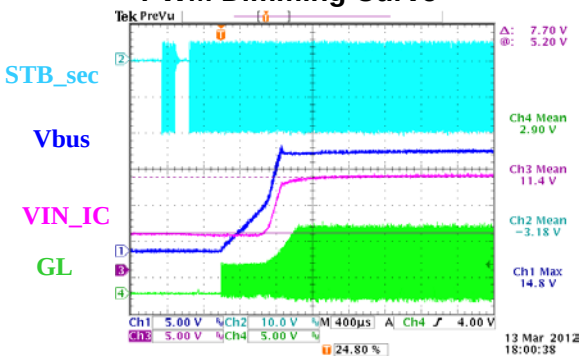
PWM+ Analog Dimming (A_Dim=0.19V)



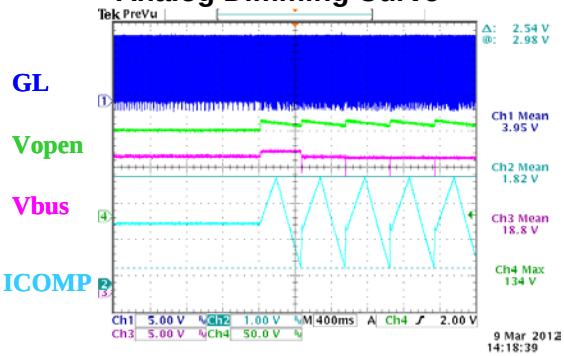
PWM Dimming Curve



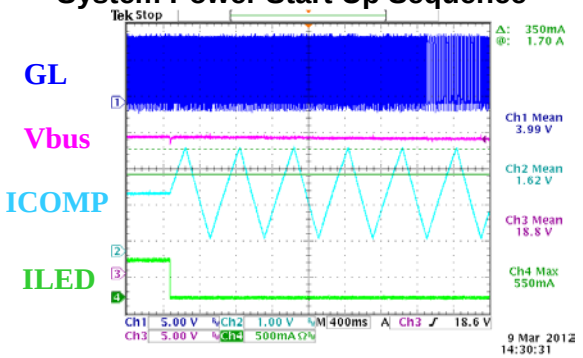
Analog Dimming Curve



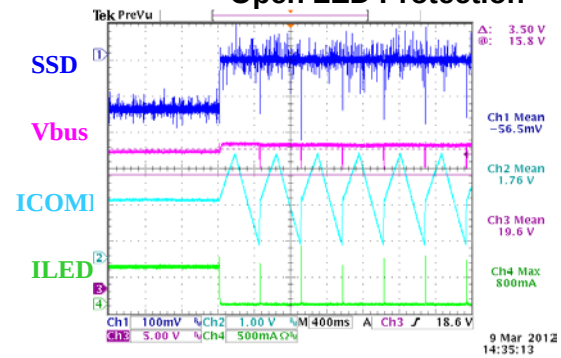
System Power Start Up Sequence



Open LED Protection

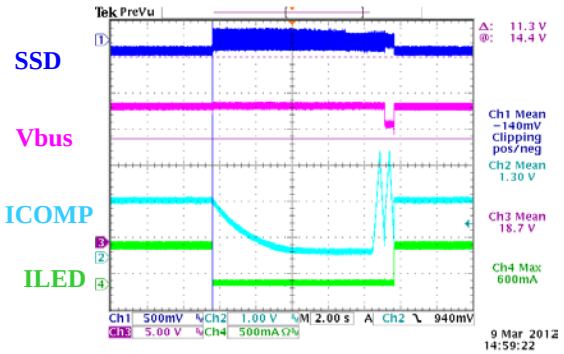


LED+ to LED- Short Protection

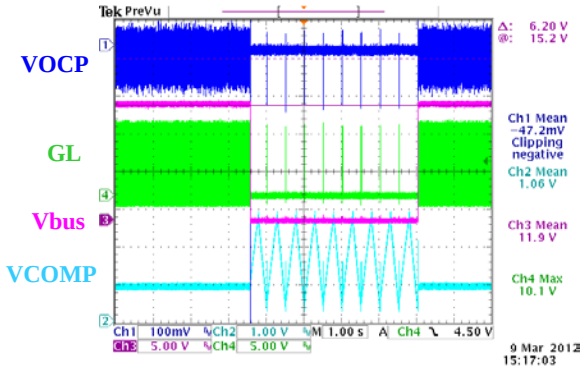


LED- to GND Short Protection

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.



LED+ to GND Short Protection



V_{bus} to GND Short Protection

5. SUMMARY

(1) The MP4653 based Real LIPS structure gets a good performance for large size TV LED backlighting. The LED current, the 12V system power supply and the 5V standby power supply are all regulated independently, and get a good accuracy and performance.

(2) The MP4653 based Real LIPS structure features low BOM cost and high efficiency.

(3) Audible noise elimination comparing with the traditional 2-stage structure.

(4) The integrated protection interface provides sufficient protection for the system.

NOTICE: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2014 MPS. All Rights Reserved.