MP4021A, Primary-Side-Control with Active PFC Offline LED Controller Application Note

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1. INTRODUCTION

The MP4021A is a primary-side-control offline LED lighting controller with PFC integrated. The primary-side-control can significantly simplify the LED lighting driving system by eliminating the opto-coupler and the secondary feedback components in an isolated single stage converter. Its proprietary real current control method can accurately control the LED current from the primary side information. Internally integrated current accuracy compensations can enhance the LED current accuracy for line input voltage variation (universal input voltage range), output voltage variation and transformer inductance tolerance.

The MP4021A integrates power factor correction function and works in boundary conduction mode. The power factor correction function can achieve the PF>0.9 in a universal input voltage range. The boundary conduction mode operation can reduce the switching losses and improve the EMI performance.

The extremely low start up current and the quiescent current can reduce the power consumption thus lead to an excellent efficiency performance.

The MP4021A provides multiple advanced protections to enhance the system safety. The protections include over-voltage protection, short–circuit protection, cycle-by-cycle current limit, VCC UVLO and thermal shutdown.

The special construction inside the FB pin allows MP4021A also quite suitable for non-isolate applications. In non-isolate condition, the feedback signal can be directly applied on FB pin.

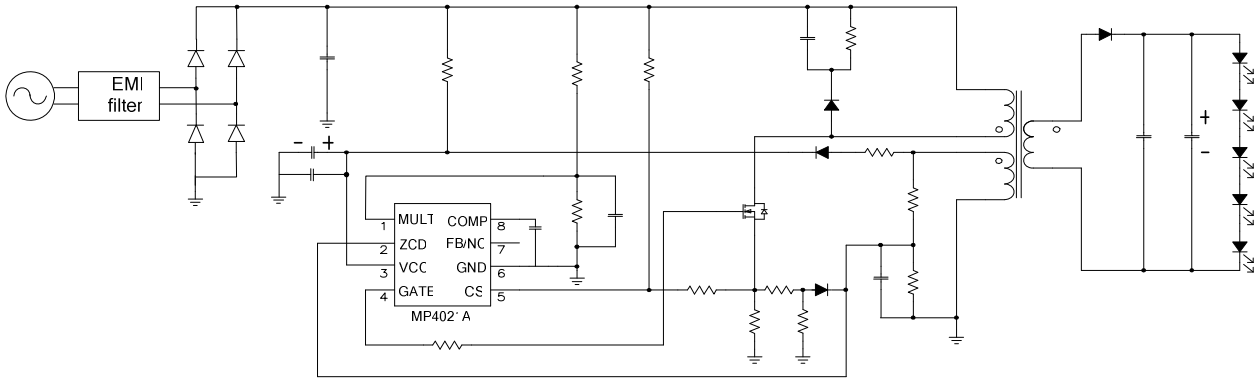


Figure 1—Typical Application

2. RIMARY-SIDE-CONTROL, BOUNDARY CONDUCTION MODE OPERATION WITH PFC

The conventional off-line LED lighting driver usually uses the secondary side control. The LED current is directly sensed in the secondary side and fed to comparison with the reference which is typically made up by TL431, the EA output is compensated and fed to primary side by an opto-coupler to determine the duty cycle and thus regulate the LED current. Although this control method has its advantage that directly control the LED current and the current accuracy can be conformed in any conditions, but it also brings obvious disadvantages, lots of circuits and components are needed in the secondary side, including sensing circuit, comparison and compensation circuit, opto-coulpler and bias power supplies which significantly increases the cost and system complexity.

Besides, the primary side input stage of a conventional LED lighting driver typically uses a full wave rectifier bridge with an E-cap filter to get an unregulated DC voltage. The E-cap should be large enough to keep a relatively low ripple on the DC voltage. This means the instantaneous input line voltage is lower than the DC voltage on the E-cap most time of a line half-cycle, thus the rectifier diodes only conduct a small portion and make the line input current like a series of narrow pulses whose amplitude maybe 10 times higher than the average DC level. A lot of drawbacks are resulted: much higher peak and RMS current draw from the line, distortion of the line input current causes a poor power factor (most time only 0.5-0.6) and induces large high harmonic contents.

As Shown in Figure 1, the MP4021A uses primary-side-control, no need any secondary feedback components, which can sharply reduce the component amount and cost. As we know, the LED current is the average current of transformer secondary side during a line half-cycle $I_o = I_{s\_avg}$, the MP4021A can calculate the average current of the transformer secondary side from the primary side information and control it to a required value, this is the MP4021A primary-side-control principle.

The MP4021A integrates power factor correction function and works in boundary conduction mode. The boundary conduction mode, makes the transformer work on the boundary between the continuous and discontinuous mode, which is quite different from the well-known resonant converter. Figure 2 shows the drain-source voltage waveform of primary switch in a conventional current-mode flyback converter operating in the discontinuous conduction mode (DCM). During the first time interval, the drain current ramps up to the desired current level. The power MOSFET then turned off. The leakage inductance in the flyback transformer rings with the MOSFET parasitic capacitance and causes a high voltage spike, which is limited by a clamp circuit. After the inductive spike has damped, the drain voltage equals to the input voltage plus the reflected output voltage. The drain voltage would immediately drop to the bus voltage when the current in the output diode drops to zero if the parasitic ring of the primary inductance and the parasitic capacitance is ignored. However, the drain voltage rings down to this level as shown in Fig 2 due to the parasitic resonance by the primary inductance and the total parasitic capacitance.

For example, the inductance is 1mH and the parasitic capacitance is 100pF, then the resonant frequency is 500kHz. The resonant circuit is lightly damped and the resonant frequency given below is independent of the input voltage and load currents:

$$f_{resonant} = \frac{1}{2\pi \cdot \sqrt{L_m \cdot C_{eqp}}}$$

Where L_m is the primary inductance; C_{eqp} is the equivalent primary side parasitic capacitance which including parasitic capacitance of the primary winding, the parasitic capacitance of the MOSFET and the parasitic capacitance of the secondary side (including the secondary winding and output rectifier diode) reflect to primary side.

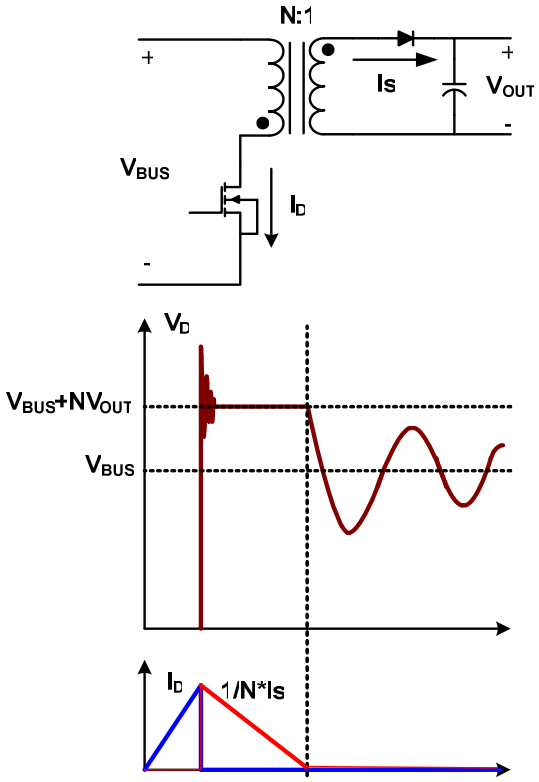


Figure 2—Single-Pulsed Flyback Converter

In a conventional fixed frequency flyback converter at DCM operation, the primary switch (MOSFET) is turned on at a fixed frequency and turned off when the current reaches the desired level. The device's turn-on time may occur at any point during this parasitic resonance. In some cases the device may turn on when the drain voltage is lower than the bus voltage (means low switching losses and high efficiency), and in some cases the switch will turn on when the drain voltage is higher above the bus voltage (means high switching loss). This characteristic is often observed on the efficiency curves of a discontinuous flyback converters with a constant load, the efficiency fluctuated with the input voltage as the turn-on switching loss changes due to the variation of the drain voltage at the turn on point.

In boundary conduction operation, the switch does not have a fixed switching frequency. The switch will always turn on by the controller when the drain voltage reaches its relatively low point. This can be achieved by detecting the auxiliary winding voltage V_{ZCD}, which is a ratio of primary winding voltage. Show in the Figure 3, setting a falling edge detecting near zero, when the secondary side current deceases to zero, the parasitic resonance make the ZCD voltage decrease, when it reaches to detecting threshold, the MOSFET turning on signal will be triggered. The detecting delay time is determined by the transformer magnetizing inductance, parasitic capacitance and ZCD filtering capacitor. The switch on time (T_1 in Figure 3) is determined by the feedback loop as conventional peak current mode control. The energy stored in the magnetizing inductor is fully transferred to the output.

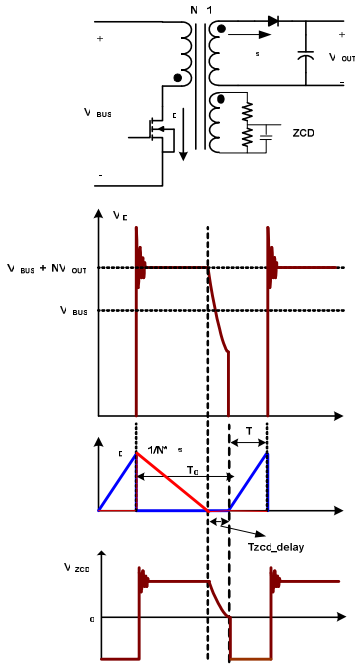


Figure 3—Boundary Conduction Mode

Compared to the conventional flyback under CCM and DCM operation, the boundary conduction mode operation can minimize the turn on switching loss, thus increasing efficiency and lowering device temperature rise.

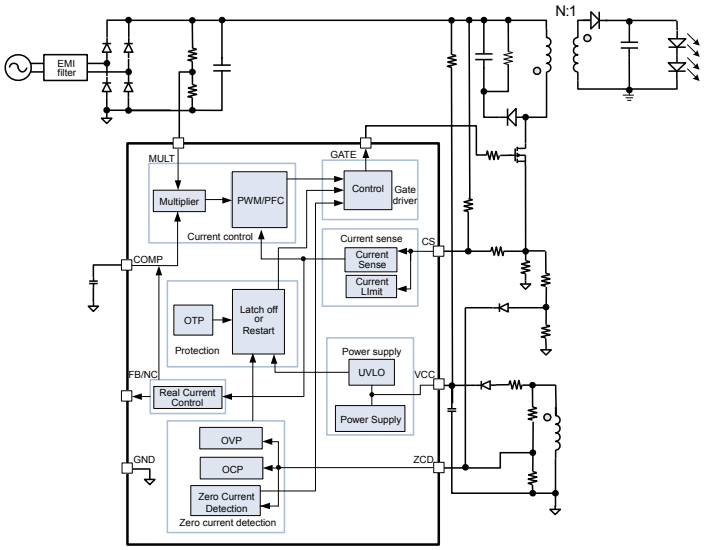


Figure 4—MP4021A Function Block Diagram and the Controlled LED Driving Converter

The MP4021A function block diagram and the controlled LED Driving Converter are shown in Figure 4. The converter consists of an EMI filter, a diode bridge rectifier, a flyback circuit with the controller MP4021A. The goal is to regulate the output LED current to a required constant value and achieve the

power factor correction function of input current. The operation of the converter can be summarized by the following description.

The AC mains voltage is rectified by the diode bridge, the rectified half sinusoid wave is applied to the flyback circuit. When the MOSFET is turned on, the transformer primary side current begins to ramp up from zero, and this current will be sensed at CS pin through a sensing resistor. The sensed current signal will be fed to the primary-side-control block to calculate its average value. The internal error amplifier compares the average value with an internal reference (0.4V), generating a signal error proportional to the difference between them. If the bandwidth of the error amplifier is narrow enough (below 20Hz), the error signal is a DC value over a line half-cycle and kept at a constant value until the average value equals the reference. That means the output LED current is regulated to a required constant value.

The error signal is fed into the multiplier block and multiplied by a partition of the rectified mains voltage. The result will be a rectified sinusoid whose peak amplitude depends on the mains peak voltage and the value of the error signal. The output of the multiplier is then fed into the negative input of the current comparator, thus it represents a sinusoidal reference for PWM. As the voltage on the current CS pin equals the value on the negative input of the current comparator, the external MOSFET is turned off. As a consequence, the peak primary current will be enveloped by a rectified sinusoid and has the same phase with the main input voltage, so a good power factor can be implemented. It is possible to prove also that this operation produces a constant ON-time over each line half-cycle.

$$V_{CS} = R_s \cdot V_{in} \cdot \frac{T_{on}}{L_m} \qquad V_{Multipier} = K_1 \cdot K_2 \cdot V_{in} * (V_{COMP} - 1.5),$$

$$\text{Have } V_{CS} = V_{Multiplier}, \qquad \text{got } T_{on} = \frac{L_m \cdot K_1 \cdot K_2 \cdot (V_{COMP} - 1.5)}{R_s}$$

Where L_m is the primary inductance, R_s is the current sensing resistor, K_1 is the multiplier gain, K_2 is the ratio of the MULT pin voltage to mains voltage.

After the MOSFET has been turned off, the transformer discharges its magnetizing energy into the load at the secondary side until its current goes to zero. When the current reaches to zero, the transformer has now run out of energy, the drain node is floating and the inductor resonates with the total capacitance of the drain. The drain voltage drops rapidly below the instantaneous line voltage and the detecting signal on ZCD drives the MOSFET on again and another conversion cycle starts. So, in each duty cycle, the MOSFET turns on at the current reaching zero, the converter works at boundary conduction mode. The relatively low drain voltage at turning on reduces both the turn on loss and the drain capacitive energy which is also dissipated at MOSFET turning on.

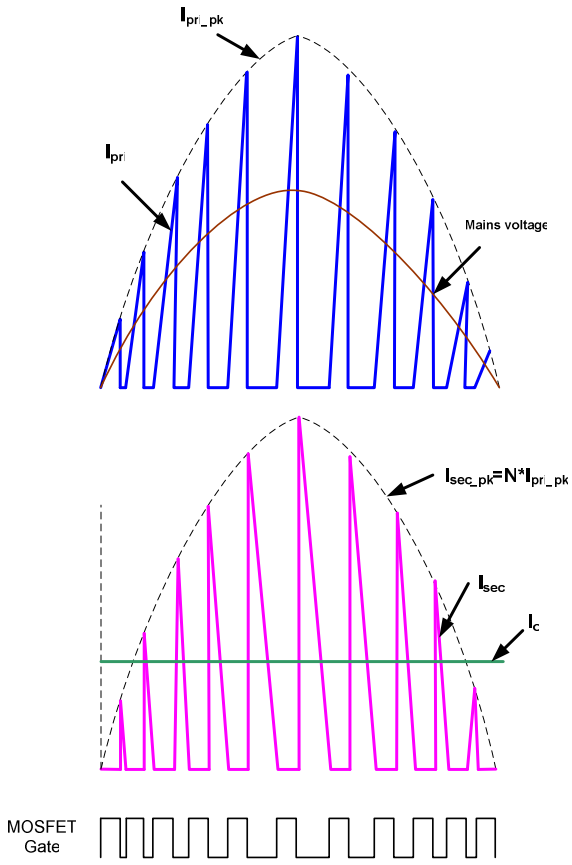


Figure 5—Transformer Both Side Current and MOSFET Gate Timing

The transformer current on both side and the MOSFET gate timing are shown in Figure 5. The operation frequency increases with the instantaneous mains voltage increases. when the mains voltage closed to the zero-crossing point, the frequency maybe very high. The MP4021A has internally set a 3.5μs minimum off time to limit the maximum switching frequency and help for high efficiency and low EMI performance.

PIN FUNCTION AND OPERATION INFORMATION

Pin1 (MULT)

The MULT pin is one of the input pin of the internal multiplier. This pin should be connected to the tap of the resistor divider from the rectified instantaneous line voltage. The output of the multiplier will be shaped as sinusoid too. This signal provides the reference for the current comparator which sets the primary peak current shaped as sinusoid in phase with the input line voltage cycle by cycle.

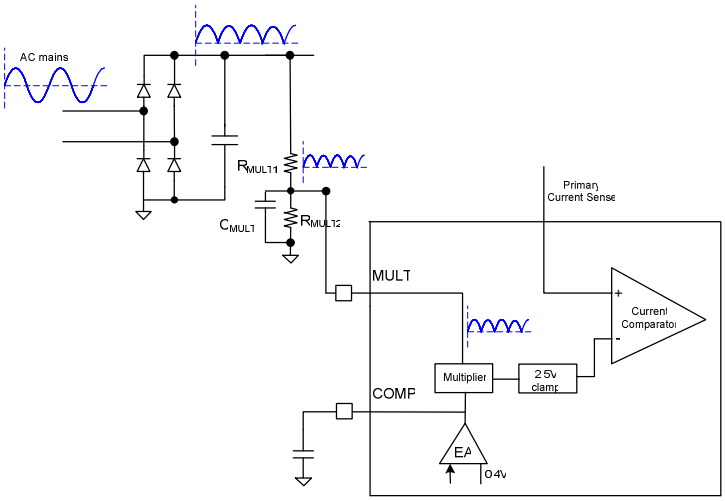


Figure 6—The MULT Pin Connection Circuitry

The MULT pin linear operation voltage range is 0~3V, for an universal AC input application, the MULT pin voltage need to be set low at the minimum AC input voltage so that the MULT voltage will not exceed 3V at the maximum AC input voltage. But also, the MULT pin voltage can not be set too low, this will cause a high COMP voltage to regulate the same LED current, The COMP voltage may saturate when the MULT pin is set too low. A recommended model to set the MULT voltage is shown as follow:

$$\sqrt{2}\cdot V_{in\_max(rms)}\cdot\frac{R_{MULT2}}{R_{MULT1}+R_{MULT2}}\approx 2.5\sim 3$$

Considering the losses, the R_{MULT1} should be large enough, for example, 85V~265VAC input, the R_{MULT1}, R_{MULT2} can be chosen as 1M, 6.8kΩ with a 100pF bypass capacitor.

Pin2 (ZCD)

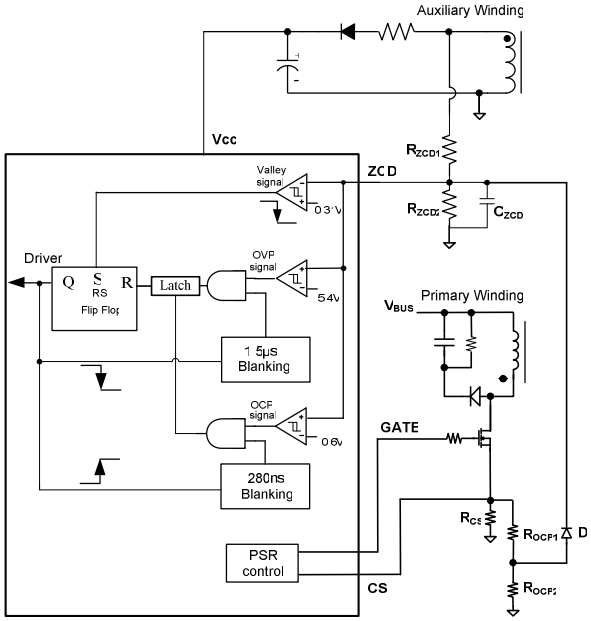


Figure 7—The ZCD Pin Connection Circuitry

The ZCD pin connection circuitry is shown in Figure 7. The ZCD pin is connected to the auxiliary winding through a resistor divider. The ZCD pin is used for three functions. One is to detect zero-cross condition of the auxiliary winding voltage after the secondary side current decreases to zero, which achieves the boundary conduction mode operation to minimize the switching losses and EMI. The second function of ZCD pin is to implement the output over voltage protection by comparing to the internal 5.4V reference. The third function is to activate the over current protection by detecting the primary-side current.

The internal gate turn-on signal occurs when the ZCD pin voltage gets a falling edge below 0.31V from the resistor divider with a 0.65V hysteresis. A ceramic by pass capacitor is needed to absorb the high frequency oscillation of the leakage inductance and the parasitic capacitance after primary switch turns off which may mis-trigger the ZCD pin detection (see Figure 9). The switching frequency of MP4021A is variable, the frequency is changing with the input instantaneous line voltage. To limit the maximum frequency and get a good EMI and efficiency performance, MP4021A employs an internal minimum off time limiter—3.5μs, shown in Figure 8.

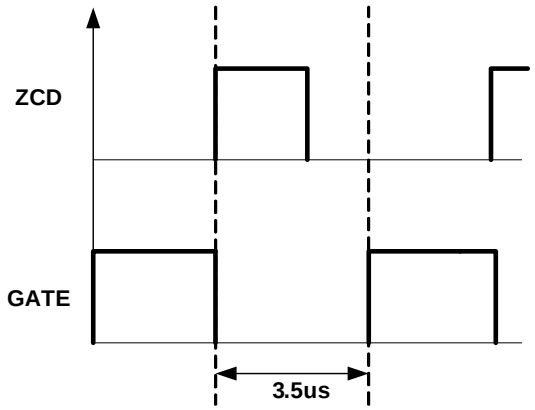


Figure 8—Minimum Off Time

The output over voltage protection is achieved by detecting the positive plateau of auxiliary winding voltage which is proportion to the output voltage (see Figure 9). Once the ZCD pin voltage is higher than 5.4V, the OVP signal will be triggered and latched, the gate driver will be turned off and the VCC voltage dropped below the UVLO which will make the IC reset and the system restarts again. The output OVP setting point can be calculated as:

$$V_{out-ovp} \cdot \frac{N_{aux}}{N_{sec}} \cdot \frac{R_{ZCD2}}{R_{ZCD1} + R_{ZCD2}} = 5.4V$$

Where V_{out_ovp} is the output OVP setting voltage; N_{aux} is the auxiliary winding turns of the transformer and N_{sec} is secondary winding turns of the transformer. Following should be considered when choosing the resistor value: the losses and the ZCD falling edge detection delay time with the ceramic bypass capacitor, enlarging the delay time will reduce output LED current, basically, the delay time should be limited in 1.5μs. To avoid the OVP mis-trigger by the oscillation spike after the switch turns off, the MP4021A integrates an internal T_{OVPS} blanking time for the OVP detection, typical 1.5μs (see Figure 9). Moving the current-limiting resistor between the output of the aux-winding and the ZCD resistor divider can also work as suppresser to avoid the mis-trigger OVP.

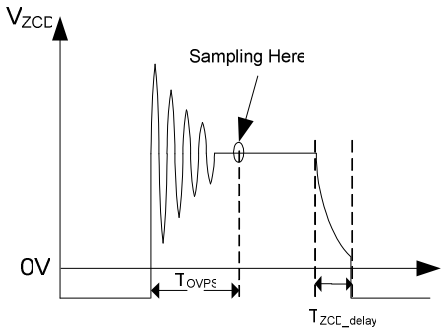


Figure 9—The ZCD Voltage

As over current protection, tie a resistor divider form CS sensing resistor to ZCD pin, shown in Figure 7. When the power MOSFET in the primary-side is turned on, the ZCD pin monitors the rising primary-side current, once the ZCD pin reaches OCP threshold, typical 0.6V, the gate driver will be turned off to prevent the chip form damage and the IC works at quiescent mode, the VCC voltage dropped below the UVLO which will make the IC shut down and the system restarts again. The primary-side OCP setting point can be calculated as:

$$I_{PRI\_OCP} \cdot R_{CS} \cdot \frac{R_{OCP2}}{R_{OCP1} + R_{OCP2}} - V_D = 0.6V$$

Where I_{PRI_OCP} is primary-side over current protection current value, V_D is the voltage drop of the diode. Please note that, when the MOS is turned on, the taps of the ZCD zero-current detector resistor divider and the OCP resistor divider are connected by a diode. So, to avoid the effect of the ZCD zero-current detector, the value of the resistors to set the OCP threshold (R_{OCP1} & R_{OCP2}) should be much smaller than those of the ZCD zero-current detector (R_{ZCD1} & R_{ZCD2}). For some applications, for example, the primary-side inductance value is very small, the minimal-off time feature could cause the system works in DCM at the zero-crossing of the BUS voltage. To improve the OCP function in this condition, please remove C_{ZCD} and reduce the value of R_{ZCD1} and R_{ZCD2} proportionally.

Pin3 (VCC)

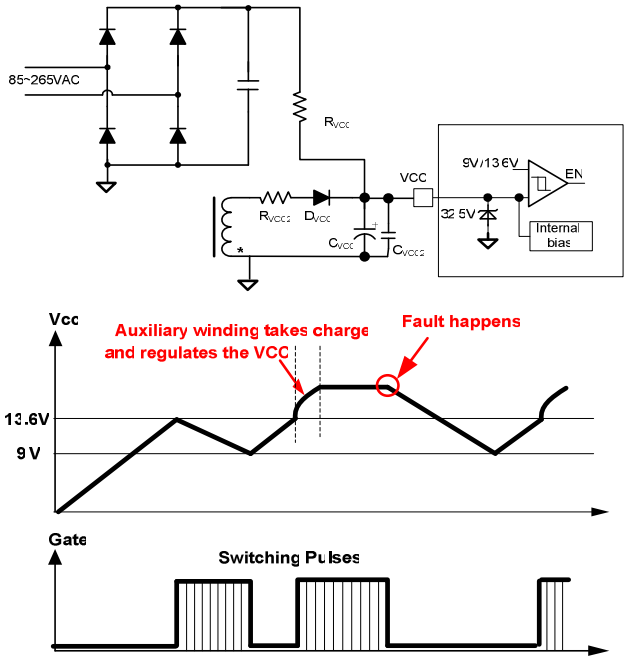


Figure 10—The VCC Pin Connection Circuitry and the Power Supply Flow-Chart

The VCC pin provides the power supply both for the internal logic circuitry and the gate driver signal. The VCC pin connection circuitry and the power supply flow-chart is shown in Figure 10. When AC power supply is on, the bulk capacitor C_{VCC1} (typically 22μF) is first charged by the start up resistor R_{VCC1} from the AC line, once the VCC voltage reaches 13.6V, the IC will be enabled and begin to switch, the power consumption of the IC increases, then the auxiliary winding starts working and mainly takes the charge of the power supply for VCC. Since the voltage of auxiliary winding is proportion to that of the secondary winding, the VCC voltage will be finally regulated to a constant value. If VCC drops below the UVLO threshold 9V before the auxiliary winding can provide the power supply, the IC will be shut down and the VCC will restart charging from AC line again. If fault condition happens at normal operation, the switching signal will be stopped and latched, the IC works at quiescent mode, when the VCC voltage drops below 9V the system restarts again. So, the R_{VCC1} should be large enough to limit the charging current which ensures the VCC voltage can drop below 9V UVLO threshold at quiescent mode (typically 0.75mA consumption current in quiescent mode). Also, a small ceramic capacitor (typically 0.1μF) is needed to reduce the noise.

Pin4 (GATE)

Gate drive output for driving external MOSFET. The internal totem pole output stage is able to drive external high power MOSFET with 1A source capability and 1.2A sink capability. The high level voltage of this pin is clamped to 13.5V to avoid excessive gate drive voltage. And for normal operation, the low level voltage is higher than 6V to guarantee enough drive capacity. Connect this pin to the MOSFET gate in series with a driving resistor. A smaller driving resistor provides faster MOSFET switching, reduces switching loss and improve MOSFET thermal performance. However larger driving resistors usually provide better EMI performance. It is a tradeoff. For different applications, the driving resistors should be fine tuned. Typically, the value can be 5Ω~20Ω.

Pin5 (CS)

The CS pin is used to sense the primary side current via a sensing resistor, the resulting voltage is internally fed both to the current comparator to determine the MOSFET turn off time and the average current calculation block to calculate the primary current average value. The output LED mean current can be calculated approximately as:

$$I_0 \approx \frac{N \cdot V_{FB}}{2 \cdot R_S}$$

Where N is the turn ratio of primary winding to secondary winding, V_{FB} is the feedback reference voltage (typically 0.4V), R_s is the sensing resistor connected between the MOSFET source and GND. The maximum voltage on CS pin is clamped at 2.5V to get a cycle-by-cycle current limit.

In order to avoid the premature termination of the switching pulse due to the parasitic capacitance discharging at MOSFET turning on, an internal leading edge blanking (LEB) unit is employed between the CS Pin and internal feedback. During the blanking time, the internal fed path is blocked. Figure 11 shows the leading edge blanking.

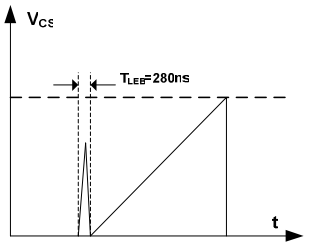


Figure 11— The Leading Edge Blanking

In the case of current sensing, shows as Figure 12, the MOSFET has a delay time due to the propagation delay of the gate control circuit, the delay time is the inherent characteristic of the control circuit, so T_{delay} can be assumed as constant. The delay will lead an error of the primary side peak current. The error increases with the input instantaneous line voltage increase. △I2 is bigger than △I1 due to the bigger rising slope (the higher input voltage, the bigger rising slope). So, the difference of △I will cause a bad output LED current line regulation.

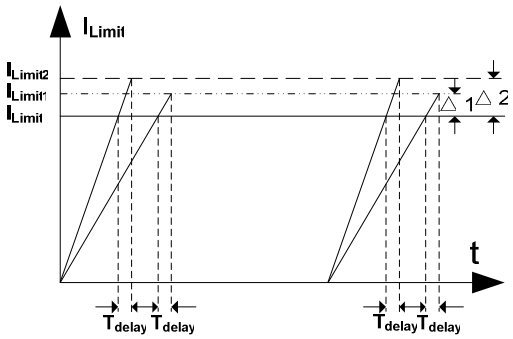


Figure 12—The Propagation Delay of the Primary Current

The propagation delay influence to the line regulation can be well improved by adding feed-forward from AC line voltage to CS pin, shown in Figure 13, the higher line voltage, the higher feed-forward offset. The feed-forward offset value need fine tune in real application and it is case by case.

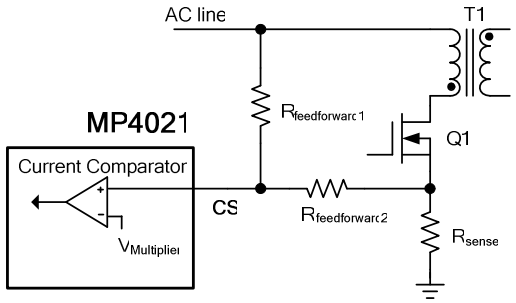


Figure 13—The Feedforward Compensation on CS Pin

Pin6 (GND)

Ground pin, current return of the control signal and the gate drive signal. It is recommended to connect power GND and analog GND to this pin in the PCB layout. The power GND for power switches and the analog GND for the control signals is desired to be separated and only connected at this pin.

Pin7 (FB/NC)

Feedback signal pin. Shown in Figure 14, the FB signal is fed to the error amplifier and comparing with the 0.4V reference, at steady state, the average value of FB will be regulated to 0.4V. The average current calculation block output is internally connected to the FB with high input impedance, if there is no other external feedback signal is applied on FB pin, the average current from CS pin will be regulated, if there is external FB signal with low input impedance apply in this pin, the external FB signal will be regulated. This structure makes the MP4021A suitable both for primary side control application without other feedback signals and direct control application with external feedback signal applied.

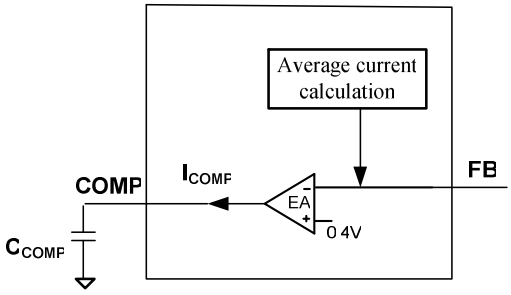
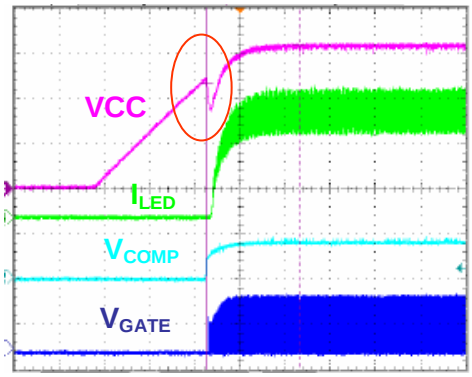


Figure 14—FB Pin Structure

Pin8 (COMP)

Loop compensation pin. Connect a compensation cap from this pin to AGND. This cap should be low ESR ceramic cap such as X7R. The COMP pin is the internal error amplifier output. In order to get a limit loop bandwidth <20Hz, the cap should be select from 2.2μF to 10μF. A larger cap results in small input and output current ripple and better thermal, EMI, steady states performance, but also, a large cap means a longer soft start time which will cause a bigger voltage drop for VCC at start up (see Figure 15), if the VCC drops below UVLO, the start up may fail. So the compensation cap selection and the VCC voltage drop at start up should be double checked in real design.



400ms/div

Figure 15—COMP and VCC Waveforms at Start Up

Output Short Circuit Protection

When the output short circuit happens, theoretically, the positive plateau of auxiliary winding voltage is also near zero, the VCC can not be held on and it will drop below VCC UVLO. The IC will shut down and restart again. And at the same time, the primary current will rise up when output short circuit occurs, so it will trigger the ZCD over current protection to prevent the damage from output short circuit failure.

Auto Restart

The MP4021A integrates an auto starter, the starter starts timing when the MOSFET is turned on, if ZCD fails to send out another turn on signal after 130μs, the starter will automatically send out the turn on signal which can avoid the IC unnecessary shut down by ZCD missing detection.

4. DESIGN EXAMPLE

8W LED Bulb Driver with High Power Factor and Excellent Line Regulation

A. Specifications

- Input AC mains: 85V~265V RMS, V_{ac_min}=85V, V_{ac_max}=265V, V_{in_max}= $\sqrt{2}\cdot V_{ac\_max}$, $V_{in}(V_{ac},t)=\left|\sqrt{2}\cdot V_{ac}\cdot\sin(2\cdot\pi\cdot f_{mains}\cdot t)\right|$, Input AC mains frequency: f_{mains}=50Hz
- Output: LED voltage V_o=16V, LED current I_o=500mA, P_o=V_O*I_O=8W
- Output OVP threshold: 22V

B. Schematic

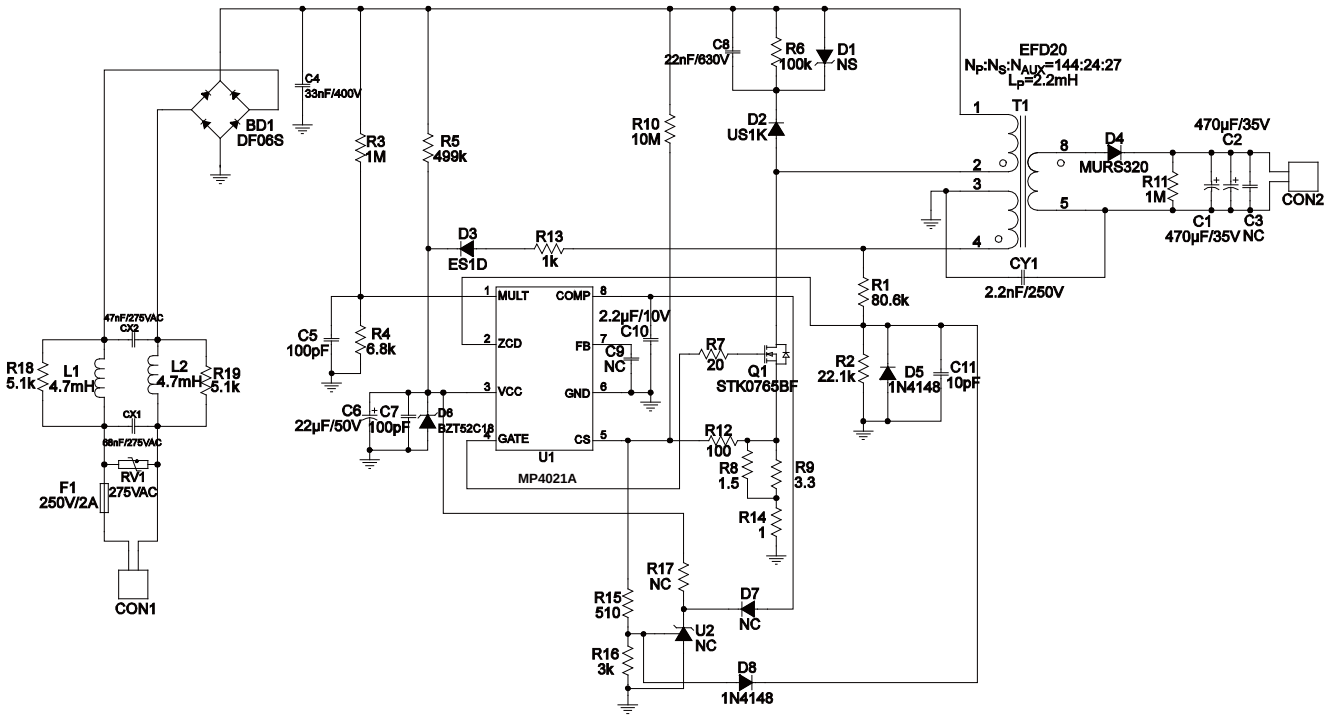


Figure 16—Schematic

C. Turns Ratio-N, Primary MOSFET and Secondary Rectifier Diode Voltage Rating Selection

Figure 17 shows the typical Drain-Source voltage waveform of the primary MOSFET and secondary rectifier diode. From the waveform, the primary MOSFET Drain-Source voltage rating V_{P-MOS} can be got as:

$$V_{P-MOS} = V_{in\_max} + N \cdot V_O + 150V \quad (1)$$

Where 150V maximum spike voltage is assumed here.

The secondary rectifier diode voltage rating V_{DIODE} can be got as:

$$V_{DIODE} = V_{in\_max} / N + V_O + 40V \quad (2)$$

Where 40V maximum spike voltage is assumed here.

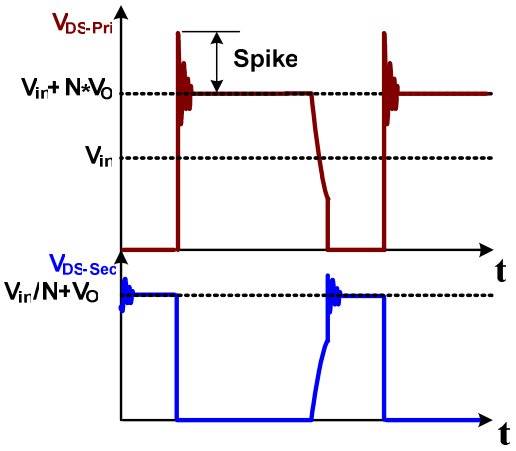


Figure 17—Drain-Source Voltage of Primary MOSFET and Secondary Rectifier Diode

From (1) and (2), the voltage rating of primary MOSFET and secondary rectifier diode versus turns-ratio N is shown in Figure 18. Then the turns-ratio N can be determined for the required MOSFET and Rectifier diode voltage rating. Sometimes N can be selected within a range, then smaller N means larger turn on time and larger primary RMS current, this will lead a larger size transformer, so a relatively larger N is preferred. Here choosing N=6, so 650V or 700V MOSFET and 150V, 200V schottky or fast recovery diode can be used.

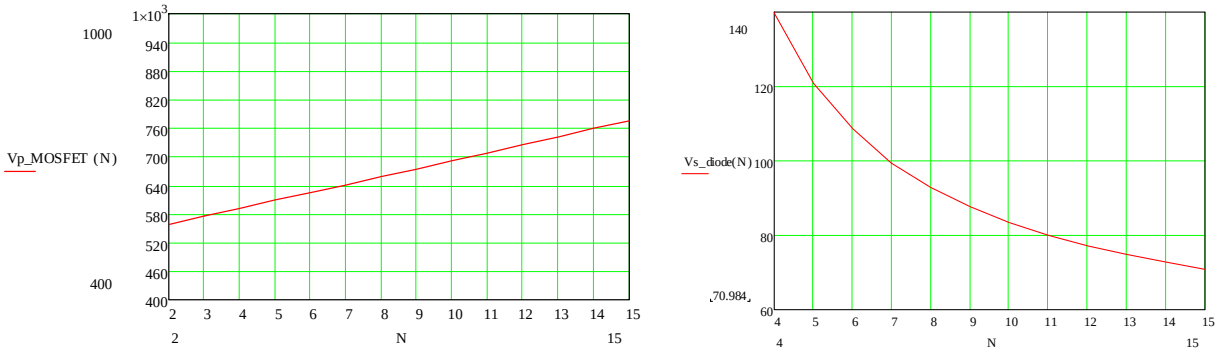


Figure 18—Voltage Rating of Primary MOSFET and Secondary Rectifier Diode vs. Turn Ratio-N

D. Transformer Design

Primary Inductance L_p

As described in page 7, the MP4021A implements constant ON-time operation during a line cycle with a given RMS line voltage. The turn-off time is variable with the instantaneous line voltage.

$$T_{on} = \frac{L_p \cdot I_p}{V_{in}(V_{ac}, t)} \quad (3), \qquad T_{off} = \frac{L_p \cdot I_p}{N \cdot V_o} \quad (4),$$

$$\text{Get:} \qquad T_{off}(T_{on}, V_{ac}, t) = \frac{V_{in}(V_{ac}, t) \cdot T_{on}}{N \cdot V_o} \tag{5}$$

Considering the T_{off} limit within MP4021A, the T_{off} equation should be modified as:

$$T_{off}(T_{on}, V_{ac}, t) = \begin{cases} \dfrac{V_{in}(V_{ac}, t) \cdot T_{on}}{N \cdot V_o} \text{ if } \dfrac{V_{in}(V_{ac}, t) \cdot T_{on}}{N \cdot V_o} > 3.5\mu s \\ 3.5\mu s, \text{otherwise} \end{cases} \tag{6}$$

Shown as Figure 19, the output LED current equals the average value of the secondary winding current during a half-line cycle. The calculating equation is shown in (7), it sums the secondary current in each cycle and then get the average value.

$$I_o(a, b, T_{on}, V_{ac}, L_p) = \begin{cases} t1 \leftarrow a \\ sum \leftarrow 0 \\ \text{while}(t1 < b) \\ \quad sum \leftarrow sum + \dfrac{1}{2} \cdot \left\{ \left[\dfrac{V_{in}(V_{ac}, t1 + T_{on}) \cdot T_{on}}{L_p} \right] \cdot N \right\} \cdot T_{off}(T_{on}, V_{ac}, t1 + T_{on}) \\ \quad t1 \leftarrow t1 + T_{on} + T_{off}(T_{on}, V_{ac}, t1 + T_{on}) \\ \dfrac{sum}{b - a} \end{cases} \tag{7}$$

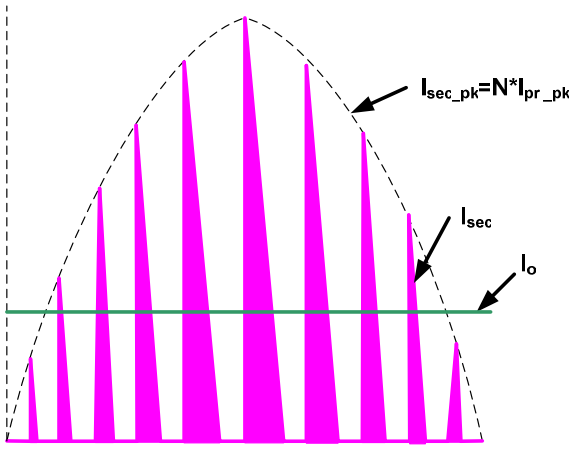


Figure 19—Secondary Side Current

Usually, the system will define a minimum frequency f_{s_min}, the minimum frequency will occur at $V_{in} = \sqrt{2} \cdot 85 \sin(\frac{\pi}{2})$, here set f_{s_min}=45 kHz,

$$I_o(0, 0.01, T_{on\_85V}, 85, L_p) = 0.5A \tag{8}$$

$$f_{s\_min} = \frac{1}{T_{on\_85V} + T_{off}(T_{on\_85V}, 85, 0.005)} = 45kHz \tag{9}$$

Combine (8) and (9), can get L_p=2.2 mH, T_{on_85V}=9.86μs.

The maximum primary peak current:

$$I_{pk\_max} = T_{on\_85V} \cdot \frac{V_{in}(85, 0.005)}{L_p} = 0.54A \tag{10}$$

When getting the Lp, the maximum operation frequency also can be calculated, the maximum frequency will occur at V_{in} reach to zero crossing at 265VAC.

$$f_{s\_max} = \frac{1}{T_{on\_265V} + T_{off}(T_{on\_265V}, 265, 0)} = 178kHz \tag{11}$$

The Primary Winding RMS Current:

$$I_{pri\_rms}(a, b, T_{on}, V_{ac}, L_p) = \left\| \begin{array}{l} t1 \leftarrow a \\ sum \leftarrow 0 \\ while(t1 < b) \\ \left\| \begin{array}{l} sum \leftarrow sum + \left\{ \frac{1}{T_{on} + T_{off}(T_{on}, V_{ac}, t1 + T_{on})} \int_0^{T_{on}} \left(\frac{V_{in}(V_{ac}, t1 + T_{on}) \cdot t}{L_p} \right)^2 \cdot dt \right\} \cdot \\ \left[T_{on} + T_{off}(T_{on}, V_{ac}, t1 + T_{on}) \right] \\ t1 \leftarrow t1 + T_{on} + T_{off}(T_{on}, V_{ac}, t1 + T_{on}) \end{array} \right. \\ \sqrt{\frac{sum}{b - a}} \end{array} \right. \tag{12}$$

The maximum primary RMS current:

$$I_{pri\_rms\_max} = I_{pri\_rms}(0, 0.01, T_{on\_85V}, 85, 2.2 \cdot 10^{-3}) = 0.156\,A \tag{13}$$

The secondary winding RMS current:

$$I_{sec\_rms}(a,b,T_{on},V_{ac},L_p) = \left| \begin{array}{l} t1 \leftarrow a \\ sum \leftarrow 0 \\ while(t1 < b) \\ \left| sum \leftarrow sum + \left\{ \frac{N^4 \cdot V_o^{\,2} / L_p^{\,2}}{T_{on} + T_{off}(T_{on}, V_{ac}, t1 + T_{on})} \int_0^{T_{off}(T_{on},V_{ac},t1+T_{on})} \left(\frac{V_{in}(V_{ac}, t1 + T_{on}) \cdot T_{on}}{N \cdot V_o} - t \right)^2 \cdot dt \right\} \cdot \right. \\ \left. \left[T_{on} + T_{off}(T_{on}, V_{ac}, t1 + T_{on}) \right] \right. \\ \left. t1 \leftarrow t1 + T_{on} + T_{off}(T_{on}, V_{ac}, t1 + T_{on}) \right. \\ \\ \sqrt{\frac{sum}{b-a}} \end{array} \right. \quad (14)$$

The maximum secondary winding RMS current:

$$I_{sec\_rms\_max} = I_{sec\_rms}(0, 0.01, T_{on\_85V}, 85, 2.2 \cdot 10^{-3}) = 0.933\,A \quad (15)$$

The Transformer Core Selection

The transformer core needs to be appropriately selected for a certain output power within the entire operation frequency. Ferrite is widely adopted in flyback transformer. The core area product ($A_E A_W$) which is the core magnetic cross-section area multiplied by window area available for winding, is widely used for an initial estimate of core size for a given application. A rough indication of the required area product is given by following:

$$A_E \cdot A_W = \left(\frac{L_p \cdot I_{Pk\_max} \cdot I_{rms\_max}}{B_{max} \cdot K_u \cdot K_j} \right)^{4/3} cm^4 \quad (16)$$

Where K_u is winding factor which is usually 0.2~0.3 for an off-line transformer. K_j is the current-density coefficient (typically 0.042~0.045 A/m^2 for ferrite core). I_{Pk_max} and I_{rms_max} are the maximum peak current and RMS current of the primary inductance. B_{max} is the allowed maximum flux density in normal operation which is usually preset to be the saturation flux density of the core material (0.3T~0.4T). So the estimated least core area product is 0.0347 cm^4.

Please refer to the manufacture's datasheet to select the proper core which has enough margins. Also, the core shape should taken consideration to best meet the layout dimension. Here choosing EFD20 core.

A_E = 0.31 cm^2, A_W = 0.507 cm^2, A_E*A_W=0.157 cm^4.

The core magnetic path length: l_c=5.3 cm

The relative permeability of the core material: $\mu_\gamma = 2400$

Primary and Secondary Winding Turns

With a given core size, there is a minimum number of turns for the transformer primary side winding to avoid saturation. The normal saturation specification is E-T or volt-second rating. The E-T rating is the maximum voltage, E, which can be applied over a time of T seconds. (The E-T rating is identical to the

product of inductance L and peak current) Equation (17) defines a minimum value of N_P for the transformer primary winding to avoid the core saturation:

$$N_P = \frac{L_p \cdot I_{pk\_max}}{B_{max} \cdot A_E} \times 10^4 \quad (17)$$

Where:

L_p = the primary inductance of the transformer (H)

B_{max}= the maximum allowable flux density (T)

A_E= the effective cross sectional core area (cm^2)

I_{pk_max}= the maximum primary peak current (A)

The maximum allowable flux density B should be smaller than the saturation flux density B_{sat}. Since B_{sat} decreases as the temperature goes high, the high temperature characteristics should be considered.

Here get: $N_p = 144$

Secondary turn count is a function of turn ratio N and primary turn count N_P:

$$N_S = N_P / N = 24 \quad (18)$$

Wire Size

Once all the winding turns have been determined, wire size must be properly chosen to minimize the winding conduction loss and leakage inductance. The winding loss depends on the RMS current value, the length and the cross section of wire.

The wire size could be determined by the RMS current of the winding:

$$S_{pri} = \frac{I_{pri\_rms\_max}}{J} = 2.596 \cdot 10^{-2} (mm^2) \quad (19)$$

$$S_{sec} = \frac{I_{sec\_rms\_max}}{J} = 1.554 \cdot 10^{-1} (mm^2) \quad (20)$$

Here J is the current density of the wire which is 6A/mm^2 typically.

Due to the skin effect and proximity effect of the conductor, the diameter of the wire selected is usually less than 2*Δd (Δd: skin effect depth):

$$\Delta d = \sqrt{\frac{1}{\pi \cdot f_{s\_min} \cdot \mu \cdot \sigma}} = 0.36 (mm) \quad (21)$$

Where μ is the magnetic permeability of the conductor, which is usually equals to the permeability of vacuum for most conductor, i.e. $4\pi \times 10^{-7}$ H/m, σ is the conductivity of the wire (for copper, σ is typically 6×10^7 S/m at 0 deg, σ will be larger as temperature increases, which means the Δd will get smaller).

Therefore, multiple strands of thinner wire or Litz wire is usually adopted to minimize the AC resistance, the effective cross section area of multi-strands wire or Litz wire should large enough to meet the requirement set by the current density.

Here can choose 0.2mm*1 wire for primary winding, 0.3mm*2 wires for secondary winding, the wire area for primary is S_1=3.14*10^{-2} mm^2, for secondary is S_2=1.66*10^{-1} mm^2.

The Auxiliary Winding

The auxiliary winding is mainly used to provide power for VCC and detect the current zero crossing for boundary mode operation, so the current requirement for auxiliary winding is very small, larger than 10mA is enough. The auxiliary winding output DC voltage is proportion to the output LED voltage with the turn ratio of N_{aux}/N_s. Since the output LED voltage is 16V, considering the voltage drop in VCC current limit resistor R13, the N_{aux} can be selected a bit larger than the secondary winding turns N_s. Here, N_{aux}=27, 0.18mm wire is selected.

The Window Area Fill Factor Calculation

After the wire sizes have been determined, it is necessary to check whether the core window area can accommodate all the selected windings. The window area required by each winding should be calculated respectively and added together, the area for interwinding insulation and spaces existing between the turns should also be taken into consideration. The fill factor, means the winding area comparing to the whole window area of the core, should be well below 1 due to these interwinding insulation and spaces between turns. It is recommended that a fill factor no greater than about 20% be used.

$$\frac{N_p \cdot S_1 + N_s \cdot S_2 + N_{aux} \cdot S_3}{A_W} = 0.091 < 0.2 \quad (22)$$

If the required window area is larger than the selected one, either wire size must be reduced, or a larger core must be chosen. Of course, a reduction in wire size increases the copper loss of the transformer.

The Air Gap

With the selected core and winding turns, the air gap of the core is given as:

$$G = \mu_0 \cdot A_E \cdot \frac{N_P^2}{L_p} - \frac{l_c}{\mu_r} = 0.36(\text{mm}) \quad (23)$$

Where A_E is the cross sectional area of the selected core, μ_0 is the permeability of vacuum which equals $4\pi \times 10^{-7}$ H/m. L_p and N_P is the primary winding inductance and turns respectively, l_c is the core magnetic path length and μ_r is the relative magnetic permeability of the core material.

The Transformer Manufacture Instructions

There are two main considerations for the transformer manufacture. To minimize the effect of the leakage inductance spike, the coupling between the transformer primary side and the secondary side should be as tight as possible. This can be accomplished be interleaving the primary and secondary winding in transformer manufacture (shown in Figure 20). To minimize the coupling influence from primary winding to auxiliary winding, the same mean dots of the two windings should be separated far away, a good mode is to place the GND pin of the auxiliary winding between the two dots, refer to Figure 21.

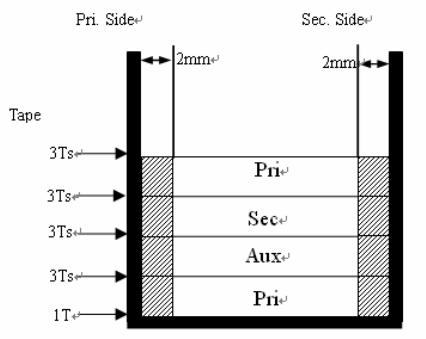


Figure 20—The Transformer Winding Diagram

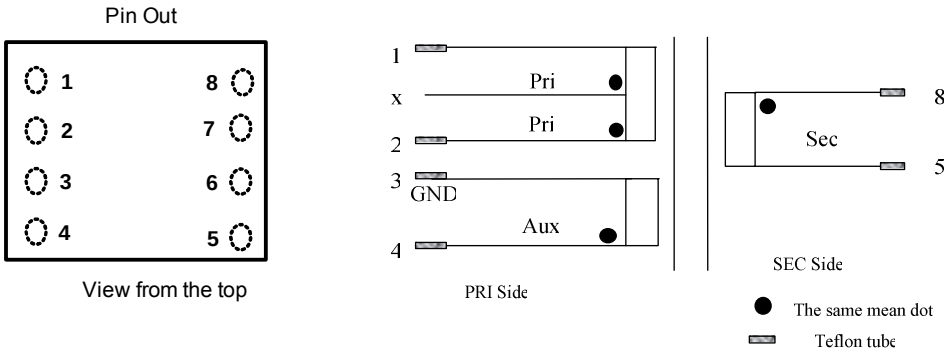


Figure 21—The Transformer Pin Out and the Connection Diagram

E. Input EMI Filter (L1, L2, CX1, CX2, CY1)

The input EMI filter is comprised of L1, L2, CX1, CX2 and together with the safety rated Y class capacitor CY1. The value of the components should be selected mainly to pass the EMI test standard, but also need take the power factor into consideration.

F. Input Bridge (BD1)

The input bridge can use standard slow recovery, low cost diodes. Just three items need mainly considered in selecting the diodes bridge, the maximum input RMS current, the maximum input line voltage and the thermal performance.

G. Input Capacitor (C4)

In order to get a high power factor, the input decoupling capacitor should be limited in value. The function of the capacitor is mainly to attenuate the switching current ripple for the transformer high frequency magnetizing current. The worst condition will occur on the peak of the minimum rated input voltage. The maximum high frequency voltage ripple of the cap should be limited in 20%, or the big voltage ripple will influence the sensing accuracy of the MULT pin which will also influence the PFC function.

$$C4 \approx \frac{I_{pk\_max} - \sqrt{2} I_{pri\_rms\_max}}{2 \cdot \pi \cdot f_{s\_min} \cdot V_{ac\_min} \cdot 0.2} = 68nF \quad (24)$$

In real applications, the input capacitor will be designed with taking EMI filter and the power factor value into account, the real value usually could be smaller than the calculated value, here, a 33nF/400V film cap is selected.

H. Output Capacitor (C1, C2)

The output voltage ripple has two components, the switching frequency ripple associated with the flyback converter, and the low frequency ripple associated with the input line voltage (50Hz). The selection of the output bulk cap depends on the output current, the admitted overvoltage and the desired voltage ripple. But for LED load application, the requirement is usually for the LED current ripple. In this case, the load is 5 LEDs in series, 500mA output current, 40% current ripple limitation, in order to meet this limitation, the output voltage ripple should be within 10% of the output voltage.

The maximum RMS current of the output capacitor can be obtained as:

$$I_{out\_cap\_rms\_max} = \sqrt{I_{sec\_rms\_max}^{2} - I_{o\_rms}^{2}} \quad (25)$$

Where I_{o_rms} is the output RMS current and $I_{sec\_rms\_max}$ is the maximum secondary RMS current in (15).

The maximum RMS current should be smaller than the RMS current specification of the capacitor.

The maximum switching voltage ripple occurs at the peak of the minimum rated input line voltage, and the ripple (peak-peak) can be estimated by:

$$\Delta V_{o\_swtiching} = \frac{I_{o\_max} \cdot T_{off}(T_{on\_85V}, 85, 0.005)}{C_{out}} + (I_{sec\_pk\_max} - I_{o\_max}) \cdot R_{ESR} \quad (26)$$

Where I_{o_max} is the maximum instantaneous output LED current, the value is the 500mA mean value pluses the 20% peak ripple; $T_{off}(T_{on\_85V}, 85, 0.005)$ is the turn off time at the peak of the minimum rated input line. R_{ESR} is the ESR of output capacitor, typically 0.03 each cap; $I_{sec\_pk\_max}$ is the maximum peak current of the secondary winding.

The maximum low frequency (twice line frequency, 100Hz) ripple can be estimated the function of the capacitor impedance and the peak capacitor current (equals the I_{o_max}).

$$\Delta V_{o\_line} = I_{o\_max} \sqrt{\frac{1}{(2\pi \cdot 2f_{line} \cdot C_{out})^{2}} + R_{ESR}^{2}} \quad (27)$$

It can be seen from the calculations, the output voltage ripple is dominated by the low frequency ripple (100Hz).

Let $\Delta V_{o\_line} = 1.4V$, get the C_{out}=690μF. Here selecting two 470μF/35V bulk caps in parallel to minimize the ESR and the sharing the capacitor RMS value. A 30kΩ pre-load resistor is also added to limit the output voltage under open load condition.

I. RCD Snubber (R6, C8, D2)

The peak voltage across the MOSFET at turn-off includes the instantaneous input line voltage, the reflecting voltage from secondary side, and the voltage spike due to leakage inductance. To protect the MOSFET from over voltage damage. A RCD snubber is usually adopted to absorb the leakage inductance energy and clamp the drain voltage as shown in Figure 22. The value of the capacitor C8 and resistor R6, depend on the energy stored in the leakage inductance, and the energy must be dissipated by the RC network during each cycle. Figure 23 shows the voltage of the primary MOSFET and the snubber capacitor A point during turn-off.

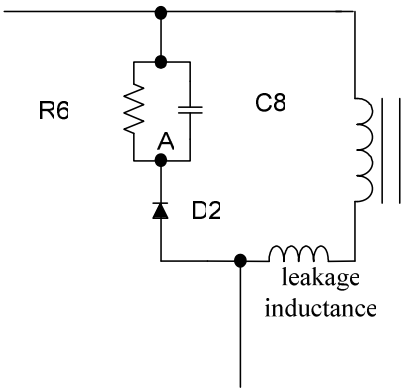


Figure 22—RCD Snubber on Primary Side

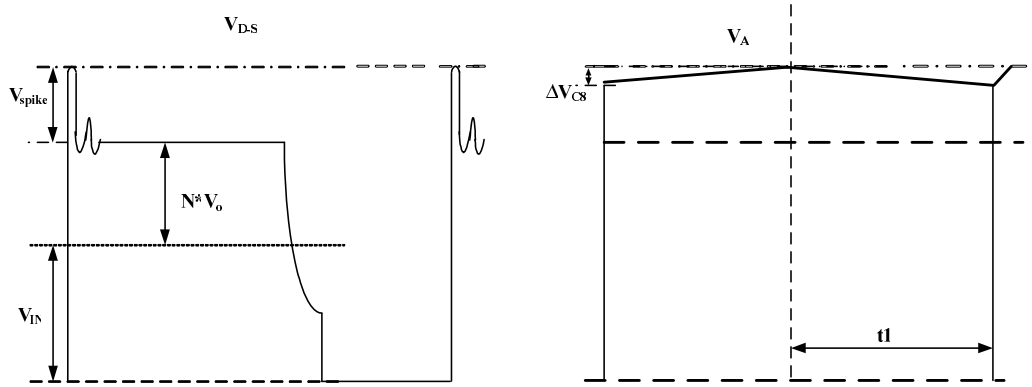


Figure 23—MOSFET Drain Voltage and Snubber Capacitor A Point Voltage

The energy stored in the leakage inductance at maximum input voltage can be obtained as:

$$E_{Lk\_max} = \frac{1}{2} \cdot L_{leakage} \cdot I_{pk\_V_{in\_max}}{}^{2} \quad (28)$$

Where $I_{pk\_Vin\_max}$ is the peak current at maximum input voltage in primary side. Assuming all the leakage inductance energy is transferred to the snubber cap. A secondary relationship is:

$$E_{Lk\_max} = \frac{1}{2} \cdot C8 \cdot \left[(V_{in\_max} + N \cdot V_o + V_{spike})^2 - (V_{in\_max} + N \cdot V_o + V_{spike} - \Delta V_{C8})^2 \right] \quad (29)$$

Where V_{spike} is the spike voltage clamped by the RCD snubber, ΔV_{C8} is the voltage changing on the snubber cap caused by the leakage inductance.

Assuming $\Delta V_{C8} << V_{spike}$, and the $\frac{1}{4} \cdot 2\pi \cdot \sqrt{L_{leakage} \cdot C8} < T_{Vin\_max}$,

$$\Delta V_{C8} = V_{spkie} \cdot (1 - e^{-\frac{t1}{R6 \cdot C8}}) \quad (30)$$

Where t1 is the time $T_{Vin\_max} - \frac{1}{4} \cdot 2\pi \cdot \sqrt{L_{leakage} \cdot C8}$. T_{Vin_max} is the switching period at V_{in_max}.

For selecting the snubber resistor R6, the reflecting voltage from secondary side must be taken into consideration, this voltage will constantly add on the snubber resistor after MOSFET turns off, so the resistor R6 should be large enough to reduce reflecting voltage loss.

In this case, according to the equation (6), (7), (10), the $I_{pk\_Vin\_max}$=0.349A, T_{on_265V}=2.05μs, T_{vin_max}=10.09μs, the leakage inductance is estimated as 1% of the primary inductance, 22μH, selecting the snubber parameters: C8=22nF, R6=100kΩ. Get, V_{spike}=123V, ΔV_{C8}=0.45V.

The voltage rating for the snubber cap and the diode should be larger than the V_{in_max}, the diode can use fast recover diode, such as FR107. It is hard to theoretically calculate the power dissipation of the snubber resistor R6, it needs to monitor the thermal performance of the resistor in test, if the temperature rise is high, it needs to change to a bigger power dissipation resistor.

J. VCC Power Supply (R5, R13, C6, C7, D3, D6)

The detailed VCC power supply function is described in page 11. The circuitry consists of R5, R13, C6, C7, D3, D6. Following should be taken into consideration for selecting the bulk capacitor C6, the voltage ripple at VCC and the VCC dropping time at quiescent mode, usually, the VCC ripple should be limited within 1V, typically 22μF is selected. The start resistor R5 with C6 determines the system start delay time, if a shorter delay time is required, select a smaller R5, but the power dissipation of the resistor and the charging current need to be taken care, here a 499kΩ resistor is selected. The resistor R13 is used to limit the charging current from the auxiliary winding, normally, there is oscillation spike voltage at the rising edge of the positive plateau of the auxiliary winding, the charging current should be limited within 100mA. But there will be about 2mA constant operation mean current flow through the resistor, so the value of the resistor can not be too large, usually, the resistor is selected from 100Ω~1kΩ. The voltage rating for the rectifying diode D3 should meet the following equation:

$$V_{D3} > VCC_{max} + \frac{N_{aux}}{N_p} \cdot V_{in\_max} + V_{aux\_negtive\_spike} \quad (31)$$

Where VCC_{max} is the maximum VCC voltage, in this case, VCC_{max}= 15V, N_{aux} and N_p are the auxiliary winding and primary winding turns, $V_{aux\_negtive\_spike}$ is the maximum negative spike on auxiliary winding, in this case, $V_{aux\_negtive\_spike}$= 40V,

A 100pF ceramic bypass capacitor (C7) is added to reduce the high frequency noise influence on VCC pin, and a 18V zener diode (D6) is also added to limit the VCC voltage at open load condition.

K. ZCD and OVP Detector (R1, R2, C11, D5)

Please refer to page 9 for detailed design information.
The resistor divider by R1 and R2 sets the OVP threshold:

$$V_{o\_ovp} \cdot \frac{N_{aux}}{N_s} \cdot \frac{R_2}{R_1 + R_2} = 5.4V \quad (32)$$

Where V_{o_ovp} is the output OVP setting voltage; N_{aux} is the auxiliary winding turns of the transformer and N_s is secondary winding turns of the transformer. In this case, V_{o_ovp}=20V, N_{aux}=27, N_s=24, we can select R2=22.1kΩ, R1=80.6kΩ. A 10pF ceramic bypass capacitor (C11) is added on ZCD pin to absorb the high frequency oscillation on ZCD voltage at MOSFET turning off. Also, a diode (D5) is connected from ZCD pin to GND to clamp the ZCD negative voltage which can help improve the noise influence for the ZCD pin.

L. Gate Driving Resistor and MULT Pin Resistor Divider (R7, R3, R4, C5)

Considering both fro the EMI performance and the MOSFET switching speed, the gate driving resistor (R7) is selected as 20Ω.

For the MULT pin resistor divider setting information, please refer to page 8. Here selecting the R3=1MΩ, R4=6.8kΩ,, C5=100pF.

M. Current Sensing Resistor and Feedforward (R8, R9, R10, R12, R14)

The current sensing resistor can be approximately set by the following equation:

$$R_s \approx \frac{V_{FB} \cdot N}{2 \cdot I_o} \quad (33)$$

Where N is the turn ratio of primary winding to secondary winding, V_{FB} is the feedback reference voltage (typically 0.4), R_s is the sensing resistor connected between the MOSFET source and GND.

But in real application of primary side control, it is hard to get a totally accurate equation for the output current, because there are many factors influencing the output current setting value, such as the internal logic delay of the IC, the transformer inductance, the MOSFET input and output capacitor, the ZCD detection delay time, even the RCD snubber and the gate driver resistor…etc. So, this is why the current sensing resistor is last decided in design and the value must be fine tuned in bench test to get the required output current. For the feedforwad compensation function description, please refer to page 12. There are the same influence factors for the feedforward compensation, it also need fine tune case by case.

In this application with bench test, the sensing resistor is tuned as 2Ω and feedforward compensation can be very small (R10=10MΩ, R12=100Ω).

N. ZCD OCP Detector (R15, R16, D8)

Please refer to page 11 for detailed design information.
The primary-side OCP setting point can be calculated as:

$$I_{PRI\_OCP} \cdot R_{CS} \cdot \frac{R_{16}}{R_{15} + R_{16}} - V_{D8} = 0.6V \quad (34)$$

Where I_{PRI_OCP} is primary-side over current protection current value, V_D is the voltage drop of the diode. To avoid the effect of the ZCD zero-current detector, the value of the resistors to set the OCP threshold (R_{15} & R_{16}) should be smaller than those of the ZCD zero-current detector (R_1 & R_2). In this case, we select R15=510Ω, R16=3kΩ, D8 is 1N4148, the primary-side OCP setting point is limited to less than 800mA.

O. Layout Guideline

- The path of the main power flow should be as short as possible, and the wire should be as wide as possible, the cooper pour for the power devices should be as large as possible to get a good thermal performance.
- Separate the power GND and the analog GND, connect the two GND only at a single small point (here is the anode of D5).
- In order to minimize the coupling influence from the primary winding to the auxiliary winding, the same mean dot of the two windings should be far away. It is better to be separated by the GND.
- The IC pin components should be placed as close as possible to the corresponding pin, especially the ZCD bypass capacitor and the COMP pin capacitor.
- The primary side and the secondary side should be well isolated, the trace from the transformer output return pin to the return point of the output filter capacitor should be as short as possible.

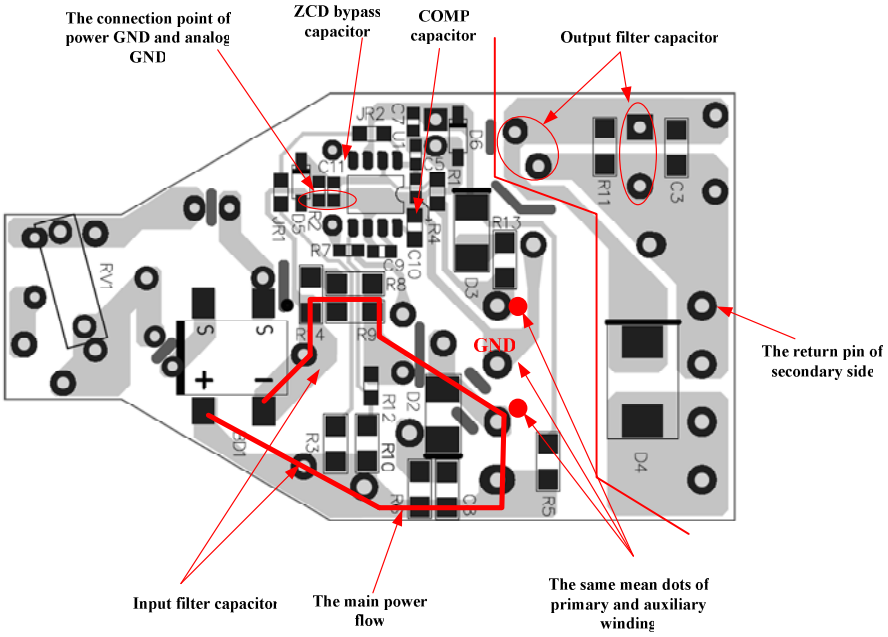


Figure 24—The Bottom Layer

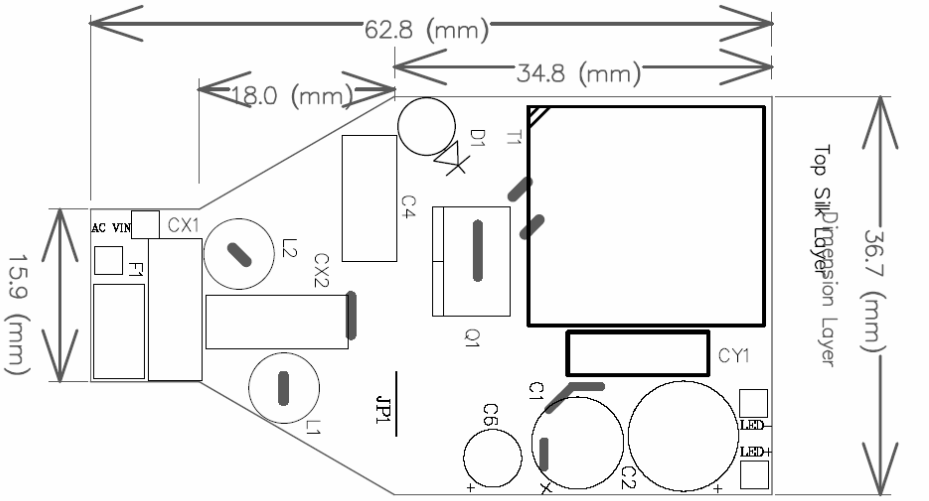


Figure 25—The Top Layer

P. BOM

Qty	RefDes	Value	Description	Package	Manufacturer	Manufactuer_P/N
1	BD1	DF06S	BRIDGE, 600V, 1A	SMD	Fairchild	DF06S
2	C1, C2	470μF/35V	Electrolytic Capacitor, 35V	DIP	Rubycon	470μF/35V
1	C3	NC				
1	C4	33nF/400V	CBB, 400V	DIP	Panasonic	ECQE400VDC333K
2	C5, C7	100pF	Ceramic Capacitor, 50V, X7R	0603	LION	0603B10K500T
1	C6	22μF/50V	Electrolytic Capacitor, 50V	DIP	Jianghai	CD281L-50V22
1	C8	22nF/630V	Ceramic Capacitor, 630V, X7R	1206	TDK	C3216X7R2J223K
1	C9	NC				
1	C10	2.2μF/10V	Ceramic Capacitor, 10V, X7R	0805	Murata	GRM21BR71A225KAO1
1	C11	10pF	Ceramic Capacitor, 50V, COG	0603	Murata	GRM1885C1H100JAO1
1	CX1	68nF	Film Capacitor, X2, 275V	DIP	Carli	PX683K3IC39L270D9R
1	CX2	47nF	Film Capacitor, X2, 275V	DIP	Carli	PX473K3IC39L270D9R
1	CY1	2.2nF/250V	Y Capacitor, 250V	DIP	Hongke	JYK09F222ML72N
1	D1	NC				
1	D2	US1K	Diode, 1A, 800V	SMA	Vishay	US1K-E3/61T
1	D3	ES1D	Diode, 1A, 200V	SMA	Taiwan Semi	ES1D
1	D4	MURS320	Diode, 3A, 200V	SMC	ON Semi	MURS320T3
2	D5, D8	1N4148	Diode, 0.15A, 75V	SOD-123	Diodes	1N4148W
1	D6	BZT52C18	Zener Diode, 5mA, 18V	SOD-123	Diodes	BZT52C18-F
1	D7	NC				
1	F1	250V/2A	Fuse, 250V, 2A	DIP	COOPER	SS-5-2A
2	L1, L2	4.7mH	Inductor, 4.7mH	DIP	Any	
1	Q1	STK0765BF	MOSFET, 7A, 650V	TO-220F	AUK	STK0765BF
1	R1	80.6kΩ	Film RES, 1%	0603	Yageo	RC0603FR-0780K6L
1	R2	22.1kΩ	Film RES, 1%	0603	Yageo	RC0603FR-0722K1L
2	R3, R11	1MΩ	Film RES, 1%	1206	Yageo	RC1206FR-071ML
1	R4	6.8kΩ	Film RES, 1%	0603	Yageo	RC0603FR-076K8L
1	R5	499kΩ	Film RES, 1%	1206	Panasonic	ERJ8ENF4993V
1	R6	100kΩ	Film RES, 5%	1206	Yageo	RM12JTN104
1	R7	20Ω	Film RES, 1%	0603	Yageo	RC0603FR-0720RL
1	R8	1.5Ω	Film RES,1%	1206	Royalohm	1206F150KT5E
1	R9	3.3Ω	Film RES,1%	1206	Royalohm	1206F330KT5E
1	R10	10MΩ	Film RES,1%	1206	Royalohm	1206F1005T5E
1	R12	100Ω	Film RES, 1%	0603	Yageo	RC0603FR-07100RL
1	R13	1kΩ	Film RES, 1%	1206	Royalohm	1206F1001T5E
1	R14	1Ω	Film RES, 1%	1206	Royalohm	1206F100KT5E
1	R15	510Ω	Film RES, 1%	0603	Yageo	RC0603FR-07510RL
2	JR1, JR2	0Ω	Film RES, 5%	0603	Royalohm	RR1608(0603)L0R0JT
1	R16	3kΩ	Film RES, 1%	0603	Yageo	RC0603FR-073KL
1	R17	NC				
2	R18, R19	5.1kΩ	Film RES, 5%	1206	Liz	CR06T05NJ5K1
1	RV1	NC				
1	T1	EFD20	L_P=2.2mH, N_P:N_S:N_{AUX}=144:24:27	EFD20	Yangyang	FX0136
1	U1	MP4021A	Offline LED Lighting Controller	SOIC8	MPS	MP4021GS-A-Z
1	U2	NC				

5. EXPERIMENTAL RESULT

All measurements performed at room temperature

5.1 Efficiency Vs Line Voltage

Vin (VAC)	Pin (W)	Vo (V)	Io (mA)	efficiency (%)
86	10.09	15.82	512	80.28
90	9.93	15.78	509	80.89
100	9.76	15.77	507	81.92
110	9.65	15.76	506	82.64
120	9.59	15.75	505	82.94
136	9.51	15.75	504	83.47
151	9.48	15.75	504	83.73
175	9.43	15.74	503	83.96
201	9.46	15.74	502	83.53
221	9.5	15.74	503	83.34
231	9.53	15.73	503	83.02
251	9.59	15.74	504	82.72
263	9.64	15.73	504	82.24

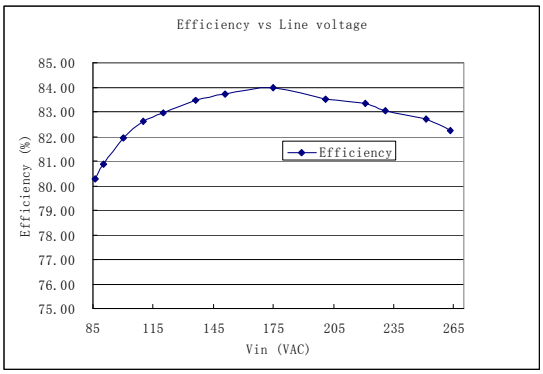


Figure 26— Efficiency Vs Input Line Voltage

5.2 Output LED Current Line Regulation

Vin (VAC)	86	90	100	110	120	136	151	175	201	221	231	251	263
Io (mA)	512	509	507	506	505	504	504	503	502	503	503	504	504

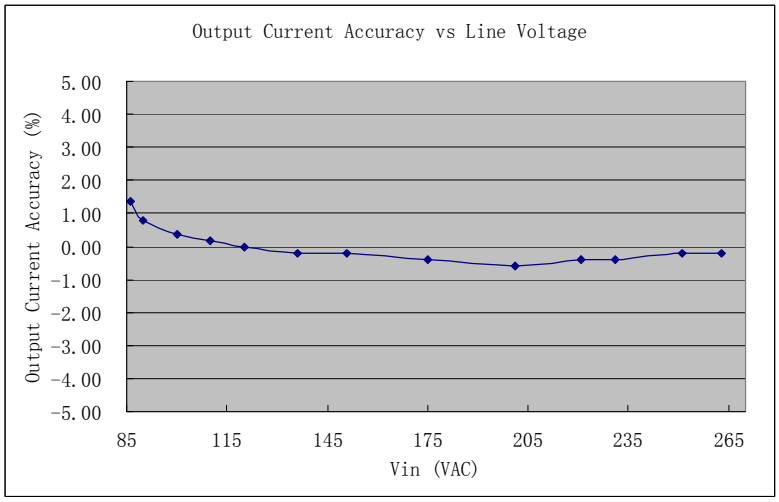


Figure 27— Output Current Accuracy Vs Input Line Voltage

5.3 PF, THD VS Line Voltage

Vin (VAC)	86	90	100	110	120	136	151	175	201	221	231	251	263
PF (%)	99.2	99.2	99.1	99	98.8	98.5	98.2	97.4	96.4	95.3	94.8	93.4	92.5
THD (%)	14.9	14.8	14.8	15	15.1	15.1	15.2	16.5	16.7	16.7	16.9	16.8	17
Third harmonic (%)	14.2	14.2	14.1	14.3	14.4	14.5	14.5	15.2	15.4	15.4	15.4	15.4	15.5

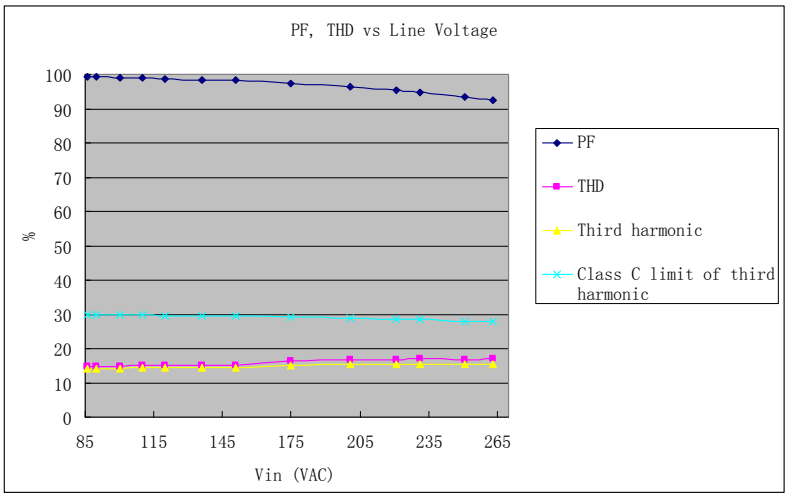


Figure 28— Output Current Accuracy Vs Input Line Voltage

5.4 Conducted EMI

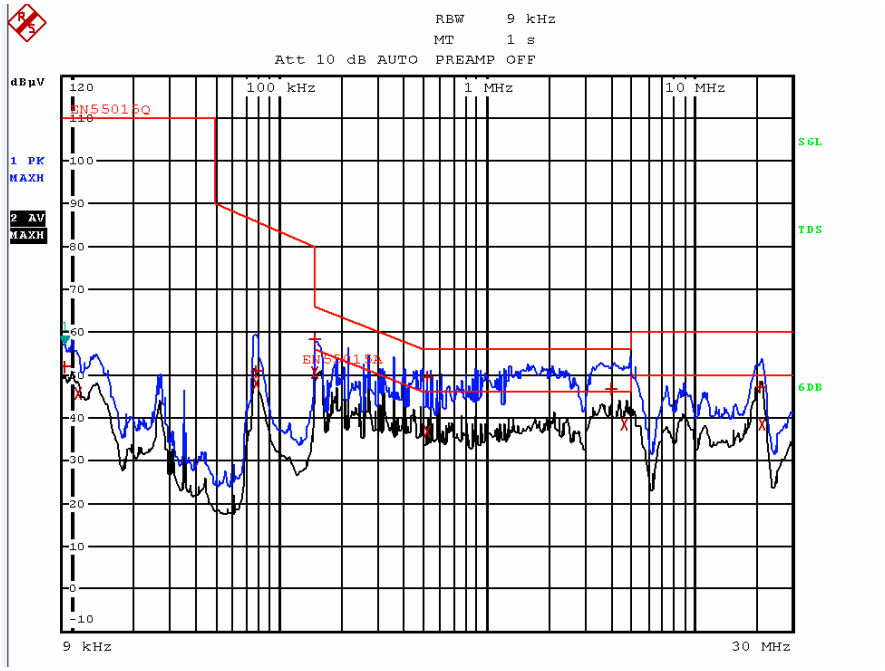


Figure 29— Conducted EMI performance at 220V AC input

5.5 Steady State

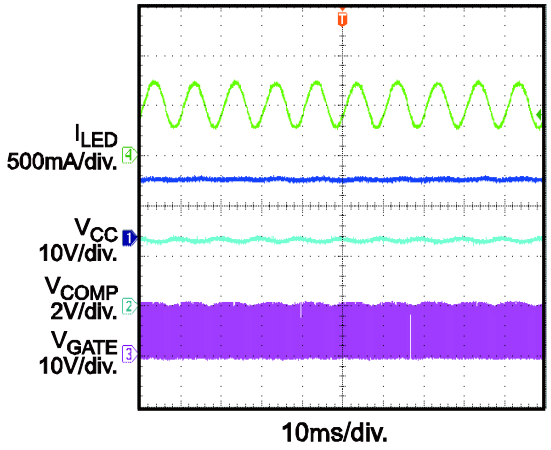


Figure 30— 110 VAC, Full Load

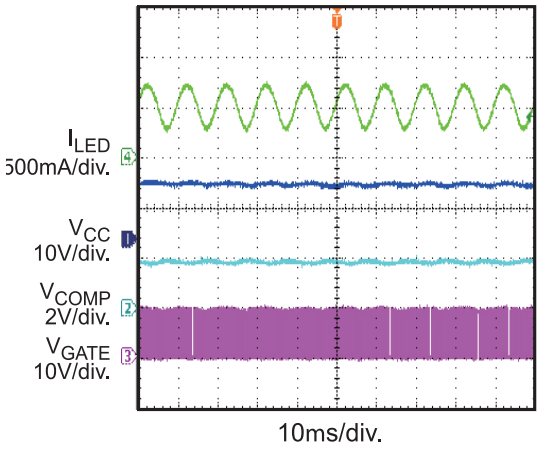


Figure 31— 220 VAC, Full Load

5.6 Input Voltage and Current

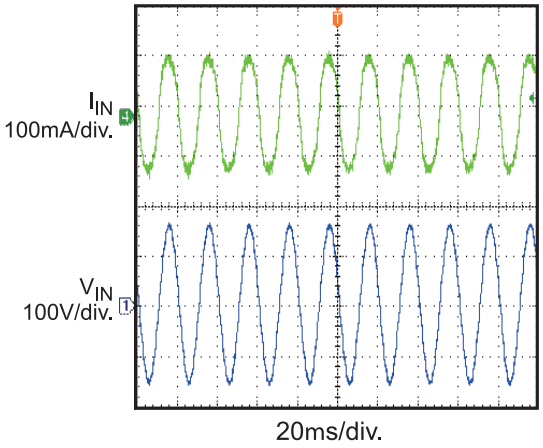


Figure 32— 110 VAC, Full Load

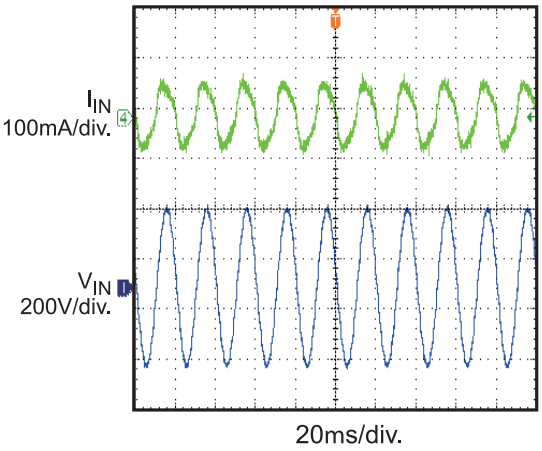


Figure 33— 220 VAC, Full Load

5.7 Boundary Conduction Operation

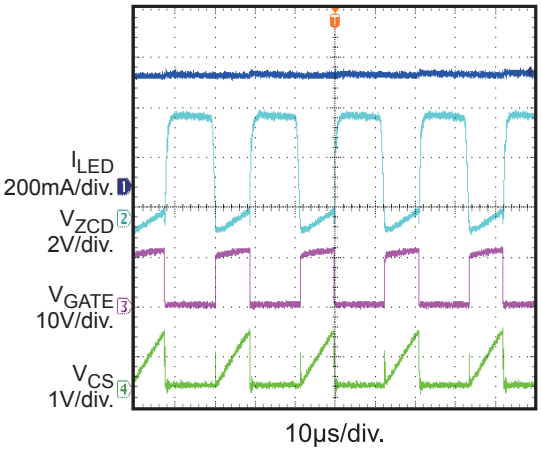


Figure 32— 110 VAC, Full Load

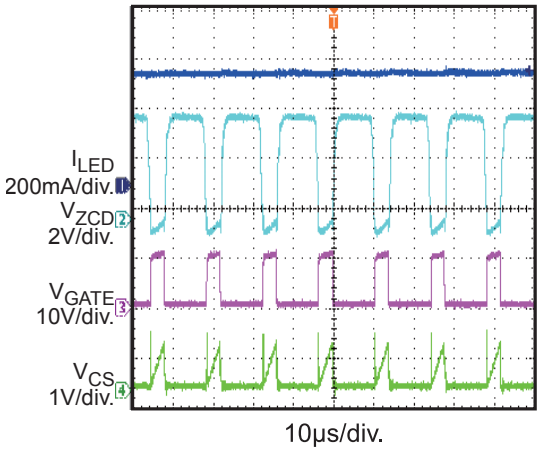


Figure 33— 220 VAC, Full Load

5.8 Start Up

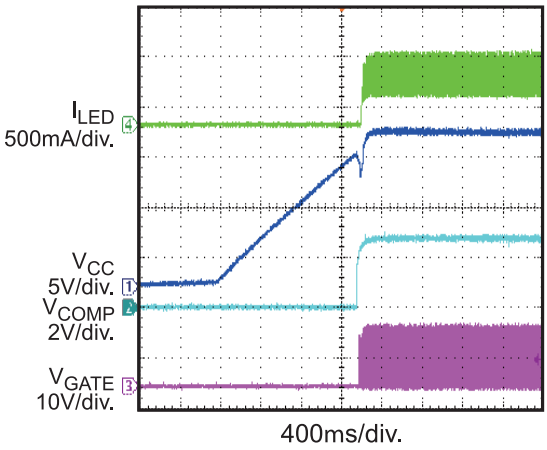


Figure 34— 110 VAC, Full Load

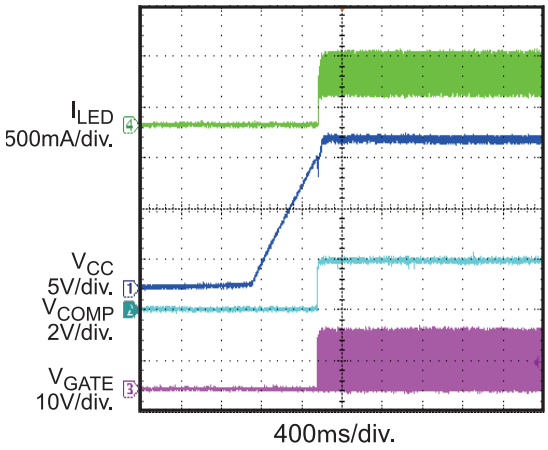


Figure 35— 220 VAC, Full Load

5.9 OVP (Open load at normal operation)

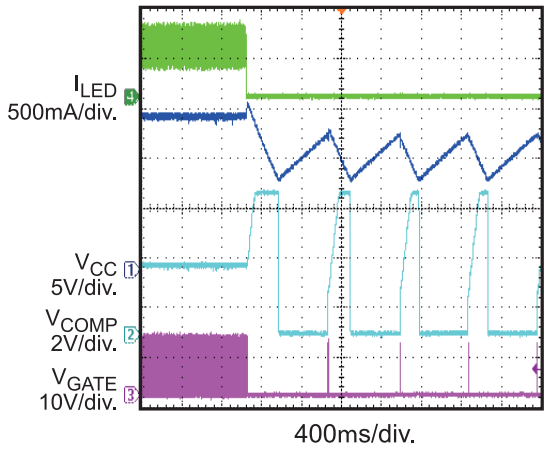


Figure 36— 110 VAC

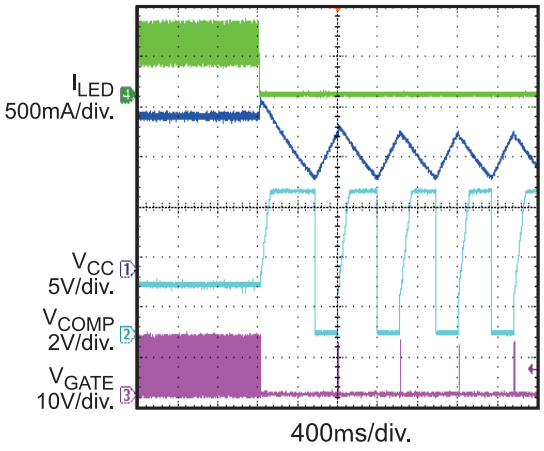


Figure 37— 220 VAC

5.10 SCP (Short LED+ to LED- at normal operation)

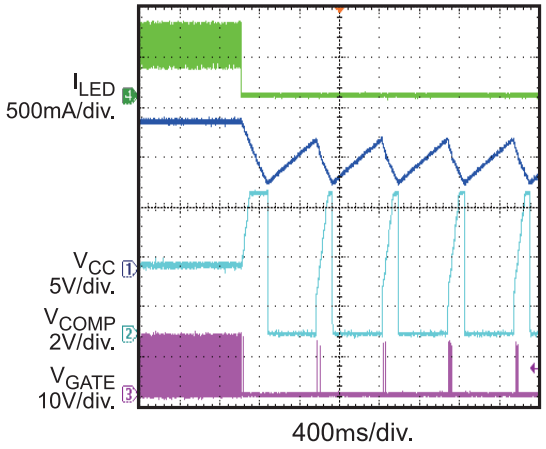


Figure 38— 110 VAC

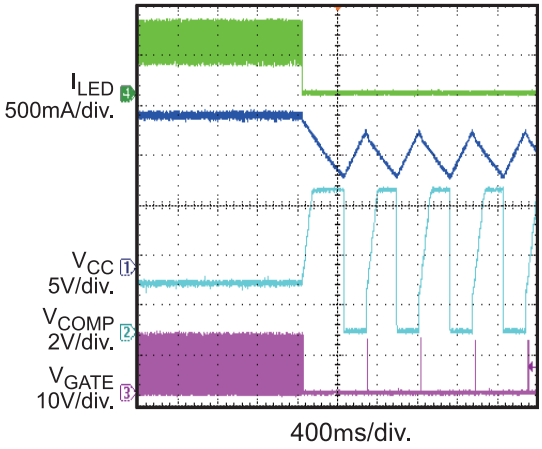


Figure 39— 220 VAC

ANNEX

Design Guide for Replacing MP4021 with MP4021A

Prepared by Zhijun Ye

Feb 09, 2012

CONTENT

A-1. INTRODUCTION

The MP4021/MP4021A is a primary-side-control offline LED lighting controller with PFC integrated. The MP4021A are designed to be a pin and functionality compatible chip with MP4021. The MP4021A is the improved revision of MP4021.

This note is a guide to assist users of MP4021 converting existing designs to MP4021A and it summarizes the differences between MP4021 and MP4021A to be aware of for applications. For detailed information on the chips, please refer to the datasheets.

The features in MP4021A that are not in conflict with those in MP4021 are not listed in this document.

A-2. SUMMARY OF IMPROVEMENTS

Compared with the MP4021, the MP4021A features four electrical characteristic improvements and one added protection function. They are all summarized in **Table A-1**.

Table A-1—Functional Improvements

Item	*MP4021*	*MP4021A*	*Improvements*
1. The Distribution of Feedback Voltage	±3.5%	±2.65%	Circuitry optimization to improve the accuracy of LED current regulation
2. The Lower COMP Clamp Voltage	0.9V	1.5V	
3. The Gain of the Multiplier	K=0.6	K=1	Prevent COMP saturation
4. VCC UVLO	12V / 8V	13.6V / 9V	Raise GATE output voltage to increase driving capacity
5. Over-current Detector	No	Yes	More reliable SCP

Item 1 to 4 almost have no impact on the existing MP4021 solutions. For Item 5, an additional SCP detector circuitry is applied to implement ZCD over-current protection for MP4021A's solution.

Figure A-1 shows a typical 8W LED Bulb driver application for universal input with MP4021A.

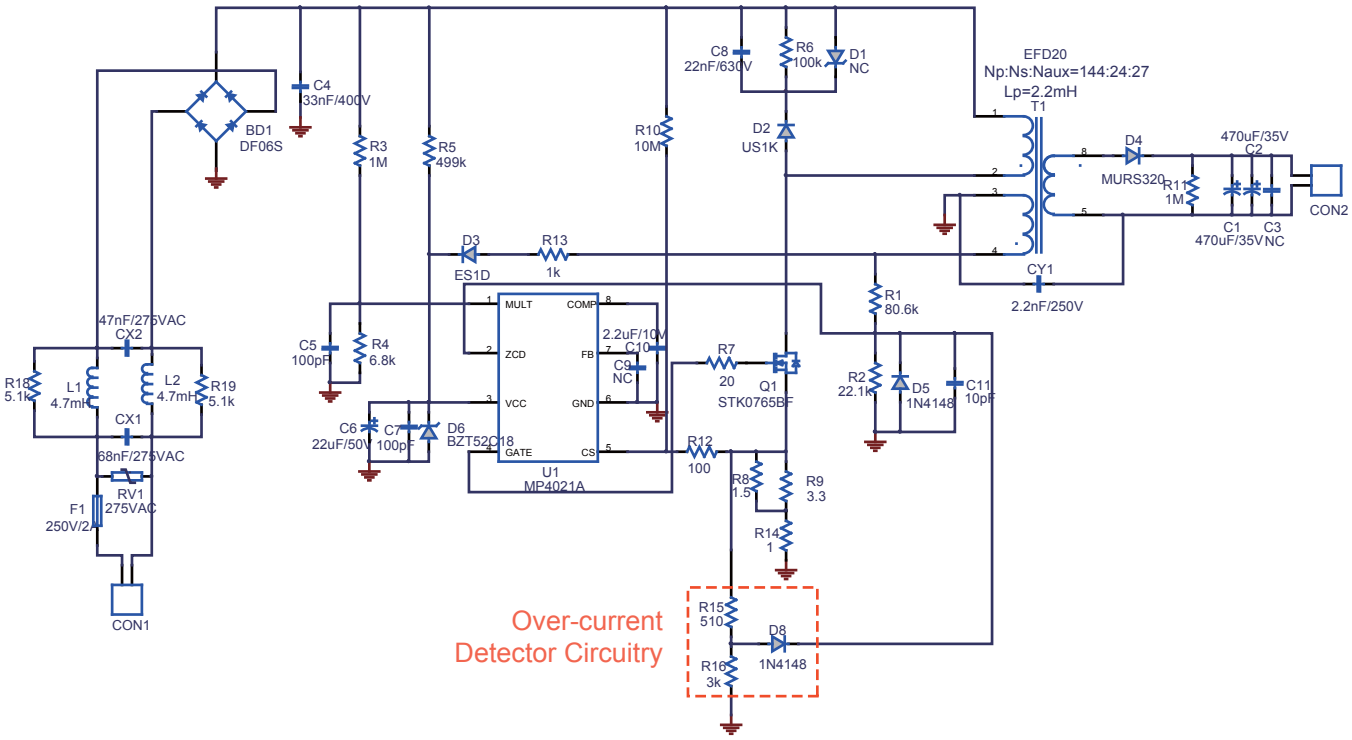


Figure A-1—Universal Input, Isolated Flyback Converter, Drive 5 LEDs in Series, 500mA LED Current for 8W LED Bulb Lighting with MP4021A

R15, R16 & D8 are used to monitor the OCP condition. The primary-side OCP threshold is set by the forward voltage of D8 and the divider ratio of R15 and R16.

A-3. ZCD OVER-CURRENT PROTECTION

Figure A-2 is the MP4021A Function Block Diagram of ZCD OCP Circuitry.

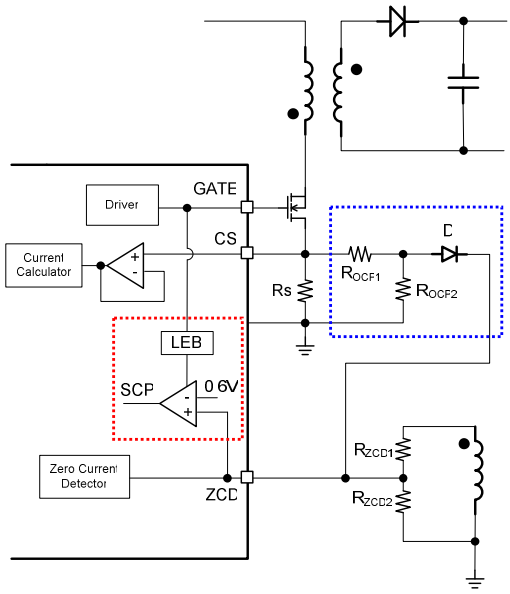


Figure A-2—MP4021A Function Block Diagram of ZCD OCP Circuitry

The MP4021A's ZCD pin is multi-purpose. As over current detector, the MP4021A integrates a SCP comparator, shown in red block of **Figure A-2**. For primary-side control proposal, Rs is the primary sensing resistor which samples the primary current. Tie a resistor divider form CS sensing resistor to ZCD pin thru a diode, shown in blue block of **Figure A-2**. When the power MOSFET of the primary-side is turned on, the ZCD pin monitors the rising primary-side current, once the ZCD pin reaches OCP threshold, typical 0.6V, the gate driver will be turned off to prevent the chip form damage. And then the IC works at quiescent mode, the VCC voltage dropped below the UVLO which will make the IC shut down and the system restarts again.

The primary-side OCP setting point can be calculated as:

$$I_{PRI\_OCP} \cdot R_S \cdot \frac{R_{OCP2}}{R_{OCP1} + R_{OCP2}} - V_D = 0.6V$$

Where I_{PRI_OCP} is primary-side over current protection current value, V_D is the voltage drop of the diode. R_{OCP1} and R_{OCP2} is used to program the over current protection threshold (I_{PRI_OCP}).

Please note that, when the MOS is turned on, the taps of the ZCD zero-current detector resistor divider and the OCP resistor divider are connected by a diode. So, to avoid the effect of the ZCD zero-current detector, the value of the resistors to set the OCP threshold (R_{OCP1} & R_{OCP2}) should be about 10 times smaller than those of the ZCD zero-current detector (R_{ZCD1} & R_{ZCD2}).

A-4. DESIGN EXAMPLE OF ZCD OCP CIRCUITRY

Take the solution of **Figure A-1** for example.

***Step 1*: Check the max V_{CS} @ min input voltage for normal operation. (V_{CS_MAX})**

According to the bench test result, V_{CS_MAX} @ 85VAC =1.2V

***Step 2*: Set primary-side OCP point (V_{CS_OCP}) to about 15%-20% higher than V_{CS_MAX}.**

V_{CS_OCP} = (1+20%) x V_{CS_MAX} = 1.44V

Since R_{ZCD2}=22.1kΩ, set R_{OCP2}=3kΩ & the forward voltage of 1N4148 is about 0.6V

***Step 3*: Set the ZCD OCP resistor divider by the equation:**

$$R_{OCP1} = \frac{V_{CS\_OCP} \cdot R_{OCP2}}{0.6 + V_D} - R_{OCP2} = 600\Omega$$

Here, set R_{OCP1}=510Ω to get a lower threshold.

***Step 4*: Verify the setting on the bench.**

For SCP, with lower primary-side OCP point, the system can earlier run into quiescent mode.

But make sure to be left sufficient margin to avoid SCP mis-triggering at low line input.

A-5. BENCH TEST RESULTS

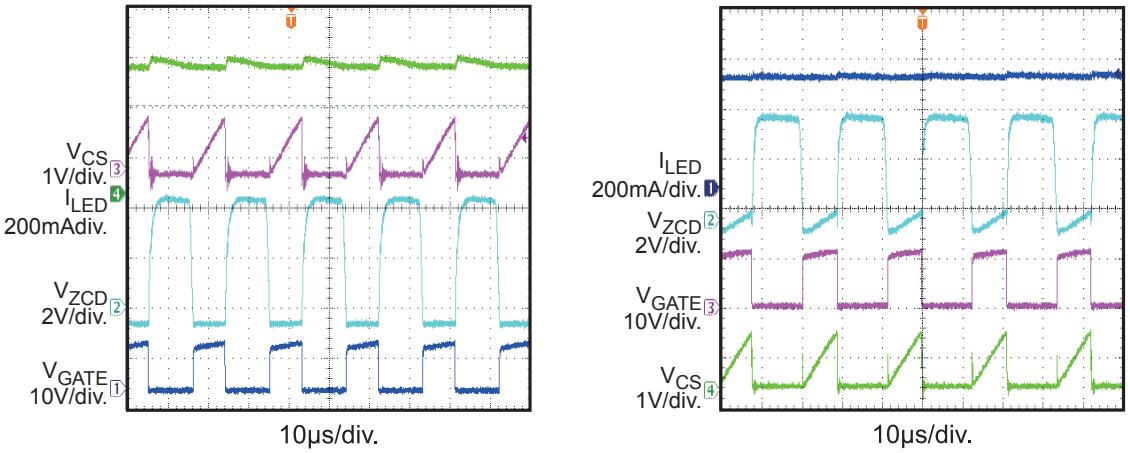
Based on the solution of **Figure A-1**.

A-5.1 Steady State

For normal operation, the main difference is ZCD waveform when the primary-side MOS is turned on.

With MP4021, the ZCD negative voltage is clamped to -0.6V by external ZCD diode D5.

With MP4021A, the sampled CS voltage is added on ZCD pin thru the ZCD OCP circuitry.



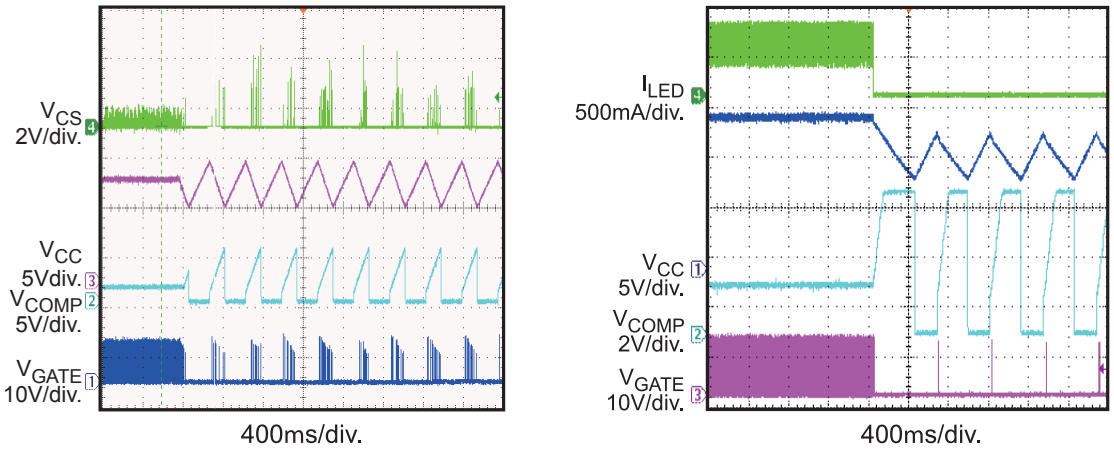
(a) MP4021 solution ***(b) MP4021A solution***

Figure A-3— The Operation of Steady State @ 110VAC, Full Load

A-5.2 Short LED+ to LED- at Normal Operation

Once output short circuit occurs, the voltage of the auxiliary winding falls down following the output voltage of the secondary winding and then the VCC drops to lower than UV threshold and re-starts the system. The MP4021's GATE keeps switching until VCC drops to UVLO.

With MP4021A, as long as the primary-side over-current condition is detected, ZCD OCP is triggered and switching stops until the system re-starts again.



(a) MP4021 solution ***(b) MP4021A solution***

Figure A-4—The SCP Operation @ 220VAC, Full Load

A-5.3 Thermal Test at Output SCP

Table A-2—Thermal Test at Output SCP
(Burn-in 0.5 hour@265VAC)

(a) The solution with MP4021

RefDes	Description	Temp(℃)	△(℃)
L1,L2	Differential inductor	33	5.1
BD1 package	Bridge diode	39.4	11.5
BD1 pin	Bridge diode	39.5	11.6
C1	Bulk Cap	45.8	17.9
T1 windings	Transformer	83	55.1
T1 core	Transformer	74.1	46.2
U1 package	MP4021	39.7	11.8
U1 pin	MP4021	39.6	11.7
D4	Output diode	116.7	88.8
R6	Snubber resistor	57.2	29.3
C8	Snubber cap	61.4	33.5
D2	Snubber diode	55.2	27.3
Q1	MOSFET	45.6	17.7
R8, R9	Sense resistor	46.2	18.3

(b) The solution with MP4021A

RefDes	Description	Temp(℃)	△(℃)
L1,L2	Differential inductor	29.4	6.7
BD1 package	Bridge diode	30.5	7.8
BD1 pin	Bridge diode	28.5	5.8
C1	Bulk Cap	25.2	2.5
T1 windings	Transformer	28.9	6.2
T1 core	Transformer	28.6	5.9
U1 package	MP4021	27.2	4.5
U1 pin	MP4021	28.1	5.4
D4	Output diode	30.3	7.6
R6	Snubber resistor	34.3	11.6
C8	Snubber cap	36.1	13.4
D2	Snubber diode	33.5	10.8
Q1	MOSFET	29.7	7
R8, R9	Sense resistor	30.6	7.9

The MP4021A solution is with ZCD OCP circuitry. Once output short circuit occurs, the system can works in hiccup mode, all the components are cool.

Please consult datasheets and applications (AN038 and AN059) for details on the different electrical characteristics and performances between MP4021 and MP4021A.