

Application Note

Design Guidelines for Off-line Flyback Converters Using MP3900

ABSTRACT

This paper presents design guidelines for offline flyback converters with PWM controller-MP3900 of MPS. Design of a flyback converter with MP3900 is made easier through use of this step-by-step design procedure from this paper. Experimental results based on the design example are presented in the last part.

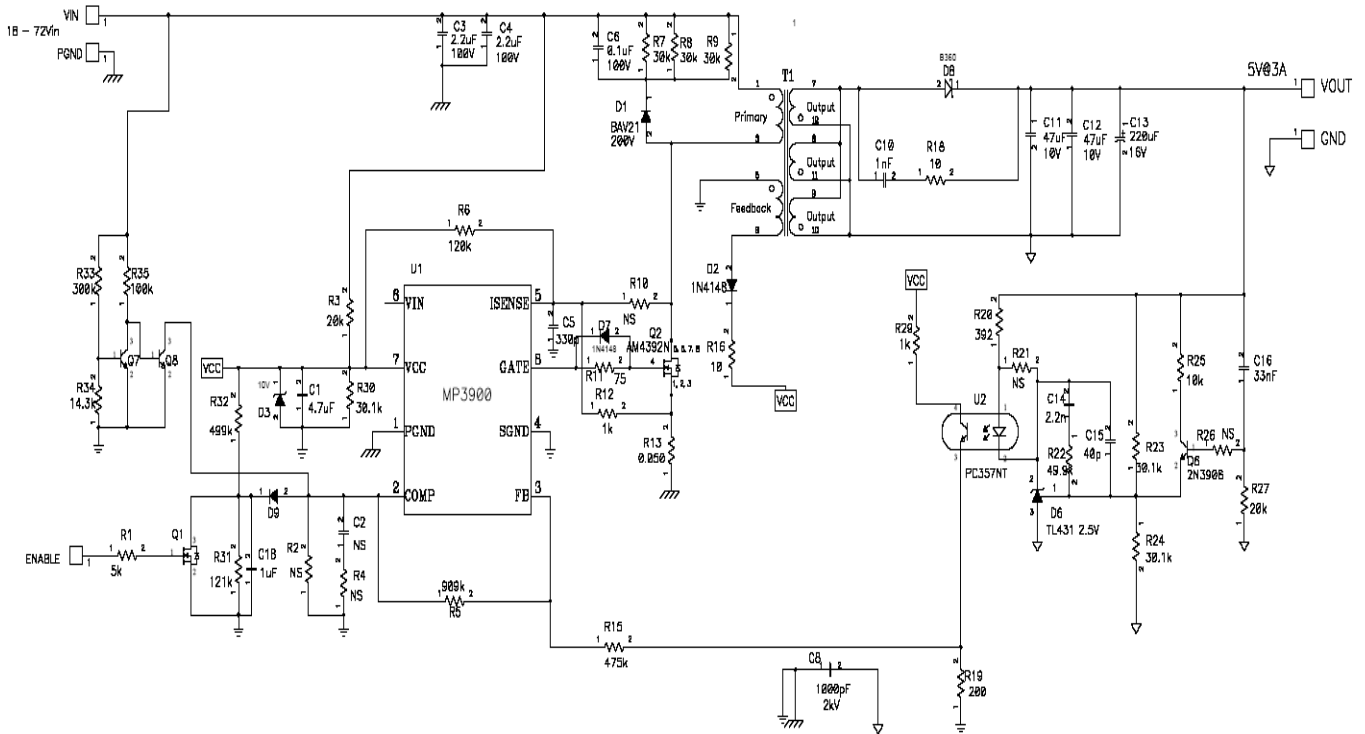


Fig.1 Basic off-line Flyback Converter Using MP3900

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INTRODUCTION

MP3900 is a PWM controller that drives an external MOSFET capable of handling 10A current. It has a typical quiescent operational current of 180uA and can accommodate off-line, telecom and non-isolated applications. Internal undervoltage lockout, slope compensation and peak current limit are all provided to minimize the external component count. This paper presents practical design guidelines for an off-line flyback converter employing MP3900. Step-by-step design procedure for flyback converter using MP3900 can be applied to various offline applications, mainly including transformer design, output filter design, component selection and control loop design.

DESIGN PROCEDURE

Fig.1 is used as the reference for design procedure presented in this section.

Predetermine the Input and Output Specifications.

Input voltage range: $V_{in(max)}$, $V_{in(min)}$.

Output: V_{out} , $I_{out(min)}$, $I_{out(max)}$, P_{out}

Estimated efficiency: E_{ff} , It is used to estimate the power conversion efficiency to calculate the maximum input power. Generally, E_{ff} is set to be 0.7~0.85 according to different output applications.

Switching frequency: f_s

Higher frequency reduces cost, output ripple and converter size, but also degrades efficiency and thermal performance. MP3900 employs fixed frequency 330kHz.

Determine Flyback Converter Operation

A flyback converter has two kinds of operation modes: Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). Discontinuous mode (Fig.2) operation provides better switching conditions (zero switching on current) for rectifier diodes, requires less transformer magnetic inductance and usually means a smaller transformer size. The current ripple is large which usually results in higher winding loss and core loss. Continuous mode operation (Fig.3) offer higher output power, less ripple current. Generally, DCM is recommended for high voltage and low power applications; CCM is preferred for low voltage and some high power applications. In a typical application, the converter usually operates in CCM at heavy load condition and DCM in light load condition. Here, we choose the flyback converter to operate in CCM at full load condition for our design procedure.

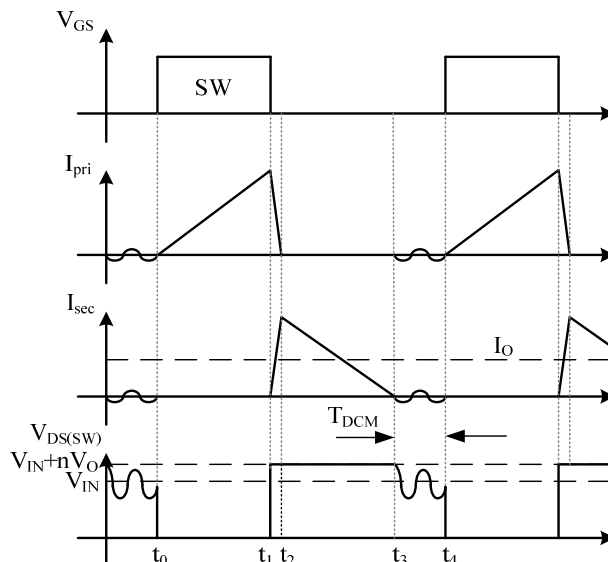


Fig.2 DCM Operation of Flyback Converter

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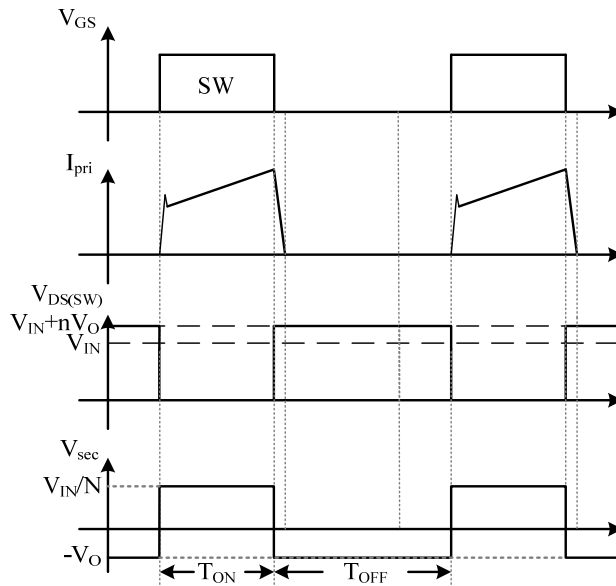


Fig.3 CCM Operation of Flyback Converter

Transformer Design

The design of the transformer is one of the most important stages in the flyback converter design. A flyback transformer is actually a coupled inductor. Unlike a true transformer, its main purpose is to store energy, not simply to transfer it. The design of the flyback transformer is different from the transformer for other topologies, like forward, half bridge and full bridge. In order to store and return energy to the circuit efficiently and with minimum physical size, a small non-magnetic gap (typically air gap) is required in series with a high permeability magnetic core material. Virtually, all of the energy is stored in the so-called non-magnetic gap(s). The core provides an easy, low reluctance flux path to link the energy stored in the gap to the winding. The transformer, in essence, efficiently couples the energy storage location to the external circuit. Flyback transformer design is somewhat iterative process, due to the number of variables involved.

1. Determine the transformer turn ratio N

The turn ratio of a flyback converter transformer is an important parameter, which affects the current levels associated with the primary side and secondary rectifier diode and thus the power loss related to the primary side and secondary side.

The turn ratio is affected by the maximum duty cycle for a given application. In CCM condition with a given D_{max} , the minimum turns ratio can be calculated as:

$$N = \frac{D_{max}}{1 - D_{max}} \cdot \frac{V_{in(min)}}{V_{out}} \tag{1}$$

For a flyback converter operating in CCM condition with current mode control, the maximum duty cycle D_{max} is usually set to be less than 50%.

Also, the voltage stress at the MOSFET drain due to the reflected output voltage is also affected by the turn ratio (Higher turn ratio causes higher voltage stress on the primary MOSFET). Too high turns ratio N means the voltage rating of the primary side switch is high, which usually means higher conduction loss and switching losses even though the secondary side power loss reduces due to the lower voltage rating diode which can be used. There is a tradeoff to optimize the turn ratio N.

2. Determine the transformer primary side inductance L_m

For both operation modes (CCM & DCM), full load with minimum input voltage is considered to be the worst case in designing the transformer inductance. Therefore, L_m can be calculated as:

$$L_m = \frac{V_{in(min)} \cdot D_{max}}{\Delta I \cdot f_s} \cdot D_{max} \tag{2}$$

Here, ΔI is the ripple of transformer primary inductor current, see Fig.4

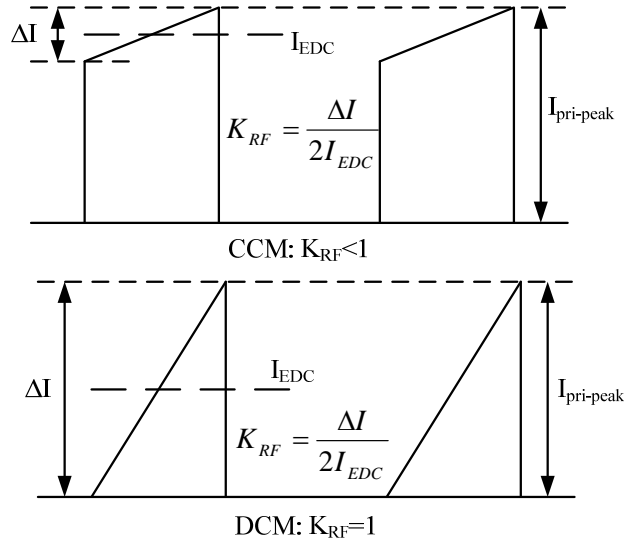


Fig.4 Transformer Primary Inductor Current

Normally ΔI is represented by the current ripple factor K_{RF} , which is equal to:

$$K_{RF} = \frac{\Delta I}{2I_{EDC}} = \frac{\Delta I \cdot V_{in(min)} \cdot D_{max}}{2P_{in}} \tag{3}$$

For DCM operation $K_{RF}=1$ and for CCM operation $K_{RF}<1$. In order to have good core utilization and reasonable overall efficiency, it is reasonable to set K_{RF} between 0.3 and 0.5. Therefore, L_m can be calculated from (2) and (3) as follows:

$$L_m = \frac{(V_{in(min)} \cdot D_{max})^2}{2P_{in} \cdot f_s \cdot K_{RF}} \text{ (H)} \tag{4}$$

3. Transformer core selection

A core appropriate for certain output power at the operating frequency needs to be selected. Ferrite is widely adopted in flyback transformer. The core area product ($A_e A_w$) which is the core magnetic cross-section area multiplied by window area available for winding, is widely used for an initial estimate of core size for a given application. A rough indication of the required area product is given by following^[1]:

$$A_e \cdot A_w = \left(\frac{L_m \cdot I_{peak} \cdot I_{rms} \times 10^4}{B_{max} \cdot K_u \cdot K_j \cdot f_{sw}} \right)^{4/3} \text{ cm}^4 \tag{5}$$

where K_u is winding factor which is usually 0.25~0.3 for an off-line transformer. K_j is the current-density coefficient (typically 400~450 for ferrite core). I_{peak} and I_{rms} is the peak current and RMS current of the primary inductance. B_{max} is the allowed maximum flux density in normal operation which is usually preset to be the saturation flux density of the core material (0.3T~0.4T).

To select the proper core refer to the manufacture's datasheet. Usually, the shape of the core is not a significant consideration for continuous mode operation due to low AC losses. For discontinuous mode operation, the winding area window is chosen as wide as possible to minimize AC winding losses. EC, ETD, EFD, LP cores are all E-E core shapes with large wide windows. Applications requiring low profile can benefit from using EFD cores.

4. Primary and secondary winding turns

With a given core size, there is a minimum number of turns for the transformer primary side winding to avoid saturation. The normal saturation specification is E-T or volt-time rating. The E-T rating is the maximum voltage, E, which can be applied over a time of T seconds. (The E-T rating is identical to the product of inductance L and peak current) Equation (8) defines a minimum value of N_p for the transformer primary winding to avoid the core saturation:

$$N_p = \frac{L_m \cdot I_{peak}}{BA_E} \times 10^6 \text{ (turns)} \quad (8)$$

Where:

L_m = the primary inductance of the transformer (H)

B = the maximum allowable flux density (T)

A_E = the effective cross sectional core (mm^2)

I_{peak} = the peak current in the primary side of the transformer, which is given as,

$$I_{peak} = I_{EDC} + \frac{1}{2} \cdot \Delta I = \frac{P_{in}}{V_{in(min)} \cdot D_{max}} + \frac{V_{in(min)} \cdot D_{max}}{2 \cdot L_m \cdot f_s} \quad (9)$$

The maximum allowable flux density B should be smaller than the saturation flux density B_{sat} . Since B_{sat} decreases as the temperature goes high, the high temperature characteristics should be considered.

Secondary turn count is a function of turn ratio n and primary turn count N_p :

$$N_s = N_p / N \quad (10)$$

5. Wire size

Once all the winding turns have been determined, wire size must be properly chosen to minimize the winding conduction loss and low leakage inductance. The amount of loss depends on how much current is being drawn from the winding, the length of wire and what wire size is used.

The wire size could be determined by the RMS current of the winding. For a flyback converter, the RMS current on secondary side is:

$$I_{rms-sec} = \sqrt{\frac{1-D_{max}}{3} \left[3 \left(\frac{I_{out}}{1-D_{max}} \right)^2 + \left(\frac{V_{out} \cdot (1-D_{max}) \cdot N^2}{2 \cdot L_m \cdot f_{SW}} \right) \right]} \quad (11)$$

Then, the wire size required is:

$$S = \frac{I_{sec}^{rms}}{J} \text{ (mm}^2\text{)} \quad (12)$$

Here J is the current density of the wire which is 5A/mm^2 typically.

Due to the skin effect and proximity effect of the conductor, the diameter of the wire selected is usually less than $2 \cdot \Delta d$ (Δd : skin depth):

$$\Delta d = \sqrt{\frac{1}{\pi \cdot f_s \cdot \mu \cdot \sigma}}$$

Where μ is the magnetic permeability which equals $4\pi \times 10^{-7}$ H/m, σ is the conductivity of the wire, for copper, σ is typically 6×10^7 S/m.

Therefore, multiple strands of thinner wire or Litz wire is usually adopted to minimize the AC resistance, the effective cross section area of multi-strands wire or Litz wire should large enough to meet the requirement set by the current density. The primary wire size selection is similar.

After the wire sizes have been determined, it is necessary to check whether the window area with selected core can accommodate the windings calculated in the previous steps. The window area required by each winding should be calculated respectively and added together, the area for interwinding insulation and spaces existing between the turns should also be taken into consideration. The fill factor, means the winding area to the whole window area of the core, should be well below 1 due to these interwinding insulation and spaces between turns. It is recommended that a fill factor no greater than about 30% be used. For transformers with multiple outputs this factor may need to be reduced further.

Based on these considerations, the total required window area is then compared to the available window area of a selected core. If the required window area is larger than the selected one, either wire size must be reduced, or a larger core must be chosen. Of course, a reduction in wire size increase the copper loss of the transformer.

6. Air gap

With the selected core and winding turns, the air gap of the core is given as:

$$G = \mu_0 \cdot A_E \cdot \frac{N_P^2}{1000L_m} - \frac{l_c}{\mu_r} \quad (13)$$

where A_E is the cross sectional area of the selected core in mm^2 , μ_0 is the magnetic permeability which equals $4\pi \times 10^{-7}$ H/m. L_m and N_P is the primary winding inductance and turns respectively, l_c is the core magnetic path length in mm and μ_r is the relative magnetic permeability of the core material.

Choose the primary MOSFET and secondary rectifier diode

During flyback converter operation, when the primary MOSFET is turned off, the input voltage (V_{in}) together with the output voltage reflected to primary side (V_{RO} , $V_{RO}=N \cdot V_{out}$) are imposed on the MOSFET (Fig.5) which should never exceed its voltage rating.

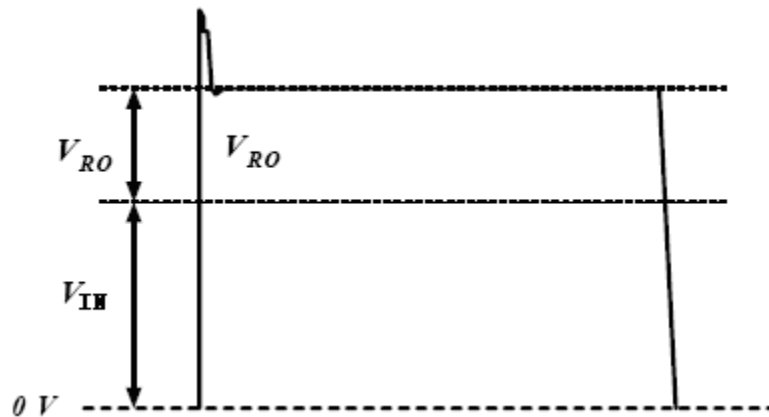


Fig.5 Voltage Imposed on Primary Side MOSFET

Generally, when we choose the primary MOSFET, 20%~50% voltage rating margin should be left for the spikes caused by the leakage energy.

$$V_{DS-pri} = K_s \cdot (n \cdot V_{out} + V_{in(max)}) \quad (14)$$

K_s is the margin factor, which is set to be 1.2~1.5.

Also, in order to improve the efficiency, total gate charge Q_g and MOSFET on-resistance should also be considered. Large $R_{ds(on)}$ results in high conduction loss given in (15) while large Q_g results in high switching loss given in (16), consider that the MOSFETs with low $R_{ds(on)}$ usually have high Q_g , there is a trade off for the MOSFET selection between switching loss and conduction loss.

$$P_{conduction} = R_{ds(on)} \cdot I_{in}^2 \tag{15}$$

$$P_{sw} = \frac{Q_{gs} \cdot R_G}{V_{DR} - V_{TH}} \cdot V_{DS} \cdot I_{IN} \cdot f_{SW} + \frac{Q_{gd} \cdot R_G}{V_{DR} - V_{PLT}} \cdot V_{DS} \cdot I_{IN} \cdot f_{SW} \tag{16}$$

Where V_{TH} is the MOSFET turn on threshold voltage, V_{PLT} is the plateau voltage, R_G is the gate resistance, V_{DS} is the drain-source voltage.

The maximum reverse voltage of the rectifier diode can be obtained as:

$$V_D = V_{out} + \frac{V_{in(max)}}{n} \tag{17}$$

Generally, 20%~50% voltage rating margin should be left for the spike voltages and the current rating of the rectifier diode should be larger than the maximum output current $I_{out(max)}$. In order to improve the efficiency, the schottky diode is preferred.

Design the RCD snubber

In practice, a small amount of energy is stored in the leakage inductance, which cannot be transferred to the output side in flyback converter. This amount of energy may result in a high voltage spike on the drain of the main switch, which should be restricted to protect the MOSFET.

The purpose of the RCD snubber (Fig.6) is to clamp the drain voltage. The parallel RC circuit may be connected with input. The value of the capacitor, C_{sn} , and resistor, R_{sn} , depend on the energy stored in the parasitic inductance, as this energy must be released into the RC network during each cycle. The voltage across the capacitor and resistor sets the clamp voltage, V_{CLAMP} . Fig.7 shows the voltage of the primary MOSFET during turn-off phase with respect to V_{CLAMP} .

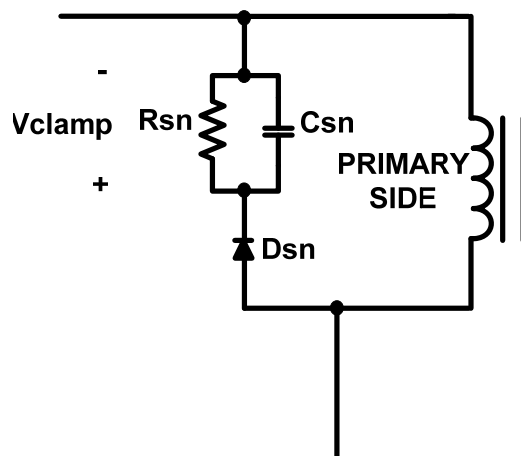


Fig.6 RCD Snubber on Primary Side

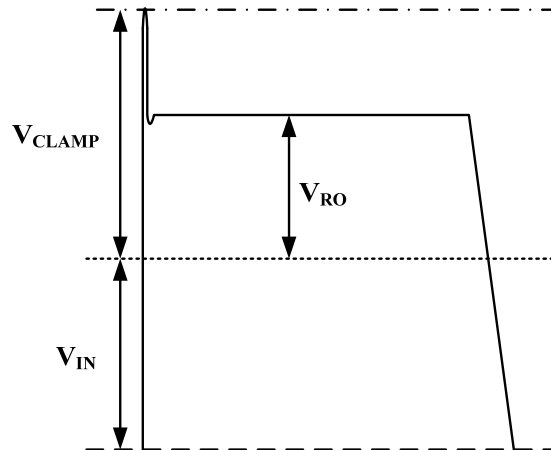


Fig.7 MOSFET Drain Voltage and Snubber Capacitor Voltage

The energy stored in the leakage inductance can be obtained as:

$$P_{sn} = \frac{1}{2} \cdot L_{leakage} \cdot I_{pripeak}^2 \cdot f_s \quad (18)$$

Where $I_{pripeak}$ is the peak current in primary side

For small leakage inductance application, the leakage energy given in (18) is partly dissipated in this RCD clamp circuit. For large leakage inductance application, the energy absorbed by the RCD clamp circuit is much larger than that given in (18) due to the long commutation time between the primary side and secondary side, thus part of the magnetizing energy is fed to the RCD clamp circuit instead of the output side. The theoretical analysis is quite complex and will not be elaborated on here. Generally, we simply assume the energy stored in the leakage inductance is completely dissipated in the RCD clamp circuit. Typically, we can assume an acceptable clamp voltage V_{CLAMP} which is usually 50~100% higher than the reflected output voltage V_{RO} . The resistance can be calculated based on (19). In practice, this resistance can be adjusted based on the power loss and the acceptable clamp voltage, which usually is slightly higher than that calculated by (19).

$$V_{CLAMP} = \sqrt{P_{sn} \cdot R_{sn}} \quad (19)$$

The snubber capacitor C_{sn} should be selected considering the voltage ripple of V_{CLAMP} given in (20). Generally, a 5~10% ripple voltage is reasonable.

$$\Delta V_{sn} = \frac{V_{CLAMP}}{C_{sn} \cdot R_{sn} \cdot f_s} \quad (20)$$

Design the input and output filters

An input capacitor is required to supply the AC current to the flyback converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors are preferred, and tantalum or low-ESR electrolytic capacitors may also suffice. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{in} = \frac{P_{out}}{f_{SW} \cdot C_{in} \cdot V_{in(min)}} \quad (21)$$

set ΔV_{in} to be below 1% of the input voltage.

The RMS current of the output capacitor can be obtained as:

$$I_{cap-in} = \sqrt{I_{rms-pri}^2 - I_{in}^2} \quad (22)$$

where I_{in} is the input current and $I_{rms-pri}$ is the primary RMS current :

$$I_{rms-pri} = \sqrt{\frac{D_{max}}{3} \left[3 \left(\frac{P_{in}}{V_{in(min)} \cdot D_{max}} \right)^2 + \left(\frac{V_{in(min)} \cdot D_{max}}{2 \cdot L_m \cdot f_{SW}} \right)^2 \right]} \quad (23)$$

The RMS current should be smaller than the capacitor RMS current rating. Similarly, the RMS current of the output capacitor can be obtained as:

$$I_{cap-out} = \sqrt{I_{rms-sec}^2 - I_{out}^2} \quad (24)$$

where I_{out} is the output current and $I_{rms-sec}$ is the secondary RMS current :

$$I_{rms-sec} = \sqrt{\frac{1-D_{max}}{3} \left[3 \left(\frac{I_{out}}{1-D_{max}} \right)^2 + \left(\frac{V_{out} \cdot (1-D_{max}) \cdot N^2}{2 \cdot L_m \cdot f_{SW}} \right)^2 \right]} \quad (25)$$

The RMS current should be smaller than the RMS current specification of the capacitor. The voltage ripple on the output can be estimated by:

$$\Delta V_{out} = \frac{I_{out} \cdot D_{max}}{C_{out} \cdot f_{SW}} + (I_{speak} - I_{out}) \cdot R_{ESR} \quad (26)$$

where I_{speak} = the secondary side peak current; R_{ESR} = ESR of output capacitor

Sometimes it is impossible to meet the ripple specification with a single electrolytic cap due to the high ESR. Then, additional LC filter stages or adding ceramic capacitor with low ESR to parallel with the electrolytic capacitor can be used.

Design feed back loop

Generally, offline and telecom power supplies require the galvanic isolation between a relative high input voltage and low output voltages. The most widely used devices to transfer signals across the isolation boundary are optocouplers. Fig.8 shows the typical isolated power supply with the primary-side PWM controller and optocoupler isolation.

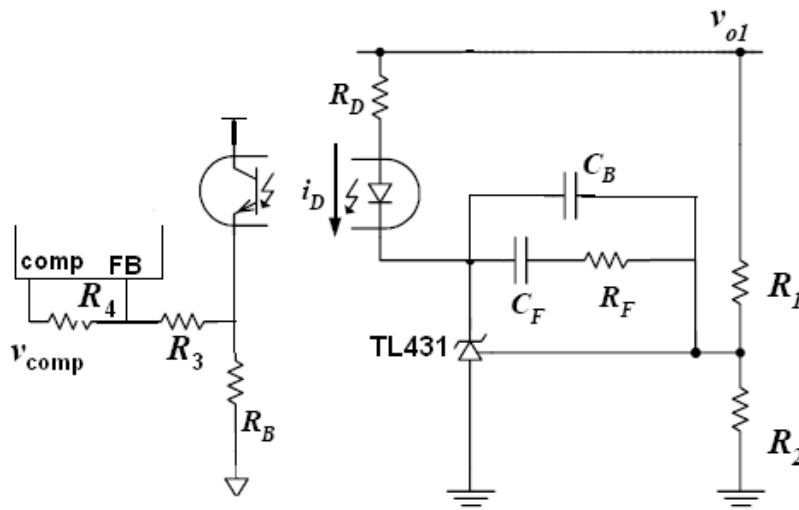


Fig.8 Feedback with Optocoupler Used in Isolated Power Supply

The small signal block diagram of the isolated power supply with optocoupler in fig.8 could be described as fig.9^[2].

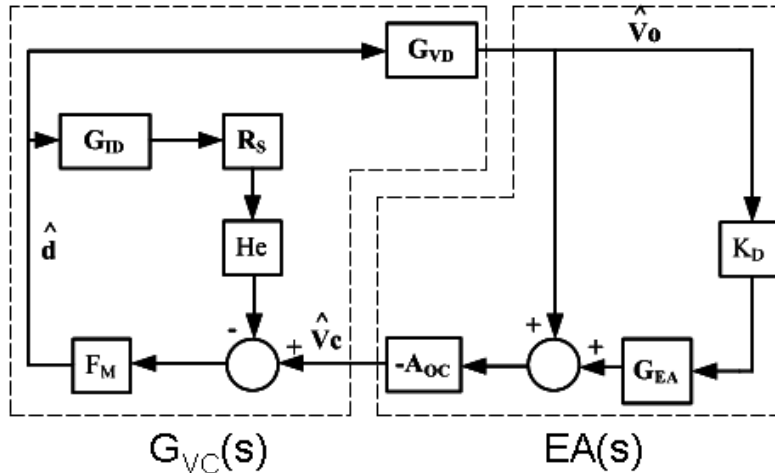


Fig.9 Small-signal block diagram of isolated power supply with current mode control

The detailed small-signal block diagram of the converter with the current-mode control shown in Fig.9, the expressions of the internal blocks are given as follows [2][3][4].

G_{VD} : duty-ratio to output transfer function, for flyback converter,

$$G_{VD} = \frac{V_{OUT}^2 \cdot N}{V_{IN} \cdot D^2} \cdot \frac{(1 + \frac{s}{w_{ESR}}) \cdot (1 - \frac{s}{w_{RHP}})}{s^2 + s \cdot \frac{w_0}{Q} + w_0^2} \quad (27)$$

where: $w_{ESR} = \frac{1}{R_{ESR} \cdot C_{out}}$ $w_{RHP} = \frac{R_L(1-D)^2 \cdot N^2}{D \cdot L_m}$ $w_0 = \frac{1}{\sqrt{L_m \cdot C_{OUT}}} \cdot \sqrt{\frac{(1-D)^2}{1 + \frac{R_{ESR}}{R_{LOAD}}}}$

$$Q = \frac{1}{w_0} \cdot \frac{1}{\frac{L_m}{(1-D)^2 \cdot R_{LOAD}} + C_{OUT} \cdot R_{ESR}}$$

G_{ID} : duty-ratio to inductor current transfer function, for flyback converter,

$$G_{ID} = \frac{V_{IN} \cdot (1+D)}{N \cdot R_{LOAD} \cdot C_{OUT} \cdot (1-D)} \cdot \frac{1 + \frac{s}{w_{RC}}}{s^2 + s \cdot \frac{w_0}{Q} + w_0^2} \quad (28)$$

Where: $w_{RC} = \frac{1+D}{R_{LOAD} \cdot C_{out}}$

F_M : PWM gain,

$$F_M = \frac{1}{(S_n + S_e) \cdot T_s} \quad (29)$$

Where: S_e is the external ramp slope. S_n is sensed current ramp, $S_n = \frac{V_{in}}{L_m} \cdot R_{sense} \cdot G_{CEA}$, here R_{sense} is the current sense resistor; G_{CEA} is the current sensing amplifier gain.

H_e : sampling transfer function, for flyback converter,

$$H_e = 1 + \frac{s}{w_n \cdot Q_z} + \frac{s^2}{w_n^2} \quad (30)$$

Where: $w_n = \frac{\pi}{T_s}$, $Q_z = \frac{-2}{\pi}$

R_S : Current sensing gain

K_D : output voltage divider gain

G_{EA} : error amplifier transfer function

A_{OC} : optocoupler circuit gain

From Fig.8, the control-to-output transfer function with the current loop close could be obtained as:

$$G_{VC}(s) = \frac{F_M \cdot G_{VD}}{1 + F_M \cdot G_{ID} \cdot R_S \cdot H_e} \quad (31)$$

Notice that there is a right half plane (RHP) zero (w_{RHP}) in the control-to-output transfer function of equation. Because the RHP zero reduces the phase by 90 degrees, the crossover frequency should be placed below the RHP zero.

The feedback compensation network transfer function of Fig.8 is obtained as:

$$EA(s) = \frac{v_{comp}}{v_{o1}} = -A_{OC} \cdot K_D \cdot G_{EA} = -\frac{w_i}{s} \cdot \frac{1 + s/w_{zc}}{1 + s/w_{pc}} \quad (32)$$

where: $w_i = CTR \cdot \frac{R_4 R_B}{R_D \cdot [R_3 - gm \cdot (R_3 + R_4)]}$, CTR is the current-transfer-ratio of the optocoupler, gm is the error amplifier transconductance.

$$w_{zc} = \frac{1}{R_F C_F}$$

$$w_{pc} = \frac{1}{R_F C_B}$$

When the input voltage and the load current vary over a wide range, it is not easy to determine the worst case for the feedback loop design. The gain together with zeros and poles vary according to the operating condition. One simple and practical way to this problem is designing the feedback loop for low input voltage and full load condition with enough phase and gain margin.

Fig.10 shows the simplified bode plot of $G_{VC}(s)$, $EA(s)$ and control-to-output transfer function with the compensator $T(s)$.

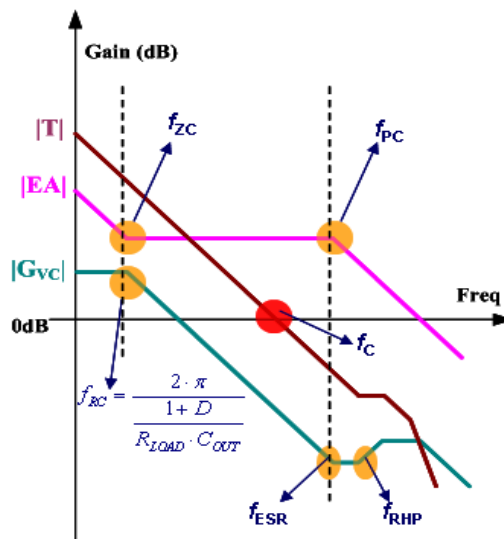


Fig.10 Simplified Bode Plot of the Power Supply with Current-Mode Control

The procedure to design the feedback loop is given as follows:

- (A) Decide the cross frequency f_C , noticed that the flyback system has a right half plane (RHP) zero which would decrease the phase margin by 90deg, in order to minimize the effect of RHP zero, set crossover frequency below 1/3 of the RHP zero ($f_C < f_{RHP}/3$)
- (B) Set the compensator's zero f_{ZC} to cancel the pole of G_{VC} (f_{RC}).
- (C) Set the compensator's pole f_{PC} to cancel the lower zero of G_{VC} (lower one of f_{ESR} and f_{RHP}) caused by the ESR of the output capacitor or the right half plane zero.
- (D) Calculate the gain of $G_{VC}(s)$ and $EA(s)$ at crossover frequency f_C , make the sum of Gain (G_{VC}) and Gain (EA) at f_C zero, so that the crossover frequency of the system is f_C .

DESIGN SUMMARY

- A detailed reference design of flyback converter with MP3900 is shown in Fig 11. The input voltage is 18 to 72V with 5V/3A output capability, for telecom application, the efficiency is expected to be above 80% at full load condition.
- The MP3900 is adopted as the control IC, which has a fixed switching frequency of 330kHz. Soft-start and UVLO circuits are implemented outside the device.
- A 50mΩ current sense resistor is used to sense the current through the MOSFET. Also, we add an offset voltage on SENSE pin of MP3900 by using R6 and R12 to limit the maximum current and decrease the power loss of current sense resistor. This will also improve the operation of the IC at very light load condition.
- The transformer (Cooper: CTX01-18256-R) we used in this design has a turn ratio of 3:1:2 (Primary:Secondary:Aux) with 40uH primary inductance, which makes the converter DCM at light load and CCM at heavy load.

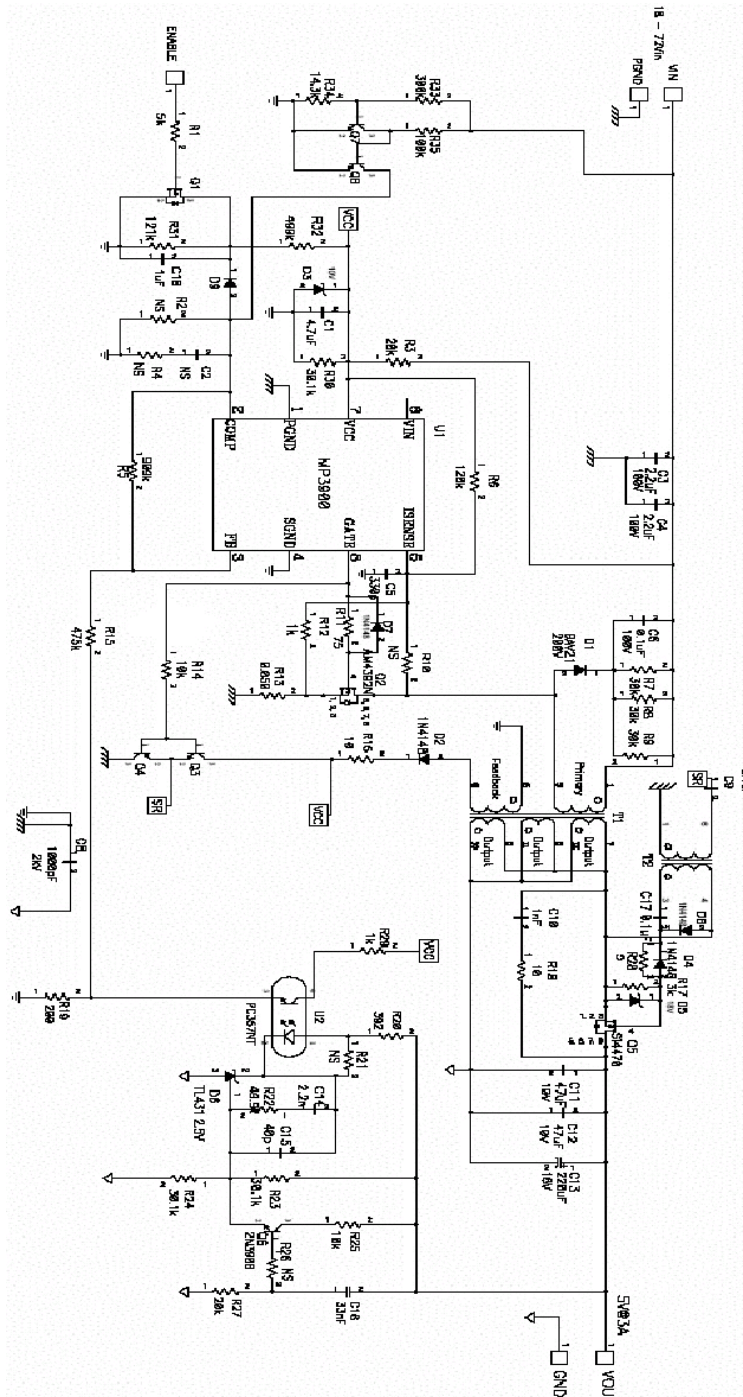


Fig.11 The Final Schematic of Flyback Converter Designed by MPS

EXPERIMENTAL VERIFICATION

In order to show the validity of the design procedure presented by this paper, the flyback converter of the design example has been built and tested (Input: 18V~72V; Output: 5V/3A). All the components in the circuit are used as design example in Fig.11.

Fig.12 shows the drain-source voltage of primary MOS and primary current waveform at minimum input voltage and full load condition. As designed, the maximum duty cycle (D_{max}) is about 0.425 and the maximum peak drain current (I_{pmax}) 2A.

Fig.13 shows the drain-source voltage of primary MOS and primary current waveform at maximum input voltage and full load condition, from which we could see that the maximum voltage stress on the primary MOS is about 120V, which is lower than the voltage rating of the MOSFET used (150V).

Fig.14 shows the drain-source voltage of primary MOS and primary current waveform at 48V input and full load condition. The voltage on the RCD snubber capacitor $V_{CLAMP} = V_{ds\max} - V_{IN}$, is 37.6V from Fig.7. It is nearly the same as the calculation result from equations (18) and (19). ($R_{CLAMP}=10k\Omega$, $L_{lk}=0.2\mu H$)

Fig.15 and Fig.16 shows the load transient and small signal bode plot of the whole system respectively. From Fig 18, the crossover frequency is about 10kHz, which is about 1/4 of the right half plan zero at 48V@3A. ($f_{RHP}=38kHz$)

Fig.17 shows the load regulation of the converter at 5V output, from which we can see that the designed converter has a good regulation in the whole load range.

Fig.18 shows the measured efficiency across the whole load range for different input voltage. The efficiency mostly ranges between 70%~80% at different input voltage and different load conditions.

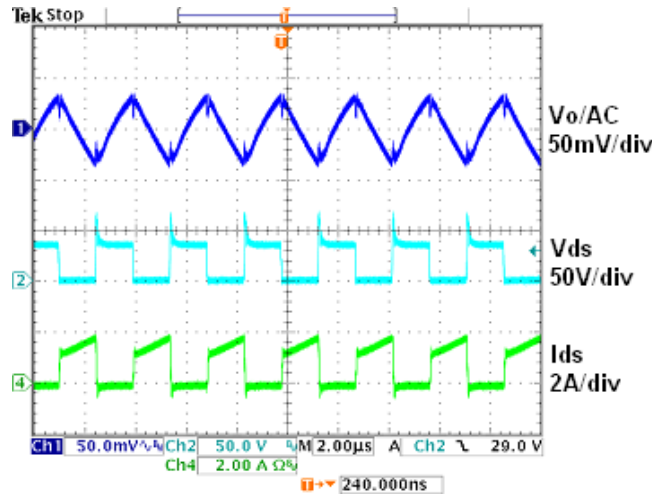


Fig.12 Waveform of Output Ripple and Primary Drain-source Voltage and Current at 18V Input and Full Load Condition

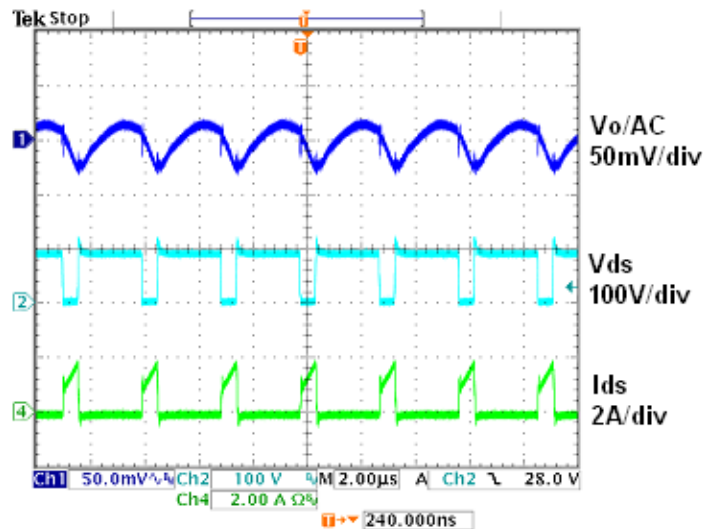


Fig.13 Waveform of Output Ripple And Primary Drain-source Voltage and Current at 72V Input and Full Load Condition

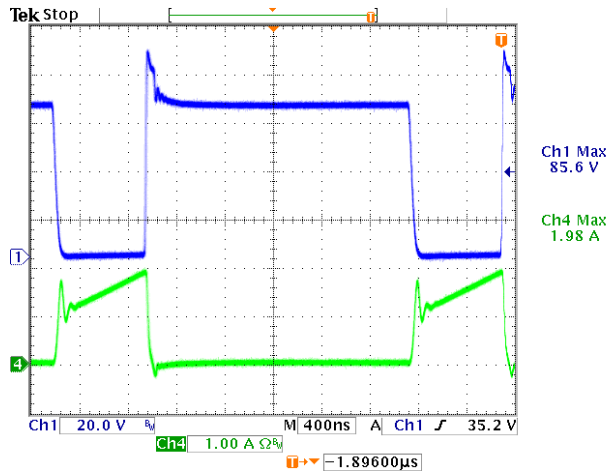


Fig.14 Waveform of Drain-source Voltage and Primary Drain-source Current at 48V Input and Full Load Condition

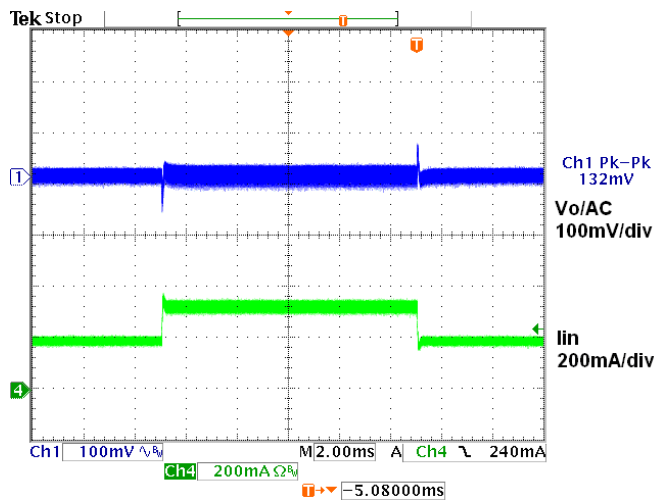


Fig.15 Load Transient of the System at 48V Input (Iout:1.5A~3A)

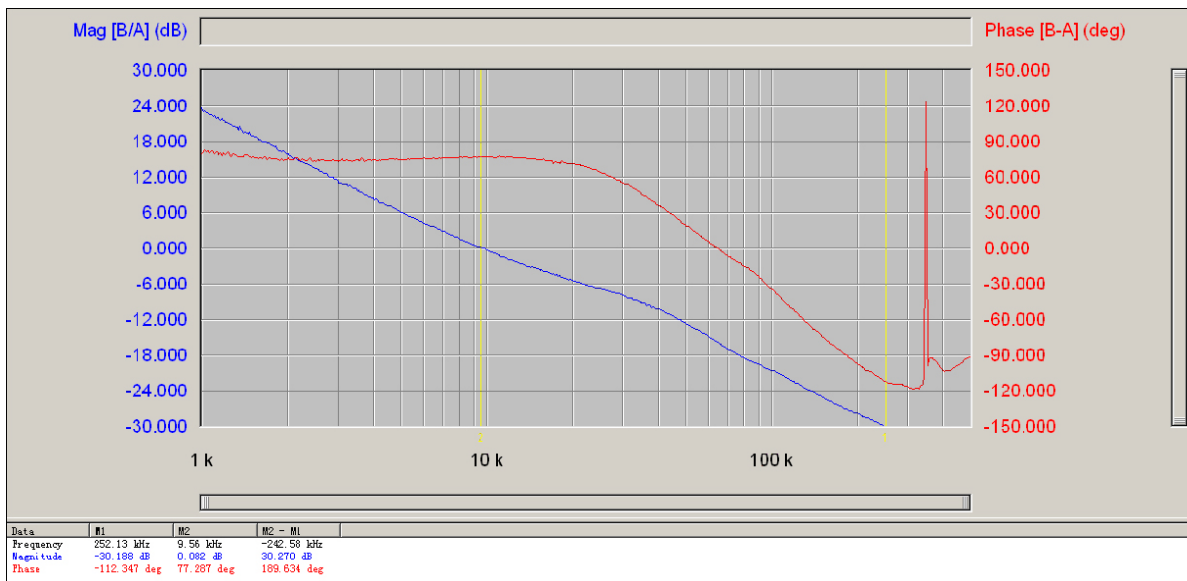


Fig.16 Small Signal of the System at 48V Input and Full Load Condition

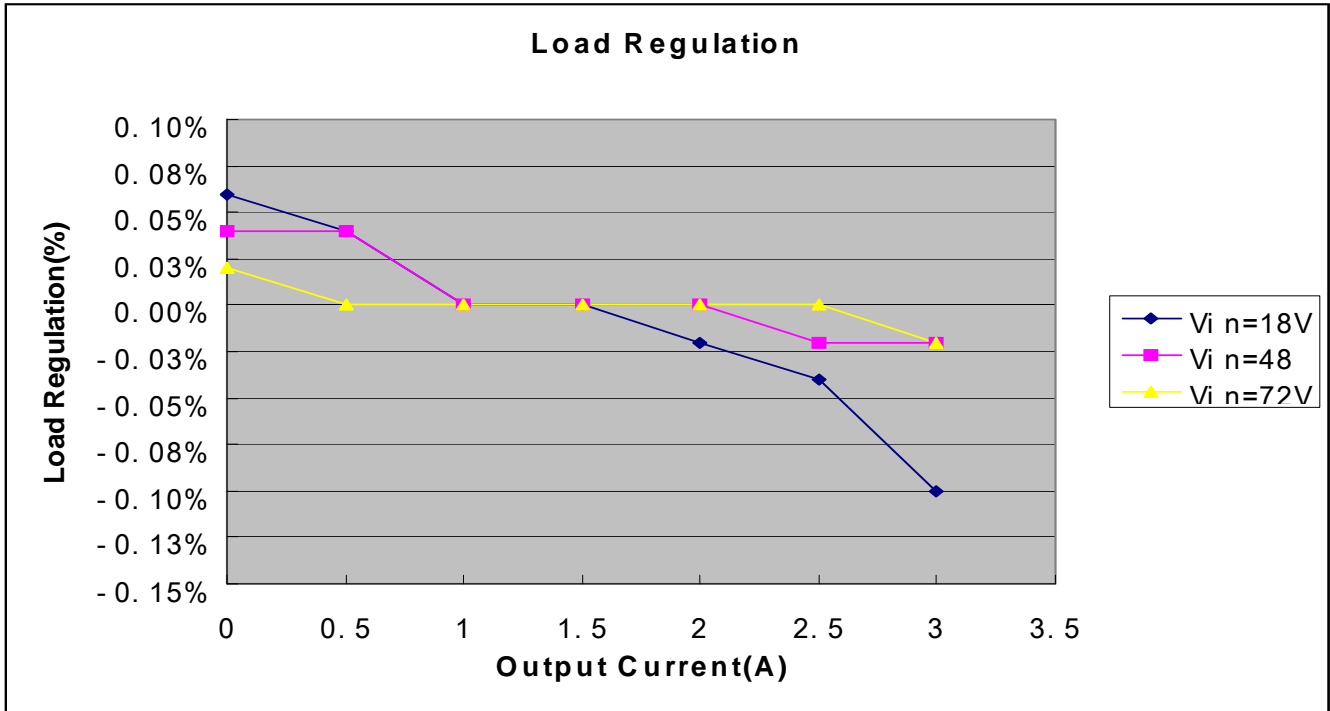


Fig.17 Load Regulation of the Converter at 5V Output

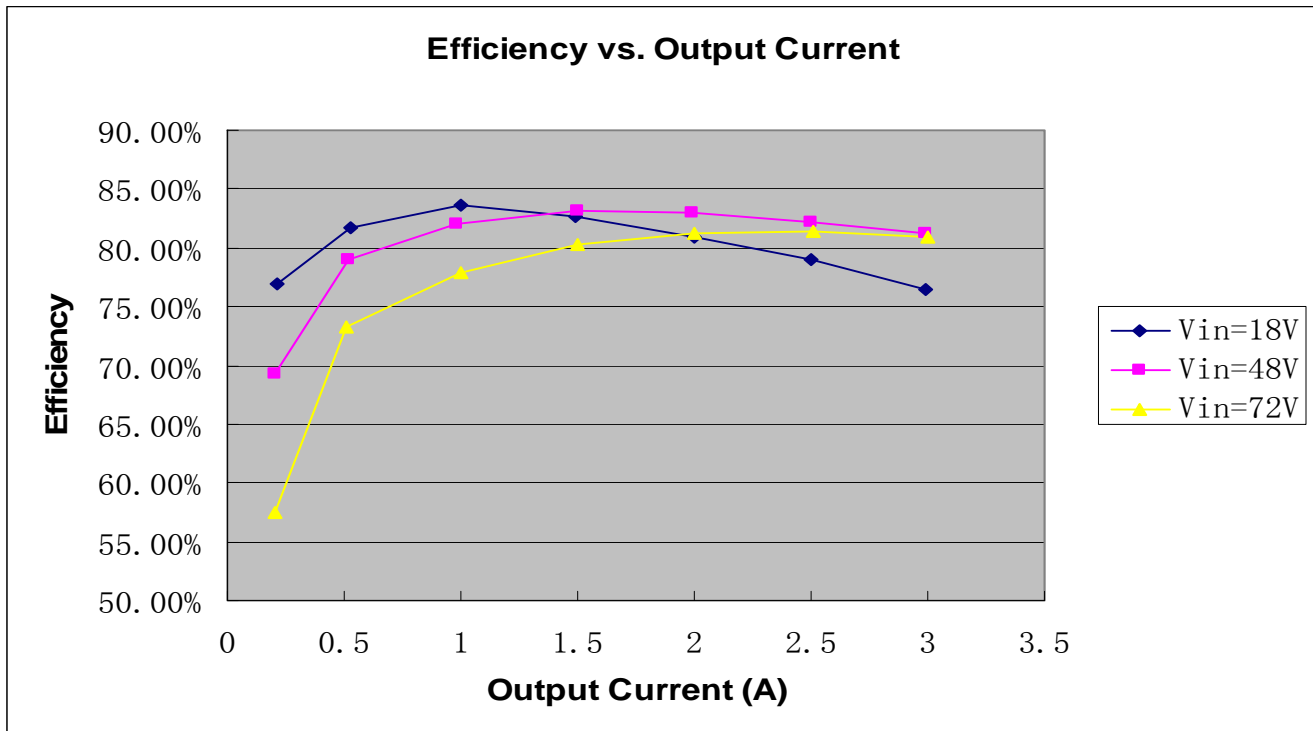


Fig.18 Efficiency of the Designed Flyback Converter

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