THE MP2905 HYSTERESIS VOLTAGE CONTROLLER

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ABSTRACT

The Hysteretic Voltage Control can provide fast transient response without additional loop compensation. With the benefits of low cost and ease of implementation, it’s very popular for power supplies of microprocessors and other high-slew-rate transition loads.

The MP2905 is a synchronous PWM buck controller with the hysteretic voltage-mode control. This application note introduces the principle of hysteretic voltage control and several different methods to design sufficient ripple voltage for stable operation of the synchronous Buck based on MP2905, and at last, the 25A application design with MP2905.

1. INTRODUCTION OF THE PRINCIPLE OF HYSTERETIC VOLTAGE CONTROL

Compared with the fixed-frequency PWM control method, hysteretic voltage control doesn’t have an oscillator and the error amplifier. There is only a hysteresis window with two references, high reference and low reference as figure 1 shown. The output voltage is fed back to keep tracking references within the hysteretic window. Both references determine the turn-on and turn-off of the transistor to control the output voltage.

When FB is higher than the high reference, high side switch turns off, low side switch turns on, the output voltage falls down, FB falls down, too.

When FB drops to a lower level than the low reference, high side switch turns on, low side switch turns off, and the output voltage rises up, and FB rise up, too.
It can react on the load current transient in the same switching cycle that the transient occurs. The key factor of hysteretic voltage control is to generate a sufficient amount ripple voltage on FB-pin to compare with the references.

MPS offers a hysteretic voltage-mode control, synchronous PWM buck controller - MP2905. This application note introduces several methods to generate the ripple voltage on FB and the application example based on MP2905.

2. METHODS TO GENERATE THE RIPPLE VOLTAGE ON FB

There are several methods to generate the ripple voltage on FB. This chapter shows three methods one by one.

2.1 Ripple Voltage from output Cap ESR.

It is known that the voltage ripple determined by ESR is the sawtooth waveform. So we consider to feed back the ripple voltage on ESR of output capacitor directly to FB as shown in figure 2.

Take MP2905 as an example, the required sawtooth signal level is approximately 10 mV at the comparing point (FB-pin). This determines the Vripple at the output node like this, \( V_{\text{ripple}} = V_{\text{OUT}} \times 10\text{mV} / V_{\text{FB}} \), otherwise the circuit may be unstable. Ceramic capacitor is not suitable due to the very low ESR here. Electrolytic capacitors and tantalum capacitors are good choices, because of their larger ESR.

The operating frequency of this schematic depends on the ESR of output cap, capacitance, inductance, \( V_{\text{IN}}, V_{\text{OUT}} \) and the voltage-divided resistances.
When the high side MOS is on, the circuit performs as figure 3 indicates. Assume the turn on period of the high side MOS is $D \cdot T$, where $D = \frac{V_{out}}{V_{in}}$, $T$ is the operating period. The ripple of the output voltage is mainly determined by the ESR, so:

$$V_{ripple-PP} = \Delta i_L \cdot ESR$$  \hspace{1cm} (2.1)

$\Delta i_L$ can be calculated by:

$$L \frac{\Delta i_L}{D \cdot T} = V_{IN} - V_{OUT}$$

$$\Delta i_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times L \times f}$$ \hspace{1cm} (2.2)

Where $f$ is the operating frequency.

The ripple voltage at FB:

$$\Delta V = \frac{R2}{R1 + R2} \times V_{ripple-PP}$$ \hspace{1cm} (2.3)

Combining the formula (2.1), (2.2), and (2.3), we get:

$$\Delta V = \frac{R2}{R1 + R2} \times ESR \times \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times L \times f}$$

$$f = \frac{R2}{R1 + R2} \times \frac{V_{OUT} \times (V_{IN} - V_{OUT}) \times ESR}{V_{IN} \times L \times \Delta V}$$ \hspace{1cm} (2.4)

Actually, the $\Delta V$ is not only due to the Hysteresis windows. It is influenced by the delay in the circuit, such as driving signal propagation delay. Especially at higher frequency and higher $V_{IN}$, the delay and noise impact frequency. As a result, the frequency calculated given by (2.4) may be inaccurate.

Moreover, the frequency is variable with load, because the inductance isn’t constant. It’s variable with load and temperature. Figure 4 shows an example that inductance drops as output current increasing. In this curve, the inductance @ 0A is 0.82uH, and drops to 0.65uH@25A. Suppose the frequency is 500kHz@0A, according to formula (2.4), the frequency@25A should be $(500 \times 0.82)/0.65 = 630$kHz. Besides inductance variation, the output ripple is also influenced by some parasitics such as ESL of output capacitor. This brings a larger frequency variation with load. This method is not recommended for higher current application.
If we use ceramic cap with lower ESR, the frequency will be very low based on the formula (2.4). Due to the low frequency and the resultant large output voltage ripple, ceramic caps cannot be used with this design method. If a ceramic is needed, the next method can overcome these problems.

**2.2 Ripple Voltage from DCR of inductor**

In the Buck circuit, the ripple on the DCR of inductor is a sawtooth waveform. So we can feed back the DCR voltage instead of the ESR ripple of the output cap, as shown in figure 5. R1 and C5 forms a lossless sensing circuit to get the voltage across the DCR of the inductor. R4 and the ceramic cap C4 filter the output ripple for C5. With this filter, the noise on the feedback ripple of the output voltage can be greatly decreased.

This section will introduce this DCR feedback method based on the MP2905.

![Figure 4 A inductor curve- Inductance vs Current](image)

![Figure 5 Method Two - Feedback ripple from inductor's DCR to FB](image)
2.2.1 Setting frequency

Figure 6 shows the equivalent circuit when low side switch is on. Assuming $R_4=0$ and no $C_4$, the current going through $C_5$ is:

$$i_c = \frac{V_{FB}}{R_2//R_1} = C_5 \frac{dv}{dt} = C_5 \times \frac{\Delta V \cdot f}{(1-D)} \quad (2.5)$$

![Figure 6 Equivalent circuit when Low-side MOSFET on](image)

$$f = \frac{1}{R_{FB}} \times \frac{1}{C_5} \times \frac{V_{FB}}{\frac{V_{IN}}{V_{OUT}}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (2.6)$$

Where $R_{FB} = \frac{R_1}{R_2} = \frac{R_1 \times R_2}{R_1 + R_2}$.

Assuming that $\Delta V$ is equal to the hysteresis of the comparing window, it is obvious that the frequency is variable with $V_{IN}$. The higher input voltage, the higher frequency will be. We have to also consider the circuit delay when calculating the voltage ripple on $FB$ as Figure 7 shows.

The Delay consists of the $FB$ propagation delay, dead time, driving circuit delay, etc. For simple calculation, only the hysteresis and $FB$ propagation delay are considered and $\Delta V$ is revised as:

$$\Delta V' = V_{HY} + V_{DELAY} \quad (2.7)$$

Where $V_{HY}$ is hysteresis of the comparing window, $V_{DELAY}$ is the voltage caused by delay. To calculate the voltage caused by delay, $V_{DELAY}$, we need to get the rising and falling slope of $FB$ ripple.

When high side switch turns on, $FB$ is rising, figure 8 shows the Equivalent circuit. The current going through $C_5$ is:

$$i_c = C_5 \frac{dv}{dt} = \frac{V_{IN} - V_{FB}}{R_1} - \frac{V_{FB}}{R_2} = \frac{V_{IN}}{R_1} - \frac{V_{FB}}{R_{FB}}$$

![Figure 7 Delay Time influence on FB ripple](image)
The FB rising speed is:
\[ \text{Rising\_slope} = \frac{dv}{dt} = \frac{i_c}{C_5} = \frac{I}{C_5} \left( \frac{V_{IN}}{R_I} - \frac{V_{FB}}{R_{FB}} \right) \]  
(2.8)

The falling slope of FB can be calculated from the formula (2.5),
\[ \text{Falling\_slope} = \frac{i_c}{C_5} = \frac{I}{C_5} \frac{V_{FB}}{R_{FB}} \]  
(2.9)

Table 1 lists the MP2905 FB propagation and dead time. The data are also listed in the Datasheet of MP2905.

<table>
<thead>
<tr>
<th>FB Propagation Delay</th>
<th>FB Falling to LG Falling</th>
<th>50ns</th>
</tr>
</thead>
<tbody>
<tr>
<td>FB Rising to HG Falling</td>
<td>70ns</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Dead time</th>
<th>HG low to LG high</th>
<th>40ns</th>
</tr>
</thead>
<tbody>
<tr>
<td>LG low to HG high</td>
<td>40ns</td>
<td></td>
</tr>
</tbody>
</table>

The voltage caused by FB propagation:
\[ V_{\text{delay1}} = \text{Rising\_slope} \times 70\text{ns} + \text{Falling\_slope} \times 50\text{ns} \]
\[ = \frac{I}{C_5} \times (70\text{ns} \times \frac{V_{IN}}{R_I} - 20\text{ns} \times \frac{V_{FB}}{R_{FB}}) \]  
(2.10)

During the time SW falls and rises, and the dead time, the FB doesn’t fall linearly because it is affected by the driving circuit. It’s difficult to calculate it accurately. We estimate it by 20ns of linear falling slope.
\[ V_{\text{delay2}} = \text{Rising\_slope} \times 20\text{ns} + \text{Falling\_slope} \times 20\text{ns} \]
\[ = 20\text{ns} \times \frac{I}{C_5} \times (\frac{V_{IN}}{R_I} - \frac{V_{FB}}{R_{FB}}) + 20\text{ns} \times \frac{I}{C_5} \frac{V_{FB}}{R_{FB}} \]
\[ = \frac{I}{C_5} \times 20\text{ns} \times \frac{V_{IN}}{R_I} \]  
(2.11)

Then,
\[ V_{\text{delay}} = V_{\text{delay1}} + V_{\text{delay2}} \]
\[ = \frac{I}{C_5} \times (90\text{ns} \times \frac{V_{IN}}{R_I} - 20\text{ns} \times \frac{V_{FB}}{R_{FB}}) \]  
(2.12)
Combining formula (2.6), (2.7) and (2.12), the more accurate frequency can be obtained:

\[
f = \frac{I}{RC} \times \frac{1}{C_5} \times \frac{V_{FB}}{V_{HY} + \left(90ns \times \frac{V_{IN} - 20ns \times V_{FB}}{R_1}\right) \times \left(I - \frac{V_{OUT}}{V_{IN}}\right)}
\]

(2.13)

Where \(V_{HY}\) is 22mV, \(V_{FB}\) is 590mV, and \(R_{FB} = \frac{R_1 \times R_2}{R_1 + R_2}\).

According to formula (2.13), frequency is variable with \(V_{OUT}\), \(V_{IN}\), \(C_5\) and Voltage-divided resistors \(R_1\) and \(R_2\). As a result, the variation between frequency and input voltage is nonlinear, a higher \(V_{IN}\) doesn’t mean a higher frequency.

### 2.2.2 Setting Output voltage

In this method, the Feedback point is at the SW node, so the voltage regulated is the DC component of SW. It is equal to \(V_{OUT}\) plus \(V_{DCR}\) (inductor series resistance)

\[
V_{OUT} = \frac{R_1 + R_2}{R_2} \times V_{FB} - V_{DCR}
\]

(2.14)

Since \(V_{DCR}\) is variable with load, then \(V_{OUT}\) is also variable with load, which results in bad load regulation at the output terminal. Choosing an inductor with smaller DCR (several milliohms) can improve the load regulation.

### 2.2.3 Transient Response

Because the circuit feeds back the DC component of SW instead of the real \(V_{OUT}\), there is a droop caused by the DCR of inductor in steady state, which benefits the transient performance. Transient response is highly sensitive to the inductor, the sensing capacitor \(C_5\) and the voltage divided resistors \(R_1\) and \(R_2\). The time constant of the sensing network is \((R_1 \times C_5)\), the inductor’s time constant is \((L/DCR)\). If the time constant of the sensing network \(C_5\) and \(R_1\) is the same as the inductor \(L\) and DCR, the transient response can be improved. The formula below shows the relation.

\[
R_1 \times C_5 = \frac{L}{DCR}
\]

(2.15)

If the formula (2.15) is satisfied, the voltage spike during the load transient can be minimized, below is an example.

Test condition: \(V_{IN}=12V\), \(V_{OUT}=1.8V\), \(I_{OUT}=0~5A\), slew rate=1A/us,

- Setting frequency=350KHz,
- Selecting \(C_5=10nF\), \(R_1=12.7k\Omega\), \(R_4=1\Omega\), \(C_4=4.4uF\).

The time constant of \(C_5\) and \(R_1\) is:

\[
\tau_{RC} = R_1 \times C_5 = 127 \times 10^{-6} S
\]

Choose an inductor \(L=2.2uH\) with DCR=10.2m\(\Omega\).

The time constant of inductor is:

\[
\tau_{LR} = L/DCR = 216 \times 10^{-6} S > \tau_{RC}
\]

Figure 9 is the test result. It’s not good. There is a spike when load stepping.
Select another inductor with $L=2.2\mu H$, $DCR=14m\Omega$. The time constant of this inductor is:

$$\tau = \frac{L}{DCR} = 157 \times 10^{-6} \text{s}.$$  

It's near the time constant of $R1$ and $C5$. Figure 10 shows the transient response. There is no spike when load stepping, the transient performance is improved a lot.

If one chose an inductor $L=2.2\mu H$, $DCR=21m\Omega$, then the time constant of inductor is:

$$\tau = \frac{L}{DCR} = 104 \times 10^{-6} \text{s} < \tau_{RC}$$

Figure 11 shows the transient response. There isn't a spike during the load transfer, but transient response time is a little longer, and the voltage droop is bigger than figure 8 and figure 9 because of the larger DCR.
In a word, to get the good transient response, the time constant of L and DCR should be accordant with the time constant of R1 and C5.

2.2.4 Output sensing filter - R4 and C4
R4 and C4 filter is used to filter the noise on \( V_{OUT} \). If there is no filter or it’s insufficient, FB ripple will be influenced by SW noise, badly. Then the frequency is extremely variable with load current because of the SW noise varying with the load.
Let’s monitor waveforms on point A and point B in figure12. The condition is 12V\(_{IN}\), 1.8V\(_{OUT}\), \( I_{OUT} = 0 \sim 5A \), C5=10nF, R7=12.7k\( \Omega \), R4=10\( \Omega \), C4=100nF.

![Figure 12 Detect point A and point B](image)

Figure 13 shows waveforms under no load condition. The filter corner frequency is not low enough to get rid of noise, so there is a ripple at point B. FB ripple (point A) is influenced by noise a little. The frequency is about 300KHz.
Figure 13 FB ripple at no load condition with insufficient filter

Figure 14 shows waveforms at 5A load. The noise is bigger at 5A load, therefore the waveform at point B is not a DC value. The influence of the increased ripple on the FB(point A) causes the frequency to increase from 300kHz up to about 400kHz.

When we set R4=10Ω, C4=4.7uF, the bandwidth is reduced and the influence from noise is eliminated.

Figure 15 FB ripple with sufficient filter
In figure 15, FB ripple is not influenced by $V_{OUT}$ ripple. Point B is very clean, and the frequency drifts little under different load condition: 340KHz under no load condition and 364KHz under 5A condition. However, this doesn’t mean that the lower corner frequency of the filter the better. Too low corner of a frequency in the filter will worsen the transient response. So, there is a tradeoff between frequency variation and transient response. Based on the test result, it is recommended to set $R4=1\Omega$, $C4=4.4\mu F$. It also has some relationship with layout. It’s better to keep the wire from $V_{OUT}$ to point B as short as possible, and point B should be close to chip. Then a smaller filter may be enough.

For the other parameters design, please refer to MP2905 datasheet.

Although we can use ceramic caps at the output in this method, there are some additional disadvantages, such as bad load regulation, variable frequency with load current, and a more complex design. The third method may be better than the present one with respect to these issues.

2.3 Ripple Voltage from external circuit

In this method, we use three external components to generate ripple.

Figure 16 shows a simplified diagram based on MP2905. The voltage divider $R1$ and $R2$ feeds back the output voltage. $C4$, $R4$, and $C5$ circuitry form an additional ramp signal generator. $C4$ is a DC-blocking capacitor. It’s used to block the SW’s DC component. Only the AC component is sent to the filter $R4$ and $C5$ to generate the ripple voltage for comparison with the hysteresis. The two components are summed together at FB. Because the DC component at FB is only decided by $V_{OUT}$, so there is no droop.

The $V_{OUT}$ can be decided by the reference voltage and the R-divider:

$$V_{OUT} = (1 + \frac{R1}{R2}) \times V_{FB}$$

(2.16)
By proper selection of R4 and C5, we can get the amplitude of the additional ramp signal generator which is much higher than the output ripple. As a result, the output ripple can be ignored, the switching frequency mainly depends on R4, C5 values. It is impacted little by output filter characteristics including inductance, the DCR of inductor, ESR, ESL and the capacitance of the output capacitor.

Figure 17 shows the process of getting ramp signals. SW is a square waveform including DC and AC components. After the DC blocking capacitor C4, the DC component is decoupled. The waveform at point D is a square wave without DC component, its high level is \((V_{\text{IN}}-V_{\text{OUT}})\), low level is \((-V_{\text{OUT}})\). Across the filter R4 and C5, the square wave is integrated to the sawtooth ripple.

![Figure 17 Waveform of ripple generation](image-url)
2.3.1 Setting frequency

Figure 18 shows the equivalent circuit of high side MOS on.

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\begin{figure}
\centering
\includegraphics[width=0.8\textwidth]{figure18}
\caption{Equivalent circuit of high side MOS on}
\end{figure}
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According to Kirchoff’s electric current law (KCL), we can get:

\[ i_{C5} + i_{R2} = i_{R4} + i_{R1} \quad (2.17) \]

Consider \( V_{FB} \) as a stable DC voltage, the currents through \( R1 \) and \( R2 \) are:

\[ i_{R2} = \frac{V_{FB}}{R_2}, i_{R1} = \frac{V_{OUT} - V_{FB}}{R_1} \]

substituting \( V_{OUT} \) by (2.16), \( i_{R1} = i_{R4} = \frac{V_{FB}}{R_2} \), therefore,

\[ i_{C5} = i_{R4} \quad (2.18) \]

These formulas show that DC component goes through the voltage divider formed by \( R1 \) and \( R2 \). AC component goes through \( R4 \) and \( C5 \). \( FB \) can be considered as zero, when analyzing the AC signal. Therefore:

\[ i_{R4} = \frac{V_{IN} - V_{OUT}}{R_4} \quad (2.19) \]

Combining (2.17) and (2.18) yields:

\[ i_{C5} = i_{R4} = \frac{V_{IN} - V_{OUT}}{R_4} = C_5 \times \frac{dv}{dt} = C_5 \times \frac{\Delta V}{DT} \quad (2.20) \]

\[ f = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times C_5 \times R_4 \times \Delta V} \quad (2.21) \]

In the same way, \( \Delta V \) consists of a hysteresis window and a delay component as in formula (2.7). The delay is the same as that described in figure 6. First, calculate the rising and falling slope of \( FB \).

According to formula (2.20), \( FB \) ripple rising slope is:

\[ \text{Rising Slope} = \frac{dv}{dt} = \frac{i_{C5}}{C5} = \frac{V_{IN} - V_{OUT}}{C5 \times R4} \quad (2.22) \]

Figure 19 shows the equivalent circuit of low side MOS on.

\[ i_{C5} = C_5 \times \frac{dv}{dt} = i_{R4} = \frac{0 - (-V_{OUT})}{R_4} = \frac{V_{OUT}}{R_4} \quad (2.23) \]

\[ \text{Falling Slope} = \frac{dv}{dt} = \frac{i_{C5}}{C5} = \frac{V_{OUT}}{C5 \times R4} \quad (2.24) \]
Calculate the FB propagation delay voltage as in formula (2.10),
\[ V_{\text{DELAY1}} = \text{Rising \_slope} \times 70 \text{ns} + \text{Falling \_slope} \times 50 \text{ns} \]
\[ = \frac{V_{\text{IN}} - V_{\text{OUT}}}{C_5 \times R_4} \times 70 \text{ns} + \frac{V_{\text{OUT}}}{C_5 \times R_4} \times 50 \text{ns} \]
\[ = \frac{1}{C_5 \times R_4} \times (V_{\text{IN}} \times 70 \text{ns} - V_{\text{OUT}} \times 20 \text{ns}) \]  (2.25)

Estimate the dead time and driving circuit delay voltage as in formula (2.11),
\[ V_{\text{DELAY2}} = \text{Rising \_slope} \times 20 \text{ns} + \text{Falling \_slope} \times 20 \text{ns} \]
\[ = 20 \text{ns} \times \frac{V_{\text{IN}} - V_{\text{OUT}}}{C_5 \times R_4} + 20 \text{ns} \times \frac{V_{\text{OUT}}}{C_5 \times R_4} \]
\[ = 20 \text{ns} \times \frac{V_{\text{IN}}}{C_5 \times R_4} \]  (2.26)

The total delay voltages are:
\[ V_{\text{DELAY}} = V_{\text{DELAY1}} + V_{\text{DELAY2}} = \frac{1}{C_5 \times R_4} \times (90 \text{ns} \times V_{\text{IN}} - 20 \text{ns} \times V_{\text{OUT}}) \]  (2.27)

Combining (2.7), (2.27) and (2.21):
\[ f = \frac{V_{\text{OUT}} \times (V_{\text{IN}} - V_{\text{OUT}})}{V_{\text{IN}} \times C_5 \times R_4 \times \Delta V} \]
\[ = \frac{V_{\text{OUT}} \times (V_{\text{IN}} - V_{\text{OUT}})}{V_{\text{IN}} \times C_5 \times R_4 \times \left(90 \text{ns} \times V_{\text{IN}} - 20 \text{ns} \times V_{\text{OUT}}\right)} \]  (2.28)

Where \( V_{\text{FB}} \) is 590mV

Frequency is influenced by \( V_{\text{OUT}}, V_{\text{IN}}, C_5 \) and \( R_4 \). Assuming \( V_{\text{OUT}}, V_{\text{IN}} \) are constant, we can easily set the frequency by \( C_5 \) and \( R_4 \). And frequency also has nonlinear variation with input voltage.
Note: If the time constant of C5 and R4 is too large, and the duty cycle is large, such as greater than 30%. The frequency calculated by formula 2.28 is not accurate, because the FB ripple doesn't rise and fall linearly. Usually, we recommend selecting R4 10%~30% less than the calculation.

2.3.2 Transient Response
In this configuration, there is a cap C5 paralleled with the low side voltage divided resistor. Obviously, it could worsen the transient response because of the delay. In order to minimize the effect on the transient, the capacitance of C5 should be small. However, too small of a C5 may influence the stability of FB ripple and introduce noise on FB. Capacitance between 2nF and 10nF is recommended for C5. Since frequency is set by C5 and R4, so it’s better to use a smaller C5 and bigger R4 to set the frequency.

Besides decreasing C5’s value, voltage divided resistances R1 and R2 should be small enough, too. Small R1, R2 and C5 means short time constants, so that the time delay from VOUT to FB pin is short. When the output changes with load stepping, the ΔVo will be feedback to FB pin with little delay. So the circuit responds to the ΔVo quickly. However, the no load power consumption is higher with smaller voltage divided resistances.

The inductor also influences the transient response. Small inductance will have better transient response, but higher current ripple, so, there is a tradeoff.

2.4 SUMMARY
Method one is the simplest way to generate the ripple voltage for hysteresis voltage controller. But, it needs a large ripple on ESR to guarantee the stability and set the frequency. It is well known that ESR of capacitor can’t be designed by application. So the frequency setting has to depend on the existing ESR parameter. Generally, the higher the frequency, the lower the voltage ripple for a given output capacitance will be. So if the ESR is not big enough, circuit may be unstable at higher frequencies.

Method two can use ceramic caps at the output. The frequency is set by R1, R2 and the sensing capacitor C5 (see figure 4). However, the load regulation characteristics make the design not suitable for higher current applications.

Method three seems to be a good solution for any current and any frequency application. Frequency is easy to be set with three additional components, which are independent of the output inductor and the output capacitor. The load regulation and transient response are good as well.

3. MP2905 DESIGN EXAMPLE FOR 25A APPLICATION
Compared to the other two, method three is a good choice for 25A application. The 25A application circuit is shown in figure20. The spec is VIN=12V (typ.), VOUT=1.8V, and IOUT=25A. The parameter design of the 25A circuit is detailed introduced as follows.
### 3.1 Setting frequency

With higher switching frequency, the transient can be better, and small output LC filter can be used, but power dissipation is higher. Considering these factors, the frequency is set at 300 kHz.

First, choose C5. As chapter 2.3.2 described, a 2.2nF is recommended.

Second, calculate R4 as in formula (2.28). Substitute in the known parameters,

\[
R_4 = \frac{V_{ag} \times (V_in - V_{out}) - V_{in} \times (90ns \times V_in - 20ns \times V_{out})}{V_{in} \times C_5 \times V_{HY}} \approx 83.8k
\]

Choose R4=82kΩ.

### 3.2 Setting the output voltage

External voltage divider resistors (R1 and R2 in figure 20) are used to set the output voltage. Per the chapter 2.3.2 description, voltage divider resistances should be small enough to get good transient performance. So, set R2’s value to be 1kΩ, R1 is determined by:

\[
R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right)
\]

Where \(V_{FB}=0.59V\), \(V_{OUT}=1.8V\), \(R_2=1kΩ\). Therefore,

\[
R_1 = 1000 \times \left(\frac{1.8}{0.59} - 1\right) \approx 2.05k
\]

Choosing a typical value 2.1kΩ for R1

### 3.3 Selecting the inductor

The inductor is required to supply constant current to the output load while being driven by the square input voltage. A larger value inductor is favorable to reduce ripple current and lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series DC resistance, and/or lower saturation current. Furthermore, the transient performance
may be poor. A good rule for selecting the inductance is to allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum output current. Also, make sure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

\[ L = \frac{V_{OUT}}{f_S \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \]  \hspace{1cm} (2.29)

Where \( V_{IN} \) is the input voltage, \( V_{OUT} \) is the output voltage, \( f_S \) is the switching frequency, and \( \Delta I_L \) is the peak-to-peak inductor ripple current, recommended to be 30% of the maximum output current. Substitute all the known parameters,

\[ L = \frac{1.8}{300 \times 10^3 \times 0.3 \times 25 \times (1 - \frac{1.8}{12})} = 0.68 \mu H \]

The DC current rating of the inductor must be higher than the maximum output current to keep the temperature rise within the desired range. The inductor also needs to have a low DCR to achieve good efficiency, as well as enough room above peak inductor current before saturation. The peak inductor current can be estimated as follows:

\[ I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 \times f_S \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \] \hspace{1cm} (2.30)

The maximum inductor peak current can be calculated from formula (2.30), as 28.1A.

\[ I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 \times f_S \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \]
\[ = 25 + \frac{1.8}{2 \times 300 \times 10^3 \times 0.82 \times 10^{-8} \times (1 - \frac{1.8}{12})} \approx 28.1A \]

Considering all above factors, select such an inductor: 0.82uH with 0.9mΩ DCR, 27A current rating, and 35A saturated current which is higher than 28.1A.

### 3.4 Selecting Power MOSFETs

The MOSFETs are the key points for circuit efficiency. The major parameters we should consider are:

1) On-resistance, \( R_{DS\_ON} \): the lower, the better it is.
2) Continuous Drain Current (@10sec), \( I_{DS} \): it should be higher than the peak current under full load condition. Pay attention to the variation of \( I_{DS} \) with temperature.
3) Maximum drain-to-source voltage, \( V_{DS\_(MAX)} \): it should be at least 20% higher than the input supply rail.
4) Total gate charge, \( Q_g \): the lower, the better it is.

For high-side MOSFET, the main power loss consists of conduction loss, switching loss, and driving loss.

The high-side MOSFET conduction loss can be calculated by:

\[ P_{HS\_conduction} = I_{LOAD}^2 \times R_{HS\_DS\_ON} \times D \] \hspace{1cm} (2.31)

Where \( D \) is the duty cycle, it’s defined by \( D = \frac{V_{OUT}}{V_{IN}} \).

High-side MOSFET switching loss is estimated by:

\[ P_{HS\_switching} = \frac{1}{2} \times V_{IN} \times I_{LOAD} \times (t_r + t_f) \times f_S \] \hspace{1cm} (2.32)
Where $t_r$ is the rise time of the high-side MOSFET driving signal $V_{gs}$, $t_f$ is the fall time of the high-side MOSFET driving signal $V_{gs}$, $f_s$ is the switching frequency.

High-side MOSFET driving loss is calculated by:

$$P_{\text{HS\_drive}} = Q_{g\_HS} \times f_s \times V_{\text{drive}}$$

(2.33)

Where $V_{\text{drive}}$ is the high-side MOSFET driving voltage. The value in MP2905 is 5V.

For low-side MOSFET, there isn’t switching loss, conduction loss is the main loss. We choose a MOSFET with lower $R_{DS\_ON}$. The low-side MOSFET loss consists of conduction loss, driving loss and body diode conduction loss.

The Low-side MOSFET conduction loss is calculated by:

$$P_{\text{LS\_conduction}} = I_{\text{LOAD}}^2 \times R_{\text{ON\_LS}} \times (1 - D)$$

(2.34)

Low-side MOS driving loss is calculated by:

$$P_{\text{LS\_drive}} = Q_{g\_LS} \times f_s \times V_{\text{drive}}$$

(2.35)

Body diode conduction loss is calculated by:

$$P_{\text{body\_diode}} = 2 \times V_F \times I_{\text{LOAD}} \times t_{\text{deadtime}} \times f_s$$

(2.36)

Where $V_F$ is body diode forward voltage drop, $t_{\text{deadtime}}$ is the transition time between high-side MOSFET and low-side MOSFETs.

Except for the losses above, there is output cap loss in both the high side MOSFET and the low side MOSFET. Output cap loss is defined by:

$$P_{\text{cap}} = \frac{1}{2} \times C_{\text{DS}} \times V_{DS}^2 \times f_s$$

(2.37)

where $C_{\text{DS}}$ is the equivalent output cap of MOSFET.

For the spec: $V_{IN}=12$V, $V_{OUT}=1.8$V, $I_{OUT}=25$A, the duty cycle is very small, then conduction loss in the high side MOS is limited. Switching loss accounts for the main part. So when selecting the high side MOS, we should first consider $t_r$ and $t_f$ of MOS.

For the low side MOS, the main loss is conduction loss, so the $R_{DS\_ON}$ should be as small as possible. We can even parallel two MOSFETs at low side to minimize the $R_{DS\_ON}$. However, we should pay attention to the driving loss. The $Q_g$ is very large if two MOSFETs are paralleled on the low side. The driving loss will cause the temperature to rise in MP2905.

Below is an example for MOS selection, use one MOS at high side, two MOS at low side. Table 2 shows several MOSFETs.

The $t_r$ and $t_f$ of MOS1 and MOS2 are small, so they are used as high side MOS. MOS3 and MOS4 are fit for low side MOS because of their low $R_{DS\_ON}$. Estimate the power loss in each MOS.

<table>
<thead>
<tr>
<th>Part Number</th>
<th>$R_{DS_ON}(\Omega)$</th>
<th>$Q_g$(nC)</th>
<th>$t_r$(nS)</th>
<th>$t_f$(nS)</th>
<th>$V_F$(V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 AP3R303GMT-HF</td>
<td>5</td>
<td>13.3</td>
<td>5.5</td>
<td>17</td>
<td>-</td>
</tr>
<tr>
<td>2 AP0603GM</td>
<td>10.5</td>
<td>9</td>
<td>4.5</td>
<td>10.5</td>
<td>-</td>
</tr>
<tr>
<td>3 Si7658ADP</td>
<td>2.8</td>
<td>34</td>
<td>-</td>
<td>-</td>
<td>1.1</td>
</tr>
<tr>
<td>4 AP2R403GMT-HF</td>
<td>3.6</td>
<td>20.5</td>
<td>-</td>
<td>-</td>
<td>1.3</td>
</tr>
</tbody>
</table>
According to loss analysis table3, the loss of MOS1 is lower, it is a good choice for high side MOS at the spec because of its lower tr, tf and lower Rds-on. MOS2’s loss is higher because of its higher Rds-on, but its switching loss is very small, so at higher frequency or higher V_in spec, MOS2 may have the better performance than MOS1.

| Table3 loss analysis – M1 and M2 (Vin=12V, Vo=1.8V, Io=25A, fs=300kHz) |
|-----------------|-----------|-----------|
| MOS1            | MOS2      |
| Conduction loss | 0.47W     | 0.98W     |
| Switching loss  | 1.01W     | 0.675W    |
| Driving loss    | 0.02W     | 0.014W    |
| Total loss      | 1.5W      | 1.669W    |

According to loss analysis table4, the loss of MOS3 is much lower than MOS 4, but the Qg and driving loss is much higher. MP2905’s driving signal is generated by internal LDO. If the LDO’s efficiency is not high enough, then larger Qg and higher driving loss could cause higher temperature rise at chip. The junction to ambient thermal resistance of MP2905 is 150°C/W. 0.1W driving loss causes 15°C temperature rise. Considering the loss of the MP2905 internal LDO, the temperature rise may be higher than 30°C. As a tradeoff, MOS4 with higher total loss but lower driving loss is a more reasonable choice.

| Table4 loss analysis – M3 and M4 (Vin=12V, Vo=1.8V, Io=25A, fs=300kHz) |
|-----------------|-----------|-----------|
| MOS3            | MOS4      |
| Conduction loss | 0.74W     | 0.96W     |
| Body diode conduction loss | 0.66W | 0.78W |
| Driving loss    | 0.1W      | 0.06W     |
| Total loss      | 1.5W      | 1.8W      |

For the driving circuit of the MOS, it’s better to slow down the high side and low side MOS turn on speed. It reduces the noise caused by switching, and insures enough dead time to avoid shoot through. We recommend placing series driving resistor to slow down the turn on speed. The resistance shouldn’t be too large (less than 10Ω is ok), otherwise the switching loss will increase. Part of the driving loss is now in the driving resistors which are outside the chip. Therefore, the temperature rise of chip can be lower. An anti-parallel diode is recommended, so that the turn-off speed is not reduced.

### 3.5 Current Limit setting
MP2905 current limit can be set by an external resistor (R3 in figure 16) which is connected between ILIM pin and the drain of the high side MOSFET. An internal 50uA sink current sets a voltage drop on the resistor. The voltage drop compares to the high-side MOSFET voltage drop (V_ds) to set the peak current limit threshold. Below is the diagram of the current limit function:
The voltage drop on the high side MOSFET is:

\[ V_{DS\ ON\ (max)} = I_{DS\ (max)} \times R_{DS\ ON\ (max)} \]  

(2.38)

Where \( I_{DS\ (max)} \) equals the max peak inductor current \( ILP\ (max) \). Then, \( R_{ILIM} \) can be calculated using the \( V_{DS\ ON\ (MAX)} \) with the following formula:

\[ R_{ILIM} = \frac{V_{DS\ ON\ (max)}}{50\mu A} (\Omega) \]  

(2.39)

\( R_{ILIM} \) should be kept in the range of 1kΩ~8kΩ.

The \( R_{DS\ ON} \) is variable with temperature. At higher temperature, \( R_{DS\ ON} \) is higher, and then the current limit will be lower than the calculation. We have to consider the temperature coefficient of \( R_{DS\ ON} \). Usually, the temperature coefficient \( k_{th} \) is 1.2@75°C, 1.3@90°C, and for more exact value, please refer to the DS of the MOS you select.

Then the formula 2.39 can be corrected as:

\[ R_{ILIM} = \frac{I_{DS\ (max)} \times R_{DS\ ON \times k_{th}}}{50\mu A} (\Omega) \]  

(2.40)

Design example: suppose we choose a high side MOS with 5mΩ \( R_{DS\ ON} \), 1.3 \( k_{th} \) and 0.82uH inductor as above. Then the peak to peak value of inductor current is 6.2A. Set the max DC current at 27A, then the peak current of inductor is:

\[ I_{LP} = 27 + (6.2 / 2) = 30.1A \]

Therefore:

\( V_{DS\ ON\ (max)} = 30.1A \times 5mΩ \times 1.3 = 195.7mV. \)

\( R_{ILIM} = 195.7mV / 50\mu A = 3.91kΩ. \)

The oscillation at SW when the high side MOS is on, the distribution of \( R_{DS\ ON} \), the current sense program current source and the temperature drift of the current sense program can influence the precision of the current limit. To ensure the circuit can always work at 25A, it’s better to set the \( R_{ILIM} \) to be 15%~20% higher than the theoretic calculation. In the example, we can set \( R_{ILIM} \) at 4.5kΩ.

A small parallel capacitor (C6 in figure 20) is necessary to filter the noise on R3. 10nF is recommended. Figure22 shows the noise waveform on R3, with C6 and without C6.
3.6 Setting Input Capacitor

The input current to the step-down converter is pulsating, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. The effect of electrolytic capacitors is limited, because the electrolytic capacitor is not fit to work at higher frequency.

Since the input capacitor (Cin) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

\[ I_{\text{Cin}} = I_{\text{LOAD}} \times \sqrt{\frac{V_{\text{OUT}}}{V_{\text{IN}}} \times (1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}})} \]

The worse case condition occurs at \( V_{\text{IN}} = 2V_{\text{OUT}} \), where \( I_{\text{Cin}} = \frac{I_{\text{LOAD}}}{2} \).

For simplification, choose the input capacitor whose RMS current rating greater than half of the maximum load current.

Make sure that capacitance is enough to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple can be estimated by:

\[ \Delta V_{\text{IN}} = \frac{I_{\text{LOAD}}}{f_S \times C_{\text{in}}} \times \frac{V_{\text{OUT}}}{V_{\text{IN}}} \times (1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}) \]

Big input ripple worsens efficiency and causes higher temperature rise in capacitors, and impacts the stability of the circuit.

3.7 Selecting Output Capacitor

The output capacitor (Cout) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. A low ESR capacitor is preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

\[ \Delta V_{\text{OUT}} = \frac{V_{\text{OUT}}}{f_S \times L} \times (1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}) \times (R_{\text{ESR}} + \frac{1}{8 \times f_S \times C_{\text{OUT}}}) \]
Where $L$ is the output inductance and $R_{ESR}$ is the equivalent series resistance (ESR) of the output capacitor.

In the case of a ceramic capacitor, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. The output voltage ripple can be simplified:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_s \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple is approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR}$$

In method three, the output ripple will influence the FB ripple. The system will be unstable with large output ripple. So, we should minimize the output ripple with a big capacitance and low ESR. A POSCAP is recommended at the output for its large capacitance and low ESR.

### 3.8 PCB layout guideline

PCB layout is very important to achieve stable operation. Follow these guidelines:

1) Keep the path of switching current short and minimize the loop area formed by the input cap, high-side MOSFET and low-side MOSFET.
2) IC bypass ceramic capacitors are suggested to be put close to the IN Pin.
3) Ensure all feedback connections are short and direct. Place the feedback resistors as close to the chip as possible.
4) Route SW away from sensitive analog areas such as FB.
5) Connect IN, SW, and especially GND respectively to a large copper area to improve chip thermal performance and long term reliability.
6) It is suggested to add a snubber circuit across the high side MOSFET (IN pin and SW pin) so as to reduce the SW spike.
7) The signal GND and power GND should be connected by a single point. This will ensure a clean control signal.
8) For 25A application, four-layer or even a six-layer PCB is recommended. If we use a four layers PCB, make sure the copper area is big enough to create a low thermal resistance and keep the temperature rise small. If the size of the PCB is limited, another heat sink should be used.
Figure 23 Method Three - Feedback ripple from external circuitry to FB

3.9 25A demo board SCH, BOM, PCB

Figure 24—Demo Board SCH

SPEC: \( V_{in} = 12V \), \( V_o = 1.8V \), \( I_o = 25A \), \( f_s = \text{about } 300kHz \)
### Table 5 Demo Board BOM

<table>
<thead>
<tr>
<th>RefDes</th>
<th>Value</th>
<th>Description</th>
<th>Package</th>
<th>Manufacturer</th>
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<td>C1A, C1B</td>
<td>22uF</td>
<td>Ceramic Cap, 25V, X5R</td>
<td>1210</td>
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<tr>
<td>C2A</td>
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<td>Poscap, 6.3V</td>
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<td>0603</td>
<td>TDK</td>
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<tr>
<td>C4</td>
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<td>Ceramic Cap, 10V, X7R</td>
<td>0605</td>
<td>TDK</td>
</tr>
<tr>
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<td>Apec</td>
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<td></td>
<td>MSOP10</td>
<td>MPS</td>
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</table>
Figure 25—Demo Board Layout
3.10 Demo board test result

1. FB Ripple
Test condition: Vin=12V, Vout=1.8V

2. Output Ripple
Test condition: Vin=12V, Vout=1.8V
3. Transient
Test condition: $V_{in}=12V$, $V_{out}=1.8V$, $0\sim25A$, $2.5A/us$

Figure 28—Transient Response

4. Efficiency
Test condition: $V_{in}=12V$, $V_{out}=1.8V$

Figure 29—Efficiency Curve
4. CONCLUSION

We compared three different methods to do hysteresis control based on the MP2905. Method three can fulfill any request especially with respect to the high output current case. For method 3, ceramic capacitors can be used as the output capacitors. Ceramic caps keep the output ripple lower and the physical size very compact. The frequency is independent of output filter characteristics and parasitics. The transient response of this hysteresis control is excellent with the careful design of the feedback loop.